Supplemental Materials: Neural Network Learning with Non-ideal Resistive Memory Devices

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I. EXAMPLE OF TIKI-TAKA ALGORITHM

We describe briefly a possible convergence scenario of SGD and Tiki-Taka algorithm on non-ideal device in Fig. S1. SGD algorithm consists of forward/backward/update pass. Fig. S1(b) shows when the device is within the symmetric update regime where the upward/downward updates are balanced. In this case, the mean weight value (w_{mean}) eventually reach the desirable target weight value (w_t) which minimizes the pre-defined cost function. However, when the device is in nonsymmetric update regime as described in Fig. S1(c), the biased update results in the mean weight value deviated from w_t. In this example, the device has strong downward pulse response, resulting in $w_{mean} < w_t$.

Tiki-Taka algorithm consists of a system A (w_A) which acts as a gradient accumulation layer, and system C (w_C) which plays a role as a weight layer. Figure S1(e) describes the behavior of w_A, and Fig. S1(f) describes conductance change on w_C in a hypothetical scenario. As w_C reaches to w_t with gradient fluctuates between positive/negative, w_A eventually operates near the symmetry point[S1]. Then the nonsymmetric nature of device is compensated by the feedback process between w_A and w_C, and w_C eventually reaches w_t[S1]. In this example, the feedback process between w_A and w_C is indexed with a number in chronological order. Especially, at step 8, SGD would generate downward pulse as $w_C > w_t$, resulting in the behavior described in Fig. S1(c) where w_{mean} cannot reach w_t. However, the accumulated upward gradient in w_A compensates the newly generated downward gradient, and still maintains a positive sign at step 9. As a result, the accumulated upward gradient in w_A drives w_C to move further toward positive direction in 10, achieving w_{mean} w_t. Note that it is important for w_A to be near the symmetry point where upward and downward updates are symmetric, so that w_A keeps a positive sign at step 9.

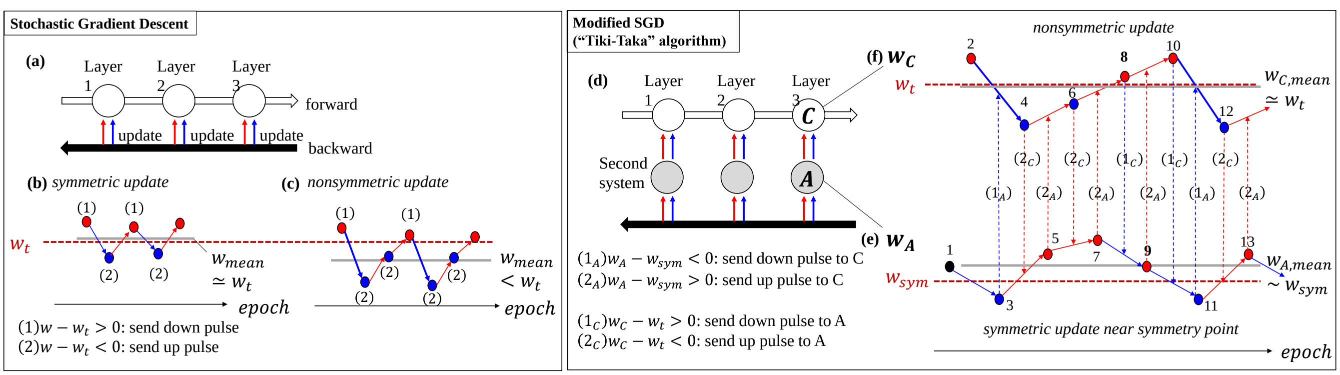

FIG. S1. Schematics for (a,b,c) SGD and (d,e,f) "Tiki-Taka" algorithm.

II. DEVICE CHARACTER: SYMMETRY POINT MEASUREMENT

The pulse responses are obtained for 5 super cycles of 400 set/reset pulses and the averaged traces are indicated as a blue and red solid line. We perform the symmetry point measurement by sending an alternating pulse sequence[S1,S2] and the mean value of the SP (g_{SP}) is plotted as a dashed line in 5. To emphasize the presence of symmetric and nonsymmetric update regime, we obtain the differential conductance from averaged pulse responses and present the results in Fig. S2(b,d). Both plots show that the SP is located near the point where the upward/downward update strength coincides. The obtained conductance value is subtracted by the measured SP conductance to ensure $\mathbf{w}_A$ is read differentially relative to their corresponding symmetry points.

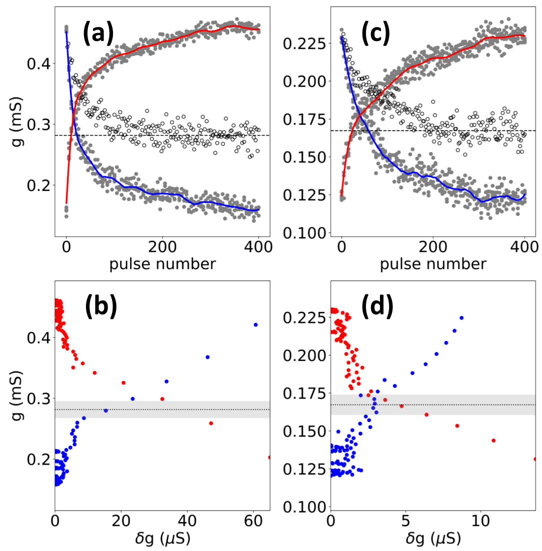

FIG. S2. (a) A $20\mu m \times 20\mu m$ ReRAM (device 1) conductance response to the 400 upward/ 400 downward pulses. The measurement is repeated for 5 cycles (gray filled circle) and averaged traces are plotted as a solid line. Repeated 2 upward/ 2downward pulse sequence has been used to measure symmetry point (SP, open circle). The SP is obtained by averaging measured conductance from half of the sequence up to the final sequence (dashed line). (b) differential conductance is obtained from averaged traces from (a). SP agrees with the point where differential conductance of up/down traces matches to each other. SP is indicated as dashed line with its rms as shaded region. We observe that the SP extracted from upward/downward traces does not exactly matches with the SP extracted from alternating pulse measurement result, which is caused by the inherent device noise and cycle to cycle variation. (c) The same measurement with (a) for another device (device 2). (d) The corresponding differential conductance measurement. The devices have been formed at 3V. The 320ns pulse is used for -1.48V(down) / 1.28V(up) for device 1 and -1.7V(down) / 1.15V(up) for device 2. We use the device 1 as W_A and device 2 as W_C.

III. DEVICE CHARACTER: DISTURBANCE

ReRAM stack is integrated to transistors and form 1T1R array. Four 200nm×200nm devices out of 32 by 20 array is selected and biased with a common switching condition described in the main text. In order to effectively apply a full drain bias to a selected ReRAM, we apply a half-bias scheme where half of the full bias $(+V/2)$ is applied to all the un-selected rows and columns. Then we apply full bias to a selected row (V) and zero bias to a selected column (0). Figure S3(a) describes the half-bias scheme when (1,1) device is selected. A clear response has been observed for a selected device in Fig. S3(a) Note that the devices sharing either the same row or column experience half of the full bias applied across source and drain. The disturbance shows fluctuations, however, no evidence of systematic drift of the conductance state is observed. Similar behavior has been observed when we select (2,1) device as shown in Fig. S3(b). The random fluctuation of the disturbed devices are different. This is due to the fact that the pulse is not optimized for individual devices and the half bias may induce different amount of disturbance for each device.

[S1] T. Gokmen and W. Haensch, Frontiers in neuroscience **14** (2020).

[S2] H. Kim, M. Rasch, T. Gokmen, T. Ando, H. Miyazoe, J.-J. Kim, J. Rozen, and S. Kim, "Zero-shifting technique for deep neural network training on resistive cross-point arrays," (2019), arXiv:1907.10228 [cs.ET].

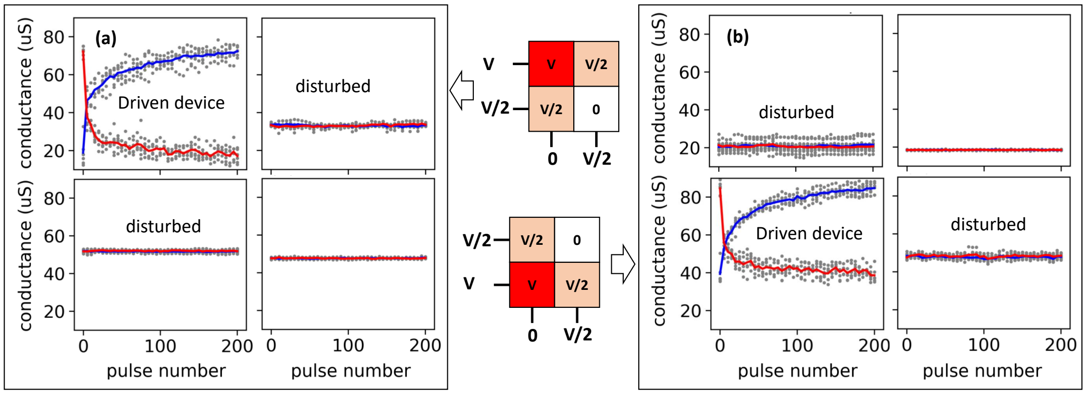

FIG. S3. (a) (row,column)=(1,1) device is selected and full bias response for upward/downward pulse is clearly observed. (1,2) and (2,1) devices are half-selected, respectively. A random fluctuation has been observed. (2,2) device is unselected and no fluctuation has been observed. (b) Similar experiment is carried out but by selecting (2,1) device. The device has been tested under 5 super cycles of upward/downward pulse sequences, and the response is indicated as gray symbols. The averaged upward/downward pulse responses are indicated as blue/red solid line, respectively.