Supplementary Material

# Supplementary Data

# Supplementary Figures and Tables

## Supplementary Figures

**Supplementary Figure 1.**

صورة تحتوي على رسم بياني, مستطيل, خطة, ميدان/ مربع

تم إنشاء الوصف تلقائياً

Fig. 1: The schematic of MRL-based logic gates

(a) AND, (b) NAND, (c) OR and (d) NOR

**Supplementary Figure 2.**

**صورة تحتوي على نص, رسم بياني, خط, تخطيط**

Fig. 2: The I-V curve of the  memristor device. Current flows through the device from the bar side, the resistance of the device decreases (SET process). Current enters from the non-bar side, the devices resistance increases (RESET process)

**Supplementary Figure 3.**

صورة تحتوي على رسم بياني, خط, رسم تقني, التصميم

تم إنشاء الوصف تلقائياً

Fig. 3: The schematic diagram of the leaky integrate-and-fire model.

**Supplementary Figure 4.**

**صورة تحتوي على نص, رسم بياني, لقطة شاشة, خطة

تم إنشاء الوصف تلقائياً**

Fig. 4: The Schematic of the proposed MRL-based LIF neuron

**Supplementary Figure 5.**

صورة تحتوي على رسم بياني, رسم تقني, رسم, خطة

تم إنشاء الوصف تلقائياً

Fig. 5: The time diagrams for the proposed MRL-based LIF neuron. Output of the up-down counter Q1 Q2 Q3 Q4 begins incremented /decremented as the input “Stim” generated from the synapse block. Synaptic weights accumulated until the threshold value (Vth=7) is reached when the neuron fires.

**Supplementary Figure 6.**

صورة تحتوي على خط, نص, رسم بياني, تخطيط

تم إنشاء الوصف تلقائياً

Fig.6: The action potential of the memristive LIF neuron model shows three fire events taking place as the threshold value (Vth=7) is reached and one short spike due to short current because of no input spikes to inter the up-down counter “leak behavior commences”.

**Supplementary Figure 7**

**صورة تحتوي على رسم بياني, الخط, رسم, خط

تم إنشاء الوصف تلقائياً**

Fig.7: The circuit schematic for T flip-flops (TFF)

**Supplementary Figure 8.**

صورة تحتوي على رسم بياني, خطة, رسم تقني, تخطيطي

تم إنشاء الوصف تلقائياً

Fig.8: The circuit schematic of the memristor-based TFF

**Supplementary Figure 9.**

صورة تحتوي على نص, رسم بياني, خطة, رسم تقني

تم إنشاء الوصف تلقائياً

Fig.9: The circuit schematic of the memristor-based 4-bit comparator.

## Supplementary Tables

Table 1. A comparison between number of CMOS-based TFF and the proposed memristive TFF

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **TFF Design** | TGB  [22] | Modified CMOS   [22] | GDI  [22] | MRL\_ based TFF |
| **MOSFET** | 26 | 24 | 22 | 16 |
| **Memristor** | - | - | *-* | 22 |
| **Delay (Ps)** | 79.1 | 60.6 | 50.2 | 34.1 |
| **Power (µW)** | 55.3 | 42.7 | 17.5 | 12.3 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Design Element** | | **Up-down counter** | **Up- counter** | **Comparator/Synaptic** | **Comparator/Core** |
| **Device** | **MOSFET** | 34 | 32 | 16 | 16 |
| **Memristor** | 110 | 94 | 66 | 66 |

Table 2. Number of all devices in the proposed design of the Memristive LIF neuron