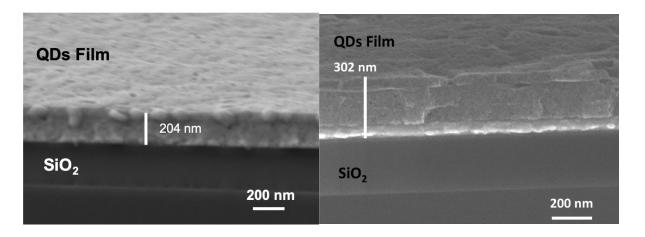
Implementation of Metallic Vertical Interconnect Access in Hybrid Intercalated Graphene/Quantum Dot Photodetector for Improved Charge Collection

Supporting Information

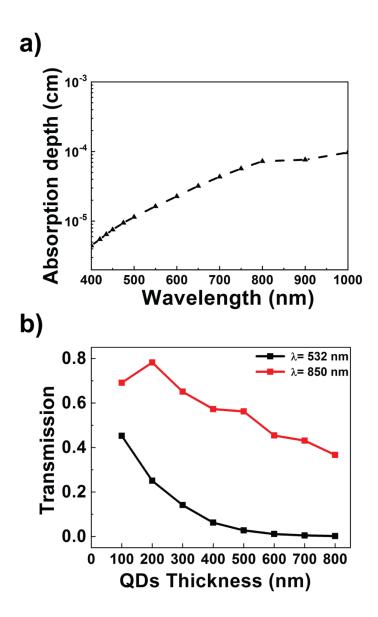
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Supp-Info SI.1: SEM images of QDs film

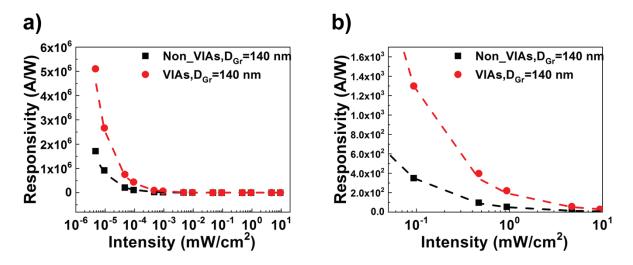


Cross-section of QD films. Left: Bottom Device consisting of a graphene followed with 10 layers of PbS QDs on top. The measured thickness of the film is ~204 nm. This indicates that each layer is ~20 nm thick. **Right**: Intercalated Gr/QD devices fabricated by repeating the deposition of 1 layer of CVD graphene and 3 layers of PbS QDs sequentially into 5 stacks, for a total of 15 PbS QD layers. The total measured thickness is ~302 nm, giving a measured graphene interspacing of $D_{Gr} \approx 302/5 = 60.4$ nm From these results we assume that the thickness of each individual QD layer is ~20 nm. We neglect the contribution of graphene to the device thickness.



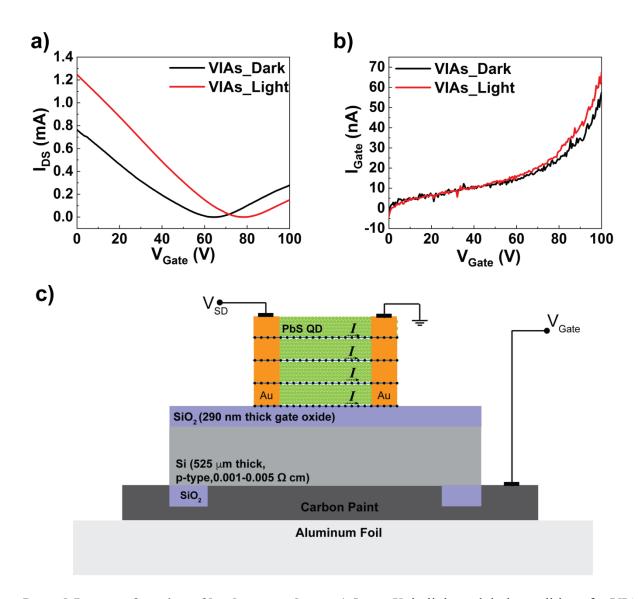
a) Light penetration depth in PbS QDs film: Penetration as a function of wavelength was extracted from transmission of light as a function of thickness of PbS QDs films by fitting to the Beer-Lambert Law. b) **Transmission vs thickness.** Transmission for λ =532 nm and λ =850 nm light for quantum dot films with band gap at λ =1000 nm used in this work. Visible λ =532 nm light is strongly absorbed with a 200 nm thick film with only 22% transmission. However, with λ =850 nm light, a significant amount of light is wasted, with large 80% transmission at 200 nm thickness. Going to thicker films it would be possible to absorb more NIR light.

Supp-Info SI.3: Photoresponse dependence on light intensity



Photoresponse dependence on light intensity: Photoresponsivity increases as incident power decreases. Same data as Figure 4.c but plotted in log-linear scale: a) Light intensity from 10⁻⁶ to 10 mW/cm², and b) Light intensity from 10⁻¹ to 10 mW/cm².

Supp-Info SI.4: I_{Ds} and I_{Gate} as a function of back-gate voltage



 I_{DS} and I_{Gate} as a function of back-gate voltage: a) I_{DS} vs V_G in light and dark conditions for VIAs devices. b) I_{Gate} vs V_G in light and dark conditions for VIAs devices, indicating that the leakage through the back gate is minimal with respect to the main drain current in a). c) Schematic configuration of back-gated VIAs device, backside SiO₂ was partially scratched and attached to aluminum foil by carbon paint. The gate voltage was applied to the aluminum foil.