Supplementary Materials for

Reservoir computing using dynamic Solid Electrolyte Based Device for temporal data classification

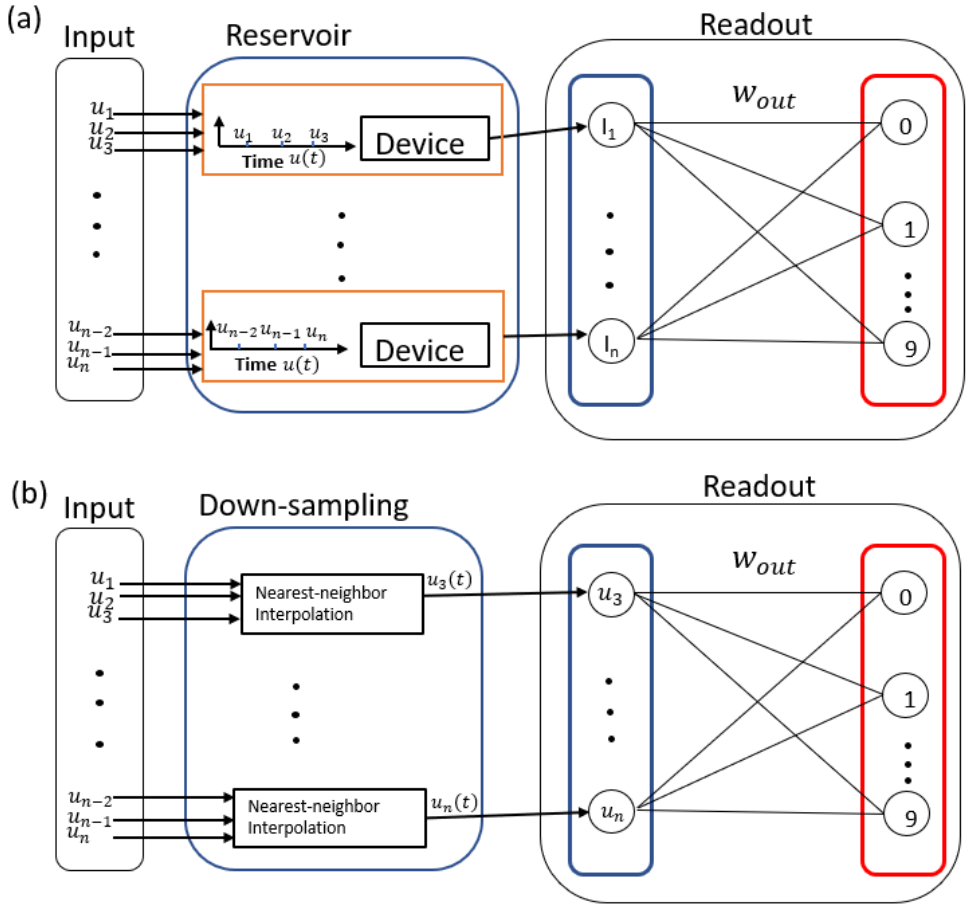

Figure S1. (a) An RC system in which the input is converted into a temporal sequence and then into a voltage pulse stream that is fed to the device. The device conductance is measured only once at the end of each sequence (b) a conventional network with a down-sampling function. The down-sampling function uses Nearest-neighbor interpolation to compress a group of multiple inputs into a single output (which is dependent on the last input in the sequence. This clearly doesn't preserve the temporal information). This is then fed to the readout function.

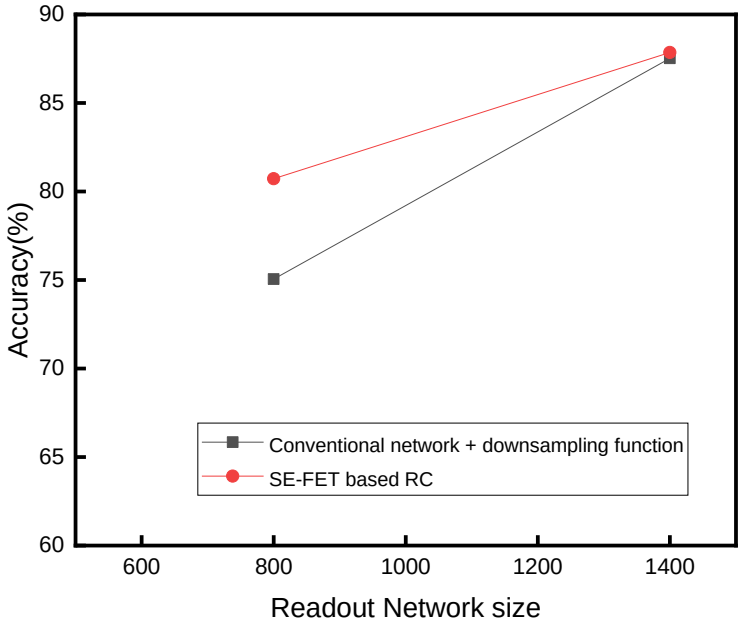

Figure S2. Learning accuracy vs. network size for an RC system based on a SEFET (Fig.S1(a)) and a conventional network with a down-sampling function (Fig.S1(b)). The smaller readout network size of 800(80 features*10 output i.e. (0 to 9 digit) and 1400(140*10) is the result of reducing the input image of dimension 24*20 to 4*20 (containing 80 features) and an image of size 21*20 to 7*20(containing 140 features). This is achieved by reading the 6-bit and 3-bit sequence only once at the end of each sequence, respectively in the RC system. For the conventional network with a down-sampling function, the same sized readout network is obtained by down-sampling the input image in a ratio of 6 to 1 and 3 to 1 using Nearest-neighbor interpolation. With a smaller readout network, the SE-FET-based RC system outperforms the conventional network with a down-sampling function. However, for a larger readout network, there is no significant difference between a conventional network and an RC system, as less down-sampling is involved. Similar results are reported by Du et al (2017).

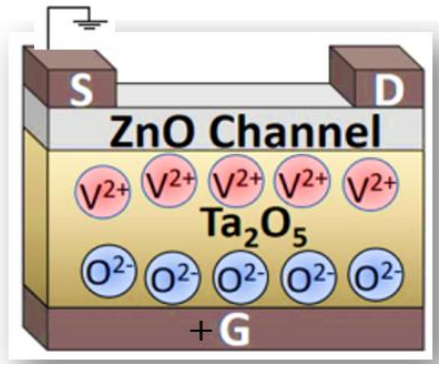

Figure S3. Schematic of a Ta_2O_5/ZnO SE-FET device, showing charge separation of oxygen ions and vacancies at respective opposite interfaces of the Ta_2O_5, upon application of an applied gate voltage(Pillai and De Souza, 2017; Kumar et al., 2018; Song et al., 2019).

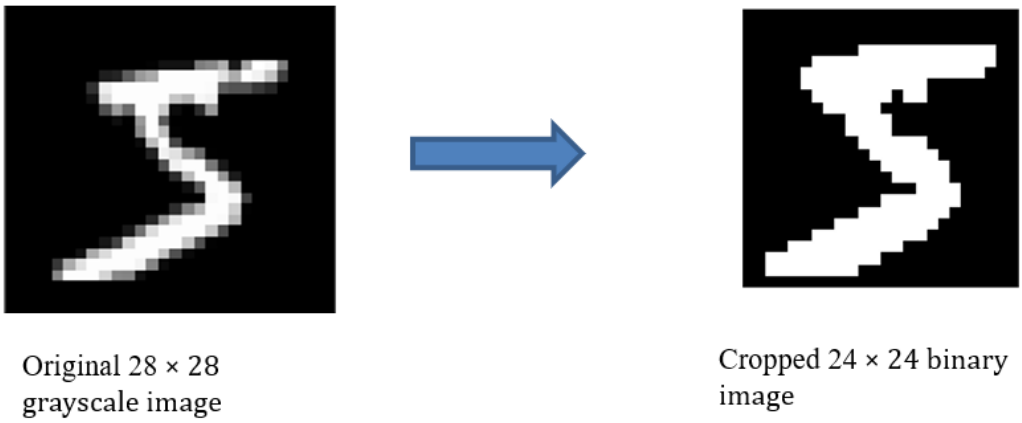

Figure S4. MNIST image of digit 5 as an example. The original grayscale images of size 28 × 28 were pre-processed to a binary image cropped to size 24× 24 by removing the unused area.

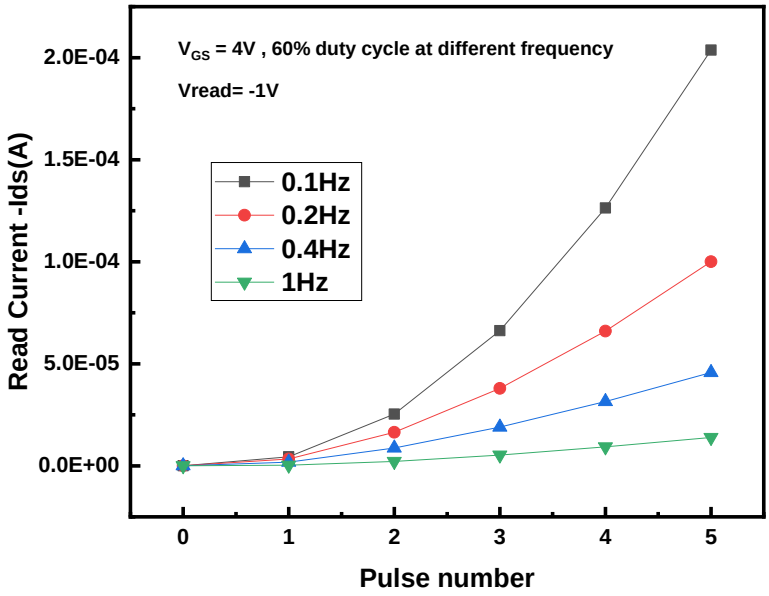

Figure S5. Potentiation of conductance in the SE-FET for different frequencies with respect to the number of pulses.

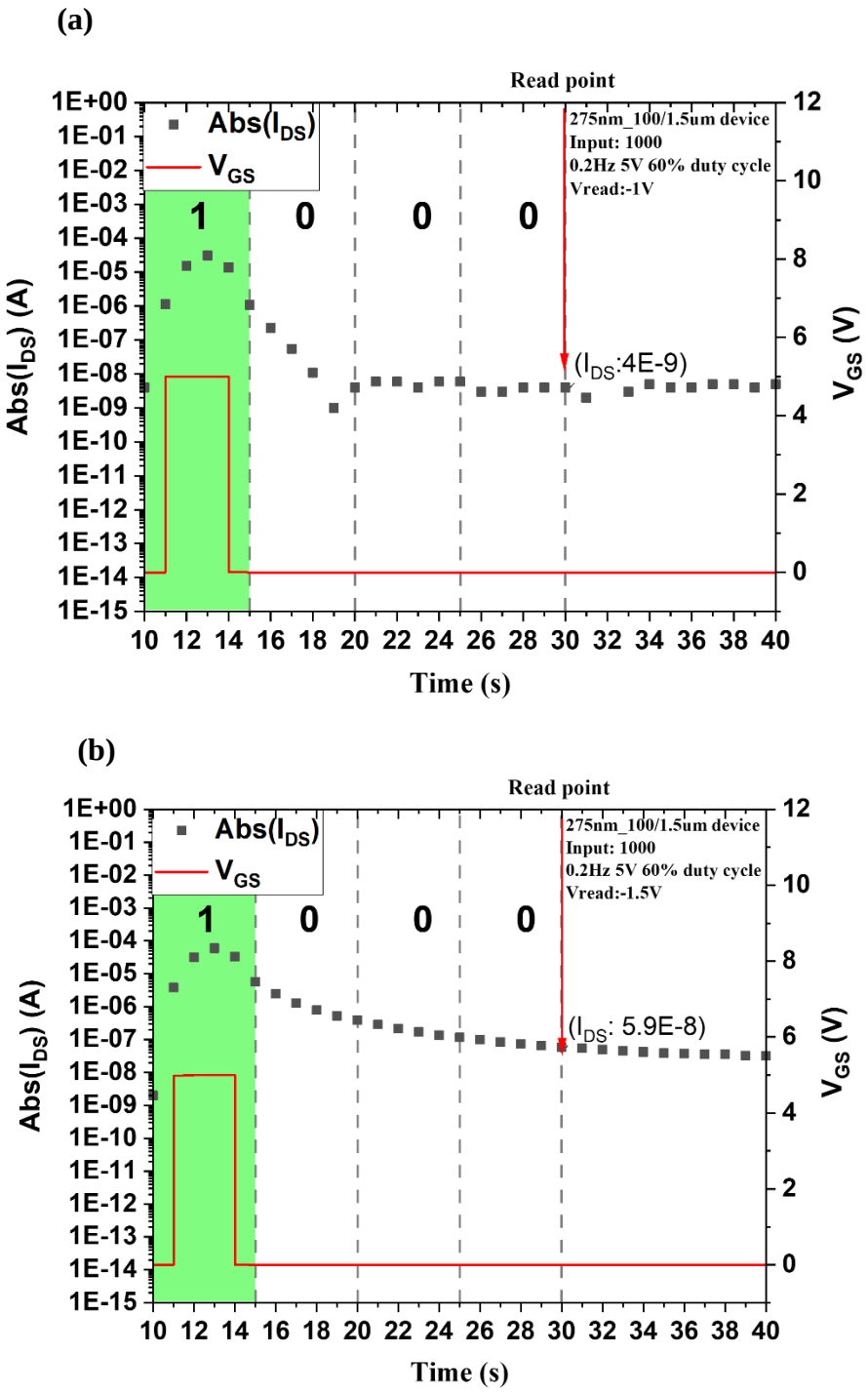

Figure S6. Short-term memory (a) After a write pulse of 5V a periodic read voltage of -1V is used to monitor the fading of memory which takes approx. 5 seconds to revert to the initial state. (b) A read voltage of -1.5V results in an almost infinite fading time. These results show that a negative read voltage can be used to adjust the time constant of memory fading.

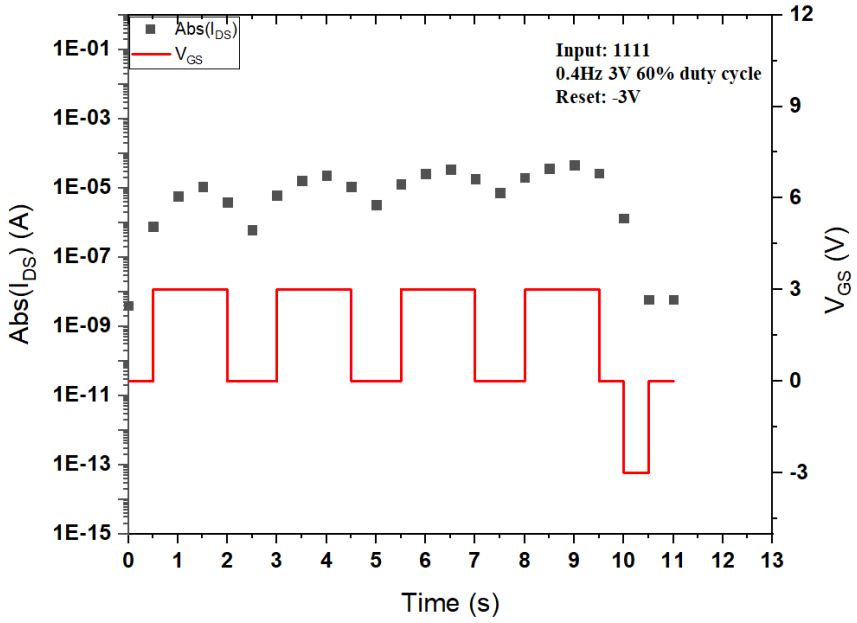

Figure S7. The SE-FET device is reset to the initial state by using a small reset pulse of -3V with a pulse width of (0.5s) after an input sequence of '1111'.

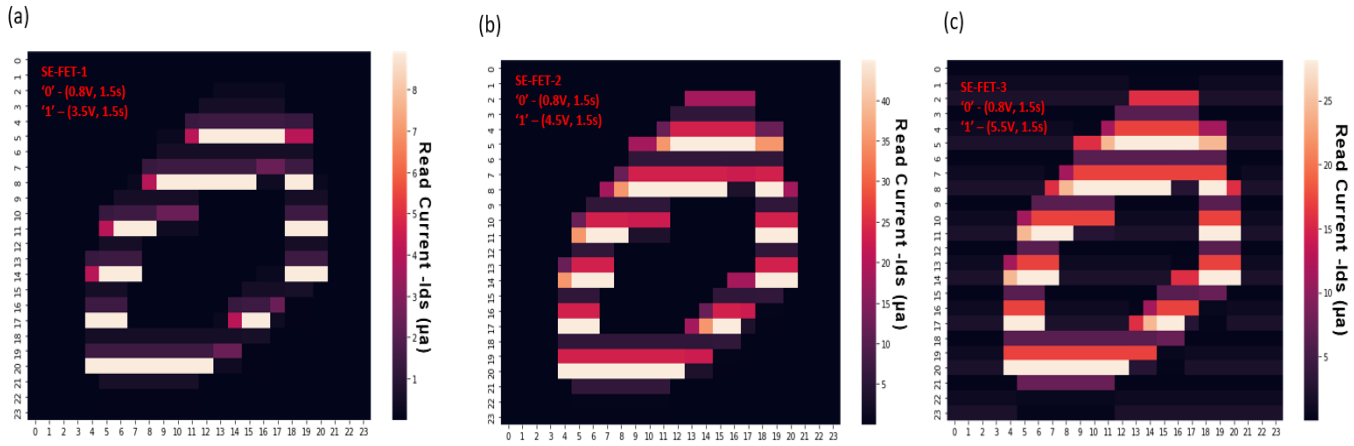

Figure S8. The heatmap of the complete recorded output response of digit 0 for three different devices. The difference in magnitude of the read current ranging from (0 - ~60µa) and device-to-device variability increases the reservoir dimensionality. (a) Response of device 1, when subjected to (0.8V, 1.5s) for '0', bit and (3.5V, 1.5s) for '1' bit. (b) Response of device 2, when subjected to (0.8V, 1.5s) for '0', bit and (4.5V, 1.5s) for '1' bit. (c) Response of device 3, when subjected to (0.8V, 1.5s) for '0', bit and (5.5V, 1.5s) for '1' bit.

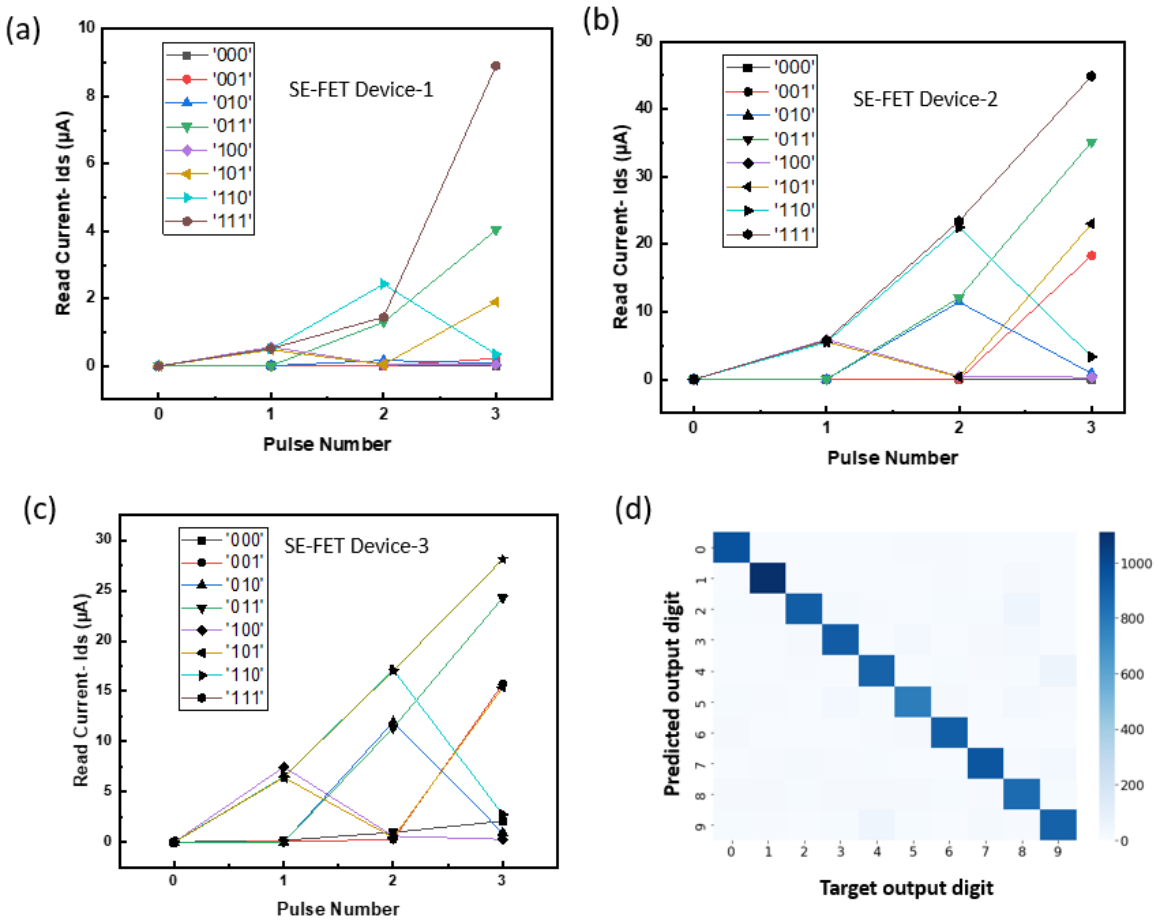

Figure S9. Response of 3 different SE-FET devices when subjected to all possible combinations of 8 different temporal inputs showing similar trends as well as device-to-device variability. (a) Response of device 1 when subjected to 0.8V for '0' bit and 3.5V for '1' bit. (b) Response of device 2 when subjected to 0.8V for '0' bit and 4.5V for '1' bit. (c) Response of device 1 when subjected to 0.8V for '0' bit and 5.5V for '1' bit. (d) The confusion matrix shows the experimentally obtained classification results for the SE-FET-based reservoir computing system using all three devices with the same voltage combining horizontal (row-wise) + vertical (column-wise). An overall mean recognition of 94.44% is achieved.

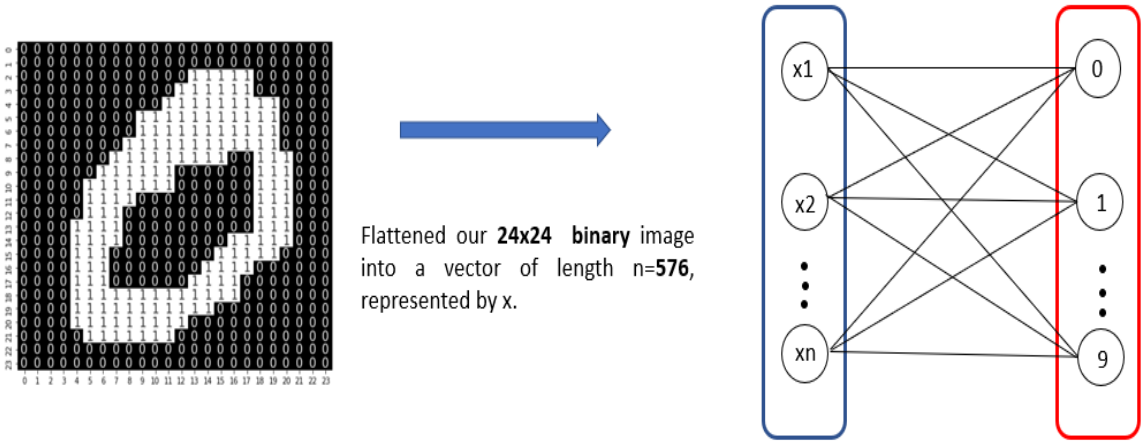

Figure S10. Hand-written digit recognition using conventional network: A preprocessed binary MNIST image of digit '0' is shown as an example. The original grayscale 28 × 28 image is pre-processed to a binary format and cropped to 24× 24 removing the unused area. Then the image was flattened into a vector of length n=576, represented by x that was trained using Logistic Regression.

Table s1. The comparison of all the different approaches of implementing a dynamic SE-FET-based RC system to that of the fully connected conventional network.

	Conventional network	SE-FET based reservoir computing system	SE-FET based reservoir computing system- with different gate voltages for each device	SE-FET-based reservoir computing system- with the same gate voltage for each device.	SE-FET based reservoir computing system- with different gate voltages for each device- horizontal + vertical scan	SE-FET-based reservoir computing system- with the same gate voltage for each device- horizontal + vertical scan
Mean accuracy	**90.82%**	**91.19%**	**92.44%**	**92.97%**	**94.26%**	**94.44%**
standard deviation	**0.61%**	**0.54%**	**0.57%**	**0.52%**	**0.46%**	**0.42%**
Sequence Length	**-**	**4-bit**	**3-bit**	**3-bit**	**3-bit**	**3-bit**
Number of devices	**-**	**1**	**3**	**3**	**3**	**3**

Reference

Du, C., Cai, F., Zidan, M. A., Ma, W., Lee, S. H., and Lu, W. D. (2017). Reservoir computing using dynamic memristors for temporal information processing. *Nat. Commun.* 8, 1–10. doi:10.1038/s41467-017-02337-y.

Kumar, A., Balakrishna Pillai, P., Song, X., and De Souza, M. M. (2018). Negative Capacitance beyond Ferroelectric Switches. *ACS Appl. Mater. Interfaces* 10, 19812–19819. doi:10.1021/acsami.8b05093.

Pillai, P. B., and De Souza, M. M. (2017). Nanoionics-based three-terminal synaptic device using zinc oxide. *ACS Appl. Mater. Interfaces* 9, 1609–1618. doi:10.1021/acsami.6b13746.

Song, X., Kumar, A., and De Souza, M. M. (2019). Off-State Operation of a Three Terminal Ionic FET for Logic-in-Memory. *IEEE J. Electron Devices Soc.* 7, 1232–1238. doi:10.1109/JEDS.2019.2941076.