Views

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Patterning roadmap: 2017 prospects

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Abstract: Road mapping of semiconductor chips has been underway for over 20 years, first with the International Technology Roadmap for Semiconductors (ITRS) roadmap and now with the International Roadmap for Devices and Systems (IRDS) roadmap. The original roadmap was mostly driven bottom up and was developed to ensure that the large numbers of semiconductor producers and suppliers had good information to base their research and development on. The current roadmap is generated more top-down, where the customers of semiconductor chips anticipate what will be needed in the future and the roadmap projects what will be needed to fulfill that demand. The More Moore section of the roadmap projects that advanced logic will drive higher-resolution patterning, rather than memory chips. Potential solutions for patterning future logic nodes can be derived as extensions of 'next-generation' patterning technologies currently under development. Advanced patterning has made great progress, and two 'next-generation' patterning technologies, EUV and nanoimprint lithography, have potential to be in production as early as 2018. The potential adoption of two different next-generation patterning technologies suggests that patterning technology is becoming more specialized. This is good for the industry in that it lowers overall costs, but may lead to slower progress in extending any one patterning technology in the future.

Keywords: EUV; IRDS; ITRS; nanoprint technology; roadmap.

1 Introduction

The International Technology Roadmap for Semiconductors (ITRS) (http://www.itrs.net/) was published every year for almost 20 years (i.e. 1998 to 2013). The roadmap projected semiconductor technology progress for a 15-year period and included sections on system integration, device properties, process technologies such as lithography and metrology, process integration and interconnect, packaging, and many other areas. Seventeen International Technology Working Groups (ITWG) were responsible for each of these roadmaps. The ITRS roadmap was reorganized in 2014 and published in 2015 to more closely represent the new ecosystem of the Electronics Industry.[1] In 2016, the International Roadmap for Devices and Systems (IRDS) was introduced.[2] The IRDS roadmap is more top-down driven, while the ITRS roadmap was more bottom-up driven.

The ITRS roadmap was driven by semiconductor producers. There were many of these producers, and there were many tool and material providers. One of the key functions of the roadmap was to communicate expected future chip needs to the many potential providers of future tools and materials. This enabled vendors to focus their efforts on what their customers considered their key challenges, which provided better research and development results to the industry. Over the many years, the roadmap has been published, the semiconductor industry and its suppliers have undergone tremendous consolidation. Tool vendors have also consolidated. The reasons for this consolidation will not be discussed here, but the practical consequence is that now only a few large companies are doing leading-edge development of semiconductor process technologies, and many of their key suppliers have also become large companies with only two or three companies developing new leading-edge tools of a particular type. The necessary intercompany interactions to drive and develop a new, say, etcher tool, are many fewer than there used to be. Companies like Intel can talk directly to their key suppliers without the need of a roadmap, and so semiconductor companies are much less interested in contributing to a public industry-wide roadmap.

On the other hand, there is still a need for a roadmap. Research institutions, such as universities that do research that might apply to semiconductor production,

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1 http://www.itrs2.net/itrs-reports.html.

2 see http://irds.ieee.org.

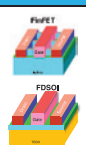
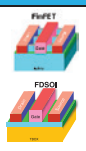
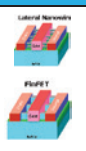
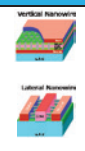
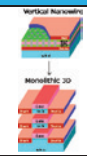
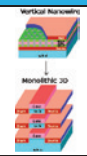
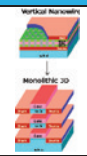
YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA VGAA	VGAA M3D	VGAA M3D	VGAA M3D
							

Figure 1: Projected logic device architectures from the 2015 roadmap.

want to know industry trends and forecasts. Governments and industry associations that worry about the future of various industries also want to know such information. Chip customers can now design or have chips designed for them without having to interface with traditional semiconductor companies. These companies need to understand what is possible in the future and what is not. This new ecosystem is what led to the development of the IRDS roadmap. The IRDS roadmap is developed by focusing on the larger factors influencing device needs. It has different focus teams that take inputs on the large-scale factors influencing future computing needs and turn those inputs into individual roadmaps. Such factors are the growth of big data, the need for bigger and more efficient cloud computing, the need for better connectivity, and so on. The traditional chip scaling roadmap is part of the 'More Moore' section of the roadmap. In the More Moore focus team, the future semiconductor performance needed to meet industry needs is projected, and then technical projections of the chip technology needed to meet these goals are prepared. The IRDS roadmap also has other sections that reflect the expanded and diverse current world of semiconductor applications. They are 'Application Benchmarking', 'System and Architecture', 'Outside System Connectivity', 'Beyond CMOS', 'Packaging Integration', and 'Factory Integration'.

2 Patterning needs of the new roadmap

In the More Moore team, we try and understand future chip needs for higher performance and predict the device changes that follow logically from these needs. The results of this exercise are clear. Continual change in logic device architecture will be needed to drive better chip performance. Figure 1 below shows the sorts of new devices predicted by this roadmap.[3]

The roadmap shows leading-edge logic devices moving from finFET design to lateral nanowires to vertical nanowires and finally to monolithic 3D, where logic devices are stacked on top of each other. The reason for the device structure changes is that simple shrinks of current device designs will give too many undesirable side effects, such as high power consumption due to increased 'leakage', to be feasible. At some point in the 2020s, scaling up by stacking devices on top of each other will take over from scaling sideways, and at that point, logic device minimum half pitches will probably stop shrinking and may even get bigger. This change from lateral scaling to vertical scaling is already happening for flash memory. Rather than just putting two or four layers of memory cells on a flash chip, the industry opted to use much larger memory bit sizes but still get improved bits per chip using 24 layers of devices or more. Scaling of 3D flash to provide more bits per chip is expected, but even if minimum dimensions shrink, they will still be far larger than the current 2D flash minimum dimensions. DRAM memory continues to shrink, but the projected change in dimensions is slower than that for logic devices. High-performance logic devices are expected to be the types of chips that drive new patterning requirements.

Figure 2 shows projected logic device ground rules from the 2016 IRDS Roadmap.[4] The vertical gate all around structures are likely to drive the formation of sub-10-nm hole-type features, and the requirements of metal levels are likely to drive the patterning of 10-nm lines and spaces or smaller. With these projected ground rules in mind, let us look at how various patterning technologies might

3 http://irds.ieee.org/images/files/pdf/2016_MM.pdf.

4 See http://irds.ieee.org/images/files/pdf/2016_MM.pdf and notes therein.

LOGIC DEVICE GROUND RULES	2015	2017	2019	2021	2024	2027	2030
MPU/SoC Metalx ½ Pitch (nm)	28.0	18.0	12.0	10.0	6.0	6.0	6.0
MPU/SoC Metal0/1 ½ Pitch (nm)	28.0	18.0	12.0	10.0	6.0	6.0	6.0
Contacted poly half pitch (nm)	35.0	24.0	21.0	16.0	12.0	12.0	12.0
L_g: Physical Gate Length for HP Logic (nm)	24	18	14	10	10	10	10
L_g: Physical Gate Length for LP Logic (nm)	26	20	16	12	12	12	12
Channel overlap ratio - two-sided	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Spacer width (nm)	12	8	6	5	4	4	4
Contact CD (nm) - finFET, LGAA	22	14	16	12	11	11	11
Device architecture key ground rules							
FinFET Fin Half-pitch (new) = 0.75 or 1.0 M0/M1 (nm)	21.0	18.0	12.0				
FinFET Fin Width (nm)	8.0	6.0	6.0				
FinFET Fin Height (nm)	42.0	42.0	42.0				
Lateral GAA Lateral Half-pitch (nm)			12.0	10.0			
Lateral GAA Vertical Half-pitch (nm)			12.0	9.0			
Lateral GAA Diameter (nm)			6.0	6.0			
Vertical GAA Lateral Half-pitch (nm)				10.0	6.0	6.0	6.0
Vertical GAA Diameter (nm)				6.0	5.0	5.0	5.0
Device effective width - (nm)	92.0	90.0	56.5	56.5	56.5	56.5	56.5
Device lateral half pitch (nm)	21.0	18.0	12.0	10.0	6.0	6.0	6.0
Device width or diameter (nm)	8.0	6.0	6.0	6.0	5.0	5.0	5.0

Figure 2: 2016 IRDS projected logic device ground rules.

meet these projected requirements. Note that spacer width is a process-derived dimension, not a lithographically printed dimension.

3 Next Generation Patterning Techniques

3.1 Multiple patterning (MP)

There is not really a need for a 'multiple patterning' roadmap. Multiple patterning is an established technology that is extremely powerful. Shrinking the pitch of lines and spaces by double patterning or extending double patterning to quadruple patterning brings a pitch reduction of up to 50%, which is the equivalent of two generations of 30% node-to-node critical dimension shrinks. All the line and space dimensions through 2021 in Figure 2 can be met with ArF immersion lithography and quadruple patterning. With enough development, the dimension shown for metal levels in 2024 and beyond could be done with octuple patterning. Via, contact or other hole type levels can also be made using multiple patterning, and the same principle applies to them, although more multiples than quadruple are needed earlier in the roadmap.

However, continual extension of multiple patterning brings cost issues and extreme process complexity. Multiple patterning does not improve overlay either. If multiple patterning is done using an ArF immersion scanner, you get the overlay that scanner can provide, only worse, because the additional sources of edge placement error from all the patterning steps require better control of the original image pattern placement. As overlay requirements scale with the final CDs after the multiple patterning is finished, this is a big issue for semiconductor producers. Alternatives to multiple patterning are needed not to enable smaller resolution, but to improve cost, process complexity, and/or enable better overlay. These issues with multiple patterning affect high-performance logic chips the most, both because of their tight overlay requirements and because of the patterning complexity needed for these devices.

3.2 Extreme ultraviolet lithography (EUVL)

EUVL is a form of projection lithography that uses 13.5-nm radiation. This radiation requires imaging in a vacuum and an all-reflective optical system using specially designed multilayer reflective mirrors. The mirrors' reflectivity is around 65%, and there are at least 10 of them in the optical path from source to wafer, so the actual imaging power is much lower than the input power from the imaging source. The development of suitable sources for EUV imaging tools was much slower than originally projected. Production-grade tools with sufficient power to enable usable scanner throughput became available last year.[5] Production development for logic chip use is underway, with an earliest possible

5 See the article by I. Fomentov in this issue of Advanced Optical Technology on page 173.

implementation in 2018. The driving forces for their adoption is improvement in process simplicity by reducing the need for multiple patterning and improvement in chip production cycle time by reducing total process steps. EUV has the potential to address the smallest CDs in Figure 2 above, if combined with multiple patterning or DSA.

There are still issues that must be resolved. Line roughness and contact hole size uniformity are issues because of the small size of the features being printed combined with shot noise and resist stochastics. Defectivity in manufacturing is another concern, particularly as no manufacturing-grade pellicle is yet available, although development efforts are underway.[6] EUV resist improvements are strongly desired by the industry to improve line width roughness and enable thinner imaging films. A reliable supply of low-defect EUV masks may also be a concern.

3.3 Nanoimprint (NIL)

NIL is a technology of creating a pattern using a kind of stamping process. A flexible 1X mask with indentations in the size and shape of the desired features is used to form and cure a relief pattern on a wafer.[7] It has excellent pattern fidelity and promises low cost, but had issues with overlay, mask making and inspection, and defects. It has excellent resolution, but these other issues prevented implementation until now. However, the overlay and defects have shown great progress, and the currently accessible mask dimensions are suitable for 3D flash memory production. Manufacturing introduction for 3D flash memory is possible as early as 2018. The driving force for this is improved cost compared to other patterning options. Implementation for other sorts of semiconductor chips would require substantial improvements in overlay, and in patterning and inspection of 1X masks.

3.4 Maskless lithography (ML2)

Maskless lithography involves using an ebeam writing tool to pattern directly in resist without using a mask. In order to get sufficient writing speed, thousands of small ebeams must be written at once. The key issue is to develop a reliable tool that can scan many individual beams with controllable blanking, that is, turning individual beams on and off whenever necessary to get a random pattern written. Designs for these tools depend on specialized semiconductor chips with multiple built-in ebeam emitters that are the actual electron sources for the writing. Development of such a tool for mask making has been demonstrated.[8] Work is underway to make such a tool that will write semiconductor chip applications.[9] The tool's resolution capability is determined by the overall design. The current leading effort, MAPPER, is targeted at 32-nm critical dimension. This is not small enough for the critical levels of logic chips now in development. However, the ability to personalize chips and write different chips on the same wafer is an important way to reduce the cost of small-volume products. The MAPPER is currently working on improving the reliability of the beam-generating chip. Success in this would be a key milestone. The successful overall development of such a direct-write tool could enable widespread use of such tools in specialized applications.

3.5 Directed self assembly (DSA)

Directed self-assembly uses certain types of polymers that can separate into different phases of controlled sizes when annealed. Over time, the critical dimensions of leading-edge chips have shrunk to the point where they are accessible via this technique. The technique requires using guide features patterned by some patterning method, usually ArF immersion lithography. So far, it only gives very simple repeating patterns, necessitating additional patterning steps to, say, 'cut' large patterns of long lines and spaces into lines of usable lengths for semiconductor circuits. Nonetheless, it promises to be a cheaper way to multiply pattern density than other available methods. A lot of work has been done on this up to the point of making functioning test chips using DSA for some patterns.[10] However, two issues that remain are defects

6 See the article by D. Brouns in this issue of Advanced Optical Technology page 221.

7 See the article by Choi and Resnick and the article by Landis and Teyssdre in this issue of Advanced Optical Technology page 229 and page 277.

8 http://semiengineering.com/executive-insight-elmar-platzgummer/ and http://www.ims.co.at/wp-content/uploads/2017-02-15_IMS-JEOL-press-release-on-MBMW-101.pdf.

9 See, for example, G. DeBoer, M. Dansberg, J. Peijster, E. Slot, S. Steenbrink, et al., 'MAPPER: Progress Towards a High Volume Manufacturing system', Proc. of SPIE, Vol. 8680, · doi: 10.1117/12.2011486.

10 C. Liu, C. Estrada-Raygoza, H. He, M. Cicoria, V. Rastogi, et al., 'Towards Electrical Testable SOI Devices Using Directed Self-Assembly for Fin Formation', Proc. of SPIE, Vol. 9049, doi: 10.1117/12.2046462.

and pattern placement. Defects are a particular problem because, so far, there are some defects that are not detectable until after etch, making rework impossible. DSA has some variability in the position of a contact hole or line not directly connected to an alignment feature, which is one of the causes of pattern placement error. These issues have not been resolved well enough yet to permit volume manufacturing. The original material system widely used for DSA, PS-b-PMMA, has probably missed the window for implementation. Newer polymer systems that print smaller features than are reachable with PS-b-PMMA are probably needed to reach the critical dimensions now under development.

4 Path forward

It was once an article of faith and a practical reality that once a better patterning technology came along, everyone who wanted to make more advanced chips would use it. This can no longer be assumed. Different types of chip production could use different patterning solutions. It is quite possible that 3D flash memory will use nanoimprint for many levels, while high-performance logic chips will use EUV lithography for some levels. 2D flash memory and DRAM could continue to be made by multiple patterning. If direct-write ebeam lithography tools for chips are successful, small-volume products could use multiple patterning for creating a common pattern of devices followed by ebeam direct write for chip personalization. Thus, several technologies could be successful, but with a smaller market for each than might have been hoped for. This is a form of patterning specialization, which is good for reducing industry costs; but could provide a long-term financial strain for the vendors that supply patterning tools and materials. Already there is only one EUV exposure tool supplier, and there are likely to be fewer successful EUV resist vendors than there were successful ArF resist vendors.

In the IRDS roadmap for chips, much of the projected improvement in performance or capability comes from the implementation of new design features, such as lateral nanowires, and improved wiring and contact designs, rather than from shrinking of critical dimensions. There are upcoming challenges in logic devices for printing the smallest metal lines and for patterning holes for vertical gate all around structures. These can potentially be addressed through extensions of the techniques described above, for example, by the combination of EUV and multiple patterning, by DSA techniques or by EUV using higher NA tools. Flash memory is already scaling to higher device density by adding layers to 3D flash structures, rather than by critical dimension shrinks. In 10 years, logic devices could be scaling this way, too. Improvements in patterning technology will not stop happening, but they could slow down in pace, both because there is less need for them and because of consolidation in the vendor supply chain.

5 Summary and conclusions

Developers of new patterning technologies have made remarkable progress. Of the four 'next-generation' technologies typically mentioned in lithography roadmaps,[11] two of them, EUV lithography and nanoimprint, could be in production as early as next year. This is despite the tremendous success and extendibility of multiple patterning techniques, techniques that will continue to be used. Further extension of these patterning devices to smaller critical dimensions needed by future high-performance logic chips is expected.

The driving forces for improved semiconductor chips have changed. Instead of driving chip progress by enabling smaller dimensions, chip progress is mostly driven by introducing new types of chips and new types of devices. These new types of devices enable the industry to take advantage of advances in patterning technology. The tremendous success of lithography has made it possible for the chip industry to do this and to count on the patterning capability to do this. This has led the ITRS roadmap to evolve into the IRDS roadmap, where the roadmap is driven top-down more than bottom-up. The latest IRDS roadmap projects further device changes that will need further patterning improvements to implement. The new patterning technologies needed for this are already under development.

Acknowledgments: My thanks to Paolo Gargini and Mustafa Badaroglu for helpful discussions.

11 See, for example, M. Neisser and S. Wurm, 'ITRS lithography roadmap: 2015 challenges', Advanced Optical Technologies. Volume 4, Issue 4 doi: 10.1515/aot-2015-0036 and M. Neisser and S. Wurm, 'ITRS lithography roadmap: status and challenges', Advanced Optical Technologies, Volume 1, Issue 4, Pages 217–222 (2012).

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