



# Dual-Mode Memristor Synaptic Circuit Design and Application in Image Processing

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Memristor is a kind of synaptic element with nanometer size and continuously variable memristance. The bridge synaptic circuit constructed by the memristor has a simple structure and precise control. In practice, because of the non-linear characteristics of memristor, it is not easy to control synaptic circuit and errors in weights appear. Therefore, a novel memristor synaptic circuit is proposed in this paper, called the dual-mode memristor bridge synaptic neural network. The proposed method can make the weights more linear by controlling the input voltages and make the outputs more linear by using symmetrical positive and negative pulses. Therefore, the proposed synaptic circuit is easier to be controlled. In this paper, the numerical simulations are conducted and verify the feasibility. Furthermore, the simulation experiments are conducted for edge extraction of grayscale birds' images in the airport for bird recognition applied for the bird repelling applications.

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# INTRODUCTION

Artificial neural networks have always been a hot field of research. Since the human brain has hundreds of millions of neurons and synapses [1], it is very important to realize synaptic circuits in order to build a machine similar to the brain. Due to the dynamic characteristics of synapses and the requirements of nanometer size, it is difficult to make breakthroughs. It was not until the emergence of the memristor that it brought new developments in the fields of electronics and neuroscience [2]. Memristor is a basic circuit element proposed by Professor S. T. Cai in 1971 based on the complete principle of the circuit theory system. In 2008, scientists working in the HP laboratory developed a physical model of the memristor [3] and verified the memristor's passiveness, non-linearity, nanoscale size, information non-volatility, and other characteristics through physical experiments. Because the memristor has unique physical characteristics, it can be used in many fields such as artificial neural networks and image processing [4–7].

In artificial neural networks, a large number of research results indicate that the memristor can be used to simulate artificial synapses [8, 9]. Furthermore, because of its characteristics, the memristor synaptic circuits are promising. Among them, the most widely studied analog synapse structure is a memristive bridge structure, which has the advantages of simple structure, precise control, and high integration. In the cellular neural network [10], weight simulation can be realized by digital multiplication circuits and analog multiplication circuits. For the traditional CMOS digital multiplication circuits, they occupy large areas and consume a lot of energy. However, the bridge synapse circuits constructed by the memristor are simple and convenient and have high

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efficiency and low energy consumptions. There are two types of classic memristive bridge synaptic circuits, called type I memristive bridge circuit and type II memristive bridge circuit. Literature [11] proposed the synaptic bridge circuit composed of four identical memristors. The synaptic weight simulations are realized by controlling the relationship among four memristors. This structure can realize three types of synaptic weights such as positive, negative, and zero. Literature [12] proposed the synaptic bridge circuit composed of five identical memristors. Four memristors are used to control the weight whether positive or negative, and the last memristor realizes the simulation of synaptic weights. The circuit cannot achieve zero synaptic weight. At the same time, literature [12] also mentioned the phenomenon of non-linearization of the memristance for the simulated synapse circuit, which will cause errors of the weight in the simulation. In literature [13], the bipolar pulse method is used to overwhelm the non-linearity of the memristance. However, it uses a synaptic bridge circuit composed of five identical memristors, which cannot be expressed as zero for synaptic weight. Literature [14] proposed a bridge synaptic circuit composed of three identical memristors and two MOS transistors, which made up the deficiency that the weight of synaptic circuits could not be zero composed of five identical memristors; however, it does not overwhelm the nonlinearization of the memristor. The hardware realization for image processing has great meaning for bird repelling application for airports. Because the memristor has the characteristics of low energy consumption and fast processing speed, the neural network along with the memristor for image processing has the advantages of simple structure, low energy consumption, and fast processing speed in hardware implementation, and it can effectively solve the task of image processing of bird images in order to assist bird repelling.

Edge extraction is one of the fundamental tasks in computer vision. There are many effective and efficient methods to solve this problem; however, these methods have high complexity and are difficult to implement in hardware. Therefore, the method that combines the memristor and neural network can not only meet the hardware implementation but also complete the edge extraction tasks for vision or image processing [15–18]. Literature [17] established a neural network with memristive bridge synapses and used networks to process gray-scale images. Literature [18] proposed a memristive cellular neural network that combines a memristive device and a cellular neural network, through which the edges of color pictures can be extracted effectively. However, the above-mentioned literature adopted linear memristor models, without considering the non-linear factors of memristors.

Bird strikes are huge threats for modern civil aviation which bring about huge amounts of harm for life and economic losses. Therefore, researchers and relevant departments are currently eager to find suitable bird repellent methods. The current bird repelling generally depends on the radar to obtain bird information and then uses the corresponding bird repelling equipment. However, the information shown on the radar is only associated with approximate bird flying directions and cannot identify the type and the number of birds. The more the detailed bird information obtained, the more effective the targeted bird repelling methods adopted. The image processing method can identify bird species and the number of birds counting according to birds' images flying around or through the airports.

The main contribution of this paper is to propose a new dual-mode memristive bridge synaptic circuit to simulate synaptic weights and construct a dual-mode memristive bridge synaptic neural network by combining the dual-mode memristive bridge synaptic circuit with the cellular neural network. Furthermore, the proposed network is applied to edge extraction for images. The proposed method can better solve the weight simulation errors caused by non-linear memristor, thus speeding up the edge extraction and improving the accuracy of obtaining the cellular neural network template.

The paper is arranged as follows. In *Preliminary*, the linear and non-linear memristors are modeled mathematically, and the corresponding simulations are conducted. *Synaptic Circuit-Based on Memristor* proposes a new type of memristive bridge synapse circuit and a dual-mode memristive bridge synapse circuit. These two circuits, respectively, overwhelm the non-linearization of the synapse weights and output voltages to reduce the weight simulation errors. In the *Dual-Mode Memristive Synaptic Neural Network and its Application in Image Processing*, this paper introduces a dual-mode memristive bridge neural network, the corresponding method is performed on bird images. The last section concludes the paper.

## PRELIMINARY

#### **HP Memristor Model**

The physical model of the HP memristor is shown in **Figure 1**. It is composed of two layers of titanium dioxide  $(TiO_2)$  film sandwiched between two metal platinum electrodes.

Based on the definition in literature [3], the resistance value of the HP memristor, M(t), is defined as

$$M(t) = M_{OFF} + (M_{ON} - M_{OFF})\frac{\omega(t)}{D}$$
(1)

where  $\omega(t)$  is the thickness of the current doped layer and *D* is the total thickness of the two TiO<sub>2</sub> films.  $M_{OFF}$  and  $M_{ON}$  are the memristance limits when  $\omega(t) = 0$  and  $\omega(t) = D$ , namely, the maximum resistance value and the minimum resistance value. Substituting  $x(t) = \omega(t)/D$  into **Eqs 1**, **2** is derived:

$$M(t) = M_{OFF} + (M_{ON} - M_{OFF})x(t).$$
 (2)

For an ideal memristor model, its ion drift model is

$$\frac{dx}{dt} = \frac{\eta_v M_{ON}}{D^2} i(t) \qquad , (3)$$

where  $\eta_{\nu}$  is the constant of memristor ion mobility in the uniform field,  $\eta_{\nu} \approx 10^{-14} m^2 \cdot s^{-1} \cdot V^{-1}$ , i(t) is the current traveling the memristor.

Since the physical memristor is a nanometer-sized circuit component, the memristor can generate a huge electric field when applying a tiny voltage. Therefore, the ion movement inside the memristor owns significant non-linear characteristics. Therefore, when **Eq. 3** is multiplied by the non-linear window function, **Eq. 3** is rewritten as



$$\frac{dx}{dt} = \frac{\eta_v M_{\rm ON}}{D^2} i(t) f(x), \tag{4}$$

where f(x) is the window function.

The window function used in this paper is [4]

$$f(x) = 1 - (1 - 2x)^{2p},$$
(5)

where *p* is a positive integer and *p* is used to describe the degree of non-linearity. This paper selects p = 1 as the window function for obvious non-linearity analysis.

Mathematical models of controlled memristor mainly include two kinds. One is a charge-controlled memristor, and the other is a magnetic flux-controlled memristor. This paper mainly introduces charge-controlled linear memristor and non-linear memristor.

## Mathematical Model of Charge-Controlled Linear and Non-Linear Memristor

According to the equation  $Q(t) = \int_0^t i(t)dt$  (*Q* is the quantity of electric charge), integrating the time on both sides of **Eq. 3**, and substituting it into **Eq. 2**, then the mathematical model of the charge-controlled linear memristor is obtained in **Eq. 6**:

$$M(t) = M(0) + k_1 Q(t)$$

$$k_1 = \frac{\eta_{\nu} M_{ON} (M_{ON} - M_{OFF})}{D^2},$$
(6)

where M(0) is the initial memristance which is  $M(0) = M_{OFF} + (M_{ON} - M_{OFF})x(0)$ .

According to the equation  $Q(t) = \int_0^t i(t)dt$ , integrating the time on both sides of **Eq. 4**, and substituting it into **Eq. 2**, then the mathematical model of the charge-controlled non-linear memristor is obtained in **Eq. 7**:

$$M(t) = M(0) + \Delta M \left(\frac{1}{1 + e^{4k_2 Q(t)}} - \frac{1}{2}\right)$$

$$k_2 = \frac{\eta_v M_{ON}}{D^2},$$
(7)

where  $\Delta M = M_{OFF} - M_{ON}$ .







 $i = 2 \times 10^{-4} \sin(2\pi t)$  for linear and non-linear charge-controlled memristor models.



### **Numerical Simulations**

This section will use MATLAB to simulate characteristics of the two types of memristors mentioned in the above section. The parameters of the two types of memristors are listed as follows:

$$M_{ON} = 100\Omega, M_{OFF} = 20K\Omega, D = 10nm, \eta_{\nu} = 10^{-14}m^2 \cdot s^{-1} \cdot V^{-1}.$$
(8)

**Figure 2** shows the relationship between the memristance changes and the amount of charge or flux for different types of linear and non-linear memristor models. The characteristic curve of the non-linear memristor tends to the physical experiment result provided in [12] which shows that the mathematical model of the non-linear memristor is reasonable.

**Figure 3** shows that the non-linear charge-controlled memristor model also has a hysteresis effect. Furthermore, both models demonstrate the typical current-voltage hysteresis loop of the memristor with  $i = 2 \times 10^{-4} \sin(2\pi t)$ .

# SYNAPTIC CIRCUIT-BASED ON MEMRISTOR

#### **Dual-Mode Memristor Synaptic Circuit**

This paper designs a dual-mode memristor bridge circuit as shown in Figure 4.

In **Figure 4**, the dual-mode switching is realized by a singlepole double-throw switch  $S_1$ . Switch  $S_1$  has two interfaces  $K_1$  and  $K_2$  and a pulse conversion control signal interface. The control signal interface is imposed by signal  $P_A$  which makes  $S_1$  switch between  $K_1$  and  $K_2$  for control and output modes. The positive and negative pulses are generated by switching through singlepole double-throw switches  $S_2$  and  $S_3$  and single-pole singlethrow switch  $S_4$ . Switch  $S_2$  has two interfaces  $K_3$ ,  $K_4$ , and switch  $S_3$ has two interfaces  $K_5$ ,  $K_6$ ; the two-pulse conversion control signal interface is imposed by signals  $P_B$  and  $P_C$ , respectively. The singlepole single-throw switch  $S_4$  has a pulse conversion control signal interface imposed by the pulse control signal  $P_D$ . The portion of the circuit for obtaining the output voltage is composed of MOS transistors  $T_1$  and  $T_2$ . The turn-on voltages of the MOS transistors  $T_1$  and  $T_2$  are both  $V_T$ , and the gate voltages of the two transistors are both  $V_1$ . In the control phase, in order to obtain the zero output voltage, let  $V_1 < V_T$ . Otherwise, in the output phase, let  $V_1 > V_T$ . The conditions of switches in the two modes are shown in **Table 1**.

There are two modes of dual-mode memristor bridge synaptic circuit, control mode, and output mode. The control mode is to make the non-linear memristor reach the required memristance faster so that the memristor can obtain the required synapse weights. The output mode is to obtain the required output with the minimum influence on the memristor's change. The dual-mode memristor bridge synapse circuit is an improvement of the type I memristive bridge circuit as shown in **Figure 5**.

As shown in **Figure 4**, in the control mode, the equations for calculating the memristances of  $M_1$ - $M_4$  in the control phase are listed as follows:

$$M_1 = M_{01} + \Delta M \left( \frac{1}{1 + e^{4k_2 \frac{-v_{ing}}{M_1 + M_2} t_{\nu}}} - \frac{1}{2} \right), \tag{9}$$

$$M_2 = M_{02} + \Delta M \left( \frac{1}{1 + e^{4k_2 \frac{v_{ing}}{M_1 + M_2} t_\nu}} - \frac{1}{2} \right)$$
(10)

$$M_3 = M_{03} + \Delta M \left( \frac{1}{1 + e^{4k_2 \frac{v_{ing}}{M_3 + M_4} t_v}} - \frac{1}{2} \right), \tag{11}$$

$$M_4 = M_{04} + \Delta M \left( \frac{1}{1 + e^{4k_2 \frac{-v_{ing}}{M_3 + M_4}t_\nu}} - \frac{1}{2} \right), \tag{12}$$

In the output mode, when the input voltage is  $V_{inN}$ , the output voltage equation of the dual-mode memristor bridge synaptic circuit as shown in **Figure 4** is derived as **Eq. 13** according to the voltage division **Eqs 14**, 15:

$$V_{\text{out}} = V_A - V_B = \left(\frac{M_2}{M_1 + M_2} - \frac{M_4}{M_3 + M_4}\right) V_{inN}, \quad (13)$$

$$V_{M_2} = \frac{M_2}{M_1 + M_2} V_{inN} = V_A, \tag{14}$$

$$V_{M_4} = \frac{M_4}{M_3 + M_4} V_{inN} = V_B.$$
(15)

Let  $\omega = \frac{M_2}{M_1 + M_2} - \frac{M_4}{M_3 + M_4} = \frac{M_2 M_3 - M_4 M_1}{(M_1 + M_2)(M_3 + M_4)}$ ; then,

	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	<i>T</i> <sub>1</sub>	T <sub>2</sub>	
Control mode	<i>K</i> <sub>1</sub>	/	/	OPEN	OPEN	OPEN	
Output mode	$K_2$	CLOSE	CLOSE	CLOSE (OPEN)	CLOSE (OPEN)	CLOSE (OPEN)	
Output mode-positive pulse	$K_2$	K <sub>3</sub>	$K_6$	CLOSE	CLOSE	CLOSE	
Output mode-negative pulse	$K_2$	$K_4$	$K_5$	OPEN	OPEN	OPEN	

#### TABLE 1 | The conditions of switches in two modes.

In Table 1, the so-called positive pulse has the same polarity as  $\mathsf{V}_{\text{in}}$ 



$$V_{out} = \begin{cases} \omega \times V_{inN}, & V_1 > V_T \\ 0, & V_1 < V_T \end{cases},$$
(16)

where  $\omega$  satisfies

$$V_{out} = \begin{cases} \text{negative}, & M_2 M_3 < M_4 M_1 \\ 0, & M_2 M_3 = M_4 M_1 \\ \text{positive}, & M_2 M_3 > M_4 M_1 \end{cases}$$

#### Control Mode and Output Mode Algorithm

According to **Eqs 9–12**, we can know there are two methods to make the synaptic weight change more linear for the non-linear memristor. One is to increase the duration of  $t_v$  with the input  $V_{in}$  unchanged. The other is to change the input  $V_{in}$  and keep the duration of  $t_v$  unchanged. Because of the timeliness requirement of the synapse circuit, the paper employs the method by varying the input  $V_{in}$  in the control mode.

In order to obtain the more accurate models, this paper uses the simulated annealing method random search algorithm to select a suitable input  $V_{in}$  because of its simple structure and the fast search speed.

When the input  $V_{int}$  is sampled in a sufficiently small interval,  $T_{s}$ , by dividing the duration of  $t_T$ . Then, the simulated annealing method can be used to obtain a more accurate input voltage  $V_{int}$ . This method is applied to the memristive bridge synapse circuit as shown in **Figure 4**.

The detailed specific steps are listed as follows.

Step 1: Set the initial input voltage  $V_{int}$ , temperature T, end temperature  $T_z$ , the maximum number of iterations L for each



temperature *T*, the interval time  $T_s$  and the maximum value of the input voltage that is changed at each moment through measurement. The input voltage is selected at each moment between the initial input voltage and the maximum voltage.

Step 2: T = jT, j is the descent rate and  $j \in (0, 1)$ , n is the number of iterations. To obtain the evaluation function for each iteration,  $E_{t_T}(n) = M_{\text{linear}_{t_T}} - M_{\text{non-linear}_{t_T}}$ , for each memristance under the current input voltage; that is, the valuation function is the memristance difference between the linear memristor and the non-linear memristor at time  $t_T$ .

Step 3: Select a new input voltage  $V_{in}$  at time  $t_T$  randomly within the set voltage range. Then, calculate the memristances and evaluation function of the non-linear memristor  $E_{t_T}(n + 1) = M_{\text{linear}_{t_T}} - M_{\text{non-linear}_{t_T}}$ .

Step 4: If  $E_{t_T}(n+1) > 0$ , then  $\Delta E_{t_T} = E_{t_T}(n+1) - E_{t_T}(n)$ ; otherwise, n = n+1, and return to Step 3.

Step 5: If  $\Delta E_{t_T} < 0$ , accept the changed input voltage; otherwise, judge whether to accept this voltage according to the probability  $e^{-\frac{\Delta E_{t_T}}{T}}$ . Let n = n+1.

Step 6: If  $\Delta E_{t_T} < -10^5$ , terminate the algorithm.

Step 7: If n < L, return to Step 3.

Step 8: If  $T < T_z$ , terminate the algorithm; otherwise return to Step 2.

According to the above steps, the same parameters of memristors are set for the non-linear memristor and the linear memristor bridge synapse circuits as shown in Eq. 8.

As shown in **Figure 6**, when the simulated annealing method selects an accurate input voltage, the memristance  $M_1$  coming



from the non-linear memristive bridge synapse circuit can be significantly linearized.

It can be seen from **Figure** 7 that the output voltage of the nonlinear memristor bridge synapse circuit is not linear by using improved simulated annealing method, and the absolute values of output voltages are much greater than those of the linear memristor bridge synapse circuit as the time goes further because of non-linearity of the input voltage.

As mentioned above, when an input voltage or current works on the memristor, the memristance will change. However, if positive and negative pulses are applied on the memristor, the effect of input voltage applied on memristance can be reduced according to the memristance measurement method mentioned in [19]. Therefore, the output mode must be able to automatically switch the voltage direction as shown in **Figure 4**. As illustrated in **Table 1** and **Figure 4**, in the positive pulses, the current flows from C to D, and the output voltage is obtained. In the negative pulse, the current flows from D to C, which is opposite to the current flow of the positive pulse, and no voltage is outputted.

According to **Eqs 8–16**, the output voltage changes for models are obtained and shown in **Figure 8**.

As shown in **Figure 8**, the red line represents the output voltage for the non-linearity because only the control mode works. If the output mode is added, the line of output voltages becomes more linear as shown in the orange line. This simulation verifies that the dual-mode memristor synapse circuit can realize that both synapse weights and the output voltages can be linearized. The speed of obtaining weights can be accelerated by using the proposed method mentioned in this paper.

## DUAL-MODE MEMRISTIVE SYNAPTIC NEURAL NETWORK AND ITS APPLICATION IN IMAGE PROCESSING

# Dual-Mode Memristive Synaptic Neural Network

Based on the analyses in the previous section, dual-mode memristive bridge synapses can more efficiently simulate weights which can be



applied to image processing template operators in cellular neural networks. The cellular neural network uses different template operators to transform the input image into the desired output image. Therefore, the synaptic circuit mentioned in the previous section can be used to construct a new type of memristive bridge neural network, which can be employed in image processing. Since the input of the traditional memristive bridge neural network is a fixed value, the memristor exhibits non-linearity which forms the template slowly, and the synapse weight difference is big. Therefore, the dual-mode memristive synaptic neural network can shape the template faster with higher accuracy compared to the traditional memristive bridge neural network.

As shown in **Figure 9**, the circuit is mainly divided into three parts such as dual-mode memristive bridge synaptic circuit, differential pair circuit, and effective load circuit.

1) Dual-mode memristive bridge synaptic circuit

As shown in **Figure 9A**, this synapse circuit in the control mode changes the input voltage to make the synapse weight change like a linear trend. In the output mode, by generating symmetrical positive and negative pulses, the synaptic weight of the memristive synapse circuit is minimally affected, and the expected template operator can be obtained faster. The entire neural network is composed of multiple dual-mode memristive bridge synaptic circuits, and the synaptic circuits are independent of each other.

2) Differential pair circuit

As shown in **Figure 9B**, the differential circuit is located on the right side of the dual-mode memristive bridge synapse circuit, which is a differential amplifier composed of transistors. The corresponding function is to convert the output voltage of the dual-mode memristive bridge synapse circuit into current.

3) Effective load circuit



As shown in **Figure 9C**, the effective load circuit is located on the right side of the differential pair circuit. It is connected in series with each dual-mode memristive bridge synaptic circuit. This circuit coverts the current coming from the differential pair circuit into the voltage signal through the resistive load.

## **Application in Image Processing**

In the field of bird repelling for airports, bird characteristics recognition requires edge extraction from bird images. This paper combines a dual-mode memristive bridge synaptic neural network with a cellular neural network template to realize the edge extraction of these pictures. The commonly used cellular neural network template is  $3 \times 3$ , so this paper uses the synaptic neural network with nine dual-mode memristive bridges as shown in **Figure 9** to implement. In each circuit, the corresponding output value can be obtained by inputting different pulse signals.

The template based on edge extraction includes  $\begin{bmatrix} 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} -1 & -1 & -1 \end{bmatrix}$ 

$$A = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 4 & 0 \\ 0 & 0 & 0 \end{bmatrix}, B = \begin{bmatrix} -1 & 2 & -1 \\ -1 & 8 & -1 \\ -1 & -1 & -1 \end{bmatrix}, I = 0.3.$$

The parameters of the memristor in **Figure 9** are listed in **Eq. 8**. The parameters of MOS tube in **Figure 9** is  $V_T = 3v$ .

The pixels of an image with  $M \times N$  are inserted into a cellular neural network with a template size of  $3 \times 3$ ; the pixels are iterated according to the following equation:

$$\begin{split} v_{x_{ij}}\left(n+1\right) &= \sum_{c(k,l) \in P_1} A\left(i,j;k,l\right) v_{y_{kl}}(n) \\ &+ \sum_{c(k,l) \in P_1} B\left(i,j;k,l\right) v_{u_{kl}}(n) + I v_{y_{ij}}(n) \\ &= \frac{1}{2} \left( \left| v_{x_{ij}}(n) + 1 \right| - \left| v_{x_{ij}}(n) - 1 \right| \right), \end{split}$$

where  $v_x$  is the state value,  $v_y$  is the output value, and  $v_u$  is the input value,  $1 \le i \le M$ ,  $1 \le j \le N$ ,  $P_1(i,j) = \{c(k,l) \mid \max\{|k-i|, |l-j|\} \le 1, 1 \le k \le M, 1 \le l \le N\}$ .

When  $|v_x| > 1$ , stop iteration and output  $v_y$ .

**Figure 10A** shows the results of edge extraction by using the non-linear memristive bridge synaptic circuit. The results of edge extraction of bird image are realized by using this template for the dual-mode memristive bridge synaptic neural network as shown in **Figure 10B**. The response speed of edge extraction is faster for the dual-mode memristive bridge synaptic neural network than that of the non-linear memristive circuit. The comparison of some indexes of the two methods is shown in **Table 2**.



<b>TABLE 2</b>   Comparison of the indexes of two kinds of memristive bridge synaptic	
neural networks.	

	The traditional method	The method of this paper
FOM	0.9557	0.9865
Iteration times	90	78

As shown in **Figure 10**, the iteration times, *t*, for obtaining templates by using the proposed dual-mode memristive bridge synaptic neural network are between 30 and 40, while the iteration times for obtaining templates in using traditional non-linear memristive bridge synaptic neural network are between 40 and 50. It is obvious that the dual-mode memristive bridge synaptic neural network is faster than the traditional non-linear memristive bridge synaptic neural network for templates recognized.

In this paper, the performance index FOM (Figure Of Merit) will be used to quantitatively compare different edge extraction algorithms, where the FOM equation is listed as follows:

FOM = 
$$\frac{1}{\max(Q_i, Q_t)} \sum_{i=1}^{Q_t} \frac{1}{1 + \alpha d_i^{2^2}}$$

where  $Q_i$  is the number of edge pixels of the original template.  $Q_t$  is the actual number of edge pixels detected.  $\alpha$  is the compensation coefficient,  $\alpha = 1/4$ , and  $d_i$  is the shortest distance between the detected edge point and edge point of the original template. FOM  $\in [0,1]$ ; the larger the index FOM, the better the effect. The edge results of the bird image extracted by different methods are evaluated, and the FOM values are shown in **Table 2**.

According to **Table 2**, it can be seen that the FOM value obtained by the proposed method in this paper is larger than that of the traditional method, indicating that the edge extraction effect of the proposed method is better. The iteration times of the proposed method are also smaller than those of the traditional method. Therefore, compared to the traditional non-linear memristive bridge synaptic neural network, the dual-mode memristive bridge synaptic neural network has a more efficient performance in edge extraction.

## CONCLUSION

This paper analyzes the memristance changes of different types of linear and non-linear memristor models in theory and verifies that the memristance changes of non-linear memristor models are much closer to the physical characteristics. Then, the paper proposes that the synaptic weight can be linearized by changing the input voltage for the non-linear memristive bridge synaptic circuits. Thus, the paper designs a method for the precise input voltage based on the simulated annealing method to make the change of the non-linear memristive bridge synaptic circuit more linear. However, when the input voltage is changed, the corresponding output voltage is also changed, and the non-linearity is aggravated. Therefore, a dual-mode memristive bridge synaptic circuit is proposed because the symmetrical positive and negative pulses put the least effects on the synaptic weight which makes the output voltages and synapse weights linearized. Finally, a dual-mode memristive bridge synapse circuit is used to form the proposed neural network in this paper which is used to extract edges for bird images. According to the simulation results, the response time and the weights of the dual-

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mode memristive bridge synaptic neural network performs faster and more precisely than those of the traditional one. Therefore, the dualmode memristive bridge synaptic circuit neural network is expected to be more real-time and to solve more complex image processing.

## DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/supplementary material; further inquiries can be directed to the corresponding author.

## AUTHOR CONTRIBUTIONS

RW and ZZM designed the research. HS and YYW guided the research. All authors contributed to the interpretation of the results, discussions, and editing of the manuscript. Furthermore, all authors have read and agreed to the published version of the manuscript.

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