Research Article

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A full-process chain assessment for nanoimprint technology on 200-mm industrial platform

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Abstract: To evaluate the maturity of the wafer-scale NanoImprint lithography (NIL) process, laboratory of electronic and communication technology (LETI) and EV Group (EVG) launched the Imprint Nanopatterning Solution Platform for Industrial Assessment program (INSPIRE), which aims at building a nanoimprint solution platform for industrial assessment and provide a unique open ecosystem for the standardization of the nanoimprint process. This program enabled to gather EVG know-how for the tool manufacturing and its long expertise in bonding activities, and the established methods and advanced microelectronic environment. Presented as an upstream phase, metrology and defectivity were performed on dedicated assessment designs to address critical dimension uniformity (CDU) at wafer scale for a large number of imprints, defectivity on imprints and masters, and alignment capabilities of the nanoimprint HERCULES® platform of EVG. We demonstrate that the critical points are the anti-sticking layer for the defectivity, the CD shrinkage for the CDU, and the stiffness of the soft stamp for the overlay uniformity. Thus, we bring to light the actual capabilities of the HERCULES® platform, and open the discussions on the opportunities for this technology with the possible improvements for the process.

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1 Introduction

Over the past 20 years, NanoImprint lithography (NIL) technique has stood out from its original microelectronic environment. Thanks to its technical capabilities and its cost-effectiveness, NIL significantly contributed to increase and diversify the number of fields, which can take advantage of micro- and nano-patterning. In spite of its diversification, NIL was not brought to an autonomous technology as it is strongly related to the other lithography processes, such as photolithography or electronic lithography among many others: NIL is a replication technique and obviously needs a nanostructured master. Nevertheless, NIL sticks out from the other lithography processes by virtue of the fundamental mechanisms that create the structures: with conventional approaches, the structures are created through a chemical contrast, whereas a topographic one is formed in the case of nanoimprint, thanks to the flow of the resist through the stamp's cavities. This forming technique, thus introduced in the world of micro- and nanomanufacturing, has called for new developments, which, nowadays, have made the NIL technology more mature and ready for high-volume manufacturing [1–3].

Among plenty of technology alternatives, the UV-based imprint, which uses a transparent stamp, became the standard. Two well-established options are now available on the market: the full wafer soft imprint [4] and the step and flash imprint, where a small stamp is stepped across the wafer to be processed [5]. These two options have both advantages and drawbacks, and, depending on the application, the defectivity, the throughput, the critical dimension control, and the overlay performances must be balanced in regard to process integration complexity and the cost. On one hand, focusing on the developments of the last years, the step and flash technology seems to be more prone to address the semiconductor markets as

presented in the review of Malloy and Litt [6] with high requirement levels for alignment capability and defect density [7]. The technology has reached impressive performances and can compete with advanced optical lithography solutions for NAND, DRAM, and Logic markets [3]. On the other hand, the full wafer option appears to be the reference for the emerging and growing markets like LEDs [2, 8], bio applications, photonics-based devices [9, 10], or optical devices [11]. For the latter option, the landscape is wide, and the expectations for the process become more and more specific, which imposes to have either a very versatile solution or to have a set of solutions in terms of material compatibility and integration processes that can be used with the wafer-scale process. In both cases, the requirements will bring developments and improvements in one or many items of the full supply chain: design rules, master manufacturing and repair, in-line metrology and defectivity, integration solutions, and the two cornerstones of this technology, the materials and the imprint tool itself. This analysis naturally brings the question of the entry barrier with respect to each market's needs, in terms of cost and, the main concern addressed in this paper, in terms of technical maturity.

To evaluate the maturity of the wafer-scale NIL process, laboratory of electronic and communication technology (LETI) and EV Group (EVG) launched the Imprint Nanopatterning Solution Platform for Industrial Assessment program (INSPIRE), which aims at building a nanoimprint solution platform for industrial assessment and provide a unique open ecosystem for the standardization of the nanoimprint process. This program enabled to gather EVG know-how for the tool manufacturing and its long expertise in bonding activities, and the established methods and advanced microelectronic environment. It stands on reason that the technology assessment could be performed in two ways, either on a final product by testing the performances, or in a larger scope and upstream phase by performing metrology and defectivity on dedicated assessment designs. The second option is the one presented in this work about the main topics addressed since the beginning of this collaboration, such as silicon masters manufacturing, critical dimension uniformity at wafer scale for a large number of imprints, defectivity on imprints and masters, and alignment capabilities.

Underneath these topics, the aim of this paper is to share parts of the results that have been collected and processed within the program and to sketch the current capabilities of the technique in the microelectronic environment. All the processes were made with different masters and design. No general presentation on the masters is made, but information is provided in every section to explain the context of each test. The remainder of this paper is as follows: first, we present the materials, and the imprint, metrology, and defectivity tools with their specifications in Section 2. In Section 3, the impact of the process on the master defectivity and the one transferred to the imprints are developed. Section 4 gives the focus on advanced analysis made on the critical dimension uniformity topic with an introduction of modeling for design corrections. Section 5 finally presents some overlay measurements and analysis, which give us the opportunities to demonstrate the critical role played by the soft stamp backplane in the process performances.

2 Equipment and materials

2.1 Equipment

2.1.1 Imprint tool

The imprints are performed on the HERCULES® NIL equipment platform using the SmartNIL process (EVG, Austria). This equipment is designed for high-volume manufacturing combining preprocessing and nanoimprinting in a fully integrated platform. The nanoimprint module is based on the SmartNIL technology, and the preprocessing includes priming, coating and baking of the wafers, and has a UV lamp of 340 W/cm^2 (365 nm). The key point of this equipment remains in the SmartNIL process, which uses a transparent working stamp polymer glued to a flexible backplane to enable conformal contact with the substrate surface. The first step of the process, illustrated in Figure 1, aims to manufacture the working stamp. An anti-sticking layer is deposited on the master prior to coating the working stamp material (green) and then laminating a transparent backplane, coated with an acrylic-based glue, onto the working stamp material. The stack of materials is cured before detaching it from the master. The second step is dedicated to the replication process in the resist: the working stamp is laminated on a wafer coated with the resist to be imprinted, a delay time is added to ensure the complete filling of the working stamp cavities, and UV curing of the resist is performed. The specificity of that process is the reusing of the working stamp for multiple imprints and efficient high-volume manufacturing.

2.1.2 In-line metrology tools

The CG4000 CDSEM from HITACHI is used to characterize the CD uniformity of both masters and imprints. The

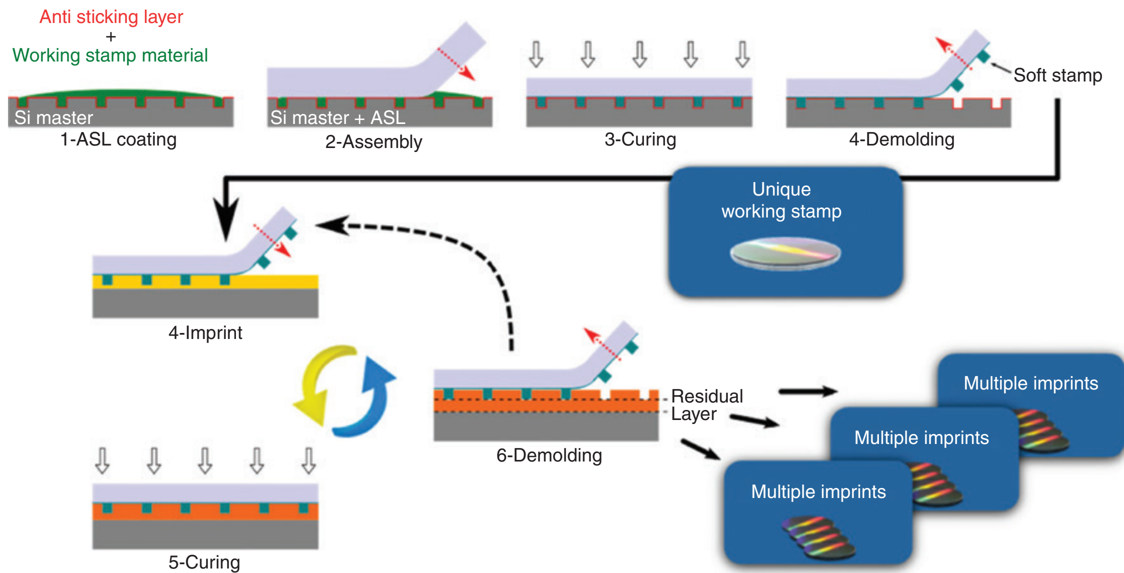

Figure 1: SmartNIL process illustration with first the manufacture of the working stamp as a bilayer foil composed of a working stamp material (green) and a polymer foil coated with an acrylic glue. The working stamp is manufactured once to produce multiple imprints with successive imprinting-curing-demolding steps.

optical and SEM alignment options of the CDSEM are used and make possible to measure the critical dimensions close to the center of each array with a positioning error of ±1 µm. In the following analysis, the CD of the line and the pitch of the array are measured. The tool is calibrated with an error of 1% on the pitch.

The HRP340 profilometer from KLA is used to measure the pattern heights of line arrays. The tool has alignment capabilities with embedded processing algorithms to extract the height of the features and statistical data from the linear scan. The tip is made of diamond with a radius of 100 nm and an angle of 120°. The force between the tip and the sample can be adjusted from 0.1 mg to 2 mg depending on the material stiffness (resist or silicon).

2.1.3 Defectivity tools

The defectivity scans were made on the COMPLUS 4T manufactured by Applied Materials (Santa Clara, CA, USA). The tool has a sensibility down to 80 nm on silicon with two light incidences: normal and oblique, and 10 sensors for bright, gray, and dark-field analysis. The tool processes the wafer from top to bottom and compare neighbored cells on a line. The tool has an embedded defect review capability and automatic defect classification option.

The review of the defects was also performed on the HCG4000 CDSEM.

2.2 Materials

Three types of materials are requested for the process: the imprint resist, the working stamp material, and the anti-sticking layer (ASL) coated on the silicon masters.

2.2.1 The anti-sticking layer

An ASL composed of fluorine-based monolayer is deposited on the silicon masters to obtain a hydrophobic surface and lower the adhesion forces between the working stamp material and the master. The ASL must fulfill some specifications in terms of process integration (if the ASL should be coated or deposited in the imprint tool directly or if it should be done on a dedicated tool due to chemical compatibility), surface energy reduction (typically evaluated with the static contact angle), and stability to UV exposure (as it will be exposed for the curing of the working stamp). Three commercial ASLs were tested for the project. Two were provided by EVG, named EVG-ASL-Si developed for silicon substrates and EVG-ASL-X developed for non-silicon substrates, and one manufactured by Daikin Corporation, named Optool DSX (Daikin, Dusseldorf, Germany). To capture the differences between the formulations, the static contact angle measurement with water was made and the data are reported in Table 1.

Table 1: Static contact angle of water of the three ASLs assessed.

6.1	EVG-ASL-Si	EVG-ASL-X	OPTOOL DSX
Contact angle (EDI)	112°	75°	118°

2.2.2 The working stamp materials

The working stamp material is a transparent material, which can capture nanostructures on the master with very high resolution and keep enough compliance to be slightly deformed during imprinting without damaging the nanostructures. Every nanoimprint technology uses its own solution, either with a bi- [2] or a multi-layer working stamp design [8]. It is a key item for the process as it will be put into contact with the imprint resists and exposed to UV curing hundreds of times. The overall thickness of the working stamp used in our case is around 200 µm, and two commercial materials were assessed: the EVG NIL UV/AS1 and EVG NIL UV/AS2 (acrylate-based materials, required dose of 68 J/cm^2). The two working stamp materials have different mechanical and chemical properties, which will impact, for example, the CDU evolutions. The AS1 has a hardness modulus of 20 MPa with a Young's modulus of 0.1 GPa, whereas the AS2 is stiffer with a hardness modulus of 55 MPa with a Young's modulus of 0.3 GPa.

2.2.3 The EVG imprint resists

The resists are UV-curable resists that can be imprinted at room temperature. They are provided by EVG and the EVG NIL UV/E1 was selected (dose for curing: 3.4 J/cm^2). This resist is liquid at room temperature, allows a capillary filling of the working stamp cavities, and has the property to be highly compatible with the working stamp for the NIL process, with low adhesion forces in between them without treating the working stamp with additional ASL. For that resist, a primer is used before coating.

3 Defectivity from master to imprint

3.1 Defectivity design

The master used for defectivity assessment is composed of trenches (width 2.5 µm, pitch 3 µm, and depth 220 nm) covering a whole 8-inch wafer and arranged in 52 dies all divided in four arrays. Alignment patterns are placed at each corner of the cells in order to be compatible with the automatic inspection tools. Each array is 1 cm^2 and separate from the neighbor cells by 1 mm empty space; this is to limit the influence of one cell to another.

The design, presented in Figure 2, has been used to manufacture several masters into SOI substrates, which were inspected for defectivity just after etching and after every further process steps like working stamp manufacturing, imprint, or cleaning, as presented in the next sections.

3.2 Defectivity on masters

The obvious reference for defectivity analysis for nanoimprint is the defectivity of the masters once they have been etched or even coated with an anti-sticking layer. This defectivity is the one that will be transferred to the imprints when one has to deal with missing patterns, collapsed lines, or any other structural defects due to handling or optical mask defect. In our case, the baseline for the imprints is around 3–6 def/cm^2 as presented in Figure 3, which shows the defect number for 18 SOI masters. As for all the master stamp inspections, the sensitivity of the COMPLUS 4T was set in order to detect defects down to 200 nm. For the purpose of our work, no classification of the defects was performed so far, but a little overview of the defectivity maps are presented to show how the signature can propagate imprint after

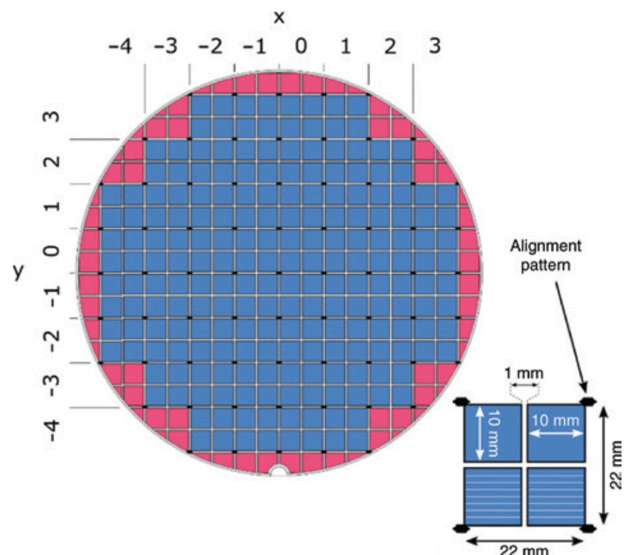

Figure 2: Defectivity design, 52 dies of four arrays of trenches each; trenches width 2.5 µm, pitch 3 µm, and depth of 220 nm. The design has alignment marks in all the die corners. The dimensions of the die and arrays are specified in the figure. The trenches are all oriented horizontally, and the imprint is made perpendicularly to the gratings.

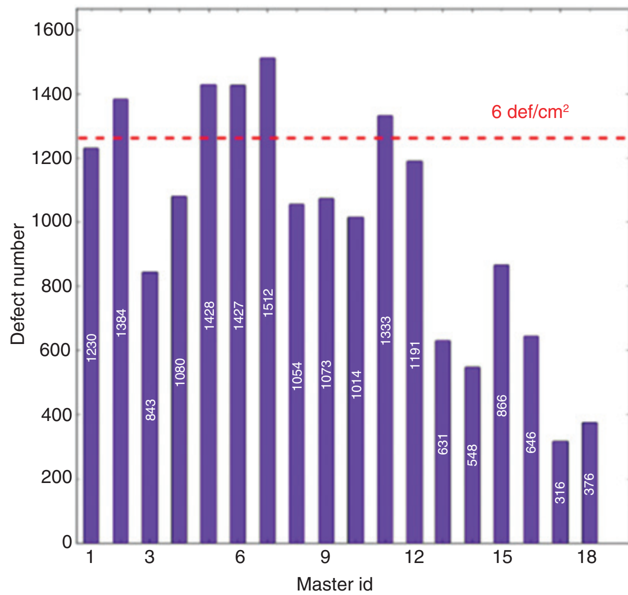

Figure 3: Evolution of defect number with respect to the master IDs before the imprint process. The defects either come from the lithography or the etching processes.

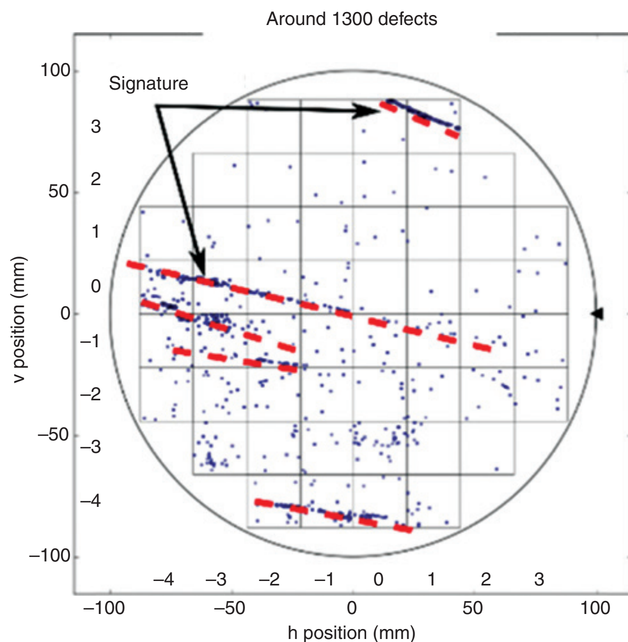

Figure 4: Example of defectivity map on SOI master before imprint. The signature reveals an organization of defects in lines. This type of master is used to check if a cluster of defects is critical for defect propagation with NIL.

imprint. One example is presented in Figure 4 for one of the highest defectivity level measured on the masters (around 6 def/cm^2), and the maps reveals an organization of defects in lines. The goal is not necessarily to optimize the master manufacturing process but rather to take advantage of the defect clusters and check how critical

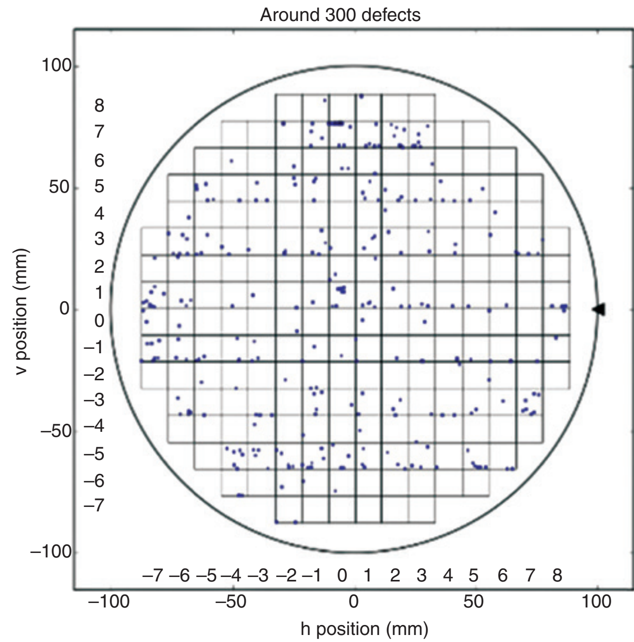

Figure 5: Example of defectivity map on a clean master before imprint (without particular signature). Type of master used for process assessment.

they are for replication. Another example is presented in Figure 5 where the master stamp has no particular signature and is used to assess to understand where and how the defectivity sources appear.

In the process that is assessed, the masters are coated with an ASL. The ASL is not mandatory, and some commercial solutions work without it [1, 2], but the masters are subjected to progressive contamination that becomes obvious after a very large number of imprints [2]. But when the inherent releasing properties are poor, an ASL is requested, and this impacts the defectivity in two ways. The first one is the self-contamination of the ASL, and one has to be sure that the solvent and polymer material are properly filtered in order to limit the organic or particle contamination of the master after ASL deposition. This step, not presented in this work, can be performed with usual material monitoring protocols. The second one is due to the releasing properties: with poor properties, particles of polymer will be scattered all over the master after demolding as illustrated in Figure 6, and with too good properties, a self-dewetting phenomenon will occur. Thus, a balance must be found. This balance will, of course, depend on the couple working stamp and master material, and the ASL must be adapted with respect to the latter one.

To illustrate this balance, we present the data obtained with three different ASLs. The reference one is the one proposed by EVG for silicon, which has a contact angle with water of 112°. The result is presented before

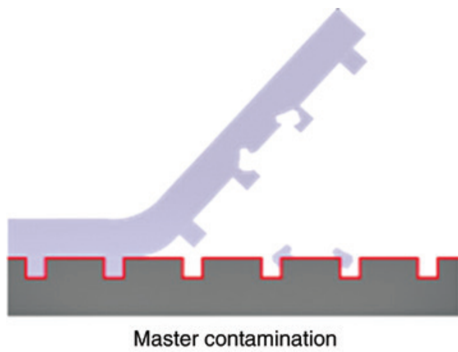

Figure 6: Illustration of defect creation during the working stamp pealing from the master when the surface energies are not optimized.

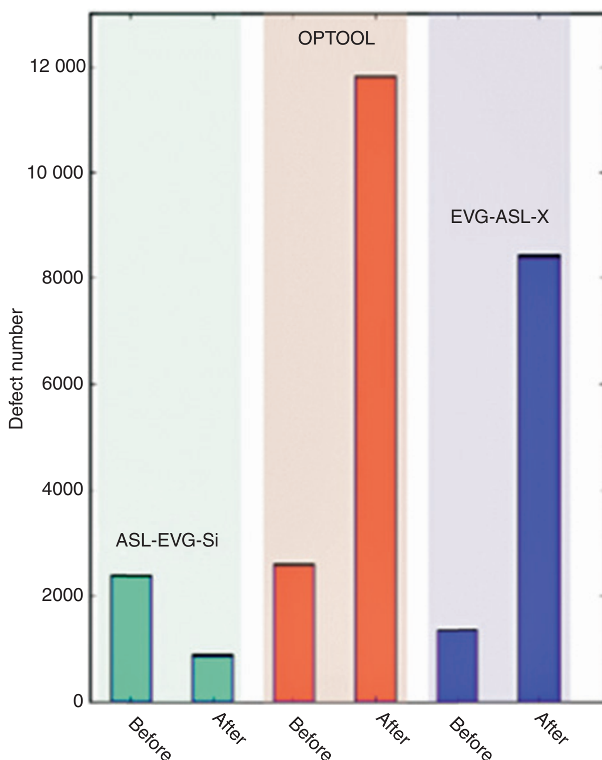

Figure 7: Comparison of the defectivity level for the three ASLs before and after the working stamp manufacture. The defectivity can decrease (ASL-EVG-Si) due to some organic contamination of the master, which is removed when pealing the working stamp.

and after the working stamp manufacture in Figure 7 and clearly shows that the AVG-ASL-Si do not degrade the defectivity (in that particular case, the defectivity even decreased as the master was already processed, cleaned in a plasma chamber, and we suspect that some organic particles were still attached to the surface). The use of the two other products gives better view of the process window. The EVG-ASL-X, which has a contact angle of 75° (so much lower) demonstrated a very high defectivity level, that is to say, bad releasing properties. This could be related to the low contact angle, but the correlation is not that straightforward as it is shown by the next case.

The OPTOOL, which has the highest contact angle (6° higher than the EVG-ASL-Si), thus, a lower surface energy, returned a number of defects increased by a factor of four or so as presented in Figure 7, which demonstrates that knowing the contact angle value is not enough to predict the releasing properties between the working stamp and the ASL. Furthermore, similar to the demonstration of Truffier-Boutry et al. [12], it happens that the OPTOOL has shown really quick degradation stages after it has been exposed to UV curing. This ASL contains, in fact, Si-O atoms bounds, which are broken by the UV light.

In the three cases, the SEM reviews clearly showed that the defects were organic material stripped from the cured working stamp material, with sizes ranging from 200 nm to a few micrometers as presented in Figure 8, with no preferential locations either at die or at wafer scale. They were equally found in the trenches, or glued to the sidewall of the lines, or directly on the top of the lines for the smaller ones. Thus, it is assumed that the defectivity increase was more related to a chemistry issue than a design one and that the ASL is the key of defectivity optimization for the NIL process.

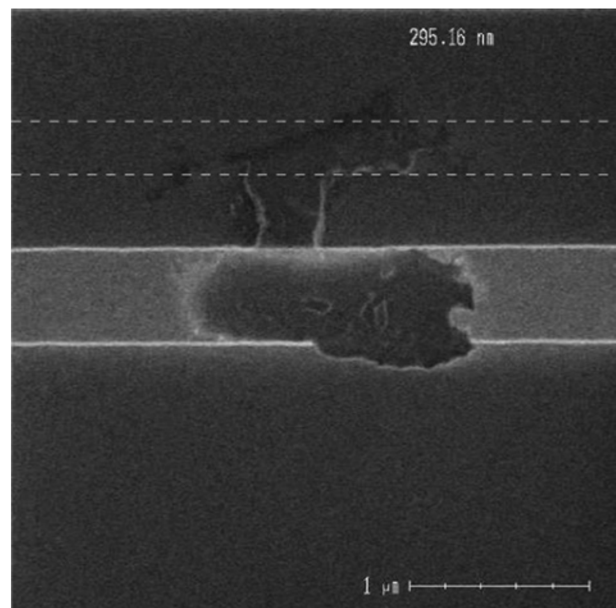

Figure 8: SEM image example for organic contamination left on the master after the working manufacture when the surface energies are not optimized.

3.3 Master cleaning

As the master can be contaminated by the working stamp material (even for an optimized ASL, one can expect to accumulate some organic particles on the master after a few working stamps are manufacture), cleaning solutions have to be found in order to keep the defectivity as low as possible as proposed by Singh et al. [13]. Few chemical and physical solutions were tested, and it appears that in some cases, the master baseline defectivity could be quite well recovered depending on the working stamp material chemistry (that can contain fluorine and/or silicon) and the master material. The idea is to find a stripping process, which will remove the working stamp particles without damaging or etching the master (made of Si and SiO_2 in our case) or transforming the working stamp material into a SiO_2-like material, which cannot be removed selectively from a SOI master afterward.

Among the solutions that have been tested, a Caro-SC1 cleaning chemistry at 140°C gave good results with the EVG-AS1 material, and the results are presented in Figure 9. The Caro process lasts 15 min and is based on a H_2SO_4/H_2O_2 solution to remove the organic material. The SC1 process lasts 40 min and is based on a $NH_4OH/H_2O_2/H_2O$ solution to remove the particles. Starting from a very high level of organic contamination (9A, 8911 defects) after several working stamp manufactures, the master was immersed into the chemistry for 10 min and then cleaned with electrodeionized water. The defectivity lowered back the defectivity (9B) to the master baseline value (344 defects), and it is worth noting that the number of defects has been reduced by a factor of 30 or so (9C) with that wet process.

3.4 Imprinted wafers

The defectivity of the imprinted wafers is one of the cornerstones of the SmartNIL process due to the fact that a unique working stamp is used to make multiple imprints. Thus, if some defects are created during the working stamp manufacture, they will be propagated imprint after imprint until a new working stamp is made. This is more critical compared to the technologies that are using the soft stamps only once [1, 2] and have a higher chance to copy a defect initiated by a particle or dust to only one imprint. So the aim of the following results is to demonstrate that the first imprint is the most important one. This implies that after a few imprints (between 5 and 25), the global number of defects is stable and that the signature on the first imprint is captured in all the following imprints. The results are presented in Figures 10 and 11. In Figure 10, one can see that the global defectivity level for five consecutive imprints (orange bars in 10A) stays below 11 def/cm^2 (compared to the 6 def/cm^2 of the master). Then, the evolution of the defect number is not a regular increase, which would be the case if a merely constant defect number was added by each imprint or any number related to the defects of the previous imprinted substrate. In fact, a fluctuating number of defects is observed around a mean value of 9 def/cm^2. Further than the defect number, the defectivity maps of the first imprint (10B) and the fifth one (10C) show similar patterns (pointed out by dashed red circles), which represents very large defect clusters. One can see that between the first and the fifth imprint, the sizes of the clusters did not increase significantly, which means that the defects are glued to the working stamp

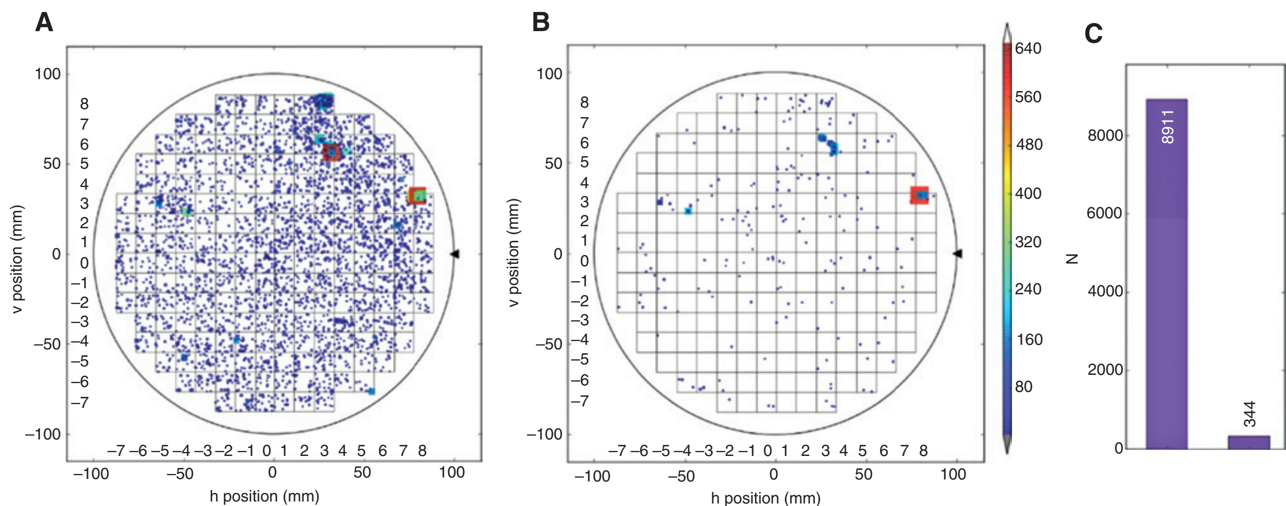

Figure 9: Defectivity maps of a SOI master contaminated with the working stamp material (A) and after a Caro-SC1 cleaning process (B). The number of defects is reduced by a factor of 38 (C), and the master has almost recovered its initial value.

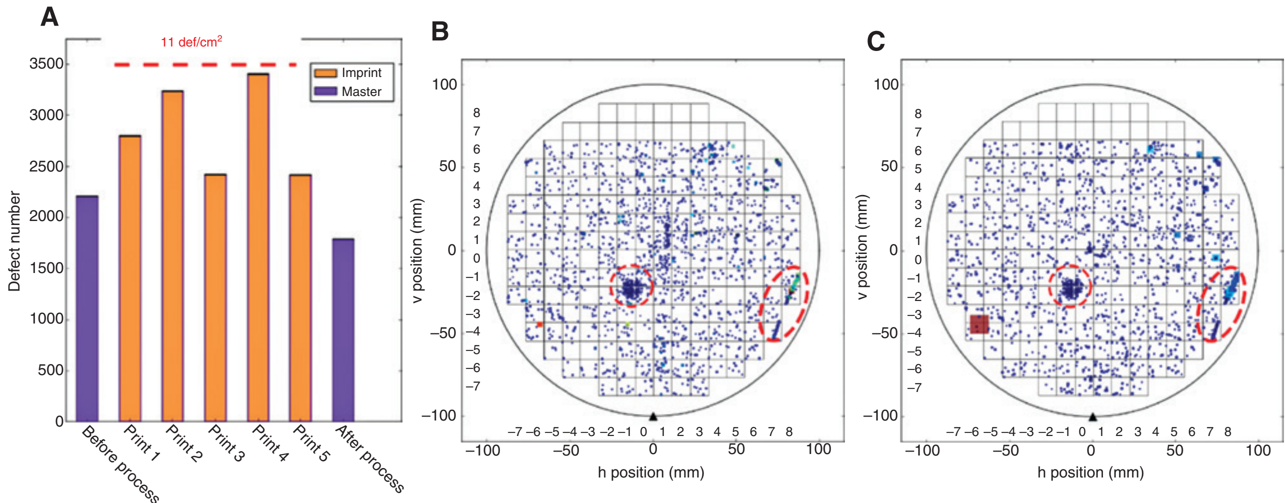

Figure 10: Evolution of the number of defects for five consecutive imprints made from the same working stamp. The histogram (A) show the defect numbers on the master before and after the working stamp manufacture, and each inspection on the imprints. The defectivity level is quite stable (below 11 def/cm^2) in terms of defects number but also in terms of signature [maps of imprint 1 (B) and imprint 5 (C)].

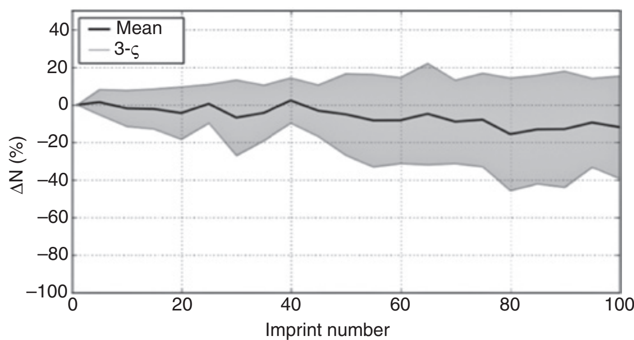

Figure 11: Relative evolution of the defect numbers on 100 consecutive imprints with the first imprint taken as the reference. The defect numbers are computed for each cells (52 cells, 1 cm^2 each), and the mean value is presented with the 3-ς distribution. The global decrease is due to a balance phenomenon of cleaning and adding organic particles between the working stamp and the imprints.

and are not detached and spread between each imprint. This assumption is coherent with the fact that these clusters were not found on the defectivity map of the master after the process: some dust was on the master prior to the working stamp material coating, and it was taken away by the working stamp. Away from the clusters, the defects are scattered randomly, and it is not clear which are due to the working stamp (so permanent defects that are on every imprint) or due to the patterning process (free particles, imprint defects, or defects in resist), and advanced tools are required to analyze these maps as the number of defects is quite large. No such analysis was performed, but local analysis allowed us to see that, in this region, there was a balance between the number of added defects and removed (or not present) ones, which, in the end, keep the global number of defects close to the one of the first imprint.

Performing the defectivity assessment on 100 consecutive imprints gives similar conclusions. In this case, one wafer over five was inspected, the number of defects per cell was extracted, and the mean value of defects per cell and per wafer was computed with the associated 3-ς value. These two statistical parameters give the global trend of the defectivity level, and the results are presented in Figure 11. The graph shows the relative evolution of the defect number by taking the first imprint as the reference. The graph shows that the mean number of defects is slightly decreasing along the replication process (a loss of 15% is noticed at imprint 100), which means that globally, the repetitive curing and demolding of the working stamp with another polymeric layer (imprint resist) does not generate that much particles and that the unglued structures/particles are taken slowly away by the imprints. In the meantime, one can also observe that the 3-ς is growing progressively imprint after imprint (with a maximum value of 25% after 100 imprints), which means that the repartition of the defects is changing during the replication process. This conclusion makes sense if, as described previously, there is a balance of adding and removing (or not adding) defects at every imprint. This balance cannot be captured when dealing with only a few imprints, and the assessment of cumulative effects on defectivity has to go through large runs to simulate a high-volume manufacturing process.

3.5 Conclusion

The defectivity results presented in this paper are not the standard ones expected in microelectronic components as targeted by the step and flash technology [7], but one has to keep in mind that no size filtering was applied in our study and that a wide range of defect sizes was considered in order to assess the process on a very large process window. Through this strategy, we were able to show that the ASL is the most critical item in the value chain to reduce the number of defects added by the process and that the defectivity is not strongly affected by the SmartNIL process, or at least some trends and stability were captured. Of course, depending on the application and the size of the defects that are critical for the devices, the trends (like the increase of the 3-ς value in Figure 11) might not be seen if the smallest defects are not taken into account.

Regarding the working stamp, itself, no turn-key solution is available yet to inspect its defectivity, which will help to qualify its quality before imprinting as it is already done for the template of the step and flash technology with e-beam inspection systems [14].

4 CDU analysis

4.1 Background

The critical dimension uniformity (CDU) analysis is another step in the assessment chain of a nano-patterning process: it reveals the disparity between one theoretical value and the ones on the final products. Here, the main issue is not the critical dimension, itself, as Hua et al. demonstrated that NIL could achieve molecular-scale resolutions [15] as soon as the master contains such geometries. From CDU analyses, the mean value, standard deviation, and min/max values can be computed to evaluate the stability of the process from one die to another. For the SmartNIL process, the CDU distribution on the imprints has basically three sources: the CDU of the master, the physical distortions due to the softness of the stamp, and the shrinkage of the polymers (from the working stamp and resist as illustrated in Figure 12). As the SmartNIL process uses a unique working stamp, a cumulative phenomenon has also to be taken into account in the CDU analysis we have shown in a previous work [16]. Assessing the influence of each source is not an easy task as, for example, no CDU measurement can be performed on the working stamp. Nevertheless, it is still possible to isolate some behaviors.

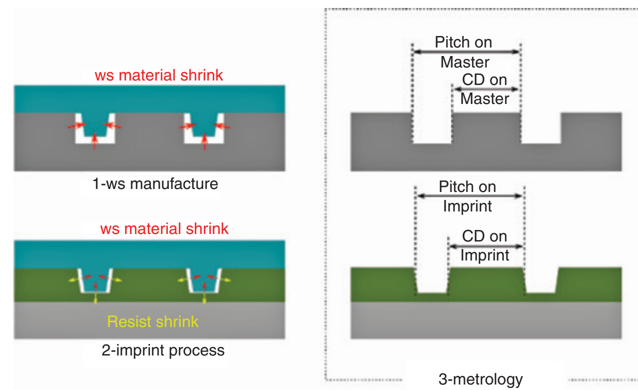

Figure 12: Illustration of CD shrink and dimensions that are measured and compared on the master and the imprints.

4.2 Design and test plan

The design used for the CDU assessment was composed of arrays of lines in vertical and horizontal directions with variable CD and densities. The duty cycles of the arrays range from three to nine: lines widths ranging from 160 to 500 nm and pitches ranging from 640 nm to 5 µm. The layout is presented in Figure 13. The measurements are performed on the CDSEM on locations scattered on the whole wafers and specified in the following sections. In the following, we first present the CD evolution for a reference design, with the CDU maps for the first and last imprint of a lot, and the statistical values for a run of 100 imprints. In a second part, we present the impact of the density of the line arrays on the relative evolutions of the critical dimensions.

4.3 CDU distribution

The first and last imprint of a lot are quite characteristic of the wafer-scale NIL process on the CDU. The first

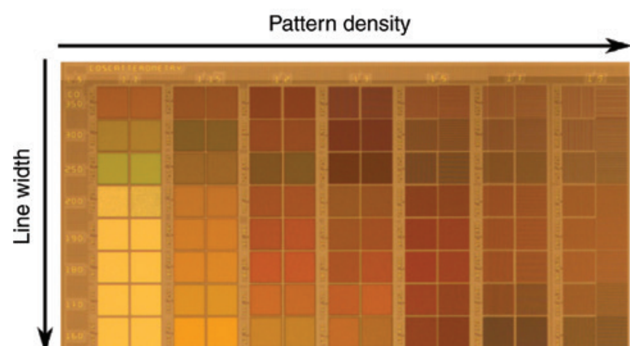

Figure 13: Arrays of lines in vertical and horizontal directions with variable CD and densities. The duty cycles of the arrays range from three to nine for CD ranging from 160 to 350 nm.

imprint is mostly influenced by the master CDU and the working stamp manufacture, which includes a high UV-exposure step. Considering the reference design (580 nm lines with a pitch of 3 μm on the master after manufacture), one can see in Figure 14 that the CDU of the first imprint has a mean value of 605 nm and a variation of 2%–3% at the wafer scale. In that case, 208 measurements have been performed on the wafer, and the figure shows the measurements that are within the range of ±1% from the mean value (green) and the value that are out of that range but below a variation of 3% (red and blue). The black cells are out of range measurements. One observation is that, compared to the master, the mean value is found to be much higher (2.8%), and it is the most important contribution of the working stamp for CDU. The other observation is that the CD variations across the wafer are quite similar (less than 3%), with the lower values located close to the edges and the highest one close to the center.

Focusing on the last imprint reveals, in addition, all the cumulative effects (cumulative imprints and exposures). The CDU map is presented in Figure 15, where the distribution has not changed that much compared to the first imprint (less than 3%), but the mean value has increased a little again (1.7% compared to the first imprint). This small increase could be explained by some shrinkage of the material, basically the working stamp material, but no specific tests have been performed, and as the soft stamp is a multi-layer that can be deformed lightly during the imprint process, there are still some doubts on the identification. Once again, a direct measurement on the working stamp would have help to identify the local behavior of the working stamp material with respect to the exposure dose, but this solution is not available yet.

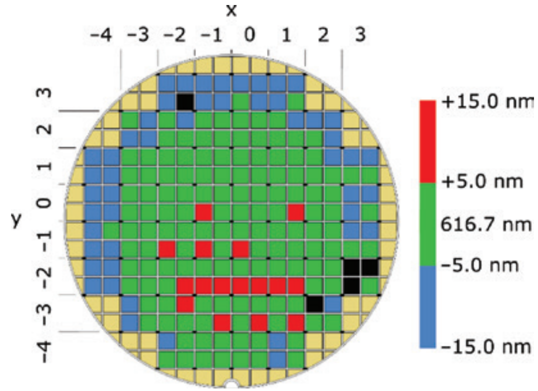

Figure 15: CD distribution on the last imprint of a lot for the reference design. The distribution is a little different than that of the first imprint, but the major difference comes from the mean value (11 nm higher).

In over 100 imprints, the shift between the first imprint and the last one can reached up to 6% of the variations (positive or negative, depending on the design). Figure 16 presents the statistical data for 20 wafers characterized among the 100 imprints. The shift after 25 imprints represents 1.4% of the mean CD value. The key point is the stability of the process over a large number of imprints, and it is clear that, even if the mean value increases, it follows a stable trend that can be modeled, for example. This stability is, furthermore, captured when looking at the 3-ς value, presented in Figure 17, which is almost constant imprint after imprint. Having a closer look at the data will show that there is a little difference between the master and the imprint (2–3 nm on the 3-ς value) and that the 3-ς is slowly decreasing with respect to the number of imprints, but it is hard to justify the trend as we are dealing with values close to the tool accuracy.

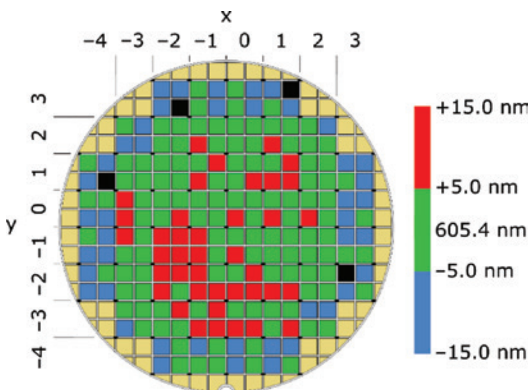

Figure 14: CD distribution on the first imprint of a lot for the reference design (CD on the master of 500 nm with a pitch of 3 μm). The distribution is mainly due to that of the master.

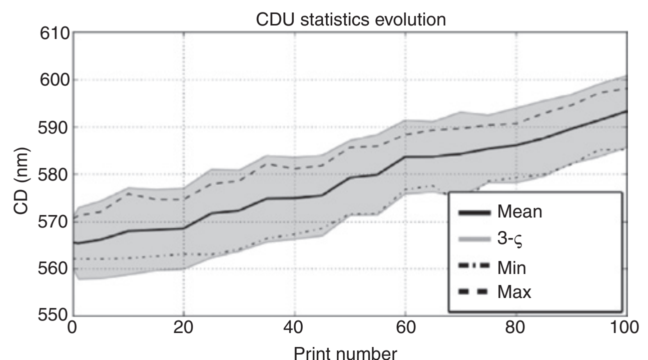

Figure 16: CD evolution vs. the number of imprints made with the same working stamp for a long run (100 imprints). A difference of 6% on the mean CD is observed between the first and last imprint.

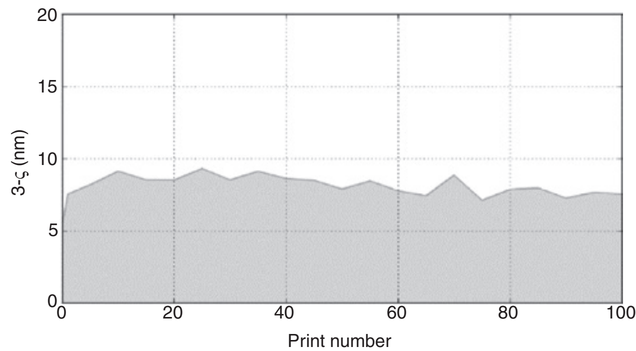

Figure 17: Evolution of the 3-ς of the CD vs. the number of imprints. Unlike the mean value of the CD, the 3-ς tends to be stable in all cases, which demonstrates that the SmartNIL process does not deteriorate the distribution of the CD imposed by the master stamp.

4.4 Mean value evolution

Two experiments are proposed to show the impact of the design and the materials on the CDU. The parameters are the working stamp material (AS1-Young's modulus 0.1 GPa and AS2-Young's modulus 0.3 GPa) and the pattern CD and densities. Both working stamps are manufactured with the EVG ASL. Fifty wafers are imprinted per working stamp with exactly the same imprint conditions (UV dose 3.4 J/cm^2, demolding speed 17 mm/s, film thickness 420 nm, 300-s delay time). For every run, imprint numbers 1, 10, 20, 25, 26, 35, 45, 50 are inspected. The data are presented in a relative difference compared to the master.

4.4.1 Pitch uniformity

The pitch evolutions are presented in Figure 18 for the design of a duty ratio of 3 (18A and 18B) and the one of 9 (18C and 18D). The results show that the pitch of the imprinted pattern does not depend on the number of imprints, but only on the working stamp material. Globally, an offset is observed between the master and the imprints: the pitch after replication by the NIL process is slightly lower than the one on the master with a reduction of 1%–2.5%. The reduction factor depends on the design and the material: it is bigger for the working stamp AS1 for the small CD (18A and 18C), and bigger for the AS2 one for larger CD (18B and 18D) when equivalent duty cycle features are compared.

4.4.2 Critical dimension

The evolution of the lines width (CD) is more prone to variations than the evolution of the pitch. In addition to an offset, a regular decrease in the CD is observed with respect to the number of imprints as is presented in Figure 19. This decrease is the main characteristic of the SmartNIL process as it is linked to the reusable working stamp used in the process as described in Section 4.3, except that the CD is decreasing this time instead of growing. This opposite variation trend is assumed to come from the design polarity, but no further analysis was made on that point.

Then, one can notice the CD jump, named CD recovery in the following due to the brutal evolution inversion, between the 25th and the 26th wafers, which correspond to the exchange of lots when the process is not continuously performed. Once again, the CD recovery depends on the working stamp material and the design on the master. The understanding of this CD recovery is beyond the scope of this paper, and noticing that it represents less than 1% of the CD variation relatively to the master, it will be taken as part of the process with no major impact. All in all, the CD variations are in the range of 1%–9% of the corresponding CD on the master and are assumed to be mainly due to the working stamp material shrinkage.

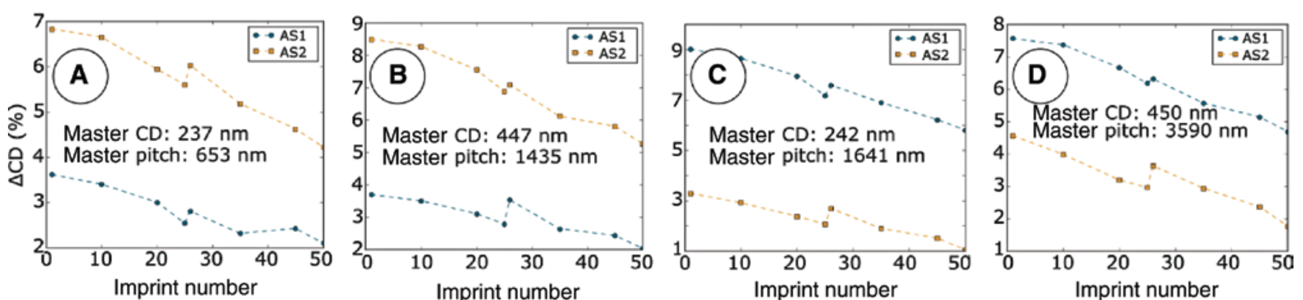

Figure 18: Evolution of the relative difference between the pitch of the line arrays of the imprints and the corresponding one of the master (named A–D), for working stamp materials AS1 and AS2, with respect to the number of imprints made with a unique working stamp. A global constant offset is observed with a value that depends on the material and the design. One data point represents the mean value of 39 CDSEM measurements made on every substrate.

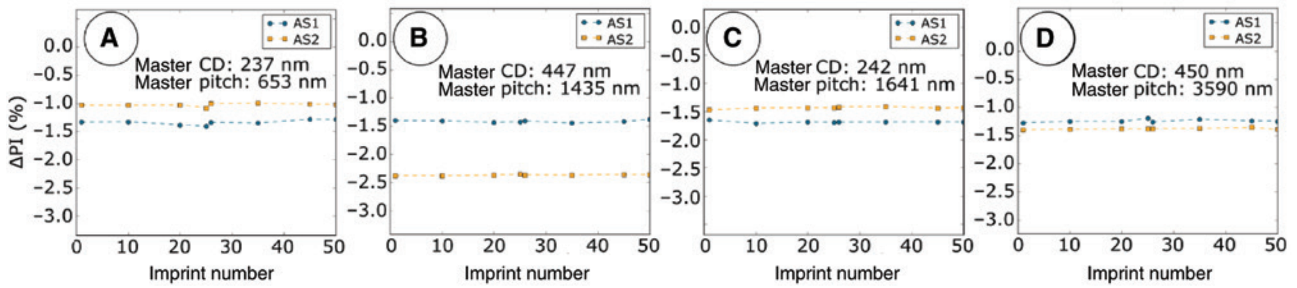

Figure 19: Evolution of the relative difference between the CD of the line arrays of the imprints and the corresponding one of the master (named A–D), for working stamp materials α and β, with respect to the number of imprints made with a unique working stamp. A global linear decrease is observed with a behavior that depends on the material, the design, and the number of imprints. The CD evolutions also present a jump in the CD between the two lots (imprint 25) whose parameters are the same as that of the pitch.

4.5 Conclusion

The CDU characterization of imprinted substrates with the SmartNIL technology has brought many information on the process for high-volume manufacturing. Further than the work presented in Section 4, many analyses have been performed to estimate the measurement error, resist shrink due to CDSEM imaging, and cross characterizations (on AFM) to validate our results. On the technical results, one major good point is that the distributions are not significantly affected by the process (constant 3-ς value in any cases). One point that is more complex is the drifts in CD (which is also captured on the height measurements) that depend on the number of manufactured imprints and the designs. For that, design rules can be an option to control the process as pointed out by Yoon et al. [17], Taylor and Boning [18], and Teyssedre et al. [19]. In our case, the pitch evolutions are smooth enough to be modeled and compensated by sizing the design on the master (the pitch does not depend on the NIL process), whereas the compensations for the CD will need advanced techniques to take into account the drifts with respect to the imprint number. On the scientific point of view, it is known that the shift either comes from material shrinkage or soft stamp tensile handling, but they are hardly separable in the experiments. On the strategy point of view, our approach was to use CDSEM, profilometers, and cross-section characterizations because it does not require advanced modeling and processing. Nevertheless, it limits the analysis to a few parameters, and they are not always convenient for statistical analysis (the SEM cross section or any non-automated tools, for example). One solution will be optical critical dimension techniques, like white light scatterometry, which is a little more complex to set up but that can bring real 3D statistical data of the tool assessment in reasonable time.

5 Wafer-scale alignment capabilities

5.1 Background

Overlay has been part of the main researches for nanoimprint. Lebib et al. [20] and Zhang and Chou [21], respectively, demonstrated on 4-inch silicon wafers that a submicron overlay and a standard deviation below 30 nm were achievable on PMMA even by using a thermal nanoimprint technique where thermal extension is occurring. In 2012, a remarkable work of Fukuhara et al. [22] on a UV NIL step and repeat alignment module allowed to reach the overlay below 60 nm with a hard template, and nowadays, this type of technology is in line with the ITRS roadmap [7] and can achieve a sub-7-nm overlay at a die scale [6]. Moving to the soft stamp and wafer-scale process like in the SmartNIL process affects significantly the overlay capabilities, and the status of the technology is presented in this section.

5.2 Design and process

The SmartNIL technology uses a full wafer-scale alignment process, which means that only two alignment keys, presented in Figure 20A, are used to align the soft working stamp on the underlying silicon substrate. The keys are located on the master and transferred in the working stamp (the cross, level 1), and on the substrate (four squares, level 2). The master and substrates were manufactured using an ASM 300 optical tool and etched into silicon. The keys are located on the horizontal axis of the wafers, at ±75 mm from the center as presented in Figure 21. The layout is also presented: it is divided into square cells of 10.2-mm width, which all have box in box features at their corners. The box in box is used to measure

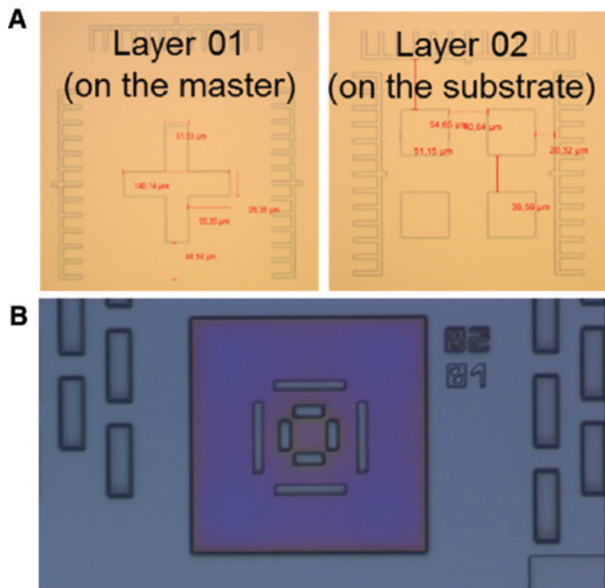

Figure 20: Alignment keys etched into the master (A, level 1) and the substrates (level 2) for the alignment assessment. The overlay evaluation after imprint is made by measuring the distances between the 4 small and 4 big bars (B).

the local overlay of the two levels through their misalignment, as illustrated in Figure 20B, and this is performed on a semi-automated tool. Micrometer features (partially visible on the sides of Figure 20B) are scattered in the cells in order to simulate a device and avoid having blank empty fields between the boxes.

The process for alignment is quite simple. Once the working stamp has been manufactured, two optical microscopes are used to locate the alignment keys, and the virtual positions are recorded. In that step, only the microscopes are moving. Then, a substrate is loaded, and the focus is made on the surface. Thanks to a large field of view, the keys on the substrate are located, and the stage is moved in order to align them with the recorded position. Finally, the imprint process starts.

A few questions are now raised from this process for the overlay measurement: what is the global overlay, and can it be estimated by only measuring the misalignment on the alignment keys? What is the variation or distribution of the overlay at the wafer scale? What influences the overlay performances, and how can the overlay be improved? Some answers are presented in the following results.

5.3 Global wafer overlay

From the overlay data, three in-plane displacements can be extracted to give an overall idea of the alignment performances: perpendicular (X) and aligned (Y) with the imprint direction, combined with a rotation. These three parameters can be evaluated with only the overlay of the

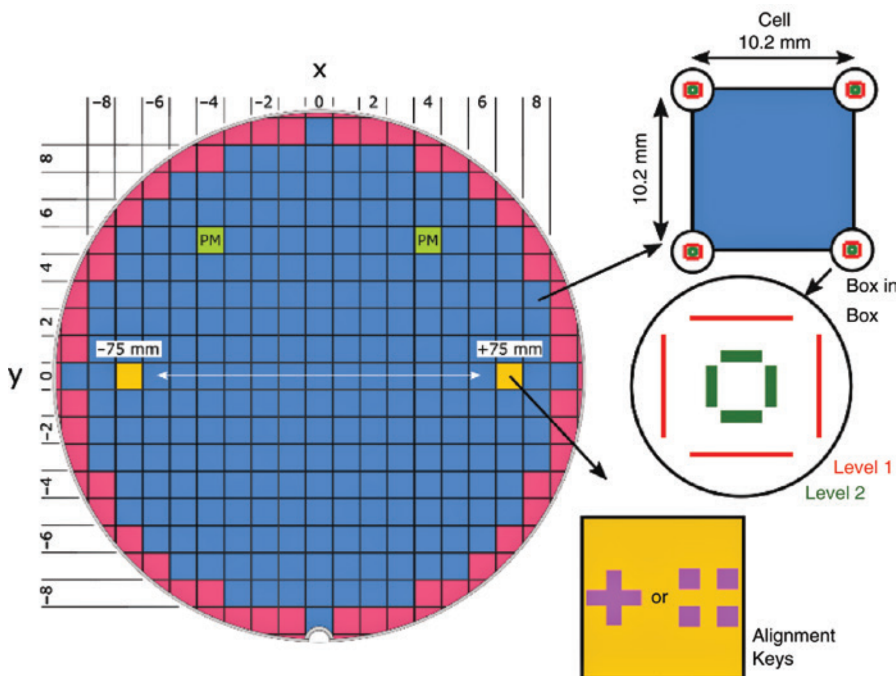

Figure 21: Layout of alignment design. The alignment keys are located on the horizontal axis at ±75 mm from the center. The box in box bars are located at the four corners of every cell.

alignment keys, as presented in Figures 22 and 23. Both figures, respectively, show the overlay in the X and Y directions for the left and right alignment keys (cyan and purple curves). In the figures, the mean values computed from data obtained on the full wafer (8 inches), and smaller area (4 and 6 inches) are also presented for comparison, with the data over 8 inches taken as the reference. The data are presented for nine imprints. In the perfect case, the two curves of left and right keys should overlap, but an offset is observed for the X direction (orthogonal to the imprint direction) due to the soft stamp deformation. The left key X overlay is mostly positive, whereas the right one is mostly negative, so they are both closer to the center of the wafer that they should be. Thus, a little contraction of the design in the working stamp is observed (6×10^{-3}% over 150 mm). Nevertheless, the mean value on the two keys gives a good approximation as it overlaps the 8 inches curve (blue). For the Y direction (imprint direction), the results are much better, and the offset between the left and right keys (which induces a rotation mainly) is lower than 400 nm.

These three parameters are more related to the process, stage capacities, image recognition and imprint stability, and any improvement will mostly raise issues and solutions on the hardware and software.

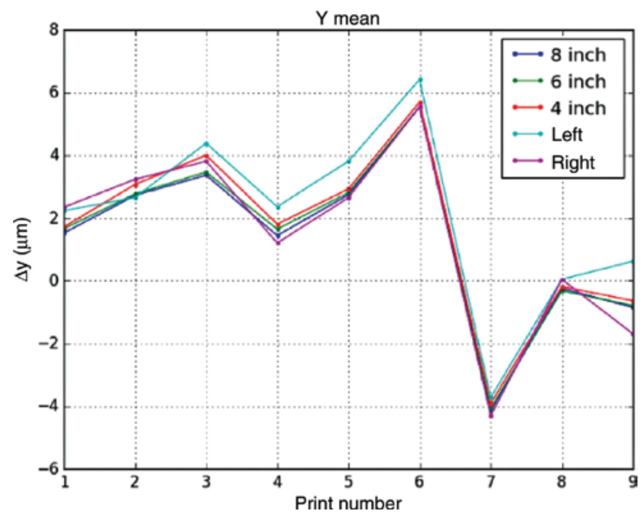

Figure 23: Evolution of the misalignment on the alignment keys in the imprint direction for a soft back foil, on the full wafer (8 inches) and on restricted areas (4 and 6 inches). A good approximation of the misalignment at the wafer scale in the imprint direction is given independently of the location on the wafer.

5.4 Overlay distribution

The distribution of the overlay data is strongly related to the stiffness of the working stamp. The stiffer the stamp, the narrower the distribution, and the stiffness can drastically change the distribution when glass quartz, silicon, or polymer stamps are used. Here, two cases are presented: with a thick (200 µm) and a standard (125 µm) soft stamp. Both cases have the same Young's modulus (150 MPa), and the same imprint conditions are set: initial polymer film thickness 420 nm, UV dose 3.4 J/cm^2

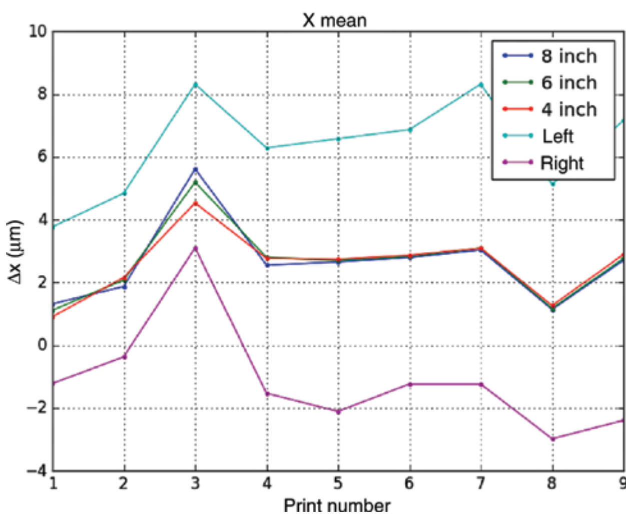

Figure 22: Evolution of the misalignment on the alignment keys in the grating direction for a soft back foil, on the full wafer (8 inches) and on restricted areas (4 and 6 inches). A good approximation of the misalignment at the wafer scale can be achieved with mean value calculation on symmetric points (left and right, for example).

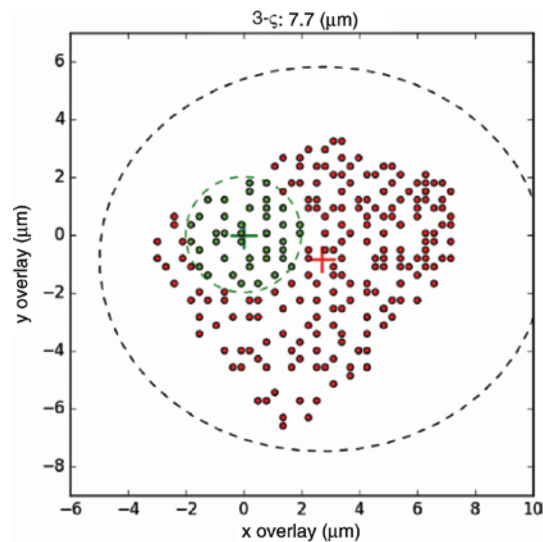

Figure 24: Overlay map with a standard back foil. The black dashed circle represents the 3-ς value computed from the data; the red cross, the mean value. The green cross and green dashed circle are the target for this technology. The mean value and 3-ς values are out of the target as the standard soft stamp is too soft.

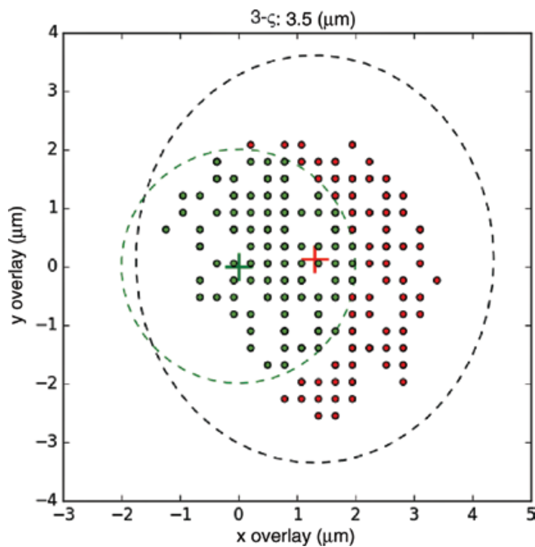

Figure 25: Overlay map with a thick back foil. The black dashed circle represents the 3-ς value computed form the data; the red cross, the mean value. With a stiffer soft stamp, the distribution is smaller, and the mean value is in the target.

per imprint, imprint speed 17 mm/s). The results are, respectively, presented in Figures 24 and 25. In the case of a soft material, the distribution has a 3-ς value of 7.7 µm, whereas a value of 3.5 µm is obtained with a thick back foil. The better control of the distribution also induces a better control of the mean value. For the assessment, the target for the SmartNIL technology is plotted in green (a circle of 2-µm radius) in Figures 24 and 25, and the data are colored in green or red whether they are in the target or not. In the case of a thick back foil, one can see that around 60% of the points are already in specification without specific improvements.

5.5 Conclusion

A quick overview of the SmartNIL alignment capabilities has been presented, and all the performances are in the range of a few micrometers. Depending on the type of back foil that is used, the performances can slightly be improved. At this stage, two points must be addressed: the process itself, in order to minimize the mean value of the overlay, and the materials, to reduce the distribution. Among the characterizations, the map distortions are still missing and are also part of the next studies. Nevertheless, the distributions that have been obtained show stability, which means that a measurement on the alignment key only already gives a good estimation of the wafer-scale alignment. This stability has to be confirmed on a large volume of imprints.

6 Conclusion

The data generated in the INSPIRE project allowed us to clarify the capabilities of the SmartNIL technology and to put in place the required tools for the assessment, pre-series inspection, and the methods for high-volume characterization. The technical results focus on dedicated design for qualification and not on devices, but they bring to light the actual capabilities of the HERCULES® platform, and they open the discussion on the possible improvements: resist formulation for the defectivity, materials and design rules for CDU, and back foil optimization for the overlay. All these points are part of the roadmap of the project.

Acknowledgment: This work has been made possible, thanks to the inspire program.

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