



OPEN ACCESS

EDITED AND REVIEWED BY
Andrea Vacchi,
University of Udine, Italy

*CORRESPONDENCE
Alberto Valero,
✉ alberto.valero@cern.ch

RECEIVED 04 April 2025
ACCEPTED 10 April 2025
PUBLISHED 16 April 2025

CITATION
Valero A, Bedoya C and Fiorini L (2025) Editorial:
Advancements and challenges in data
acquisitions and readout electronics.
Front. Detect. Sci. Technol. 3:1606018.
doi: 10.3389/fdest.2025.1606018

COPYRIGHT
© 2025 Valero, Bedoya and Fiorini. This is an
open-access article distributed under the terms
of the [Creative Commons Attribution License](#)
(CC BY). The use, distribution or reproduction in
other forums is permitted, provided the original
author(s) and the copyright owner(s) are
credited and that the original publication in this
journal is cited, in accordance with accepted
academic practice. No use, distribution or
reproduction is permitted which does not
comply with these terms.

Editorial: Advancements and challenges in data acquisitions and readout electronics

Alberto Valero^{1*}, Cristina Bedoya² and Luca Fiorini¹

¹Instituto de Física Corpuscular (University of Valencia - CSIC), Valencia, Spain, ²Department of Basic Research, Centro de Investigaciones Medioambientales y Tecnológicas, Madrid, Spain

KEYWORDS

hardware acceleration, parallel processing and pipelining, drift tubes, charge-coupled device, triboelectric sensors, FPGA

Editorial on the Research Topic

Advancements and challenges in data acquisitions and readout electronics

Data acquisition methods and readout electronics are essential components of modern scientific and industrial instrumentation. Whether capturing faint optical signals in astronomy, streaming large volumes of data for high-energy physics, or monitoring critical infrastructure, innovations in readout and data handling can enable transformative research and applications. Rapid increases in detector granularity, bandwidth, and operational complexity require new strategies in hardware design, signal processing, and data transmission. The five contributions included in this Research Topic, “*Advancements and Challenges in Data Acquisitions and Readout Electronics*”, each propose unique solutions that collectively advance the performance and scalability of electronic readout systems.

In the article “Charge-coupled device readout by digital-correlated double sampling” by [Cruz and De Vicente](#), the authors address how scientific CCD sensors continue to be central in low-noise imaging and spectroscopy. By exploiting a digital-correlated double sampling (DCDS) method, they show how precise control of sampling intervals and careful signal processing can reduce reset noise and flicker noise. Their proposed FPGA-based DCDS not only increases readout speed but also preserves the fine precision critical to astronomy and high-end imaging applications.

Wireless sensing has also become increasingly relevant for real-time diagnostics and risk prevention. In “Wi-Fi/LoRa communication systems for fire and seismic-risk mitigation and health monitoring” by [del Río Sáez et al.](#), the authors explore approaches to deploy robust and cost-effective sensing networks. They demonstrate how LoRa and Wi-Fi modules can be adapted for diverse emergency contexts: from fire and earthquake detection to personal health monitoring and triboelectric-based alert sensors. Their work underlines the need for versatile, low-power solutions capable of merging IoT sensor data with user-friendly transmission channels across large spatial scales.

Meanwhile, high-energy physics (HEP) experiments demand extremely fast data-handling methods to keep pace with the huge volumes of particle-collision data. In “Harnessing hardware acceleration in high-energy physics through high-level synthesis techniques” by [Leguina and Folgueras](#), we see how complex algorithms for track finding and particle reconstruction can be mapped efficiently onto FPGAs using high-level synthesis

(HLS). By abstracting hardware details and emphasizing parallelism, the authors significantly reduce design complexity. This approach lowers latency and expands the possibility of real-time or near-real-time event selection in extremely data-intensive scenarios.

Another major challenge in HEP is designing reliable and high-throughput readout boards operating in harsh environments. In “OBDDT-theta, a multi-channel TDC and readout board for the CMS muon drift tubes in HL-LHC” by [Bedoya et al.](#), the authors introduce a specialized board for digitizing muon signals under intense collision conditions at the High-Luminosity Large Hadron Collider. By streaming all time stamps to off-detector processing, the design facilitates refined trigger logic and meets the rising data demands of the CMS experiment. Their prototype underscores both the flexibility and the reliability needed to ensure robust long-term data-taking amid increasing luminosities.

Finally, advanced digitizers often require higher transceiver counts than are available on a single FPGA, leading to new methods for bandwidth aggregation. “High-speed ADC to FPGA communication bandwidth optimization with link aggregator” by [Collado Ruiz et al.](#) demonstrates how a customized mezzanine board and universal link aggregator devices can efficiently combine multiple moderate-speed channels into fewer high-speed lines. This technique effectively prevents underutilization of powerful FPGA transceivers and lowers overall hardware costs. Their results illustrate how thoughtful aggregation can keep pace with the surge in digitizer densities without sacrificing data fidelity.

Together, these articles reflect the breadth of innovation occurring at every level of data acquisition and readout electronics. From ultra-low-noise sampling and advanced FPGA synthesis techniques to wireless IoT networks and large-scale HEP data flows, researchers are expanding the capabilities of detectors and electronics to keep pace with ever-more ambitious science and engineering goals. As demonstrated in each contribution, success in the field increasingly depends on comprehensive, interdisciplinary approaches that integrate hardware, software, and signal processing into uniform, high-performance systems.

Author contributions

AV: Writing – review and editing, Writing – original draft, Conceptualization. CB: Writing – original draft, Conceptualization, Writing – review and editing. LF: Conceptualization, Writing – review and editing, Writing – original draft.

Funding

The author(s) declare that no financial support was received for the research and/or publication of this article.

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

The author(s) declared that they were an editorial board member of Frontiers, at the time of submission. This had no impact on the peer review process and the final decision.

Generative AI statement

The authors declare that no Generative AI was used in the creation of this manuscript.

Publisher's note

All claims expressed in this article are solely those of the authors and do not necessarily represent those of their affiliated organizations, or those of the publisher, the editors and the reviewers. Any product that may be evaluated in this article, or claim that may be made by its manufacturer, is not guaranteed or endorsed by the publisher.