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Back-End, CMOS-Compatible Ferroelectric FinFET for Synaptic Weights

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Building Artificial Neural Network accelerators by implementing the vector-matrix multiplication in the analog domain relies on the development of non-volatile and tunable resistances. In this work, we describe the nanofabrication of a three-dimensional HZO—WO_x Fin Ferroelectric Field Effect Transistor (FinFeFET) with back-end-of-line conditions. The metal-oxide channel (WO_x) is structured into fins and engineered such that: 1) the current-voltage characteristic is linear (Ohmic conduction) and 2) the carrier density is small enough such that the screening length is comparable to one dimension of the device. The process temperature, including the HZO crystallization, does not exceed 400°C. Resistive switching is demonstrated in FinFeFET devices with fins dimension as small as 10 nm wide and 200 nm long. Devices containing a single fin that are 10 nm wide are characterized: 5 µs long voltage pulses in the range (–5.5 and 5 V) are applied on the gate, resulting in analog and symmetric long term potentiation and depression with linearity coefficients of 1.2 and –2.5.

Keywords: ferroelectric switching, hafnium zirconium oxide, tungsten oxide, back-end-of-line compatible, ferroelectric fin field effect transistor, memristors, neuromorphic computing, synapse

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1 INTRODUCTION

The computing capability of classical digital computers, based on Complementary Metal Oxide Semiconductor (CMOS) transistors, has advanced considerably in the past decades, mainly due to the shrinking down of transistor's dimensions, as predicted by Moore's law (Moore, 1965). The advent of the Artificial Intelligence (AI) has imposed critical requirements in terms of energy efficiency and processing speed, to address ambitious problems such as speech and image recognition (Gokmen and Vlasov, 2016). Conventional von Neuman architectures face two main challenges: first, Moore's law is slowing down (due to rising fabrication cost and physical limitations), second, their performance is limited by the data transfer between the processor and the memory (Wong and Salahuddin, 2015). Brain-inspired neuromorphic architectures, allowing to perform computing at the site where data is stored, hence in-memory, are promising candidates to overcome this issue (Poon and Zhou, 2011). Such architectures consist of a collection of artificial neurons interconnected by plastic synapses in a crossbar topology which allows to efficiently perform the multiply and accumulate operation (Gokmen and Vlasov, 2016), a key computing task in neural networks (Kim et al., 2017; Yu, 2018). To imitate the biological synaptic plasticity, an analog programming capability of these synapses is required to define the synaptic weight. To achieve densely integrated neuromorphic circuits, both the material and the processes of the synaptic devices are required to be compatible with modern CMOS technology. Several technology implementations and physical

phenomena, such as Phase-Change Memory (PCM) (Lacaita, 2006; Raoux et al., 2010; Boybat et al., 2018), filamentary-based Resistive Random Access Memory (RRAM) (Baek et al., 2004; Lee et al., 2008; Waser et al., 2009) and Electro-Chemical Memory (ECRAM) (Fuller et al., 2017; Kim et al., 2019; Tang et al., 2019), can lead to synaptic behavior, but they all rely on structural modification of the active materials involved. The recent discovery of the ferroelectric properties in hafnia composites (Böscke et al., 2011), a material already present in CMOS technology, has attracted further scientific interest in the field of neuromorphic hardware based on ferroelectrics. Three main classes of devices exploiting ferroelectricity for synaptic as well as neuronal functionalities were demonstrated in the past: the two-terminal Ferroelectric Tunneling Junctions (FTJs) (Ambriz-Vargas et al., 2017; Tian and Toriumi, 2017; Chen et al., 2018a; Goh and Jeon, 2018; Yu et al., 2021), the three-terminal Ferroelectric Field-Effect Transistors (FeFETs) (Mulaosmanovic et al., 2017; Sharma et al., 2017; Krivokapic et al., 2018; Zeng et al., 2018; Mo et al., 2019) and the two-terminal Ferroelectric Photovoltaic (FePv) synapses (Cheng et al., 2020; Cui et al., 2021). Although, both FTJs and FeFETs have been extensively investigated recently, showing large dynamic ranges, low energy dissipation, and synaptic functions including short and long term plasticity as well as Spike-Timing-Dependent Plasticity (STDP) (Nishitani et al., 2012; Boyn et al., 2017; Chen et al., 2018a; Guo et al., 2018; Majumdar et al., 2019; Li et al., 2020) the FePv devices, based on the polarization control of the photovoltaic behavior that exploit the photoresponsivity as synaptic weight, were used for binary data storage (Guo et al., 2013) and recently as prototype synapse (Cheng et al., 2020). While in state of the art hafnia-based two-terminal synaptic weights, the small current flowing through the ferroelectric layer limits their scalability (Begon-Lours et al., 2021), three terminal devices have the advantage of separating the write process (through the high impedence gate) and the read process (through the channel). Hafnia-based FeFET devices exploiting Si as channel material and implemented on the Front End Of Line (FEOL) were demonstrated as artificial neurons (Mulaosmanovic et al., 2018). However, the FEOL integration imposes constraints on the device footprint, and limits the design flexibility. The Back End Of Line (BEOL) integration is advantageous, by allowing for a larger device area, which in turn leads to a larger number of ferroelectric domains and, hence, an improved analog (multi-level) behavior. Planar state of the art BEOL three-terminal synaptic devices based on $HfZrO_4$ (HZO) and utilizing a tungsten oxide (WO_x) channel, were realized in the past (Halter et al., 2020). However, in the last decade, the tri-gate technology (Lawrence and RUBIA, 2015) has replaced the planar one and allowed further CMOS transistor scaling. In this architecture, the gate surrounds the channel on three sides, creating a multigate device known as FinFET, with better gate-channel control and a smaller footprint with respect to a planar technology. In this work, we report on a scaled tri-gate FeFET (FinFeFET) having an overall footprint scaled down to four orders of magnitude with respect to (Halter et al., 2020). Being a Junction-Less Transistor (JLT) (Colinge et al., 2010; Colinge et al., 2011), no high-temperature source and drain implantation and annealing processes are required during the fabrication. The synaptic behavior is achieved through the partial polarization switching in HZO, which is used to electrostatically deplete or accumulate free carriers in the WO_x fins. We demonstrate the scaling of the ferroelectric technology down to device having 0.002 μm^2 area, and study the impact of the layout on the channel resistance, the influence of the fin's geometry on the dynamic range, the retention, the analog behavior as well as the continuous and linear synaptic weight modulation. Moreover, both the process and the materials exploited are compatible with CMOS technology, the proposed synaptic element is promising for large-scale and densely integrated neuromorphic hardware based on ferroelectrics.

2 RESULTS AND DISCUSSION

3D FeFET devices based on a W/TiN/HZO gate stack and 30 nm high WO_x fins were designed and fabricated using a process BEOL compatible, not exceeding 400°C. To investigate the effect of the layout on the device performances, several geometries of FinFeFETs were processed to find out the best trade-off in terms of fin's length, width and number. Fins of 4 nm, 8 and 10 nm width were explored, and for each of them, two different lengths, 200 and 500 nm, respectively, and configurations with 1, 5, 10, 20, and 40 parallel fins were fabricated. The substoichiometric and amorphous WO_x channel, deposited by a Plasma-Enhanced Atomic Layer Deposition (PEALD) process at 375°C, was first crystallized and oxidized by annealing in an oxygen atmosphere, and then structured into fins. The source and drain contacts were deposited on the WO_x channel through lift-off. Then the TiN/HZO stack was grown, and the ferroelectric crystallization of the latter was performed using a millisecond flash lamp anneal at 375°C. The device was encapsulated by a 5 nm of Al_2O_3 and a 100 nm of SiO_2 passivation layers. Contact pads were formed on top of the passivation layers and routed through openings to source, drain and gate. The detailed processing steps can be found in the **Sub-section 4.1**. In **Figure 1A** the result of the fabrication process after the FinFeFET contact lift-off step was imaged by a Scanning Electron Microscope (SEM). SEM analysis of the fins revealed that the targeted widths of 4 and 8 nm both resulted in an approximately 10 nm wide fin after the transfer of the design from the resist to the WO_x. This is the result of cross exposure of dense structures close to the resists resolution limit. The materials properties were characterized by Grazing-Incidence X-Rays Diffraction (GIXRD). **Figure 1B** shows the GIXRD (ω = 0.44°) performed after HZO crystallization by ms-flash lamp annealing: the peak at 2θ = 30.8° corresponds to the overlap between the (111) peak of the orthorhombic (ferroelectric) phase and the (011) peak of the tetragonal phases of HZO (Park et al., 2013). As a consequence of the low temperature crystallization technique (O'Connor et al., 2018), no monoclinic HZO phase (peaks at 28.2° and 31.8°) (Materlik et al., 2015a) is observed in our sample. The additional peaks at 28.6°, 33.6° and 34.5° can be attributed to (111), (202) and (220) Miller indices of the tetragonal $P42_1m$ phase of WO_3 (Jain et al., 2013), respectively. The peak at ≃ 36° is a combination of the multiple peaks from the orthorhombic and

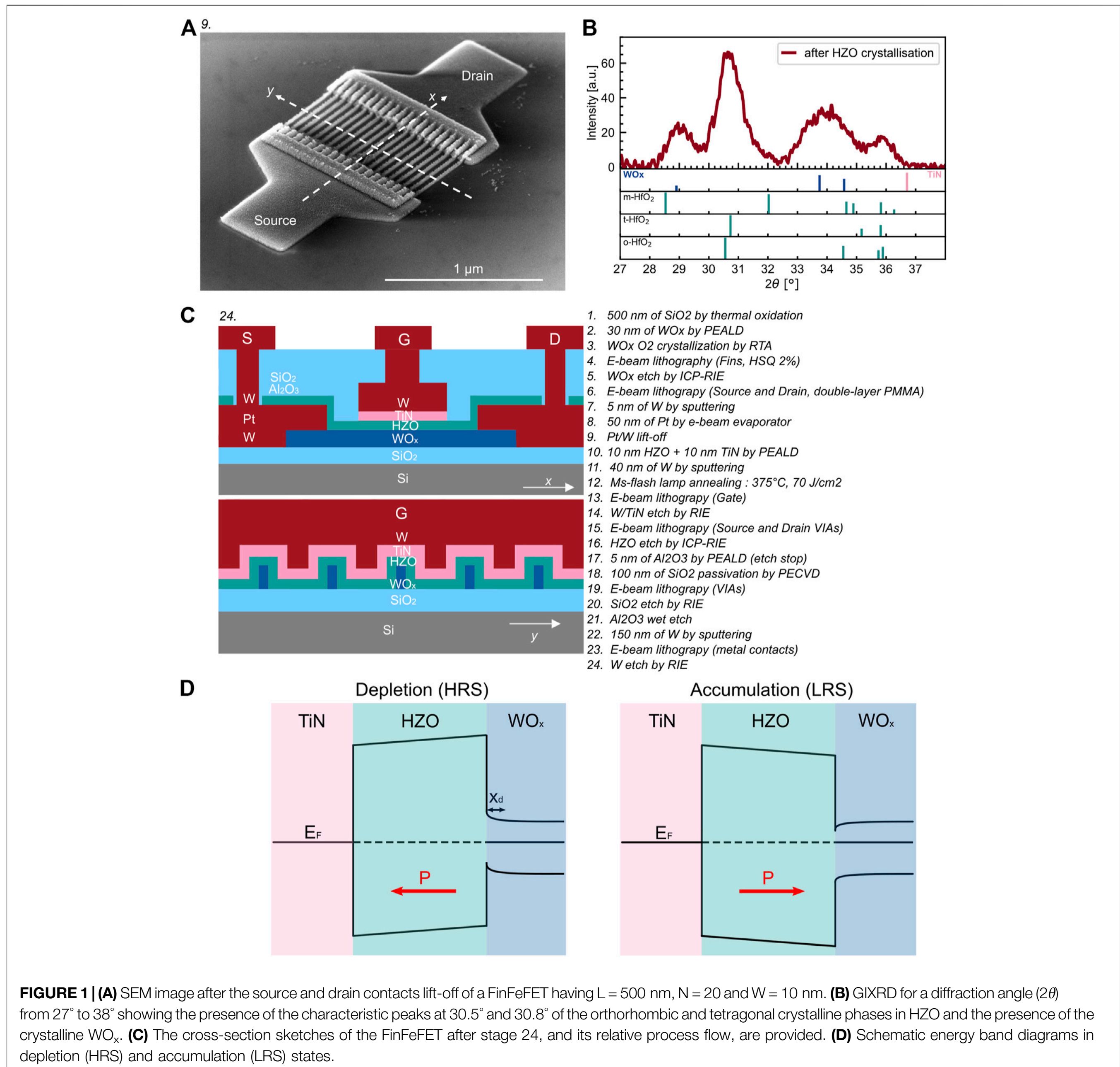

FIGURE 1 | (A) SEM image after the source and drain contacts lift-off of a FinFeFET having L = 500 nm, N = 20 and W = 10 nm. **(B)** GIXRD for a diffraction angle (2θ) from 27° to 38° showing the presence of the characteristic peaks at 30.5° and 30.8° of the orthorhombic and tetragonal crystalline phases in HZO and the presence of the crystalline WO_x. **(C)** The cross-section sketches of the FinFeFET after stage 24, and its relative process flow, are provided. **(D)** Schematic energy band diagrams in depletion (HRS) and accumulation (LRS) states.

tetragonal phases of HZO. **Figure 1C** shows the two cross-section illustrations of the FinFeFET and its relative process flow. The resistive switching of HZO—WO_x FinFeFETs was investigated through electrical characterization. Oxygen vacancies confer *n*-type semiconducting properties to sub-stoichiometric $WO_{x<3}$ (Salje and Güttler, 1984). When the HZO ferroelectric remanent polarization points toward the interface with WO_x, free carriers accumulate at the interface to screen the polarization charges in HZO, thus the channel resistance R_{SD} decreases, and the memristor is in its Low Resistive State (LRS). By contrary, when the remanent polarization points toward the TiN interface, carrier depletion occurs in tungsten oxide at the interface with HZO, causing an increase of the channel resistance R_{SD} and resulting in a High Resistive State (HRS). The schematic energy band diagrams at the equilibrium of the TiN/HZO/WO_x stack, both in depletion (HRS) and accumulation (LRS) states, are shown in **Figure 1D**.

Polarization charges are screened in the HRS state and it is possible to define a screening length (depletion width) x_d, representing the thickness of the channel where the resistance is modulated. By decreasing the carrier density n_{WO_x}, the depletion width x_d is increased (Davis, 1973). Considering the FinFeFET devices with a single fin, the overall channel resistance R_{SD} can be thought as the resistance of two channels in parallel: one of thickness x_d on the outside of the fin, in which the resistivity is modulated upon polarization switching, and a

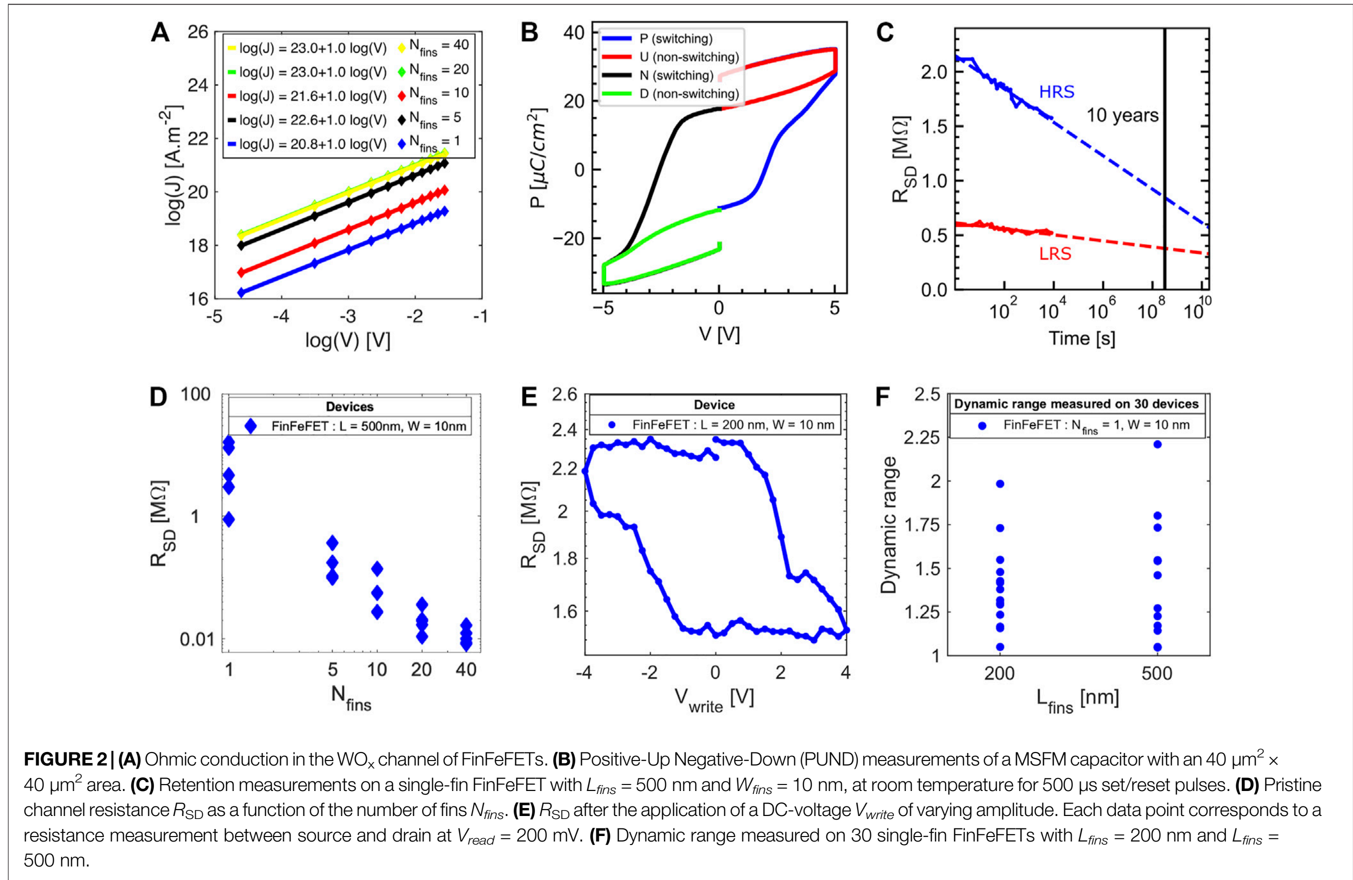

FIGURE 2 | (A) Ohmic conduction in the WO_x channel of FinFeFETs. **(B)** Positive-Up Negative-Down (PUND) measurements of a MSFM capacitor with an 40 μm^2 × 40 μm^2 area. **(C)** Retention measurements on a single-fin FinFeFET with L_{fins} = 500 nm and W_{fins} = 10 nm, at room temperature for 500 μs set/reset pulses. **(D)** Pristine channel resistance R_{SD} as a function of the number of fins N_{fins}. **(E)** R_{SD} after the application of a DC-voltage V_{write} of varying amplitude. Each data point corresponds to a resistance measurement between source and drain at V_{read} = 200 mV. **(F)** Dynamic range measured on 30 single-fin FinFeFETs with L_{fins} = 200 nm and L_{fins} = 500 nm.

bulky one which extends in the core of the fin, with a constant resistivity (Bégon-Lours et al., 2018; Halter et al., 2020). In multi-fin FeFETs, the equivalent channel resistance R_{SD} can be looked at as multiple single-fin resistances in parallel. For neuromorphic applications a large dynamic range (HRS/LRS), as well as multiple (analog) levels of the channel resistance, an absolute resistance in the tens of megohm range, good retention properties, a low device-to-device and cycle-to-cycle variation, a linear and symmetric weight-update rule, and a low power consumption are important characteristics of ideal memristors (Yu, 2018). The exact requirements vary depending on the application and from one implementation to the other. HZO is polycrystalline and the lateral domain size of HZO films prepared in the same conditions (O'Connor et al., 2018; Halter et al., 2020) is found to be ≃ 10 nm: a single fin is interfaced with several hundreds of domains. Switching only a subset of them allows the analog modulation of the channel resistance. To quantify the range of the pristine resistance from device to device, DC-electrical characterization was performed. A voltage sweep back and forth between −0.21 and 0.21 V, with a step of 20 mV, was applied between the source and the drain, keeping the gate floating. The electrical transport in the pristine state of FinFeFETs having different number of fins, is reported in **Figure 2A**. The current density J is calculated from the measured current I by $J = \frac{I}{N_{fins} \cdot h_{fins} \cdot w_{fins}}$, where N_{fins}, h_{fins} and w_{fins} are the number, the height and the width of the fins, respectively. For all the configurations, log(J) depends linearly on log(V) with a slope of 1, showing that the conduction in the channel is Ohmic. It depends on the carrier density by the relation (Sze and Ng, 2006):

$$\log(J) = \log\left(\frac{q \cdot \mu \cdot n_{WO_x}}{L_{fins}}\right) + \log(V) \quad (1)$$

where q is the elementary charge, μ the electron mobility, and n_{WO_x} the carrier density in the channel. Averaging the intercepts showed in **Figure 2A** and exploiting **Eq. 1**, the extracted $\mu \cdot n$ product in WO_x is 1.87×10^{20} (cmVs)$^{-1}$. In absence of specific structures to perform Hall measurements, it was not possible to determine the electron mobility in the channel. However, using the value of the WO_x mobility (μ_{WO_x} = 0.19 cm^2/V s) extracted by (Halter et al., 2020), the estimated carrier concentration is n_{WO_x}= 9.84 × 10^{20} cm^{-3}, which is coherent with the n-type semiconducting properties of the sub-stoichiometric $WO_{x<3}$. The remanent polarization P_r of 10 nm HZO was measured on TiN/WO_x/HZO/TiN capacitors on a different sample by Positive-Up Negative-Down (PUND) measurements (see **Subsection 4.3**) and found to be P_{r-} = −11.2 μC/cm^2 and P_{r+} = 17.7 μC/cm^2 (see **Figure 2B**). The asymmetry between positive and negative remanent polarization ($|P_{r+}| > |P_{r-}|$) indicate

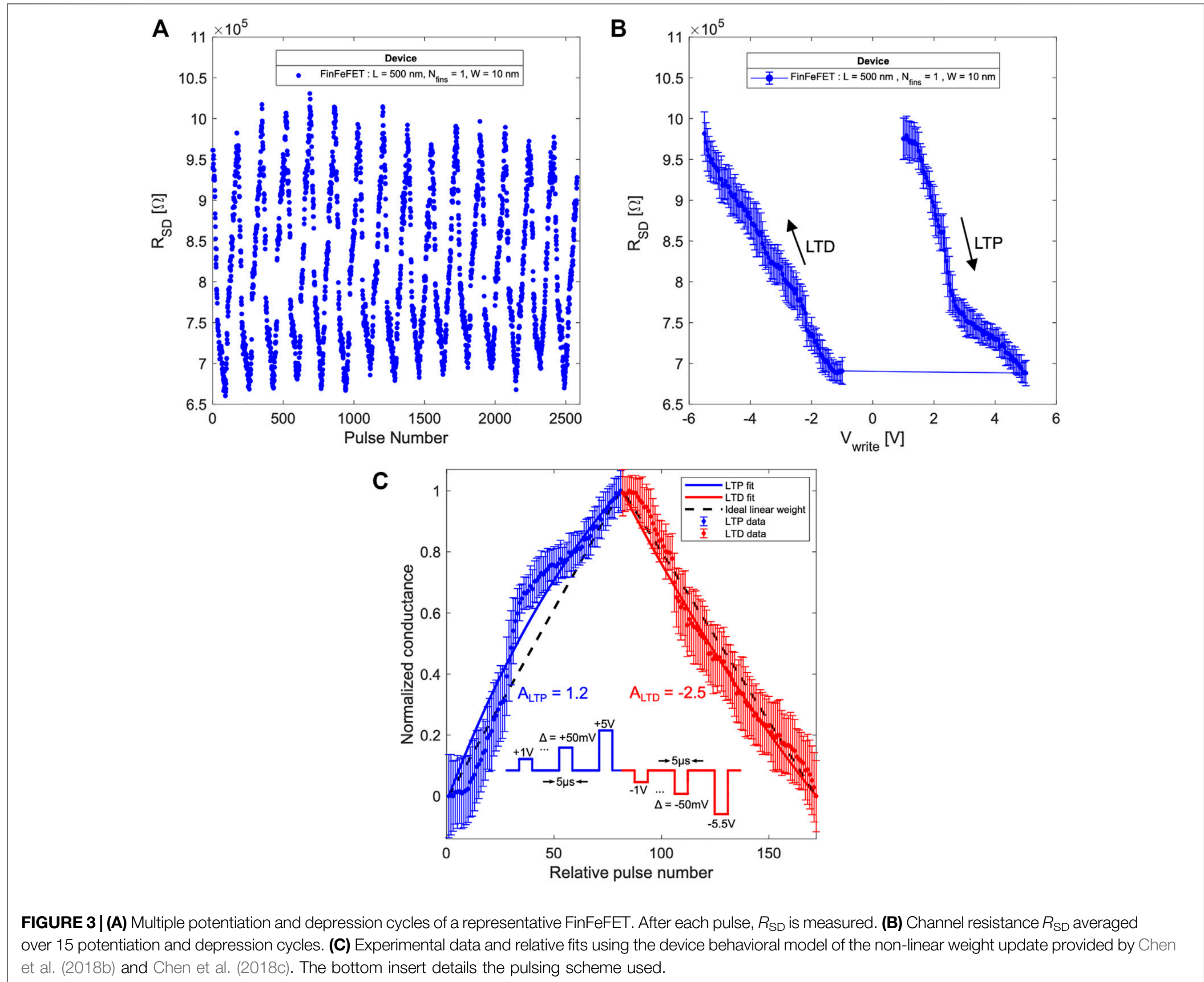

FIGURE 3 | (A) Multiple potentiation and depression cycles of a representative FinFeFET. After each pulse, R_{SD} is measured. **(B)** Channel resistance R_{SD} averaged over 15 potentiation and depression cycles. **(C)** Experimental data and relative fits using the device behavioral model of the non-linear weight update provided by Chen et al. (2018b) and Chen et al. (2018c). The bottom insert details the pulsing scheme used.

partially switched domains due to incomplete screening by the depleted WO_x layer. This results in a depolarization field across HZO (Mehta et al., 1973). Using the polarization as total charge per unit area (Q_s) we can define the electric field ($E_{interface}$) induced by it at the HZO/WO_x interface by using Gauss law (Brotherton, 2013):

$$P_{r-} = Q_s = -\epsilon_0 \cdot \epsilon_{HZO} \cdot E_{interface} \tag{2}$$

where ϵ_{HZO} is the permittivity of HZO, which for the ferroelectric phase is 29.1 (Materlik et al., 2015b). The depletion width x_d in WO_x with respect to the electric field caused by the polarization charges can be related by using Poisson's equation Brotherton (2013):

$$E_{interface} = \frac{q \cdot n_{WO_x} \cdot x_d}{\epsilon_0 \cdot \epsilon_{WO_x}} \tag{3}$$

By combining **Eqs 2**, **3**, the depletion width can be estimated as follows:

$$x_d = -\frac{\epsilon_0 \cdot \epsilon_{WOx} \cdot P_{r-}}{\epsilon_0 \cdot \epsilon_{HZO} \cdot q \cdot n_{WO_x}} = 4.5\text{nm} \tag{4}$$

where ϵ_{WO_x} is the permittivity of WO_x, equal to 189 as measured by (Halter et al., 2020). A more precise determination of x_d is not possible due to the missing μ_{WO_x} of the fins, but this approximation confirms that the effect of the polarization on the depletion width is comparable to the channel dimension. The retention properties of FinFeFET have been studied, as shown in **Figure 2C**. First, the device was set in its LRS by applying a 500 µs pulse of V_{write} = 5 V. Then, the channel resistance R_{SD} was monitored and read at 200 mV every few minutes up to 1.5 × 10^4 s. This was repeated for the HRS using a 500 µs pulse of V_{write} = −5.5 V, and the evolution of that state was monitored for the same time interval. By fitting a linear regression in the semi-log representation, a drift is observed towards lower values. Extrapolating the fit to 10 years, both the HRS and the LRS are still differentiable, but the dynamic range is reduced. Remarkably, both the states drifted towards lower values,

indicating that this drift does not originate from the back-switching of ferroelectric domains caused by the depolarization field, but possibly from an oxygen exchange between the WO_x and HZO, which progressively reduces the channel. This is more pronounced after setting the HRS (oxygen drift from HZO to WO_x by negative write field). The pristine resistance R_{SD} of each device was extracted. A decreasing trend of R_{SD} as a function of the number of fins is reported for a representative FinFeFET configuration (**Figure 2D**). Since multiple-fin configurations are a convolution of the single-fin ones, and since for neuromorphic applications, the absolute resistance should be in the megohm range (Gokmen et al., 2016), further electrical characterization was performed only on single-fin devices, which achieved the targeted resistance and the smallest footprint. The resistive switching of a representative FinFeFET (**Figure 2E**) with a 10 nm wide and 200 nm long fin, was investigated by applying a DC voltage of varying amplitude V_{write} on the gate of the memristor, having the source and the drain as common reference, and reading the channel at V_{read} = 200 mV. A more detailed description of the writing and reading procedures can be found in the **Sub-section 4.3**. By sweeping V_{write} from −4 to 4 V, R_{SD} shows a hysteresis cycle from 1.5 MΩ to 2.4 MΩ (HRS/LRS ≃ 1.53). Set and reset operations occur with a positive and negative programming voltage on the gate, respectively. 30 single fin devices were characterized as previously explained, to measure the static dynamic range (**Figure 2F**). The variability in the dynamic range may be due to processing at the limit of our lithographic capabilities, as well as an inhomogeneous WO_x material.

Several pulsing schemes on HZO based FeFETs have been investigated in the past (Jerry et al., 2018). In this work, the scheme using pulses with varying amplitudes and constant width was used since it optimizes the number of accessible polarization states (Jerry et al., 2018). The analog nature of a representative FinFeFET (**Figure 3A**) having a 10 nm wide and 500 nm long fin, was explored by applying voltage pulses of varying amplitude V_{write} while keeping a fixed pulse duration of 5 µs. For the potentiation, V_{write} was increased from 1 to 5 V, and for the depression, decreased from −1 to −5.5 V, with 50 mV steps. A slightly higher voltage was used for the depression to compensate the built-in field in HZO. After each pulse, the channel resistance R_{SD} was measured at V_{read} = 200 mV, keeping the gate floating. The memristor showed a HRS of ≃ 1 MΩ and a LRS of ≃ 0.7 MΩ (HRS/LRS ≃ 1.4). With respect to the DC-electrical characterization, almost all the devices had a decrease in dynamic range. This may be explained considering the short programming pulses and that the dynamics of ferroelectric switching in polycrystalline HZO films follow the Merz law (Chanthbouala et al., 2012), (Paruch et al., 2006), hence the coercive field (E_c) depends linearly on the logarithm of the writing time, as detailed for polycrystalline HZO devices in (Bégon-Lours et al., 2021). Another explanation could be an oxygen drift across the HZO—WO_x interface, a much slower process than ferroelectric switching, that would lead to an oxidation/reduction of the WO_x channel. The drift phenomena should be more pronounced in the DC potentiation and depression and thereby lead to the observed dynamic range dependence on the write signal length. The cycle to cycle variability was taken into account averaging all the potentiation and depression cycles (**Figure 3B**). By decreasing the range of V_{write}, the dynamic range is reduced. The number of the intermediate states is defined by the potentiation and depression step size, which can be further reduced to increase the resolution. The resistive states are not all differentiable, however the monotonic increasing and decreasing trends are desirable for online learning. The weight-update linearity was quantified by fitting the normalized weight update characteristics, by a function of the normalized pulse number, as proposed by (Chen et al., 2018b; Chen et al., 2018c):

$$f(x) = \frac{1 - \exp\left(-\frac{x}{A}\right)}{1 - \exp\left(-\frac{1}{A}\right)} \tag{5}$$

The parameter A was chosen by minimizing the root mean square error of the fitting. Values of A_{LTP} = 1.2 for the potentiation and A_{LTD} = −2.5 for the depression, respectively, were found (see **Figure 3C**).

Considering the ferroelectric synaptic weight dependence both on the pulse amplitude and duration, FinFeFETs are promising devices for Spike-Timing-Dependent Plasticity (STDP). However, STDP was not implemented with such devices in this work, since it requires tailored spike shapes as described by (Boyn et al., 2017) in ferroelectric perovskites and by (Max et al., 2020) in ferroelectric hafnia.

3 CONCLUSION

We developed a manufacturing process to allow the transfer and the scale-down of the FeFET planar technology into a multigate FinFeFET configuration. The fabrication process is compatible with the integration in the back end of line of CMOS technology and is using only abundant materials, making it suitable for large-scale integration. An Ohmic conduction in scaled WO_x fins, as well as good retention, analog states and an almost symmetric and linear potentiation and depression were obtained. Future work will focus on controlling the carrier concentration of WO_x fins, to further increase the resistance range and the dynamic range.

4 EXPERIMENTAL SECTION

4.1 Sample Fabrication

A 500 nm thick SiO_2 was grown on Si by thermal oxidation. Then, 30 nm WO_x was deposited using a $(BuN)_2W(NMe_2)_2$ precursor and O_2 plasma at T = 375°C in an Oxford Instruments Plasma-Enhanced Atomic Layer Deposition (PEALD) system. The crystallization and the oxidation of WO_x to WO_3 was performed in a Rapid Thermal Annealer (RTA) by O_2-annealing at T = 350°C for 30min. The WO_3 was then structured using an Inductively Coupled Plasma Reactive Ion Etcher (ICP-RIE) with SF_6 plasma, and Hydrogen Silsesquioxane (HSQ) 2% as negative resist. The source and drain metal contacts

were defined by lift-off using a double layer PMMA e-beam resist. 5 nm of W was first deposited by sputtering, then 50 nm of Pt was evaporated prior to the lift-off. An approximately 10 nm thick layer of HZO was grown in PEALD system through a process exploiting alternating cycles of tetrakis-(ethylmethylamino) hafnium (TEMAH) and bis(methyl-η5-cyclopentadienyl) methoxymethylzirconium (ZrCMMM) at T = 300°C. Then, further 10 nm of TiN were deposited using tetrakis-(dimethylamino)titanium (TDMAT) as precursor and N_2/H_2 plasma in a PEALD system. The sample was then immediately transferred to a sputter chamber for the deposition of 40 nm W as gate electrode. Millisecond flash lamp annealing (O'Connor et al., 2018), with a background temperature of 375°C and a flash energy density of 70 J/cm^2, was performed to crystallize HZO. The patterning of the gate electrode was achieved using a Reactive Ion Etcher (RIE) with SF_6 plasma. Source and drain vias were etched through the HZO by ICP-RIE with CHF_3/O_2 plasma. The passivation consists of 5 nm Al_2O_3 by PEALD using trimethylaluminum (TMA) as precursor and 100 nm SiO_2 by plasma-enhanced chemical vapor deposition (PECVD). Vias were etched using an RIE with a CHF_3/O_2 plasma. Al_2O_3, used as etch stop layer during SiO_2 etching, was then removed by a wet etching in MIF726 developer. Finally, the contacts were realized by depositing 150 nm W by sputtering and defined in a RIE with an SF_6/O_2 plasma.

4.2 Structural Characterization

Grazing-Incidence X-Ray Diffraction (GIXRD) measurements were performed by a Bruker D8 Discover diffractometer equipped with a rotating Cu anode generator. The Scanning Electron Microscope (SEM) system used in this work is the FEI Helios NanoLab 450S.

4.3 Electrical Characterization

The PUND measurements were performed on a TF2000 ferroelectric analyzer from aixACCT with a frequency of 1 kHz on capacitors with an area of 40 μm^2 × 40 μm^2. Prior to the PUND measurement, bipolar cycling stress with an AC amplitude of 3.5 V and frequency of 1 kHz for 10^3 cycles was applied to wake-up the HZO. The DC and the pulsed electrical characterization of the memristors were performed using an Agilent B1500A semiconductor device analyzer. Before the DC characterization of the dynamic range, a wake-up procedure of the HZO with 100 cycles of ±4 V was applied. Set (reset) of the FinFeFETs was obtained by applying a positive (negative) DC bias of decreasing (increasing) amplitude on the gate, keeping the source and drain electrodes grounded. After the application of each bias (whose duration was not controlled) of amplitude V_{write} (that varies in the −4 to 4 V range) the channel resistance was measured at V_{read} = 200 mV, keeping the gate floating. During the pulsed characterization, V_{write} pulses were generated by a Waveform Generator Fast Measurement Unit (WGFMU) of a Agilent B1500A, and applied directly to the gate through a triax cable, while grounding both the source and the drain. After each pulse, the channel resistance R_{SD} was measured, keeping the gate floating and applying a voltage sweep from −200 to 200 mV along the channel. R_{SD} was then determined by reading the resistance at 200 mV.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

AUTHOR CONTRIBUTIONS

DF has contributed with the fabrication, the electrical measurements and interpretation of the results as well as with the writing of the manuscript. MH initiated the project and contributed with the fabrication, the design and technical guidance, with the interpretation of the data and revision of the manuscript. LB-L and BO have contributed with the interpretation of the data and manuscript revision.

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Conflict of Interest: DFF, LB-L and BJO were employed by the company IBM Research Europe.

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