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Breakdown-limited endurance in HZO FeFETs: Mechanism and improvement under bipolar stress

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Breakdown is one of main failure mechanisms that limit write endurance of ferroelectric devices using hafnium oxide-based ferroelectric materials. In this study, we investigate the gate current and breakdown characteristics of $Hf_{0.5}Zr_{0.5}O_2$/Si ferroelectric field-effect transistors (FeFETs) by using carrier separation measurements to analyze electron and hole leakage currents during time-dependent dielectric breakdown (TDDB) tests. Rapidly increasing substrate hole currents and stress-induced leakage current (SILC)-like electron currents can be observed before the breakdown of the ferroelectric gate insulator of FeFETs. This apparent degradation under voltage stress is recovered and the time-to-breakdown is significantly improved by interrupting the TDDB test with gate voltage pulses with the opposite polarity, suggesting that defect redistribution, rather than defect generation, is responsible for the trigger of hard breakdown.

KEYWORDS

ferroelectrics, MOSFET, reliability, oxide breakdown, substrate hole current

1 Introduction

HfO_2-based ferroelectric thin films have been actively employed in recent electron device research thanks to their CMOS compatibility, established know-how on the fabrication process, and high scalability of thickness to 10 nm or lower (Böscke et al., 2011a; Müller et al., 2012; Park et al., 2015; Kim et al., 2018; Migita et al., 2018; Tan et al., 2021; Toprasertpong et al., 2022a; Schroeder et al., 2022). Ferroelectric field-effect transistors (FeFETs) with HfO_2-based ferroelectric thin films as gate insulators have received considerable attention, not only because of the maturity of the HfO_2 deposition technology in the advanced transistor process, but also because of their low energy consumption, high speed, and satisfactory retention during their operation. HfO_2-based FeFETs have been investigated as promising devices for low-power non-volatile memory (Böscke et al., 2011b; Trentzsch et al., 2016; Dünkel et al., 2017; Florent et al., 2018a; Müller et al., 2021) and non-von Neumann computing applications (Jerry et al., 2018; Dutta et al., 2020; Matsui et al., 2021; Toprasertpong et al., 2022b; Luo et al., 2022).

Despite their excellent properties, one of the most crucial issues to be dealt with towards the practical use of HfO_2-based FeFETs is the write endurance. There are two

major mechanisms that have been reported to determine the write endurance of FeFETs: the memory window narrowing and gate dielectric breakdown. The memory window narrowing refers to a phenomenon where a separation of the threshold voltages of the two states (high and low threshold voltage states) becomes gradually smaller and eventually becomes zero after certain operating cycles. The polarization states are no longer able to be read out through threshold voltages and FeFETs lose a capability as memory devices. On the other hand, gate dielectric breakdown refers to a situation where the gate insulator experiences hard breakdown under a certain amount of electrical stress. Hard breakdown makes gate insulators conductive, electrically connects the gate and channel, and causes FeFETs to lose their function as field-effect transistors.

Memory window narrowing and gate dielectric breakdown originate from different physics and occur almost independently; therefore, the write endurance of FeFETs, i.e., a number of write operations before failure, is determined by the mechanism that leads to earlier failure. The dominant mechanism depends on the device property and the operation scheme of each specific device and application. Write endurance of state-of-the-art FeFETs is typically dominated by the memory window narrowing (Böscke et al., 2011b; Trentzsch et al., 2016; Yurchuk et al., 2016; Dünkel et al., 2017; Florent et al., 2018a; Gong et al., 2018) because of the presence of large density of trapped charges in the vicinity of the interfacial layer (IL) between HfO_2 and Si (Toprasertpong et al., 2019; Toprasertpong et al., 2020a), while there are only a few reports showing that endurance of FeFETs is limited by gate dielectric breakdown (Ni et al., 2018; Peng et al., 2021). That is, the FeFET operation so far usually reaches failure because of memory window narrowing before gate dielectric breakdown occurs; thus, there is still a poor understanding of the gate dielectric breakdown mechanism in HfO_2-based FeFETs. On the other hand, a lot of effort has been put on the material and device-structure engineering such that there have already been some reports in recent years demonstrating FeFET memory devices with remarkably suppressed memory window narrowing (Sharma et al., 2020; Yan et al., 2020; Tan et al., 2021; Liao et al., 2022). In such devices with suppressed memory window narrowing, gate dielectric breakdown may become a dominant mechanism that limits write endurance and play a crucial role in device reliability. Furthermore, there are some applications of FeFETs using new-concept computing that are insensitive to memory window narrowing, such as reservoir computing (Nako et al., 2022). In such applications, gate dielectric breakdown will be a dominant endurance-limiting mechanism. Therefore, gaining an understanding of the mechanism of gate dielectric breakdown is important to improve the overall write endurance characteristics of HfO_2-based FeFETs.

In this study, we investigate the breakdown characteristics and the stress-induced degradation behavior as well as the underlying physical mechanism in $Hf_{0.5}Zr_{0.5}O_2$ (HZO)/IL/Si FeFETs. The carrier separation measurement and interrupted stress for time-dependent dielectric breakdown (TDDB) evaluation are employed to analyze the physical mechanism underlying gate dielectric breakdown.

2 Sample preparation

The process flow is shown in Figure 1A. We fabricated *n*-channel non-ferroelectric FETs (called here as non-ferro-FET) with a paraelectric HfO_2 gate insulator and FeFETs with a ferroelectric HZO gate insulator on p-type Si substrates with a moderate doping concentration of 4×10^{15} cm^{-3}. After the source and drain (S/D) regions were doped by phosphorus ion implantation and annealed to activate dopants, the Si substrates were cleaned by hydrochloric-peroxide mixture (HPM)-last cleaning process to grow a high-quality SiO_2 IL (Toprasertpong et al., 2020b). For FeFETs, 10-nm-thick ferroelectric HZO was deposited by atomic layer deposition (ALD) using at using tetrakis (ethylmethylamino)hafnium (TEMAH), tetrakis (ethylmethylamino)zirconium (TEMAZ), and H_2O at 300°C. For non-ferro-FETs, 10-nm-thick HfO_2 was deposited in a similar way but without TEMAZ. TiN was deposited as gate metal by sputtering and silicon-doped aluminum was deposited as S/D contacts by thermal evaporation. Samples were annealed at 400°C for 30 s in a N_2 atmosphere to crystalized the ferroelectric phase in FeFETs. The non-ferro-FETs were also annealed at the same condition. Except the ALD step, both samples were processed simultaneously in the same chamber to ensure the same device condition. Figures 1B, C show transmission electron microscopic (TEM) images of the gate stacks of a non-ferro-FET and a FeFET, respectively, indicating that HZO was crystallized whereas HfO_2 remained amorphous. The IL thickness was similar in the both samples.

3 Results and discussion

3.1 Band diagram and breakdown position

Before we discuss the experimental results of the leakage and breakdown behaviors, we examine the band diagram of the HZO (10 nm)/IL (0.7 nm)/Si gate stack and the possible gate leakage path. Figure 2A depicts an example of an ideal band diagram of the HZO/IL/Si gate stack at 3 V when HZO has ferroelectric polarization of 10 $\mu C/cm^2$. Due to high ferroelectric polarization, most literature considers a band diagram with a strong electric field across the IL, which significantly pulls down the band position HZO, as shown in Figure 2A (Müller et al., 2016; Yurchuk et al., 2016; Gong et al., 2018; Mulaosmanovic et al., 2021; Peng et al., 2021). In such a case, the breakdown of the IL is supposed to determine the gate dielectric breakdown of FeFETs. However, it has been reported that a large density of trapped

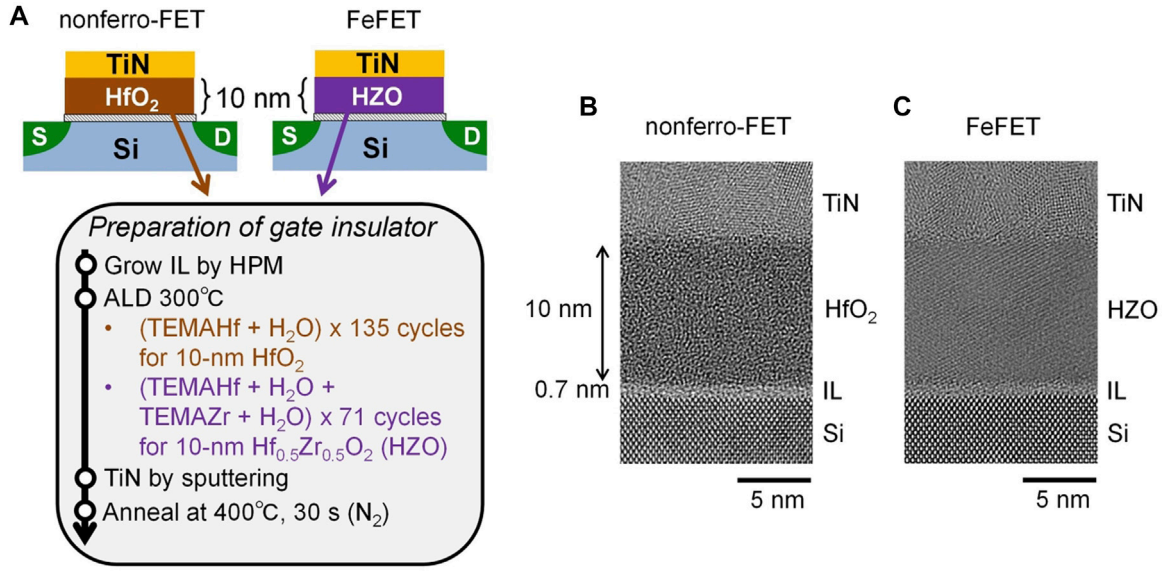

FIGURE 1
(A) Fabrication process flow. TEM images of **(B)** HfO_2 non-ferro-FET and **(C)** HZO FeFET. HZO was crystallized whereas HfO_2 remained amorphous.

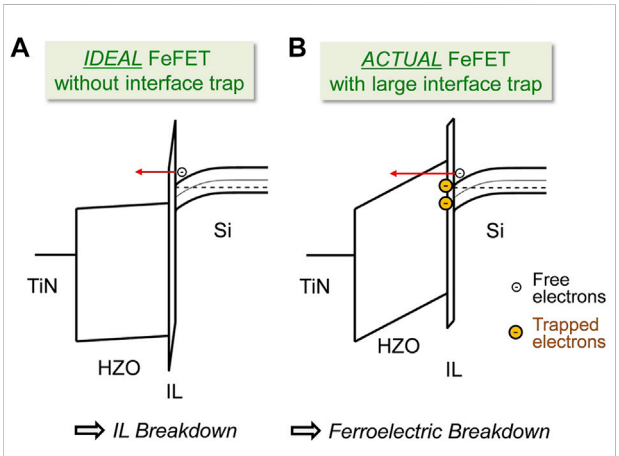

FIGURE 2
Schematic band diagram of HZO/IL/Si gate stack **(A)** when there is no interface charge trapping and **(B)** when there is a large amount of interface charge trapping, where 90% of induced electrons are trapped. Here, the Si band was scaled in the depth direction by 1:100 ratio to make the band bending clear.

charges near the HZO/IL interface electrically screens the polarization and suppresses the electric field across the IL (Toprasertpong et al., 2019; 2022c). Figure 2B depicts the band diagram with ferroelectric polarization of 10 μC/cm^2 and 90% (Ichihara et al., 2020) of induced electrons are trapped at the HZO/IL interface. It can be seen that the band of HZO is not at such a low energy position. This fact indicates that electrons have to tunnel through a thick HZO layer and thus the breakdown of HZO is necessary to describe the gate breakdown failure of FeFETs.

3.2 Device characteristics

The I-V_g characteristics of the non-ferro-FET and FeFET are shown in Figures 3A, B, respectively, for gate current I_g, drain current I_d, source current I_s, and substrate current I_{sub}. A gate length L is 10 μm and a gate width W is 100 μm. As expected, the non-ferro-FET exhibits the I_d-V_g characteristics with clockwise hysteresis, which is a feature of electron trapping during V_g scans. On the other hand, the FeFET exhibits counterclockwise hysteresis, which is a feature of ferroelectricity, with a memory window of approximately 1.8 V. Comparison of the I-V_g characteristics of the non-ferro-FET and FeFET indicates interesting features on I_g and I_{sub}. Gate current I_g in the HZO FeFET is much larger by several orders of magnitude than in non-ferro-FETs having HfO_2 with a similar physical thickness. This can be understood from the fact that the poly-crystallinity and a lot of defects such as oxygen vacancies in HZO can promote the gate leakage current, as shown in Figure 3C. It is also found that the substrate current I_{sub} in the FeFET rapidly increases by four orders of magnitude in a narrow range of V_g = 3.6 V–4.0 V during the forward V_g scan, which is in the same range that I_g also increases rapidly by two orders of magnitude. This finding suggests that a study of the behavior of I_{sub} would be helpful in understanding the behavior of the gate leakage and gate

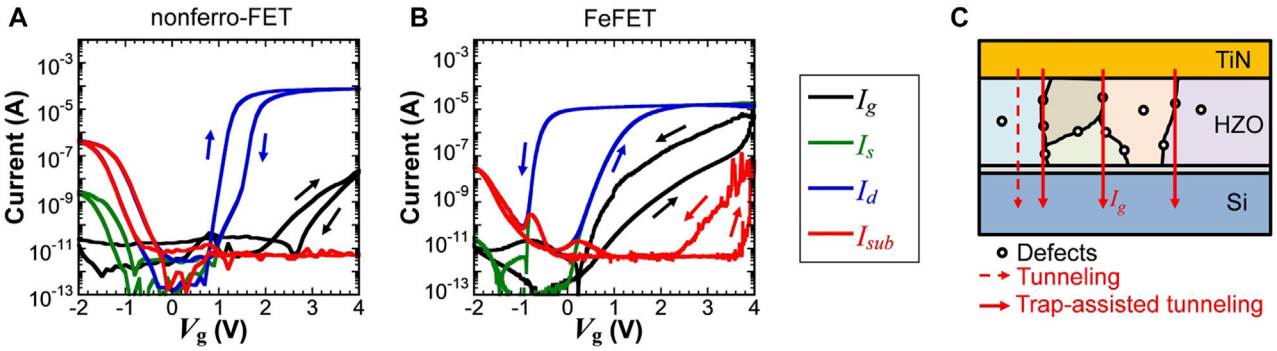

FIGURE 3
Characteristics of I_g, I_d, I_s, and I_{sub} for **(A)** HfO_2 non-ferro-FET and **(B)** HZO FeFET with L/W = 10/100 μm. I_g of a HZO FeFET is around 10^3 times higher than that of a HfO_2 non-ferro-FET. Steeply increasing substrate current I_{sub} can be found in FeFETs. **(C)** Leakage current path in ferroelectric HZO gate insulator.

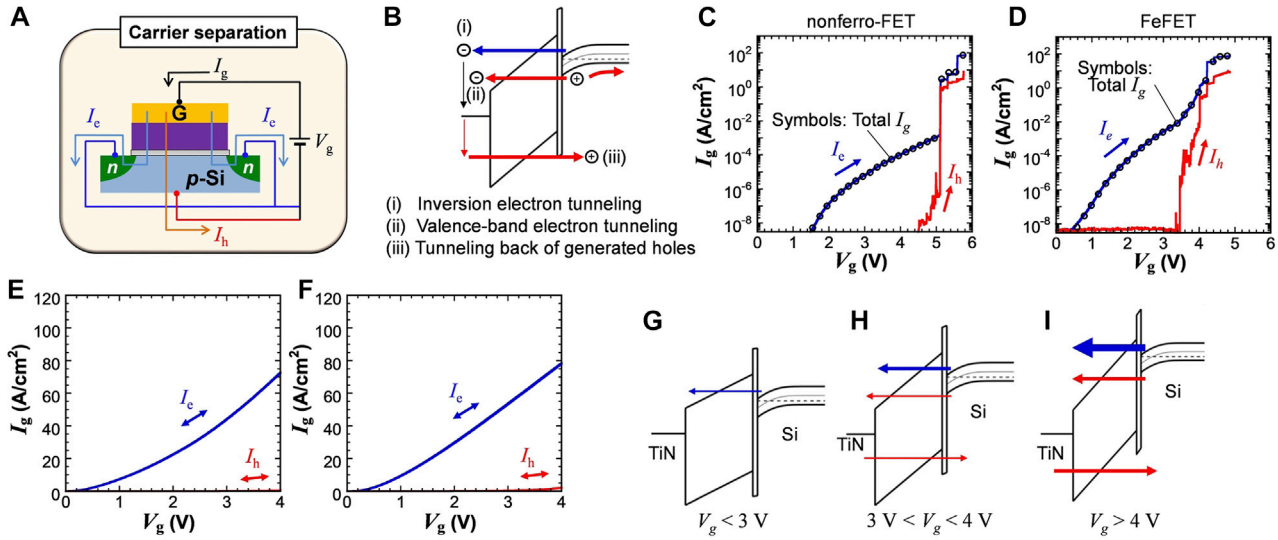

FIGURE 4
(A) Schematic of carrier separation measurement for analyzing gate current. **(B)** Current components in gate current. Inversion electron tunneling flows through S/D, while tunneling of valence-band electrons and generated holes appears as substrate current. Electron-component (blue lines), hole-component (red lines), and total (circle symbols) gate currents of **(C)** non-ferro-FET and **(D)** FeFET when V_g was scanned from 0 V until the breakdown point. The electron component dominates the gate current while the hole component rapidly increases near the breakdown voltage. Gate currents after breakdown for **(E)** non-ferro-FET and **(F)** FeFET, showing ohmic characteristics. Band diagrams and expected gate current components at **(G)** low V_g, **(H)** $V_g < V_{BD}$, and **(I)** $V_g > V_{BD}$.

dielectric degradation. The non-ferro-FET in Figure 3A does not exhibit this I_{sub} behavior.

3.3 Carrier separation measurements

Carrier separation measurements (Eitan et al., 1983; Weinberg et al., 1985) were carried out to analyze the behavior of gate leakage and gate dielectric degradation. The electrical measurement tool (Keysight B1500A with high-resolution source/monitor unit modules) was connected with FETs in a way shown in Figure 4A, where $V_d = V_s = V_{sub} = 0$. The current detected at the S/D terminal corresponds to the electron component of gate current, denoted by I_e, while the current detected at the substrate corresponds to the hole component, denoted by I_h. When V_g is larger than the threshold voltage, I_e

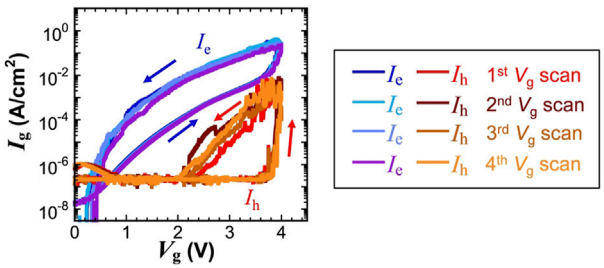

FIGURE 5
Repeatedly measured electron and hole components of I_g in the FeFET. Repeatable current implies that it is not a behavior of permanent trap generation.

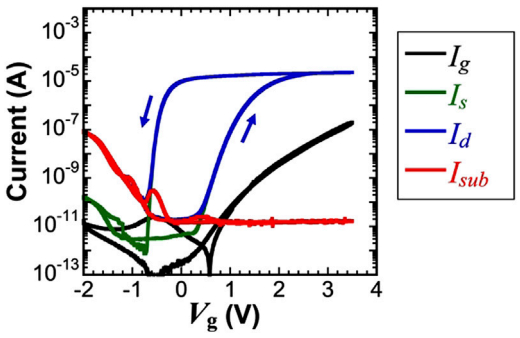

FIGURE 6
Characteristics of I_g, I_d, I_s, and I_{sub} for HZO FeFET with L/W = 10/100 μm when the V_g ranged is limited below 3.5 V. No substrate current I_{sub} is observed at positive V_g.

corresponds to the tunneling current of inversion electrons from the Si substrate to the gate, whereas I_h corresponds to the sum of the tunneling current of valance-band electrons in the Si substrate to the gate (Weinberg et al., 1985; Schuegraf et al., 1994b; Shanware et al., 1999) and the tunneling back current of holes from the gate to the Si substrate (Schuegraf et al., 1994a; Schuegraf et al., 1994b; Kobayashi et al., 1995), as illustrated in Figure 4B.

The results of the carrier separation measurements are shown in Figures 4C, D for the HfO_2 non-ferro-FET and HZO FeFET, respectively. In these measurements, V_g of pristine samples was scanned from 0 V to the positive voltage where breakdown occurs. It can be seen that tunneling of inversion electrons is the main contribution of I_g for both the non-ferro-FETs and FeFET. I_h is found to be under detection limit in a low V_g regime, but it rapidly increases at V_g close to the breakdown voltage. The breakdown voltage V_{BD} of the non-ferro-FET is approximately 5.2 V, whereas the FeFET reaches hard breakdown much earlier at approximately V_{BD} = 4.1 V. Earlier breakdown is contributed to more defects in HZO than those in HfO_2, in agreement with larger gate current shown in Figures 3A, B. Hard breakdown of the non-ferro-FET occurs at comparatively low I_h, whereas I_h of HZO FeFET keeps noisy until very high level of I_h. After breakdown, the electrical properties of the gate insulators of both the devices become ohmic and dominated by electron current, as shown in Figures 4E, F.

The band alignments are shown in Figures 4G–I. At small V_g, it is clear from the band alignment that electrons in the conduction band of Si can easily tunnel to the gate. At V_g in the mid-range, both electrons in the valence band and holes generated at the gate can tunnel more easily, resulting in increasing I_h. At large V_g, an electric field across HZO is so large that hole tunneling back can reach the valence band of HZO, resulting in large I_h. Increasing hole tunneling back consequently causes breakdown in the gate insulator, as the hole tunneling back is known to be the main cause of damage in the gate insulator (Schuegraf et al., 1994a; Schuegraf et al., 1994b; Takayanagi et al., 2001).

Results of repeated measurements of I_e and I_h in a V_g scan range of −2 V to 4 V are shown in Figure 5. It is interesting that rapidly increasing I_h and I_e at V_g > 3.5 V in the FeFET, together with noisy signals before breakdown, are recovered during the V_g backward scan, resulting in repeatable I_h-V_g and I_e-V_g characteristics. These results imply that, although rapidly increasing I_h is an indication that breakdown is going to be triggered, the permanent degradation still does not occur yet in this condition and occurs when I_h increases in a step-wise manner, which can be observed in Figure 4D at V_g = 4.1 V.

The analysis above suggests that I_h is a convenient indicator for determining appropriate operating range of V_g. Figure 6 shows the I-V_g characteristics of the FeFET when V_g was kept below 3.5 V. In this V_g range, the ferroelectric hysteresis can still be achieved with a satisfactory memory window of 1.7 V while I_h is suppressed to under the detection limit. Note that I_{sub} at negative V_g is due to gate-induced drain leakage (GIDL), which is unrelated to gate leakage currents. Although I_h does not necessarily imply to device degradation as discussed in Figure 5, hole tunneling back is flowing and leads to a higher probability that breakdown is triggered; therefore, the operating condition with high I_h should be avoided. The reliability of FeFETs operating in this way is notably improved and we cannot observe breakdown under electrical stress for a practically long time (>10^5 s).

3.4 Time-dependent dielectric breakdown: Constant voltage stress and interrupted test

TDDB tests with a carrier separation setup were carried out to gain more insights into the breakdown behavior of FeFETs.

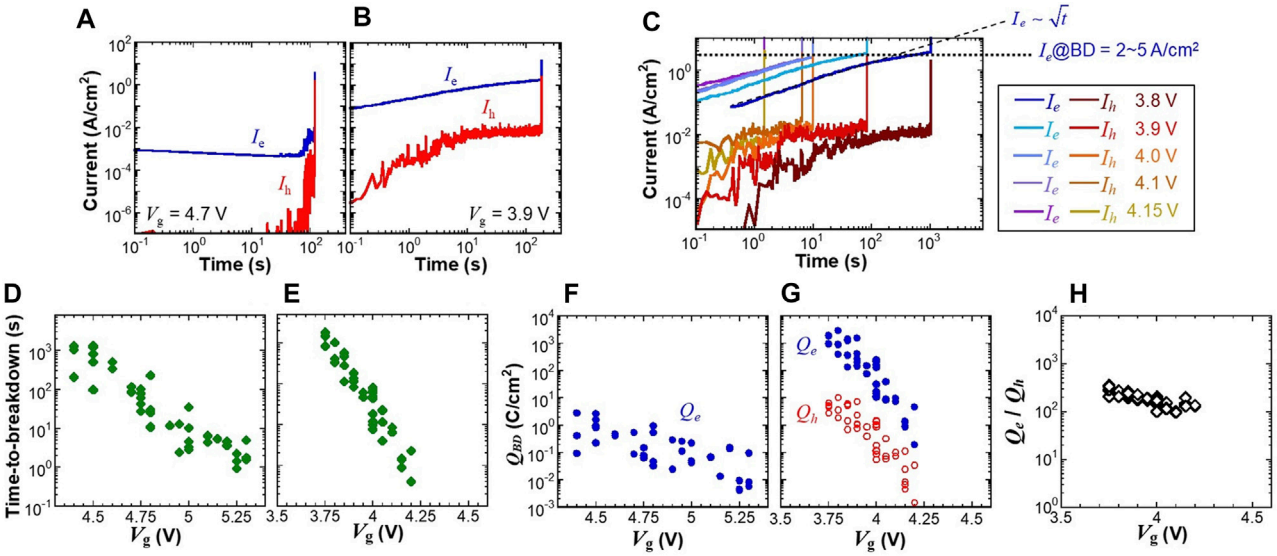

FIGURE 7
TDDB results with carrier separation for **(A)** HfO_2 non-ferro-FET at V_g = 4.7 V and **(B)** HZO FeFET at V_g = 3.9 V with L/W = 100/100 μm. A SILC-like behavior, with current increasing with stress time, can be observed in FeFETs. **(C)** TDDB of FeFET at different stress voltage V_g. Electron current increases with time by approximately $I_e \propto \sqrt{t}$. The electron and hole current levels at breakdown have weak dependency on V_g. Time-to-breakdown of **(D)** non-ferro-FET and **(E)** FeFET under constant voltage stress. The FeFET has a stronger dependence on V_g. Charge-to-breakdown Q_{BD} for **(F)** non-ferro-FET and **(G)** FeFET under constant voltage stress. Q_{BD} in the FeFET strongly depends on stressing voltage, whereas Q_{BD} in the non-ferro-FET is almost constant. **(H)** Q_e/Q_h ratio at breakdown condition for FeFET.

$I_e(t)$ and $I_h(t)$ under constant voltage stress (CVS) as a function of stress time t are shown in Figures 7A, B for non-ferro-FETs and FeFETs, respectively. Both $I_e(t)$ and $I_h(t)$ of the FeFET increase with time, which is in the opposite direction of $I_e(t)$ of non-ferro-FETs in the early stage. Note that I_h of non-ferro-FETs is so low that cannot be measured until breakdown, indicating that there is less hole tunneling back in non-ferro-FETs. We call the behavior of FeFETs having $I_e(t)$ increasing with time as a SILC-like behavior, as stress-induced leakage current (SILC) refers to a phenomenon that a leakage current increases with electrical stress. This SILC-like behavior of $I_e(t)$ of FeFETs can be fitted with a power-law function to be $I_e \propto \sqrt{t}$, independent of V_g stress, as displayed in Figure 7C. Increasing gate current over time becomes positive feedback to the damage in the gate insulator, leading to breakdown when I_e is raised to the order of A/cm^2. The I_e and I_h levels that trigger breakdown are almost independent of the stress voltage V_g.

Time-to-breakdown t_{BD} under CVS are summarized in Figures 7D, E for non-ferro-FETs and FeFETs, respectively. Not only the breakdown at lower V_g than non-ferro-FETs but also t_{BD} more sensitive to V_g can be observed for FeFETs, with t_{BD} of approximately 10^3 s at V_g = 3.75 V reduced to approximately 10^{-1} s at V_g = 4.2 V. The results of charge-to-breakdown Q_{BD} for electrons $Q_e = \int I_e(t)dt$ and holes $Q_e = \int I_h(t)dt$ are summarized in Figures 7F, G for non-ferro FETs and FeFETs, respectively. An obvious difference in the Q_{BD}-V_g properties in FeFETs and non-ferro-FETs can be observed. While the total electron fluence Q_e of non-ferro-FETs at which the breakdown of HfO_2 gate insulators occurs has only a weak dependence on stress voltage (note that Q_h could not be extracted as I_h was too low), the total electron Q_e and hole fluences Q_h at which FeFETs reach breakdown vary in a wide range, implying that the total fluence is not a factor that is responsible for the trigger of breakdown of HZO insulators in FeFETs. Figure 7H shows the ratio of Q_e/Q_h at different stress voltages. It is interesting that the electron-to-hole ratio of Q_{BD} of FeFETs is almost constant independent of stress voltage. This behavior is remarkably different from conventional SiO_2-gate MOSFETs, where the hole fluence Q_h triggers gate dielectric breakdown and the Q_e/Q_h ratio is not a constant (Chen et al., 1986; Schuegraf et al., 1994a). This finding indicates that the gate dielectric breakdown mechanism in FeFETs should be different from SiO_2-gate MOSFETs. We could not compare with non-ferro-FETs as Q_h was below the detection limit, so further investigation of the Q_e/Q_h ratio in non-ferro-FETs is needed to specify whether or not the constant Q_e/Q_h ratio is a unique feature of FeFETs. Further studies of what physical parameters trigger the breakdown of HZO insulators in FeFETs would provide a clearer understanding of the interaction between the leakage current and gate dielectric breakdown event in FeFETs.

We have observed from Figure 7B that gate leakage increases with stress time, as similar to a SILC-like behavior. Here, we investigate the device behavior during the increase of gate leakage

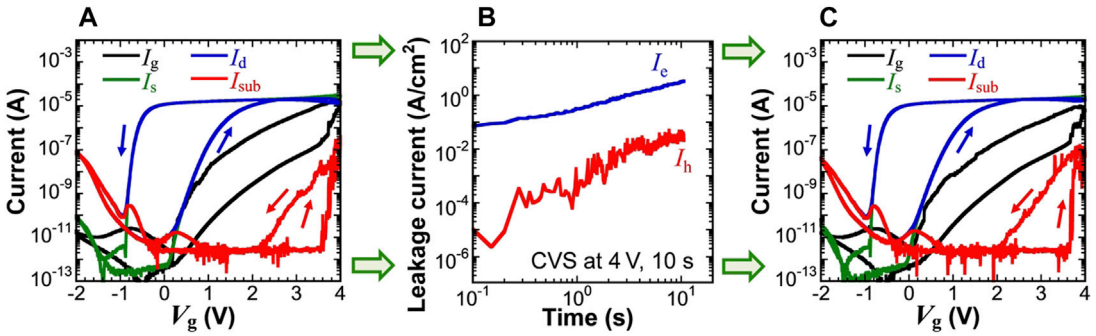

FIGURE 8
(A) I-V_g characteristics of FeFET before CVS. **(B)** Electron and hole components of gate leakage current under CVS at V_g = 4 V for 10 s **(C)** I-V_g characteristics of FeFET after CVS. Although gate current increases during CVS, it has a negligible effect on I-V_g characteristics.

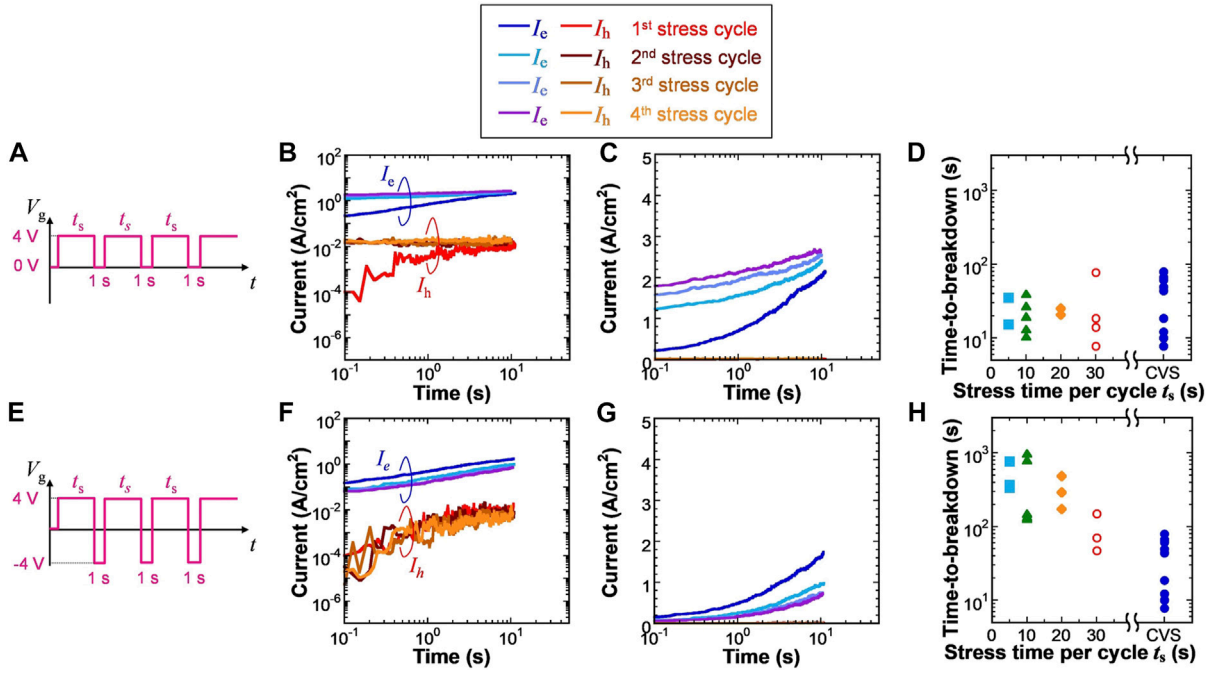

FIGURE 9
(A) Applied voltage scheme with repeating stress of 4 V for time t_s and 0 V for 1 s. **(B,C)** Electron and hole components of gate leakage current at each 4-V stress cycle for t_s = 10 s when current is plotted in **(B)** log scale and **(C)** linear scale. Between each stress cycle, tests were interrupted by 0 V for 1 s. **(D)** Total stress time (excluding 0 V interruption duration) before breakdown for different time t_s of 4-V stress. **(E)** Applied voltage scheme when the interrupted voltage is −4 V for 1 s. **(F,G)** Electron and hole components of gate leakage current at each 4-V stress cycle for t_s = 10 s, which were interrupted at -4 V for 1 s between cycles, when current is plotted in **(F)** log scale and **(G)** linear scale. **(H)** Total stress time (excluding −4 V interruption duration) before breakdown for different time t_s of 4-V stress.

current. Figures 8A, C show the I-V_g characteristics before and after a CVS at 4 V for 10 s shown in Figure 8B. Although $I_e(t)$ and $I_h(t)$ increase by approximately 100 times during the 10-s CVS test, it is found that an only small change of the I-V_g characteristics can be observed after stress. This implies that increases of $I_e(t)$ and $I_h(t)$ in FeFETs are not similar to typical SILC, where increasing current cannot be easily recovered: Increasing currents in FeFETs can be recovered after releasing the stress.

This peculiar behavior of the gate leakage current is further investigated by applying interrupt pulses during TDDB tests.

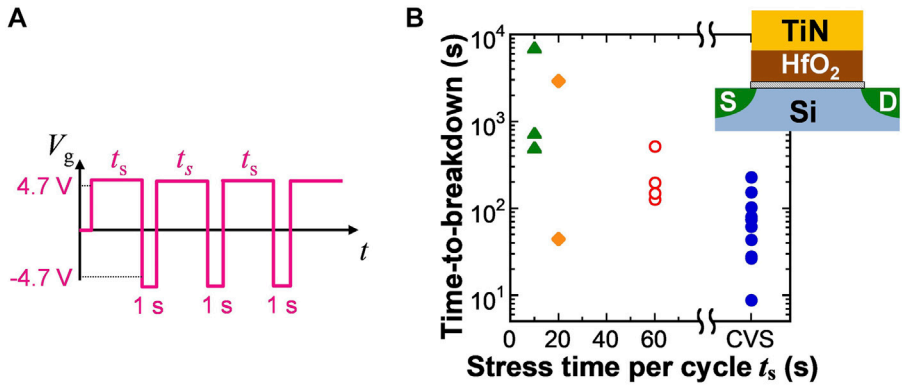

FIGURE 10
(A) Applied voltage scheme with repeating stress of 4.7 V for time t_s and −4.7 V for 1 s. **(B)** Total stress time before breakdown of HfO_2 non-ferro-FETs. CVS indicates experiments without recovery pulses.

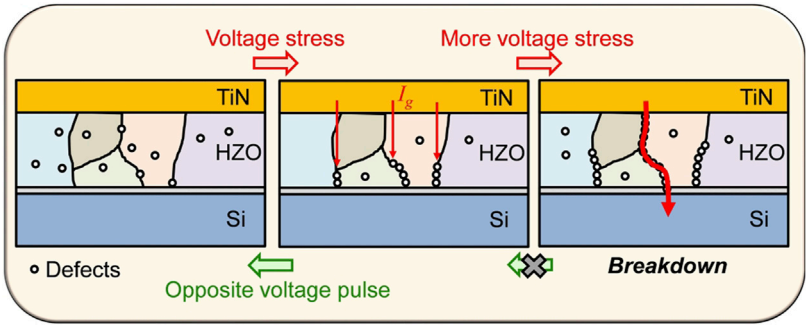

FIGURE 11
Mechanism under electrical stress. The SILC-like behavior is attributed to the redistribution of defects rather than permanent defect generation as recovery is observed. Too much stress will trigger breakdown.

Figure 9A displays a voltage waveform when TDDB tests stressed at $V_g = 4$ V were interrupted by $V_g = 0$ V for 1 s every stress time of t_s. Figures 9B, C show $I_e(t)$ and $I_h(t)$ for each stress cycle when $t_s = 10$ s (cycles of 4 V for 10 s and 0 V for 1 s). $I_e(t)$ and $I_h(t)$ increase cycle by cycle regardless of interrupts by 0 V, implying that electrical stress keeps accumulated. Figure 9D summarizes the time-to-breakdown t_{BD} (excluding interrupt time at 0 V). t_{BD} independent of interrupt frequency indicates that the interrupts at 0 V have no significant effect on t_{BD}. On the other hand, interrupting with negative voltage of $V_g = -4$ V is different. Figure 9E displays a voltage waveform when interrupted by $V_g = -4$ V for 1 s every stress time t_s. Figures 9F, G illustrate that the SILC-like gate leakage current is recovered after interrupted with $V_g = -4$ V for 1 s: increasing $I_e(t)$ and $I_h(t)$ are recovered back almost to I_e ($t = 0$) and $I_h(t = 0)$, respectively, in every cycle. Note that only the current at the first cycle was slightly different because the polarization state of pristine devices is different. This is in agreement with the repeatable I_g-V_g and I_{sub}-V_g in Figure 5. Due to the recovery of SILC-like behavior, applying negative voltage interruption in this way helps extend the time-to-breakdown t_{BD} by more than an order of magnitude, as summarized in Figure 9H.

3.5 Mechanism under voltage stress

The behavior of stress recovery by negative interrupt pulses can be found as well in HfO_2 non-ferro-FETs, as shown in Figures 10A, B. These facts suggest that although the leakage current and breakdown voltage of HfO_2 non-ferro-FETs and HZO FeFETs are different in detail due to differences in crystallinity or defect density, the fundamental mechanisms of the breakdown and recovery behavior should be generally similar in HfO_2-based materials, for instance, same type of defect generation.

Considering the above findings, we propose the mechanism under high V_g stress, shown in Figure 11. Typically, SILC as well as noisy gate leakage current (PBD; progressive breakdown) under electrical stress before hard breakdown are attributed to the generation of defects such as oxygen vacancies (Olivo et al., 1988; Rofan et al., 1991; Degraeve et al., 1995; DiMaria et al., 1995). On the other hand, the recovery and repeatable behavior of apparently degraded gate leakage currents observed in FeFETs suggests that the defect redistribution should be the main contribution of apparently degraded characteristics rather than the generation of new defects. These defects are redistributed again after applying an opposite voltage pulse, recovered to the condition close to the initial one before stress. This model is supported by the fact that oxygen vacancies can move during the voltage cycling (Pesic et al., 2016; Florent et al., 2018b). However, if the stress is large enough for defects to move to the condition that triggers hard breakdown, suddenly increasing current generates a huge density of defects, which forms a permanent conduction path and results in the failure of the device. Then, the recovery is no longer available for devices that reach the breakdown condition.

Such a memory operation that the polarization states are frequently switched in a bipolar manner can help extend the device lifetime in terms of breakdown failure. In other words, not only the improvement in the material aspect but also choosing an appropriate memory operation is important for the reliability of FeFETs. Whereas bipolar operation is favorable to improving the breakdown-limited endurance, the memory-window-limited endurance has been reported to have the opposite behavior: memory window narrowing is degraded in a bipolar operation faster than in a unipolar operation (Yurchuk et al., 2014). These findings address that the ideal writing operation on the aspects of breakdown and MW narrowing are different. Thus, the endurance tests for evaluating the real lifetime should be carefully designed. Conventional endurance tests of FeFETs using bipolar stress evaluates only one aspect of device endurance, resulting in underestimation of gate dielectric breakdown and overestimation of MW narrowing.

4 Conclusion

We investigated the behavior of stress-induced degradation and gate dielectric breakdown in FeFETs with ferroelectric HZO as gate dielectrics on Si substrates. It was observed that gate dielectric breakdown in FeFETs is dominated by the breakdown in the HZO layer, not in the IL. Increasing gate and substrate hole currents under stress, due to the defect movement in HZO, were observed before gate dielectric breakdown occurs. These increasing currents are not a permanent phenomenon: Temporary degradation is recovered by applying opposite voltage because of defect redistribution. We found that continuous electrical stress with the same polarity leads to easier hard breakdown, whereas bipolar stress frequently recovers the device distribution and help extend the time-to-breakdown. Because bipolar stress suppresses the breakdown-limited endurance while accelerates the memory window-limited endurance, accurate endurance tests should be carried out to correctly evaluate the endurance characteristics of FeFETs in practical memory operations.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

KT and ST conceived and proposed the main concepts. KT fabricated devices and characterized the electrical properties. KT, MT, and ST analyzed the data and contributed to the in-depth discussion. KT and ST wrote the manuscript. All authors contributed to the discussions regarding the manuscript.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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