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LIF neuron —a memristive realization

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This study introduces a pioneering design for leaky integrate-and-fire (LIF) neurons by integrating memristor devices with CMOS transistors, thereby forming an innovative hybrid CMOS/memristor neuron circuit. Employing Pt/TaOx/Ta as the memristor device, the proposed model was meticulously implemented and rigorously evaluated using the Cadence Virtuoso simulation environment. The simulation outcomes affirm the effective functionality of the design, marking a significant advancement in hybrid circuit engineering. Notably, the proposed neuron circuit exhibits a compact footprint, attributed to the efficient utilization of hybrid CMOS/memristor gates. This characteristic is poised to address the critical challenge of scaling in current neuromorphic systems, offering a viable pathway to substantially augment density and cater to the escalating demands of advanced computational architectures. The findings of this research hold promising implications for enhancing the efficiency and scalability of neuromorphic systems, setting a new benchmark for future developments in this domain.

KEYWORDS

memristor, memristor ratioed logic, complementary metal oxide semiconductor technology, up–down counter, logic gates, leaky integrate-and-fire neuron

1 Introduction

Inspired by the human brain, neuromorphic systems have drawn much attention in recent years due to their massive parallelism, low power consumption, fault tolerance, and capacity for adaptive learning (Indiveri et al., 2006; Benjamin et al., 2014; Mead, 1990; Yu et al., 2011). In addition to conventional computing systems, von Neumann is facing severe challenges (Stefano et al., 2018), which made brain-inspired computing an alternative approach for conventional computing systems. Thus, hardware implementation for neuromorphic systems has been an ambitious research field and very appealing to computing architecture. The complementary metal oxide semiconductor (CMOS) technology offers the platform to realize the neuromorphic systems to emulate the computations inside the human brain, which is required for implementation of neuron circuits and electronic synapses. Therefore, several works have been proposed on many neuron circuits, such as integrate-and-fire (I&F) neurons (Brink et al., 2012), leaky integrate-and-fire (LIF) neurons (Sangya et al., 2017), and electronic synapses (Seo et al., 2011). Although these CMOS-based circuits have shown maturity toward emulating and understanding the neuromorphic systems, it comes at the price of occupying a large silicon area with considerable power consumption due to the high number of transistors involved. With the aim to solve this problem, the new emerging nonvolatile memory (NVM) devices known as memristors could be a promising candidate for future computing architecture, owing to their nanoscale size and the ability to integrate

with the existing CMOS technology. Moreover, memristors can behave similarly to the human brain in adjusting or changing their responses to stimulation patterns (Gotarredona et al., 2013), making them a perfect choice to imitate biological behavior. There has been intensive research (Stefano et al., 2016; Sangsu et al., 2013; Bipin et al., 2013) covering the area of neuromorphic systems engaging memristors, whereas memristor devices are used to implement synapses with a crossbar structure. However, it is very difficult to integrate the pure memristive crossbar structure with CMOS neurons due to the differences in their logical states. In this paper, an LIF neuron model has been implemented based on the hybrid CMOS/memristor, taking the advantage of the ability to integrate standard CMOS with memristor devices and the capability of fabricating memristor devices on top of the CMOS substrate, which can provide additional storage and fast computing. The rest of this paper is arranged as follows: Section 2 briefly introduces the memristor ratioed logic (MRL), which is exploited as a design method for the LIF neuron. Section 3 includes information about implementing hybrid CMOS/memristor LIF neurons. Section 4 presents and discusses simulation results and discussion on MRL-based LIF neurons. Finally, remarks and conclusions are presented in Section 5.

2 Memristive design method

The memristor is a new emerging resistive device that adds new capabilities to the CMOS technology, which can enhance the performance of neuromorphic architectures. The integrated platform of CMOS/memristors, also known as MRL (Kvatinsky et al., 2012), offers the ability to perform all logic gates utilizing memristors and stack them in between CMOS upper layers (Cho et al., 2015), which will allow faster computing and additional storage at a reasonable chip area for neuromorphic hardware implementation. MRL is CMOS-compatible. Hence, the logical state of this method is based on the output voltage level. Thus, low and high voltage represent logical states (“0” and “1”), respectively. MRL-based AND and OR gate implementation requires only two memristors, while NAND and NOR gates require a CMOS inverter to be connected to the output of AND and OR gates to facilitate the circuits with the interface and control operation (Zidan et al., 2018). Figure 1 displays MRL-based AND, NAND, OR, and NOR. In this work, the memristor model Pt/TaOx/Ta presented in Siemon et al. (2014) was utilized to provide the proposed (LIF) neuron with the memristive behavior over other memristor models reported in Chen and Yu (2015); Kvatinsky et al. (2015) due to the model’s fast switching speed, excellent scalability, and compatibility with CMOS fabrication at low programming voltage. The memristor model Pt/TaOx/Ta has a compact structure with an oxide layer sandwiched between two electrodes that send and receive electrical signals. The stable resistive switching characteristics of the devices are strongly associated with the distribution of oxygen vacancies observed in the oxide material (TaOx). The resistance of the device given in Equation 1 changes to reflect the logical states. Logic “0” is represented by the high resistance state, while logic “1” is represented by the low resistance state.

$$R = \frac{L_{\text{disc}}}{[N \cdot e \cdot \mu_n \cdot A]}, \quad (1)$$

where L_{disc} is the length of the disc zone in which switching activity takes place, N is oxygen vacancy in the disc zone, e is the elementary charge, μ_n is the mobility of the electrons, and A is the device cross-sectional area. The I–V curve shown in Figure 2 represents the Pt/TaOx/Ta device true memristive behavior, which demonstrates the stable resistance switching characteristics of the model. The average current in the device given in Equation 2 is considered the sum of the Schottky current observed in the Pt/TaOx junction and the areal leakage current during the device high resistance state R_{OFF} .

$$I = I_{\text{Schottky}} + I_{\text{areal}}. \quad (2)$$

The device’s reliability and accuracy are impacted by Schottky current, which is responsible for changing the concentration of the oxygen vacancy. Schottky current has two components: the ionic current I_{ion} and the current passing through the electronic resistance.

3 Hybrid CMOS/memristor LIF neuron

The LIF model is the most popular structure used to emulate the behavior of biological neurons. Figure 3 depicts the simplest form of the LIF model as a parallel combination of a capacitor C_{mem} as the membrane capacitor and the leaky resistor R_{Leak} as the leak path resistance of the neuron with a voltage-controlled switch connected in parallel with the capacitor. The performance of the model shown in Figure 3 can be explained as follows: the input excitation current I_{input} charges the membrane capacitor to produce a potential V_{mem} (integrating process); when the membrane potential V_{mem} exceeds a certain threshold V_{th} , the neuron fires, and a spike is generated (firing process); at the same time, the voltage-controlled switch is closed instantly to reset the membrane potential to a predefined resting potential value lower than the threshold value (resetting process). Equations 3, 4 describe the LIF model’s basic mechanism, which indicates that excitation and leakage currents control the membrane potential and *vice versa*.

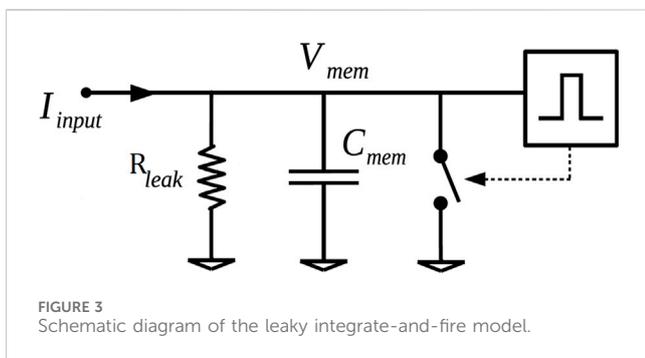
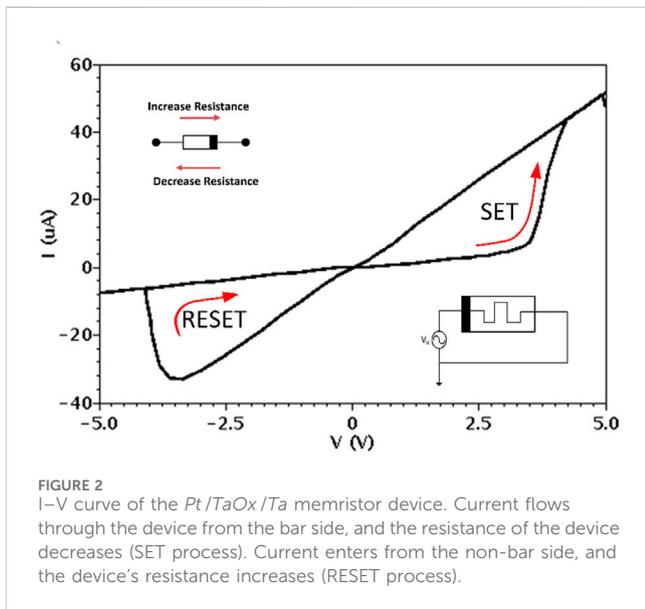
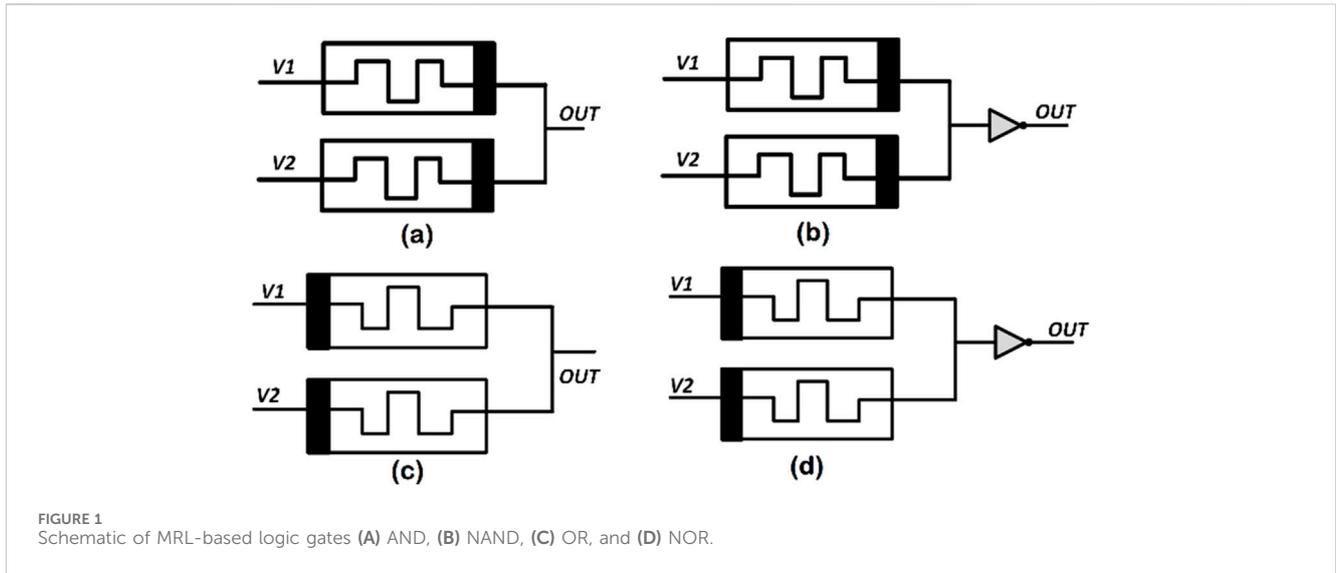
$$C_{\text{mem}} \frac{dV_{\text{mem}}}{dt} = -\frac{1}{R_{\text{Leak}}} (V_{\text{mem}} - V_{\text{reset}}) + I_{\text{input}}, \quad (3)$$

$$I_{\text{Leak}} = -\frac{1}{R_{\text{Leak}}} (V_{\text{mem}} - V_{\text{reset}}), \quad (4)$$

A proposal for a memristive LIF neuron model has been presented in Figure 4 based on the MRL method. The design involves several building blocks as follows.

3.1 Synapse block

The synaptic weight is realized in this block based on the output pulse duration, which is generated when the input spikes trigger the block. Hence, the operations are implemented assuming that multiple inputs can be combined and applied to the counter’s input using MRL-based OR gate,



assuming input spikes will not happen exactly at the same time (Heidarpur et al., 2024). The 4-bit memristor-based counter is the main element in this block. The up-counter

has been implemented using the MRL-based up-down counter (Alammari et al., 2020). The MRL-based counter can change its count direction, whether up or down, at any point within the counting sequence. Hence, up-counting is chosen from the control mode (Alammari et al., 2020). The counter starts counting from the initial value until it reaches the synaptic weight, which is defined by the pulse width. Synaptic weights with larger values have wider pulses, thus having more effect on the neuron core. Synaptic weights are sent to the neuron core block. At the same time, a feedback signal is sent to reset the counter.

3.2 Neuron core

The integration and leak function are performed in this block. The integration process commences when a pulse is received from the synapse block. The membrane potential is realized by a 4-bit memristor-based up-down counter, which was implemented and tested in the Cadence Virtuoso schematic level and previously published in Alammari et al. (2020). The counter updates its logical states every time it receives a synaptic pulse. The counter is incremented or decremented based on the pulse type received from the synapse block. The parameter Exc/Inh indicates the type of the input spike, whether excitatory or inhibitory. However, when no synapse pulse is applied to the neuron core, the leak function takes place by continuously decrementing the counter.

3.3 Neuron output

The final stage in the design is to compare the output of the up-down counter “membrane potential” with a threshold value via a 4-bit memristor-based comparator. A spike is generated when the membrane potential exceeds the threshold value. Simultaneously, a feedback signal is sent to the neuron core to reset the membrane potential to its initial value.

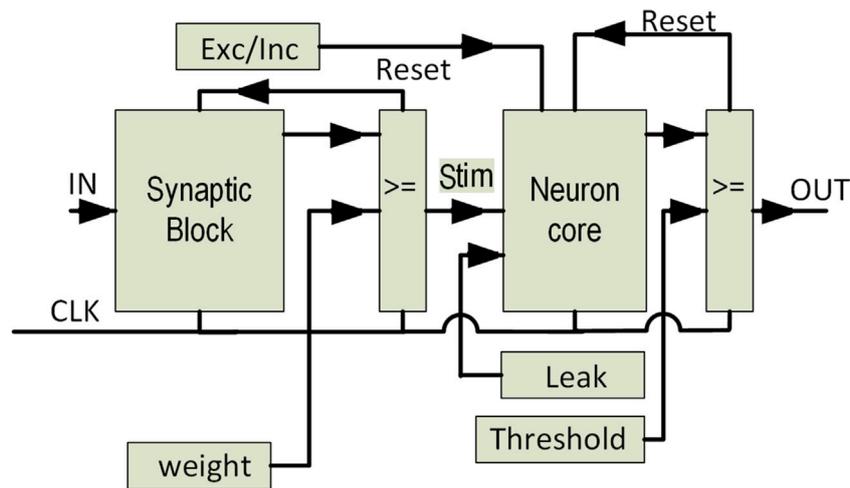


FIGURE 4 Schematic of the proposed MRL-based LIF neuron.

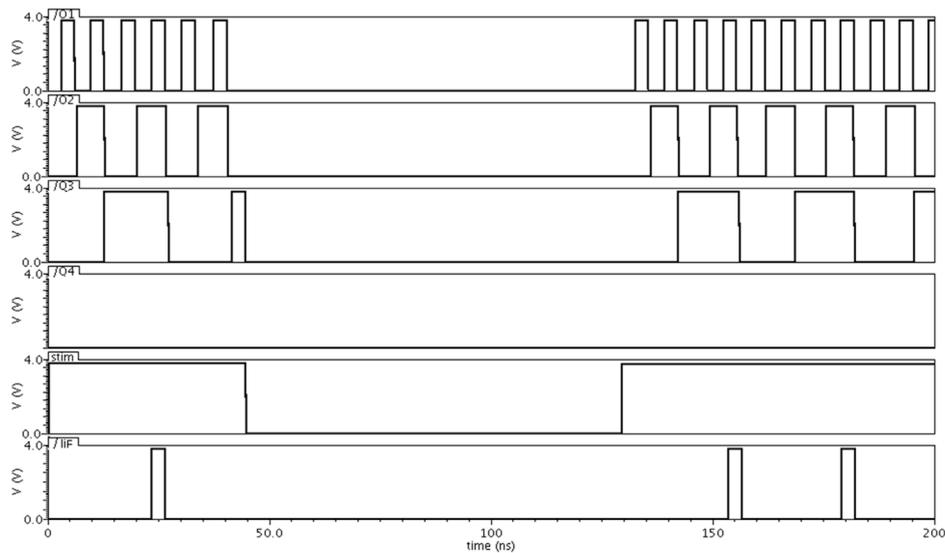


FIGURE 5 Time diagrams for the proposed MRL-based LIF neuron. Output of the up–down counter Q_1 Q_2 Q_3 Q_4 begins incremented /decremented as the input “Stim” generated from the synapse block. Synaptic weights accumulated until the threshold value ($V_{th}=7$) is reached when the neuron fires.

4 Experimental results

The model for LIF neurons has been implemented based on the MRL method. Hence, the memristor devices are employed in the structure depicted in Figure 4. The LIF neuron is made up of a few simple blocks: counters, comparators, and logical gates. The main element in the design is the memristive counter, which was implemented and tested in the Cadence Virtuoso schematic level and previously published in Alammari et al. (2020). The mechanism of the LIF neural model can be explained as follows: the up–down counter begins counting as the input “Stim” generated from the synapse block entering the counter.

The counter starts the up-counting when the parameter Exc/Inh is at logic 1. Otherwise, down-counting is performed. The width of the pulse, which is received from the synapse block, provides information about the synaptic weights. However, when no synapse pulse is applied to the neuron core, the counter has no counting activity and the counter’s value starts to decrease, emulating the leak behavior observed in the neuron model definition. Finally, a comparator is used to detect the threshold level. Figure 5 demonstrates the behavior of the memristive LIF model in Cadence Virtuoso. In the first period, the synaptic weights are accumulated, which contributes to the membrane potential until the threshold value ($V_{th} = 7$) is reached when the

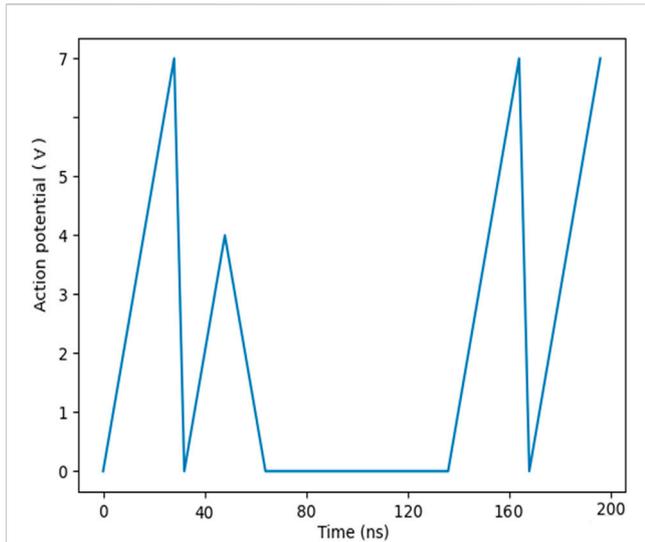


FIGURE 6
Action potential of the memristive LIF neuron model shows three fire events taking place as the threshold value ($V_{th}=7$) is reached and one short spike due to short current because of no input spikes to inter the up-down counter “leak behavior commences.”

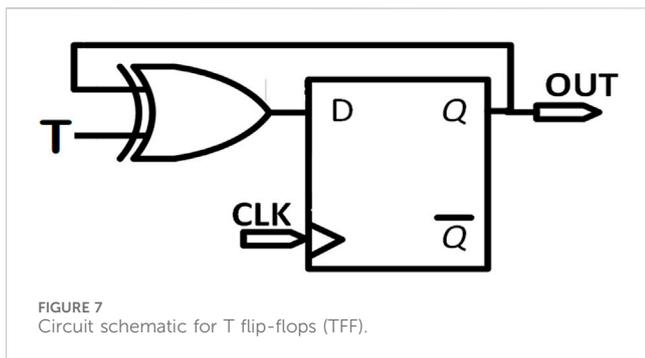


FIGURE 7
Circuit schematic for T flip-flops (TFF).

neuron fires. In the second period of the simulation, the membrane potential starts to decrease its value since there are no input spikes to the up-down counter “stim = 0,” and “the leak behavior.” Figure 6 confirms the action potential of the LIF neuron model. The exceptional features about this proposed

memristive LIF neuron circuit compared to other works utilizing memristors (Myonglae et al., 2015; Yuning et al., 2018) is the comprehensive involvement of the memristor devices in every aspect of the design. In Myonglae et al. (2015) the LIF neuron is implemented using an integrator, comparator with eight switches, and control logic, while in Yuning et al. (2018), the neuron circuit comprises an analog demultiplexer, summing amplifier, and comparator, and the digital part includes AND and OR gates with D flip-flop (DFF). However, both designs have employed memristor devices only to implement synapses. At the same time, our study design shows that both memristive counters in the synapse block and the neuron core block employ four MRL-based T flip-flops (TFF) connected with other MRL-based Boolean gates shown in Figure 1. The circuit of MRL-based TFF consists of MRL-based DFF and MRL-based 2-input XOR gate. The DFF is an edge-triggered circuit consisting of two D-latches connected in series with a master-slave configuration to prevent any possibility of invalid input states. The hybrid memristor-CMOS logic gates AND, OR, and NOR are utilized and connected based on the schematic shown in Figure 7. The DFF involves 16 memristors and 14 MOSFETs, while the XOR gate requires six memristors and two MOSFETs. Hence, the memristive TFF shown in Figure 8 consists of 22 memristor devices and 16 MOSFETs (Alammari et al., 2020). The four memristive TFFs can produce a 4-bit representing the counting sequence once TFFs are triggered. The MRL-based counter in each block of the memristive neuron circuit can change its count direction, whether up or down, at any point within the counting sequence. The TFF is an essential element in the design since it assesses both counters regarding the area, delay, and power consumption. Table 1 presents a comparison of the memristive TFF against other CMOS-based TFF (Abiri et al., 2014). The memristive comparator was implemented based on the memristor-based MRL logic gates depicted in Figure 9. The number of all devices which contribute to the circuit of the memristive neuron is listed in Table 2, which indicates that the MRL-based design is efficient in terms of the layout area. It can be seen from Table 2 that in the hybrid memristor-CMOS-based up-down counter, the number of transistors required is fewer than the number in traditional CMOS-based up-down counter with 110 memristors and 34 MOSFETs, which is less than half of the devices reported in

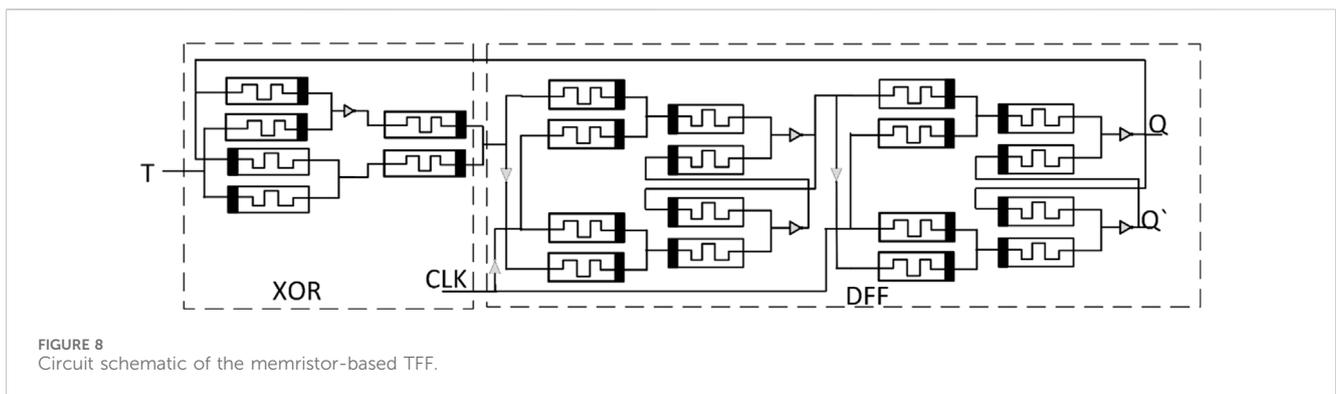


FIGURE 8
Circuit schematic of the memristor-based TFF.

TABLE 1 A comparison between the number of CMOS-based TFF and the proposed memristive TFF.

TFF Design	TGB (Yuning et al., 2018)	Modified CMOS Yuning et al. (2018)	GDI (Yuning et al., 2018)	MRL-based TFF
MOSFET	26	24	22	16
Memristor	-	-	-	22
Delay (Ps)	79.1	60.6	50.2	34.1
Power (μ W)	55.3	42.7	17.5	12.3

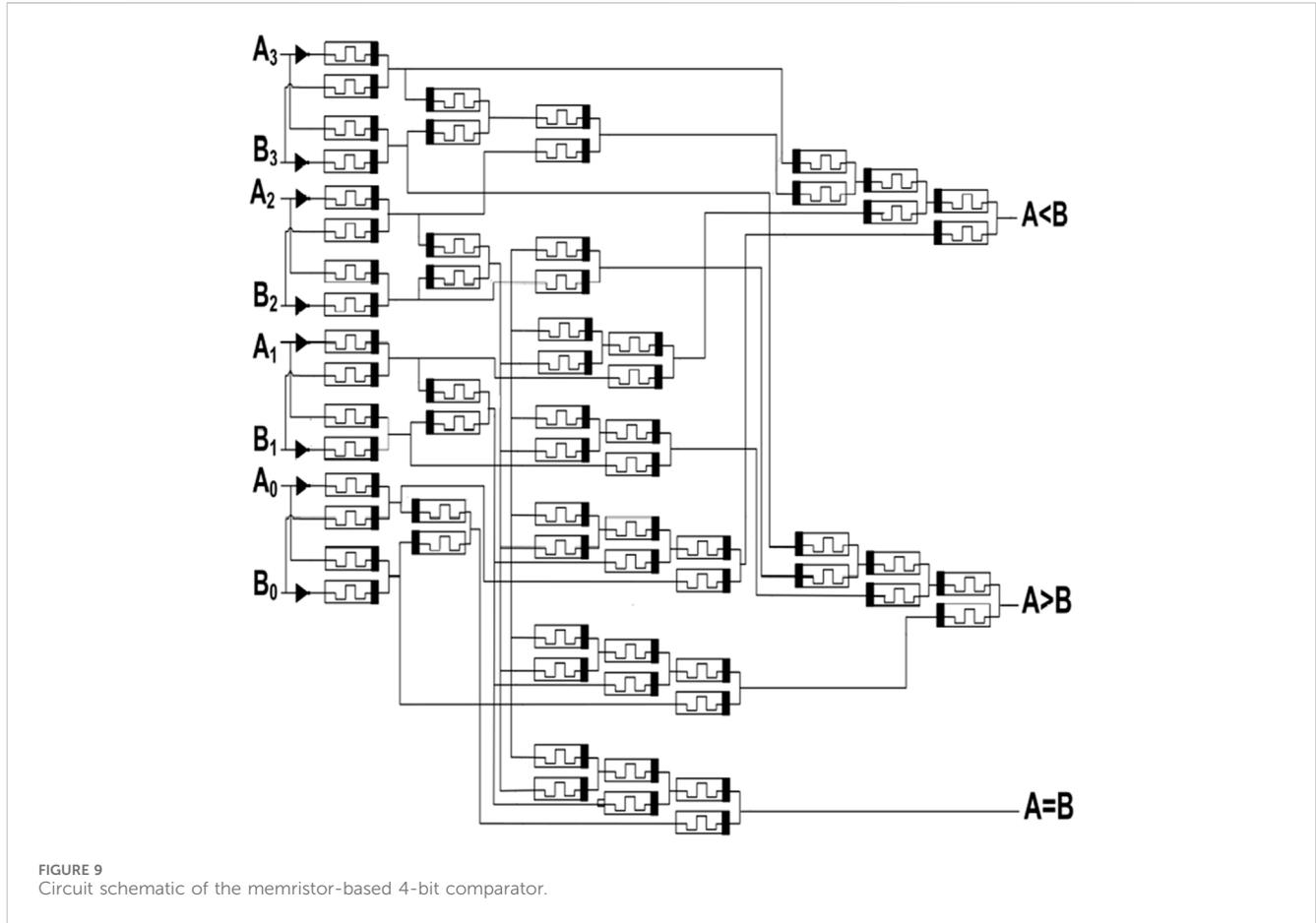


TABLE 2 Number of all devices in the proposed design of the memristive LIF neuron.

Design element		Up-down counter	Up-counter	Comparator/synaptic	Comparator/core
Device	MOSFET	34	32	16	16
	Memristor	110	94	66	66

Alioto et al. (2006); Abdel-Hafeez and Gordon-Ross (2011); Zhang and Hu (2012). The integral platform of CMOS transistors and memristor devices has led to almost 50% in area saving (Kvatinsky et al., 2012) compared to the same CMOS-based design. This is because of the limited utilized number of CMOS transistors in the proposed LIF neuron model as memristor devices can be fabricated on the upper layers of CMOS transistors (Cong and Xiao, 2011; Ru et al., 2011).

5 Conclusion

This work utilizes the *Pt/TaOx/Ta* memristor model to provide the proposed architecture of LIF neurons with memristive behavior. The proposed architecture is based on the hybrid CMOS/memristor gates, which enable integration with existing CMOS-based neurons to support large-scale neuromorphic systems. The exception of this proposal is the

involvement of the memristor devices in every aspect of the design since we divided our design into three parts: a synaptic block with a memristive up-counter, a core neuron circuit with an MRL-based up-down counter previously published, and a comparator to generate a spike when the membrane potential exceeds the threshold value. The circuit of Leak Integrate and Fire neuron is area efficient due to the MRL-based gates employed in the proposed. The design was implemented and verified in Cadence Virtuoso at each stage to confirm its functionality.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Materials; further inquiries can be directed to the corresponding author.

Author contributions

KA: data curation, formal analysis, funding acquisition, investigation, methodology, software, validation, writing—original draft, and writing—review and editing. MH: Writing—review and editing, Data curation, Validation, Software. MA: conceptualization, formal analysis, investigation, methodology, project administration, supervision, validation, and writing—review and editing. AA: conceptualization, investigation, supervision, writing—review and editing, methodology, and resources.

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Supplementary material

The Supplementary Material for this article can be found online at: <https://www.frontiersin.org/articles/10.3389/felec.2024.1366299/full#supplementary-material>

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