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Exploring the performance of GaN trench CAVETs from cryogenic to elevated temperatures

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Fabricated GaN trench current aperture vertical electron transistors (CAVETs) were characterized across a wide temperature range for the first time, including *in situ* cryogenic measurements down to 10 K and *ex situ* thermal shock testing at elevated temperatures of 773 K and 1073 K. The device featured a highly conductive AlGaN/GaN channel regrown on p-GaN following trench etching. As the temperature decreased, the field-effect mobility in the regrown two-dimensional electron gas (2DEG) channel increased from 1886 $cm^2/(V•s)$ at 296 K to 3577 $cm^2/(V•s)$ at 10 K. The device maintained a stable threshold voltage (V_{TH}). The subthreshold slope (SS) decreased from 98.32 mV/dec to 51.31 mV/dec, and the I_{on}/I_{off} ratio increased from 3×10^9 to 9×10^{10} over the same temperature range. The specific on-state resistance ($R_{on,sp}$) decreased from 1.02 mΩ cm^2 at 296 K to 0.586 mΩ cm^2 at 10 K. Furthermore, 1-min thermal shock testing was conducted as a preliminary method to assess the resilience of trench CAVET at elevated temperatures. The device maintained field effect transistor (FET) functionality after exposure to 773 K, albeit with reduced current. Testing at 1073 K resulted in more significant performance degradation, including a sharp increase in $R_{on,sp}$ and failure to achieve pinch-off due to a pronounced surge in gate leakage.

KEYWORDS

gallium nitride, current aperture vertical electron transistor, vertical transistor, cryogenic electronics, high-temperature electronics, extreme temperature applications

1 Introduction

Power electronics operating in extreme temperature environments have garnered increasing attention for applications such as space, healthcare, and transport systems. Under high-temperature conditions, power devices must retain functionality despite potential performance degradation. Conversely, at cryogenic temperatures, devices are expected to exhibit enhanced electrical performance. Gallium nitride (GaN) is considered a promising candidate for reliable operation across these extreme thermal regimes, owing to its wide bandgap of 3.4 eV and the presence of thermally stable two-dimensional electron gas (2DEG).

As temperature decreases from room temperature (RT), conventional silicon (Si) power transistors benefit from reduced scattering effects, leading to higher carrier mobility, lower on-resistance (R_{on}), and improved power density with reduced losses (Rajashekara and

Akin, 2013). However, Si devices suffer from intrinsic carrier freeze-out below ~100 K, causing a negative temperature coefficient of R_{on} (i.e., resistance increases as temperature decreases) (Ahmad, 1987). Silicon carbide (SiC) devices face additional challenges due to interface state trapping, resulting in degraded current conduction and increased R_{on} (Chen et al., 2013). Unlike Si and SiC power transistors, which rely on impurity doping to enable conduction, GaN CAVETs benefit from a 2DEG channel formed by polarization effects even without intentional doping. This intrinsic mechanism enables high current conductivity, low R_{on}, and fast switching capability at cryogenic temperatures (Nela et al., 2021). As a result, GaN CAVETs are well-suited for cryogenic power electronics applications, such as onboard electronics for space applications and image sensors, where systems operate directly at low ambient temperatures. In such environments, maintaining conventional power devices at room temperature would require bulky and inefficient thermal insulation. Cryogenically compatible electronics, by contrast, offer a more compact and efficient solution (Gui et al., 2020). Therefore, understanding the behavior of power devices at cryogenic temperatures is critical for advancing performance in emerging cryogenically cooled power electronics applications.

High-temperature operations are found in applications such as deep-well drilling, automotive systems, and spacecraft. In particular, some systems must withstand brief exposure to extreme thermal events, where temperatures rise sharply for short durations. Under such high-temperature conditions, solid-state switching devices, which serve as critical components in power electronics converters, must sustain functionality despite potential performance degradation. The 2DEG channel formed at an AlGaN/GaN heterojunction has demonstrated excellent thermal stability, supporting reliable operation at elevated temperatures (Yuan, 2022; Hassan et al., 2018). Lateral GaN high electron mobility transistors (HEMTs), leveraging a 2DEG channel along with the high critical electric field, demonstrate high power density and efficiency, making them commercially viable for medium-power and high-frequency applications (1–10 kW) (Chowdhury and Mishra, 2013; Ji et al., 2016). Nevertheless, vertical device architectures are preferred for power electronics due to superior electric field management and more efficient chip area utilization. Among GaN vertical transistors (Ji, 2017; Oka et al., 2015; Jeong et al., 2023; Zhang, 2018; Liu, 2020), the current aperture vertical electron transistor (CAVET) (Chowdhury et al., 2008; Wen, 2024; Chowdhury et al., 2012; Ji et al., 2018a) stands out as the only structure that contains a high-conductivity 2DEG channel for current transport, combining a vertical p–n junction for off-state voltage blocking (Wen et al., 2024a). For low-to-medium voltage applications, where the channel conductivity significantly influences the total R_{on}, GaN CAVETs offer a compelling advantage in power device figure of merit ($BV^2/R_{on,sp}$) due to their inherently high channel conductivity (Wen et al., 2024b). Several studies have explored GaN trench CAVET structures (Ji et al., 2018a; Wen et al., 2024c; Shibata, 2016), in which a regrown AlGaN/GaN heterostructure is formed on a selective-area p-GaN current-blocking layer (CBL) by trench etching.

Despite successful demonstrations, many fundamental properties of GaN CAVETs, including their temperature-dependent behavior, remain insufficiently explored. Prior studies have primarily focused on device performance from RT up to moderately elevated temperatures (<473 K) (Shibata, 2016; Döring, 2024). In our previous work, we reported *in situ* DC and switching characterization of GaN trench CAVETs operating at temperatures up to 573 K (Wen et al., 2024c). Building on that foundation, this work further extends the temperature characterization range by presenting the first *in situ* electrical characterization of GaN trench CAVETs from 296 K down to cryogenic temperatures as low as 10 K. Additionally, for the first time, the of CAVETs are subjected to1-minute thermal shock tests at 773 K and 1073 K to *ex-situ* access thermal survivability under high-temperature conditions. The device retained proper transistor functionality after exposure to 773 K but exhibited pinch-off failure at 1073 K. Evaluating GaN CAVETs across this broad temperature range enables an assessment of their suitability for power electronics intended for harsh and thermally demanding environments. This work provides preliminary insights into the potential of GaN CAVETs to serve as robust candidates for future power electronics applications operating under extreme temperature conditions.

2 Materials and methods

The GaN trench CAVET was fabricated on a bulk GaN substrate, as illustrated in Figure 1. We implemented an etch-then-regrowth approach to form a regrown AlGaN/GaN heterostructure by metal-organic chemical vapor deposition (MOCVD), with the channel extending along slanted trench sidewalls. The 2DEG conductivity is strongly influenced by the etch-then-regrowth process, presenting two key challenges (Ji et al., 2018b). First, Mg inevitably out-diffuses from p-GaN CBL into the channel during high-temperature MOCVD regrowth, which can significantly compensate the 2DEG charge and degrade output current (Xing et al., 2003). To address this, we insert a thin low-temperature GaN (LT-GaN) layer, named the Mg stop layer (MSL), between the p-GaN CBL and the regrown channel, effectively suppressing Mg redistribution (Wen et al., 2023). Second, the etch-then-regrowth process can easily introduce interface issues (Fu et al., 2019; Fu et al., 2021), particularly Si impurity accumulation at the regrowth interface (Fu et al., 2021). The unmodulated impurities can increase off-state leakage through a parasitic conduction path (Li et al., 2018). To mitigate interfacial Si contamination, we perform a chemical cleaning process using ultraviolet-ozone (UVO) and hydrofluoric (HF) acid treatment before MOCVD regrowth (Noshin et al., 2022).

The fabrication process of the trench CAVET is summarized in Figure 2. The structure was grown by MOCVD on a ~400-μm GaN substrate with n + doping about 1×10^{18} cm^{-3}, followed by a 3-μm n-GaN drift layer with a Si doping density of ~6×10^{16} cm^{-3}. A 300-nm p-GaN layer was grown as the CBL with Mg doping density of ~1×10^{19} cm^{-3}. On top of the p-GaN, another 100 nm of LT-GaN was grown at 1023 K to prevent Mg out-diffusion from p-GaN into the subsequent regrown layers. Trenches were etched to ~500 nm deep using inductively coupled plasma reactive ion etching (ICP-RIE) to create the aperture region. After tetramethylammonium hydroxide (TMAH) wet etching to smooth the trench sidewalls (Kodama et al., 2008), UVO cleaning and HF treatment were performed immediately before the regrowth to reduce the Si concentration accumulating at the regrowth interface. The MOCVD regrowth contained 140 nm unintentionally doped (UID) GaN and 30 nm $Al_{0.3}Ga_{0.7}N$. Then, after device isolation

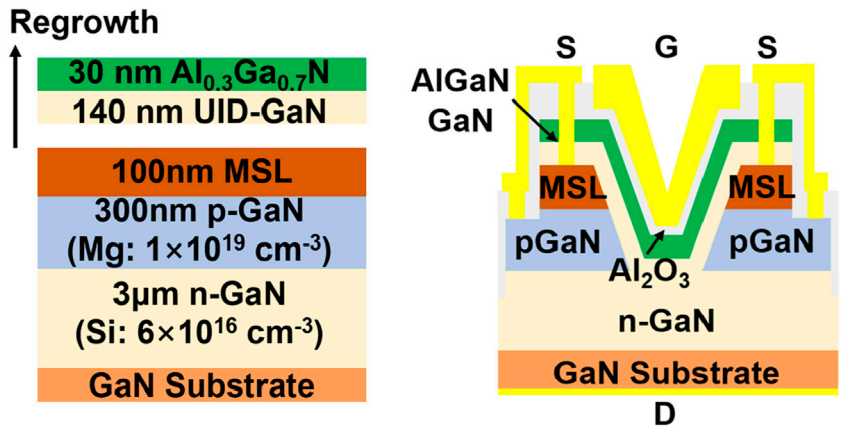

FIGURE 1
Schematic of trench CAVET fabricated on a GaN substrate.

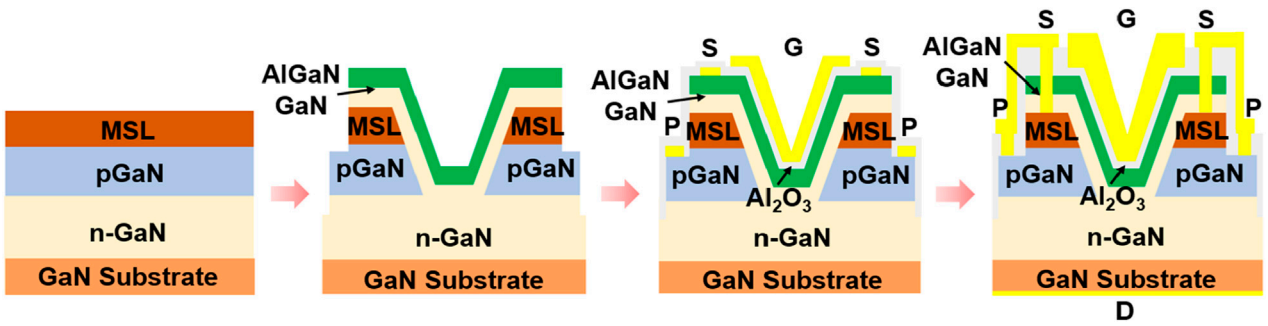

FIGURE 2
Schematic process flow of the GaN trench CAVET.

by dry etching, the p-GaN CBL was activated by rapid thermal annealing (RTA). The Ti/Al/Ni/Au metal stack was deposited on AlGaN with lift-off, followed by RTA post-annealing at 1073 K to form an ohmic source contact. Ni/Au p-GaN contact was deposited on the exposed p-GaN surface. A 15 nm layer of Al_2O_3 was deposited by plasma atomic layer deposition (ALD) as a gate dielectric with post-deposition annealing (PDA) in N_2. Ni/Au formed the gate contact covering the trench-shaped channel. A 170 nm SiO_2 r was deposited as a passivation layer using plasma enhanced chemical vapor deposition (PECVD), followed by via opening. Ti/Au formed the gate and source pads and connected the p-GaN contact to the source. A Ti/Au drain electrode was placed on the backside.

3 Experimental results

3.1 On the cryogenic characterization of GaN trench CAVET

CAVETs are unique among vertical GaN devices in that they employ a polarization-induced 2DEG channel, which enables a temperature-insensitive 2DEG channel without relying on impurity doping. This intrinsic conduction mechanism makes them highly attractive for cryogenic power electronics. Notably, in trench CAVETs, the AlGaN/GaN heterostructure that forms the 2DEG channel is *ex situ* regrown on a trench-shaped surface, with partial overlap on the p-GaN CBL. This geometry introduces challenges in the MOCVD regrowth process, particularly in achieving high-quality heterointerfaces and maintaining excellent 2DEG conductivity. Given that, we focused on characterizing the 2DEG transport properties and current conduction behavior of the trench CAVET across a wide temperature range. The fabricated wafer was measured using a cryogenic probe station equipped with liquid helium for temperature control, enabling electrical characterization down to approximately 10 K. We extracted the 2DEG charge density through capacitance–voltage (C–V) measurements at 1 MHz, as shown in Figure 3b. The C–V measurements were performed on a circular Schottky diode fabricated on the CAVET wafer (Figure 3a). The 2DEG charge density (n_s) determined from C–V was 7.36×10^{12} cm^{-2} at 296 K and 6.83×10^{12} cm^{-2} at 10 K, indicating an almost negligible variation with temperature. The measured capacitance in the accumulation region is nearly flat, which shows the capacitance of the AlGaN barrier layer (C_{AlGaN}). As the voltage bias becomes more negative, electrons in the 2DEG channel at the AlGaN/GaN heterojunction

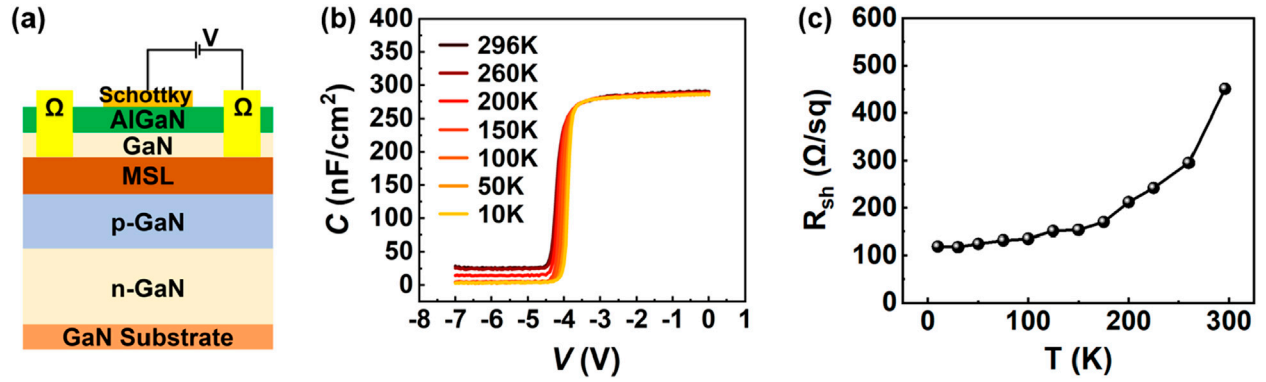

FIGURE 3
C–V characteristics and TLM of the regrown AlGaN/GaN heterostructure. **(a)** Circular Schottky diode for C–V measurements. **(b)** The C–V plot at different temperatures from 296 K to 10 K. **(c)** Temperature-dependent R_{sh} from TLM.

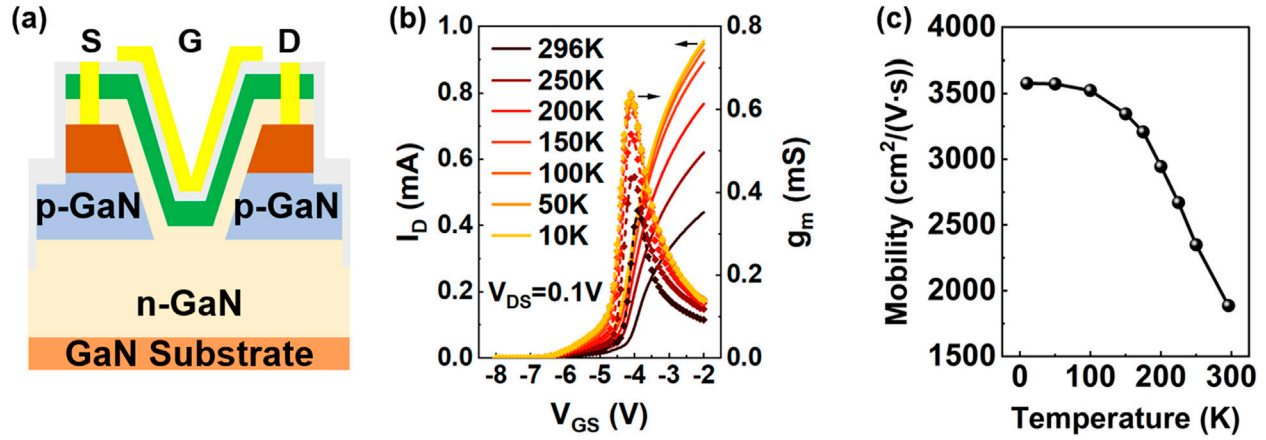

FIGURE 4
(a) Lateral trench structure on the GaN substrate, involving identical epitaxial layers to those of the CAVET. **(b)** Temperature-dependent I_D–V_{GS} with corresponding transconductance. **(c)** Extracted field-effect mobility as a function of temperature.

begin to gradually deplete under gate control, resulting in an increasing depletion width in the GaN layer. The total measured capacitance consists of the C_{AlGaN} and the GaN depletion capacitance ($C_{depletion}$) in series, as shown in Equation (1):

$$\frac{1}{C} = \frac{1}{C_{AlGaN}} + \frac{1}{C_{depletion}} \tag{1}$$

In the transition region where the 2DEG is almost depleted, the C–V curve slope becomes steeper as the temperature decreases from 296 K due to stronger electron confinement at the AlGaN/GaN interface at cryogenic temperatures (Liang et al., 2022; Nicollian and Brews, 2002; Miczek et al., 2008). When the gate bias falls below the threshold voltage, the 2DEG becomes fully depleted, and the C–V curve reaches a lower plateau. This region corresponds to the depletion capacitance of the UID-GaN channel and the MSL beneath the heterojunction. At cryogenic temperatures, the ionization rate of residual donors in GaN decreases, resulting in a wider depletion region and thus a lower capacitance.

The temperature dependence of the channel sheet resistance (R_{sh}) was extracted from the transfer length method (TLM), as presented in Figure 3c. R_{sh} decreased from 450.5 Ω/sq at 296 K to 118.9 Ω/sq at 10 K, which was primarily attributed to the improvement in 2DEG carrier mobility due to the reduction of scattering effects at lower temperatures (Zanato et al., 2004).

The transconductance ($g_m = \partial I_D/\partial V_{GS}$) extracted from I_D–V_{GS} at V_{DS} = 0.1 V across different temperatures is shown in Figure 4. Measurements were conducted on a lateral trench channel structure with identical epitaxial layers to those of the CAVET, as illustrated in Figure 4a. The field-effect mobility (μ_{FE}) of the regrown AlGaN/GaN channel was calculated using (Equation 2) the following equation (Wei et al., 2015):

$$\mu_{FE} = \frac{L_G \cdot g_m}{W_G \cdot C_g \cdot V_{DS}} \tag{2}$$

where L_G/W_G is the gate length-to-width ratio, and C_g is the capacitance between the gate and channel. The extracted mobility

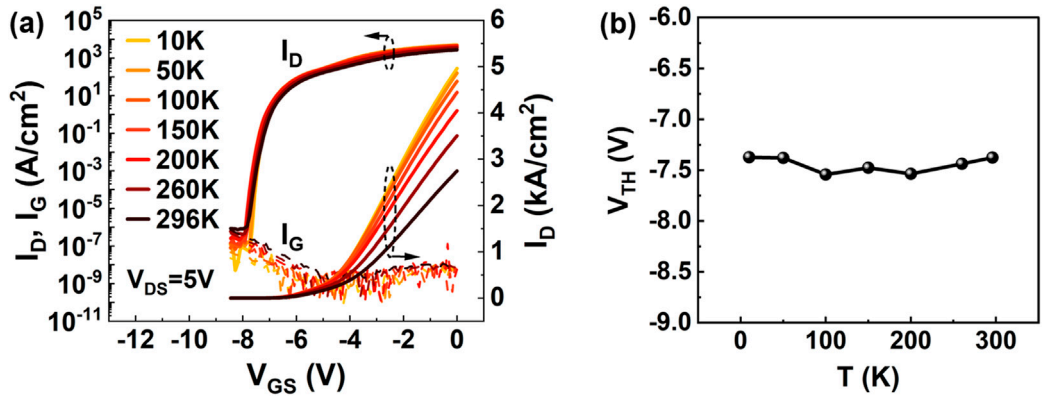

FIGURE 5
(a) Temperature-dependent I_D–V_{GS} transfer characteristics of the fabricated trench CAVET with as-grown MSL. **(b)** The extracted V_{TH} across temperatures from 296 K to 10 K.

from the peak g_m, as shown in Figure 4c, increased from 1886 cm^2/(V•s) at 296 K to 3577 cm^2/(V•s) at 10 K. In the relatively high-temperature range, polar optical (LO) phonon scattering is the dominant mobility-limiting mechanism for the 2DEG (Zanato et al., 2004; Kaasbjerg et al., 2013). As the temperature decreases from 296 K, the mobility limited by LO phonon scattering increases exponentially (Lisesivdin et al., 2010; Karmakar et al., 2023). Below approximately 100 K, the mobility gradually saturates and exhibits weak temperature dependence, consistent with prior reports (Zanato et al., 2004; Gökden, 2003). In this deep cryogenic regime, phonon-related scattering mechanisms are largely suppressed, and the remaining mobility limitation can be primarily attributed to interface roughness and dislocation scattering (Nedwell, 1999).

Figure 5a illustrates the temperature-dependent I_D–V_{GS} transfer characteristics of the trench CAVET in both logarithmic and linear scales. At lower temperatures, the off-state leakage current decreased due to the suppression of thermally generated carriers within the material (Kizilyalli and Aktas, 2015; Chen et al., 2024). Coupled with the increased on-state current at lower temperatures, the I_{on}/I_{off} ratio improved significantly from 3×10^9 at 296 K to 9×10^{10} at 10 K. The off-state leakage current decreased at lower temperatures, consistent with the reduced capacitance values observed in the lower plateau of the C–V curves in Figure 3b at cryogenic temperatures. The extracted subthreshold slope (SS) improved from 98.32 mV/dec at 296 K to 51.31 mV/dec at 10 K. Figure 5b shows the threshold voltage (V_{TH}) defined at 1 μA/mm. No significant variation in V_{TH} was observed across the temperature range, showing an average value of −7.45 V and a standard deviation of 0.069 V. The 2DEG at the AlGaN/GaN interface is primarily induced by polarization fields rather than doping, and the degenerate electron population in the 2DEG channel is nearly temperature-independent (Smorchkova et al., 1999). Because the n_s strongly influences V_{TH} (Huque et al., 2009), the observed V_{TH} stability of CAVET is consistent with the fact that n_s remained almost constant across temperatures.

Figures 6a,b compare the I_D–V_{DS} output characteristics of the fabricated trench CAVET measured at 296 K and 10 K with the gate voltage swept from 0 V in steps of −1 V. At 296 K, the specific on-resistance ($R_{on,sp}$) was 1.02 mΩ cm^2, and the maximum drain current density ($I_{D,max}$) at V_{DS} = 10 V and V_{GS} = 0 V was 3.66 kA/cm^2. At 10 K, $R_{on,sp}$ decreased to 0.586 mΩ cm^2, and $I_{D,max}$ increased to 5.82 kA/cm^2. The normalized on-resistance at each temperature, defined as $R_{on,sp}$ (T)/$R_{on,sp}$ (296 K), is plotted in Figure 6c alongside data from a lateral trench HEMT (Figure 4a). As the temperature decreased from 296 K to 10 K, both devices exhibited a similar decreasing trend in $R_{on,sp}$, which continuously decreased as the temperature dropped from 296 K and gradually saturated below 100 K. At 10 K, the normalized $R_{on,sp}$ of the lateral trench HEMT was 0.541, while that of the vertical CAVET was slightly higher at 0.576. The slightly less pronounced reduction in $R_{on,sp}$ for the vertical CAVET, compared to the lateral counterpart, indicates additional contributions from drift resistance (R_{drift}) and substrate resistance (R_{sub}). The $R_{on,sp}$ in a CAVET primarily comprises the channel resistance (R_{ch}), R_{drift}, and R_{sub} (Chowdhury, 2019). In the fabricated trench CAVET with a 3-μm drift layer, R_{ch} accounted for approximately 70% of $R_{on,sp}$ at RT, and its temperature dependence was primarily governed by channel mobility, as the 2DEG charge density remained nearly constant. At cryogenic temperatures, the bulk electron mobility is primarily constrained by ionized impurity scattering, while the 2DEG channel experiences a more pronounced mobility enhancement (Lisesivdin et al., 2010; Shur et al., 1996).

3.2 On the high-temperature survivability of GaN trench CAVET

Thermal shock testing serves as an effective preliminary method to assess the resilience of devices under extreme temperature fluctuations and rapid thermal cycling. As an initial effort to explore the impact of elevated temperatures (≥773 K) on the fabricated GaN trench CAVETs, two samples were subjected to rapid thermal annealing (RTA) in a nitrogen ambient atmosphere for 1 minute at 773 K (500 °C) and 1073 K (800 °C), respectively.

One-minute 773 K thermal shock tests were performed three times on the trench CAVET. The post-annealing I–V characteristics, including both transfer and output curves, are presented in Figure 7

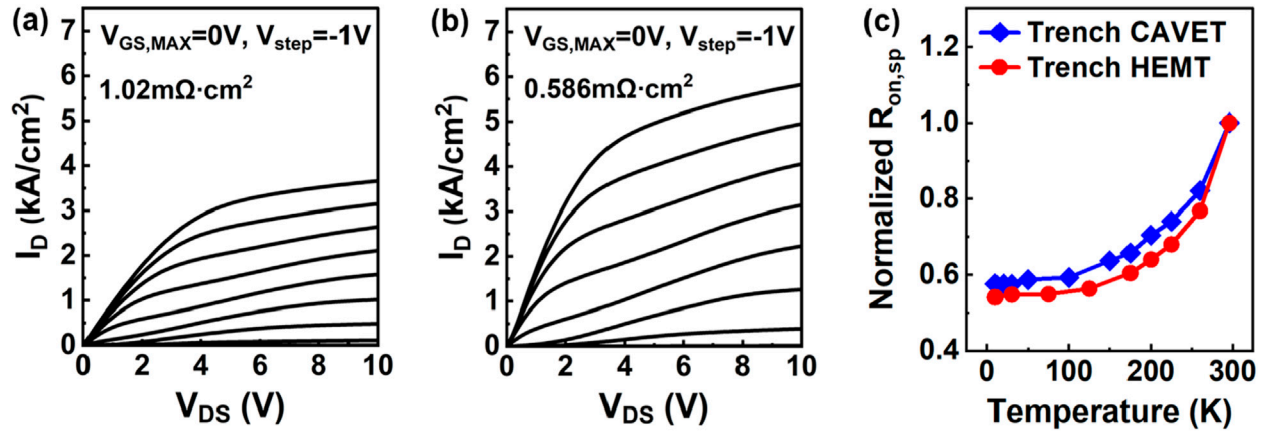

FIGURE 6
I_D–V_{DS} output characteristics of the fabricated trench CAVET at **(a)** 296 K and **(b)** 10 K. **(c)** Temperature-dependent normalized $R_{on,sp}$ of the fabricated trench CAVET and trench HEMT.

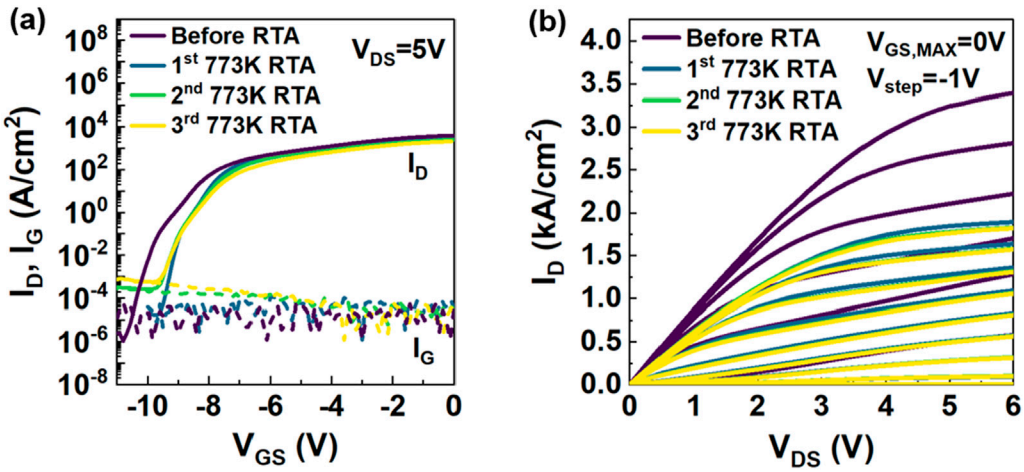

FIGURE 7
(a) I_D–V_{GS} transfer characteristics and **(b)** I_D–V_{DS} output characteristics trench CAVET after repeated 773 K thermal shock testing.

to explore the impact of repeated thermal shock tests on device transport properties. The devices retained typical FET behavior throughout the tests. The transfer characteristics in Figure 7a exhibit a positive V_{TH} shift from −9.9 V before the thermal shock to −9.2 V after the first run, with no further obvious change observed after the second and third runs. The observed rightward shift in V_{TH} after thermal shock tests may be attributed to annealing effects in the ALD-grown Al_2O_3 gate dielectric layer during thermal shock tests. Specifically, such annealing may reduce the trap state density either at the oxide/AlGaN interface or within the oxide layer, resulting in a positive shift in V_{TH} (Nakazawa et al., 2019; Gupta et al., 2019). Additionally, gradual gate degradation was observed after the repeated thermal shock tests, as reflected by an increase in off-state gate leakage current from 10^{-5} A/cm² to 10^{-3} A/cm² after three cycles. The output curves in Figure 7b show that the $R_{on,sp}$ increased to 1.58 mΩ cm² after the first test and 1.60 mΩ cm² after the third thermal test. The output current density at V_{GS} = 0 V and V_{DS} = 6 V decreased to 1892 A/cm² after the first thermal test and 1819 A/cm² after the third run.

After exposure to 1073 K, the devices exhibited more severe performance degradation. As shown in Figure 8a, proper pinch-off behavior was no longer observed due to a substantial increase in gate leakage current. Extracted from the output characteristics in Figure 8b, the $R_{on,sp}$ increased significantly to 24.2 mΩ cm², and the output current density dropped to 170 A/cm². Compared to the 773 K treatment, visible metal degradation and peel-off were observed at 1073 K, as shown in Figure 9, along with a distinct color change in the gate metal, indicating possible metal alloying contributing to the increased leakage.

These results represent the first demonstration of the thermal survivability of GaN trench CAVETs under high-temperature shocks and provide a foundation for future studies exploring their reliability under combined high-temperature and bias-stress

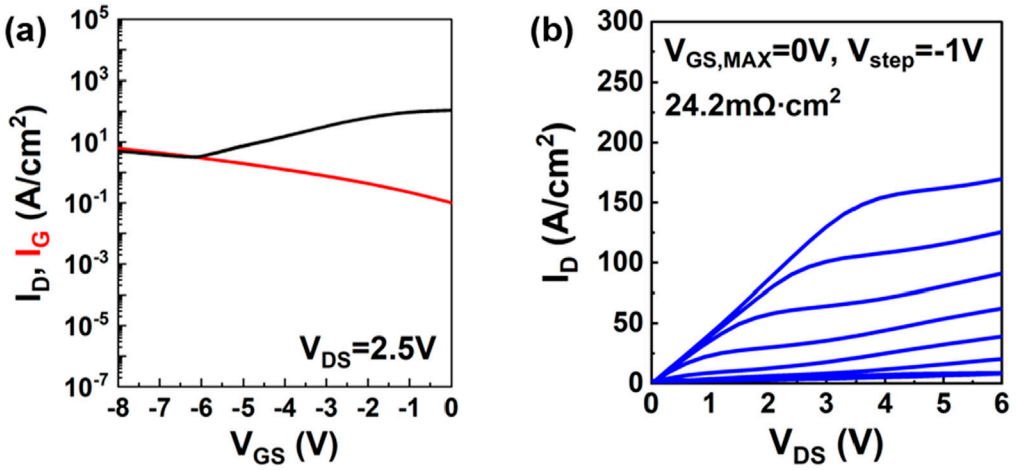

FIGURE 8
(a) I_D–V_{DS} and **(b)** I_D–V_{GS} of trench CAVET after 1073 K thermal shock testing.

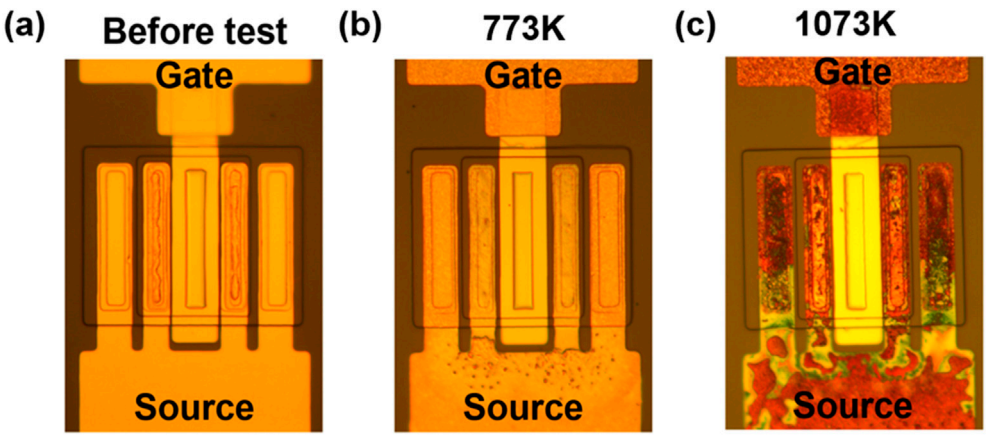

FIGURE 9
Optical images of trench CAVET **(a)** before testing, **(b)** after 773 K thermal shock, and **(c)** after 1073 K thermal shock.

TABLE 1 A summary of the GaN trench CAVET performance in this work and in Wen et al. (2024c) at different temperatures, including both *in situ* measurements (i.e., devices measured at the specified temperature) and *ex-situ* measurements (i.e., devices measured after undergoing 1-min thermal shock testing). *Note that the minimum current measurement resolution of the source measurement unit (SMU) used for gate current measurement in *ex-situ* characterization is approximately 10^{-5} A/cm^2. Currents below this threshold may not be accurately detected.

Measurement conditions	Temperature	$R_{on,sp}$	I_D at V_{GS} = 0 V and V_{DS} = 6 V	Off-state I_G
In situ	10 K	0.59 mΩ cm^2	5191 A/cm^2	~2×10^{-8} A/cm^2
In situ	296 K (RT)	1.0 mΩ cm^2	3314 A/cm^2	~4×10^{-7} A/cm^2
In situ	573 K (Wen et al., 2024c)	2.3 mΩ cm^2	1760 A/cm^2	~4×10^{-4} A/cm^2
Ex-situ	773 K	1.6 mΩ cm^2	1892 A/cm^2	~2×10^{-5} A/cm^2*
Ex-situ	1073 K	24 mΩ cm^2	170 A/cm^2	~10 A/cm^2

conditions. The electrical characteristics of the GaN trench CAVETs from this work and our prior study (Wen et al., 2024c) are summarized in Table 1, including both *in situ* measurements (i.e., devices measured at the specified temperature) and *ex-situ* measurements (i.e., devices measured after undergoing 1-min thermal shock testing).

4 Conclusion

In summary, this study presents the first investigation of the device characterization of GaN trench CAVETs over a broad temperature range. For cryogenic characterization, the 2DEG charge density was 7.36×10^{12} cm^{-2} obtained from the regrown AlGaN/GaN channel with a slight 7% reduction from 296 K to 10 K. The V_{TH} of CAVET exhibited excellent thermal stability. The field-effect mobility increased from 1886 $cm^2/(V•s)$ at 296 K to 3577 $cm^2/(V•s)$ at 10 K, contributing to improved device conductivity. Specifically, $I_{D,max}$ increased from 3.66 kA/cm^2 to 5.82 kA/cm^2, and $R_{on,sp}$ decreased from 1.06 $m\Omega\ cm^2$ to 0.586 $m\Omega\ cm^2$. Additionally, we performed 1-min thermal shock testing to preliminarily evaluate the survivability of trench CAVETs under high-temperature conditions. The device maintained normal functionality after 773 K testing with approximately 50% current reduction. Exposure to 1073 K caused more significant degradation in both $R_{on,sp}$ and gate control. These findings demonstrate the potential of GaN trench CAVETs for applications in extreme temperature environments.

Data availability statement

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

Author contributions

XW: Conceptualization, Data curation, Investigation, Methodology, Visualization, Writing – original draft, Writing – review and editing. KL: Conceptualization, Investigation, Methodology, Writing – original draft, Writing – review and editing. HK: Conceptualization, Investigation, Methodology, Resources, Validation, Visualization, Writing – original draft, Writing – review and editing. MN: Conceptualization, Investigation, Methodology, Writing – original draft, Writing – review and editing. CM: Conceptualization, Investigation, Methodology, Writing – original draft, Writing – review and editing. SC: Conceptualization, Funding acquisition, Investigation, Methodology, Project administration, Supervision, Writing – original draft, Writing – review and editing.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Generative AI statement

The author(s) declare that no Generative AI was used in the creation of this manuscript.

Publisher's note

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