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Review of Five-Level Front-End Converters for Renewable-Energy Applications

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With the objective of minimizing environment and energy issues, distributed renewable-energy sources have reached remarkable advancements along the last decades, with special emphasis on wind and solar photovoltaic installations, which are deemed as the future of power generation in modern power systems. The integration of renewable-energy sources into the power system requires the use of advanced power electronic converters, representing a challenge within the paradigm of smart grids, e.g., to improve efficiency, to obtain high power density, to guarantee fault tolerance, to reduce the control complexity, and to mitigate power-quality problems. This paper presents a specific review about front-end converters for renewable-energy applications (more specifically the power inverter that interfaces the renewable-energy source with the power grid). It is important to note that the objective of this paper is not to cover all types of front-end converters; the focus is only on single-phase multilevel structures limited to five voltage levels, based on a voltage-source arrangement and allowing current or voltage feedback control. The established review is presented considering the following main classifications: (a) number of passive and active power semiconductors; (b) fault tolerance features; (c) control complexity; (d) requirements of specific passive components as capacitor or inductors; and (e) number of independent or split dc-link voltages. Throughout the paper, several specific five-level front-end topologies are presented and comparisons are made between them, highlighting the pros and cons of each one of them as a candidate for the interface of renewable-energy sources with the power grid.

Keywords: five-level converters, renewable energy sources, power converters, multilevel, power electronics, power quality

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INTRODUCTION

Power converters capable of synthesizing, more than three voltage levels, are commonly classified as multilevel converters, where a common feature is the possibility to deal with higher voltages (Pandey et al., 2006; Debnath et al., 2015; Gupta et al., 2015). Mainly due to the required voltage levels in an application, multilevel converters are based on simple structures or based on a cascade connection of simple structures (Sadigh et al., 2015; Xiao et al., 2015; Ahmed et al., 2017).

Therefore, approaches with the split dc link, with multiple dc links (independently or not), or a mix of both are possible structures that allow synthesizing the multi-voltage levels. Dependent on the application (i.e., interface of renewable-energy sources, electric mobility, or storage systems), multilevel converters can be distinguished as active rectifiers or grid-forming or grid-tied inverters, with the possibility, in each case, of using a voltage-source or current-source structure. The main objective of a multilevel converter is to synthesize an ac voltage or current with improved quality, also contributing to preserve issues of power quality. Therefore, the key purpose of multilevel converters are to (a) deal with semiconductor limitations in high-voltage applications; (b) deal with limitations of switching frequency; (c) improve the power quality; (d) improve modularity and/or scalability; and (e) deal with controllability (Karwatzki and Mertens, 2018).

Power quality has been a concern in an electrical grid, however, the interest for this topic has increased along the last decades for both residential and industrial levels (Singh et al., 2004; Bollen et al., 2010; Ceaki et al., 2017; Lopez-Martin et al., 2018), leading to the development of various multilevel converter topologies (Singh et al., 2008), as well as control strategies (Nejabatkhah et al., 2019). Moreover, in recent years, due to the advances in semiconductors and digital control platforms, multilevel converters have emerged as a suitable alternative to the conventional static multi-pulse structures (i.e., based on transformers with specific arrangements) as well as an alternative to the conventional two-level converters. The most conventional multilevel converter, i.e., the neutral-point-clamped (NPC), was introduced in the last century, and since that date, several proposals were introduced for different applications. Reviews of multilevel converters can be found in Pandey et al. (2006); Debnath et al. (2015), and Gupta et al. (2015) where besides the analysis of the topologies in terms of required hardware and software for the control, prospective applications are also included. However, since the publication of these reviews, several multilevel converters have been proposed with innovative features in terms of topology, control, and applications (e.g., considering applications of smart grids, on-grid and off-grid renewable-energy sources, electric mobility, microgrids, power transmission, and distribution). Compared to the conventional solutions, increasing the number of voltage levels reduces the size of the passive filters for maintaining similar indices of power quality, consequently allowing to increase the power density of the equipment, which is a key factor in many applications. However, a higher number of levels increase the required hardware resources, which hints to a trade-off between levels, hardware resources, and power density. Based on these criteria, the objective of this paper is not to cover all the multilevel converters but to focus on five-level converters with the possibility to be applied as grid-tied inverters for interfacing renewable-energy sources with the power grid. Therefore, a review of several publications is presented, where the main focus is on voltage-source structures, grid-tied inverters (with current or voltage feedback control), single-phase or three-phase structures, and the five voltage levels. In this context, the main contributions of this paper are related to the following: (a) the more recent and emerging multilevel converters (five-level) identified in the literature are presented; (b) the multilevel (five-level) converters are organized according to the characteristics; and (c) a comparison is established based on the main characteristics in order to identify the pros and cons of each topology.

The paper is directly related with the application of five-level converters to interface renewable-energy sources with the power grid, however, the presented topologies can also be useful for other applications, both for coupling with the power grid (i.e., as grid-tied inverters) or for island operation (i.e., as off-grid inverters). A concrete case is the applications of energy-storage systems. In fact, the energy-storage systems are flexible systems in terms of power operation, which are capable of consuming, storing, or providing energy. Taking into account the flexibility offered, energy-storage systems can offer additional advantages for the integration of renewable-energy sources, e.g., targeting power management in a distributed architecture. The up-to-date energy-storage technologies are compiled and investigated in Yao et al. (2016), mainly from the perspective of technology efficiency, maturity, cost, lifespan, and contextualization with the final application scenarios. A review of energy-storage systems about problems and challenges for microgrid applications is presented in Faisal et al. (2018), and the past and present of the distinct technologies of energy-storage systems are presented in Boicea (2014). An overview regarding the history, evolution, and future status of energy-storage systems is presented in Whittingham (2012). Projects directly related to energy-storage systems are presented in Araiza et al. (2018) and Baxter et al. (2018), while overviews from the power electronics point of view are introduced in Molina (2017) and Mazumder (2019).

The rest of the paper is organized as follows: Section "Standards for Grid-Connected PV Installations" presents an overview of standards for grid-connected converters used for interfacing renewable-energy sources; section "Topologies of Five-Level Front-End Converters" presents the selected topologies of five-level front-end converters; and section "Modulation Techniques for Five-Level Front-End Converters" presents modulation techniques for five-level front-end converters. Section "Comparison Between Topologies" establishes a comparison among the selected topologies; section "Conclusion" ends the paper with the conclusions.

STANDARDS FOR GRID-CONNECTED PV INSTALLATIONS

Over the last decades, the market of PV installations is increasing as a contribution to meet the rising demand. In terms of power, PV installations can vary from few kW to thousands of MW. However, the increased integration of PV-based resources into the power systems can cause diverse effects in practical characteristics that are mainly associated with power-quality issues, power management, demand response, reliability, and safety.

Therefore, the integration of photovoltaic (PV) installations must accomplish with specific standards and guidelines, which

are established according to the country (i.e., the standards and guidelines can vary from country to country). Such standards are an important requirement, which must be considered in the specifications of the PV installation, as well as in the design of power electronics. IEEE 1547 and IEC 61727 are the most widely recognized standards relevant to these applications, which are established by the IEEE (Institute of Electrical and Electronics Engineers) and by the IEC (International Electrotechnical Commission), respectively. Regarding power electronics, the grid-connected front-end converters are designed with the aim to reduce specific harmonic levels, reduce total harmonic distortion (THD), increase power factor, reduce frequency deviation, and eliminate leakage currents.

Summarizing, the IEEE 1547 standard is focused on technical specifications for the interconnection and interoperability among distributed energy resources (DERs) and power systems (at different distribution voltages, emphasizing DER in radial primary and secondary distribution systems) less than 10 MVA. This standard is intended to be universally adopted, where among others, issues such as power quality, safety considerations, islanding, and response to abnormal conditions are addressed. On the other hand, the IEC 61727 standard deals directly with low-voltage non-islanded converters (grid-connected dc–ac inverters). This standard is applied for the interconnection of PV installations (less than 10 kVA) from the power system in the perspective of single-phase or three-phase residences. Regarding the aforementioned standards, **Table 1** summarizes the key points of these standards. Besides the aforementioned standards, there are other relevant standards such as the IEEE 929–2000, which is specific for PV installations with power below 10 kW. This is a recommended practice guidance regarding the interface of PV installations, where there are issues such as power quality, safety, protection, utility system operation, and islanding of PV installations. Other standards, but with lower importance, are established by the NEC, UL, and so on Hester (2002), U. Std, (2002), and Wiles (2005).

TOPOLOGIES OF FIVE-LEVEL FRONT-END CONVERTERS

In this section, a comprehensive review of the more recent topologies with a special focus on single-phase five-level inverters is provided. It should be noted that the anti-parallel diode of a controlled switch is considered a separate component, as is the case in normal applications.

A five-level three-phase inverter is proposed in Sajadian and Santos (2014), however, the three-phase system consists of three separate phases that can operate individually. In each phase, four fully controlled power switches and six diodes are needed. This topology is presented in **Figure 1**. A coupled inductor is needed for the topology. The output voltage of the converter can be calculated using (1). It should be noted that S_1 operation is complementary to S_2.

$$V_{out} = \left(\frac{1}{2}(1 - S_2) - S_3\right) V_{dc} = \left(\frac{1}{2}(1 - S_2) - (1 - S_4)\right) V_{dc} \tag{1}$$

The main advantage of this structure is that it requires fewer controlled switches and has no need for complex voltage-control algorithms for dc-link voltage-control algorithms as happens with many other topologies. The authors also claim that the topology improves power loss. However, a coupled inductor and certain operating conditions must be met.

In Korhonen et al. (2014), a five-level single-phase inverter based on neutral point and a flying capacitor is proposed that can produce $\pm v_{dc}/2$, $\pm v_{dc}/4$, and 0. As can be seen in **Figure 2**, it has eight fully controlled power switch and eight diodes. The output voltage of the converter can be calculated using

TABLE 1 | Summary of the grid requirements concerning the IEEE 1547 and IEC 61727 standards.

	IEEE 1547		**IEC 61727**	
Nominal power	**30 Kw**		**10 kW**	
Harmonic level (currents)	**Order**	**%**	**Order**	**%**
	3–9	4	3–9	4
	11–15	2	11–15	2
	17–21	1.5	17–21	1.5
	23–33	0.6	23–33	0.6
	> 35	0.3	> 35	0.3
	Even harmonics < 25% of odd harmonics THD < 5%			
DC current	**< 1% of rated current**		**<0.5% of rated current**	
Voltage variation	ΔV < 50%	0.1 s	ΔV < 50%	0.16 s
	50% < ΔV < 88%	2 s	50% < ΔV < 88%	2 s
	110% < ΔV < 120%	2 s	110% < ΔV < 120%	1 s
	ΔV > 120%	0.05 s	ΔV > 120%	0.16 s
Frequency variation	59.3 < Hz < 60.5	0.2 s	59.3 < Hz < 60.5	0.16 s

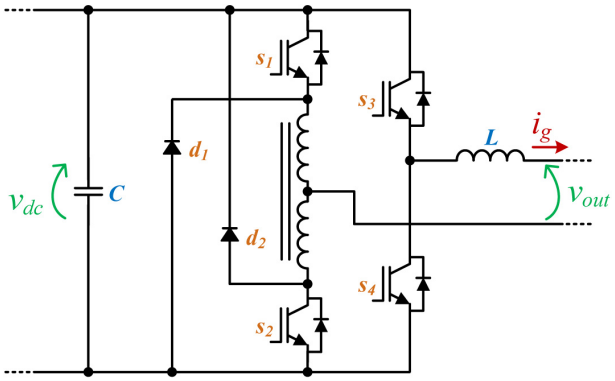

FIGURE 1 | Topology proposed in Sajadian and Santos (2014).

(2). There are multiple alternatives for the $\pm v_{dc}/4$ that can be exploited to maintain the voltage of the floating capacitor within a tight boundary.

$$v_{out} = (S_5\ S_6 - S_7\ S_8)\frac{v_{dc}}{2} + (S_5 S_7 - S_6\ S_8 + S_3\ S_4\ S_6 - S_1\ S_2\ S_7)\frac{v_{dc}}{4} \quad (2)$$

It should be noted that the switches and diodes need different voltage ratings, which can increase maintenance costs. Voltage fluctuation in the flying capacitor can affect output quality, as well as the split power source requirement, which can be limiting, and the utilized switches have different voltage ratings. Moreover, it can only produce half of the total dc-link voltage, which is not desirable. The authors compare the performance of the paper with a commercial NPC-5L topology, and the results show a very slight improvement in efficiency.

The authors in Yuan (2014) modify the structure proposed in Korhonen et al. (2014) and utilize reverse-blocking IGBTs. However, similar to the previous paper, it utilizes the redundant stages to balance the flying-capacitor voltage. The disadvantages are also similar. The authors claim that this topology requires a lower number of semiconductor count, because they are considering each of the reverse-blocking IGBTs as one semiconductor. However, a reverse-blocking IGBT is in effect composed of two back-to-back IGBTs that do not have any anti-parallel diode and this advantage is not very prominent. On the other hand, utilizing the reverse-blocking IGBTs, improves efficiency. **Figure 2** shows the proposed topology.

The output voltage of the converter shown in **Figure 2** can be calculated using (3). Comparing (3) with (2), it can be seen that they are essentially similar and the only difference is that (Yuan, 2014) (c.f. **Figure 2**) utilizes one bidirectional switch instead of two back-to-back unidirectional ones.

$$v_{out} = (S_3\ S_4 - S_5\ S_6)\frac{v_{dc}}{2} + (S_2\ S_4 - S_1\ S_5 + S_3\ S_5 - S_4\ S_6)\frac{v_{dc}}{4} \quad (3)$$

A three-phase five-level topology is proposed in Masaoud et al. (2014). It requires sixteen controlled switches and sixteen diodes. There are five voltage levels for each phase, 0, $v_{dc}/4$, $2v_{dc}/4$, $3v_{dc}/4$, v_{dc}, which, by considering a three-phase operation, would result in nine voltage levels. Although the topology has a relatively low number of switches per voltage levels for all the three-phases, it requires two different sources, where one of them should be a split-voltage source. This topology is presented in **Figure 3**. The output phase-voltage of the converter shown in **Figure 3** can be calculated using (4).

$$v_{out} = (S_3\ S_6\ S_8)\frac{v_{dc}}{2} + (S_1\ S_2\ S_5\ S_7)\frac{3v_{dc}}{4} + (S_1\ S_2\ S_6\ S_7)\frac{v_{dc}}{2} + (S_1\ S_2\ S_5\ S_8)\frac{v_{dc}}{2} \quad (4)$$

Authors in Vahedi et al. (2016) utilize a seven-level converter previously proposed by Kamal Al-Hadad called PUC to build a five-level converter with simplified control. This topology is presented in **Figure 4**. It is argued that the previously proposed seven-level converter has a very complex control and requires a high switching frequency as well as additional sensors. However, the simplified five-level converter changes the ratio $V_1 = 3V_2$ to $V_1 = 2V_2$ and also introduces a self-balancing algorithm to simplify the control. The output voltage levels are $\pm\ v_{dc}/2$ and $\pm\ v_{dc}/4$, 0, which achieve a unity voltage ratio between output and input voltage. The split power source being unnecessary is another advantage of such a system. The output phase voltage of the topology shown in **Figure 4** can be calculated based on the switch states using (5).

$$v_{out} = (S_1\ S_5\ S_6 - S_2\ S_3\ S_4)\frac{v_{dc}}{2} + (S_1\ S_3\ S_5 + S_1\ S_2\ S_6 - S_3\ S_4\ S_5 - S_2\ S_4\ S_6)\frac{v_{dc}}{4} \quad (5)$$

A single-phase five-level structure is proposed in Saeedian et al. (2018) based on the switching capacitor technique. **Figure 5A** shows the proposed structure, and the phase output voltage can be calculated using (6). Since the capacitors utilized in the topology can be easily balanced without needing any complex closed-loop control, one of the advantages of this system is a simple control. However, the most important benefit of the presented circuit is its voltage boosting capability. For an input source with a voltage v_{dc}, it can produce a five-level ac output voltage with voltage levels of 0, $\pm\ v_{dc}$, and $\pm\ 2\ v_{dc}$. For achieving this goal, one power supply, two capacitors, ten diodes, and seven power switches are required. This structure has a high number of active and passive components; however, one main advantage of this method is that it can produce an output twice the voltage level of the power supply.

$$v_{out} = (S_1\ S_7 - S_2\ S_6)\,2v_{dc} + (S_1\ S_4\ S_5\ S_7 + S_2\ S_3\ S_4\ S_7 - S_1\ S_4\ S_5\ S_6 - S_2\ S_3\ S_4\ S_6)\,v_{dc} \quad (6)$$

In Madhukar Rao and Sivakumar (2015), a single-phase five-level inverter with fault tolerance is proposed. The proposed converter consists of seven power switches as well as twelve power diodes. A diode bridge in combination with a power switch in

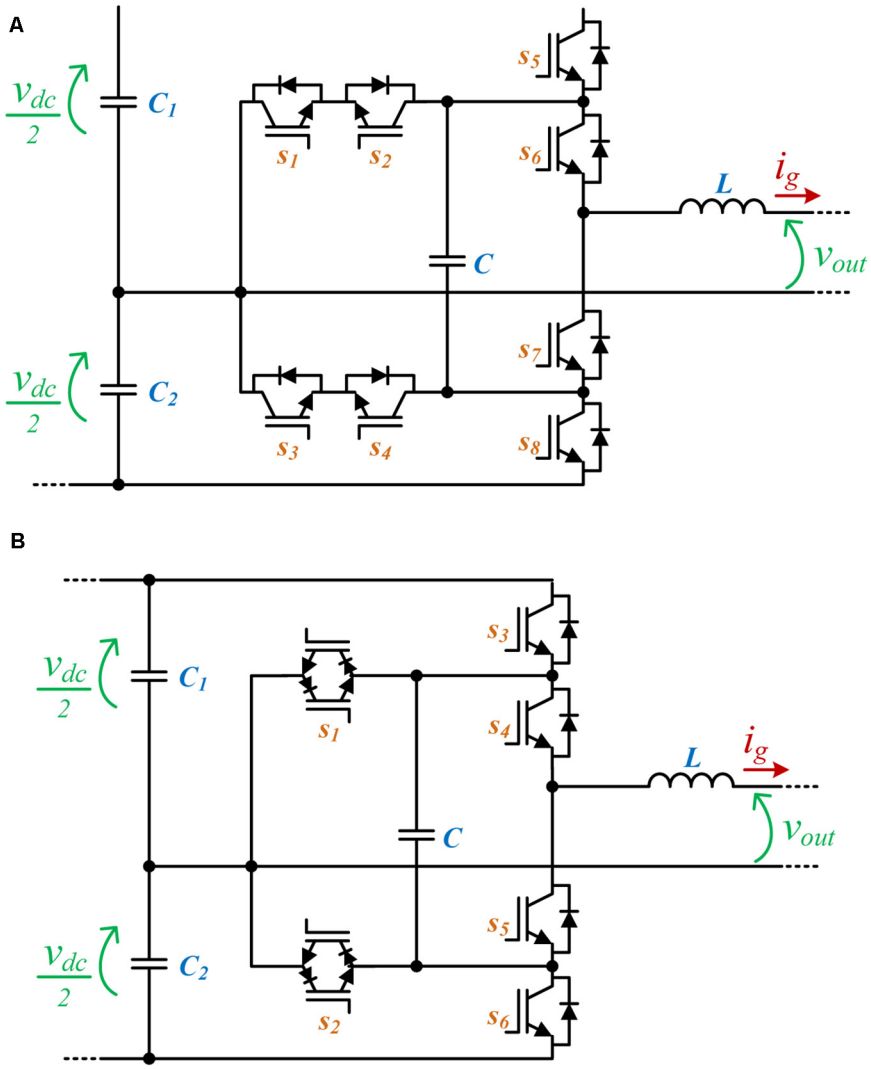

FIGURE 2 | Topologies: **(A)** proposed in Korhonen et al. (2014); **(B)** proposed in Yuan (2014).

the output is utilized to cut off the fault current. However, the utilized diode bridge of the fault circuit breaker in the output can severely hinder the efficiency of the converter. **Figure 5B** shows the structure of the converter proposed in Madhukar Rao and Sivakumar (2015). The output voltage of the topology shown in **Figure 5B** can be calculated based on (7), while S_1 can be used for interrupting the current path during faults.

$$v_{out} = (S_3\ S_4\ S_5 - S_2\ S_6\ S_7)\, v_{dc} + (S_3\ S_5\ S_6 - S_2\ S_5\ S_6)\, \frac{v_{dc}}{2} \tag{7}$$

A five-level inverter with a modular switched capacitor circuit is proposed in He and Cheng (2016). The main advantage of this topology is that the voltage levels can be increased by adding more switched capacitor bridge modules. As can be seen in **Figure 6**, the topology has twelve diode-switch sets for a five-level inverter. With each extra switched capacitor module, the output voltage amplitude can be increased to four times the input voltage v_{dc}. The first two switch groups are defined by (8) and (9).

$$S_P = S_3\ S_7\ S_9\ S_{10} \tag{8}$$

$$S_N = S_4\ S_6\ S_8\ S_{11} \tag{9}$$

Considering the defined switching groups and the remaining switches, it is possible to calculate the output phase voltages, according to (10). It should be noted that the S_P and S_N are complementary.

$$v_{out} = (S_P + S_N)[(S_2\ S_5 - S_1\ S_6)4v_{dc} + (S_2\ S_6 - S_1\ S_5)2v_{dc}] \tag{10}$$

Another five-level fault-tolerant structure is proposed in Gautam et al. (2017). This topology is presented in **Figure 7**.

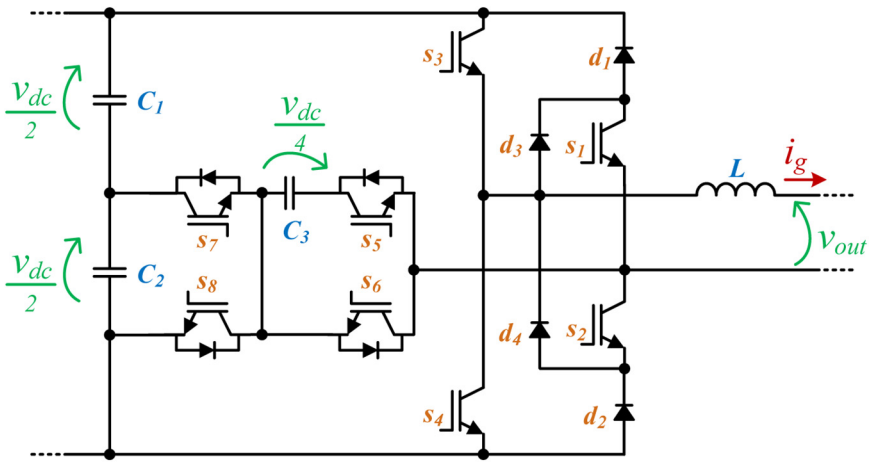

FIGURE 3 | Topology proposed in Masaoud et al. (2014).

It consists of six IGBT-diode sets, as well as a bidirectional switch and an NPC leg. Compared to many other topologies with fault current limiting capability, this one has a moderate number of switches and capacitors. The required NPC can be considered one of the disadvantages of such topologies. Moreover, this topology can produce output voltages in the range of $\pm\ v_{dc}$. The output voltage levels based on the input source and the capacitor voltage can be calculated using (11). In the case of $v_{c2} = v_{dc}/2$, there are five symmetrical voltage levels.

$$v_{out} = (S_1\ S_2\ S_6 - S_3\ S_4\ S_5)\, v_{dc} + (S_1\ S_2\ S_7 + S_2\ S_3\ S_7)\left(v_{dc} - v_{C_2}\right) - (S_3\ S_4\ S_7 + S_2\ S_3\ S_5)\, v_{C_2} \tag{11}$$

A five-level inverter for medium-voltage applications is proposed in Narimani et al. (2016). Although the paper focuses on a three-phase structure, it can be easily utilized as a single-phase system too. The system includes eight switch-diode sets as well as two extra diodes for each phase. One of the disadvantages of such a topology is the requirement of a split-source supply and three additional capacitors. The output voltage

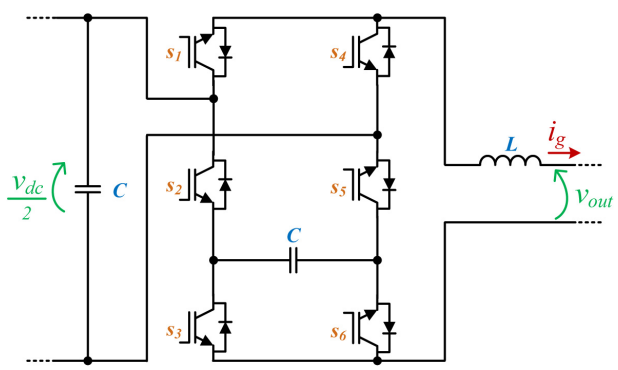

FIGURE 4 | Topology proposed in Vahedi et al. (2016).

levels include $v_{dc}/2$, $v_{dc}/4$, 0, $-v_{dc}/4$, and $-v_{dc}/2$. **Figure 8A** shows the abovementioned topology. Another disadvantage of this topology is a relatively complex balancing procedure for the three flying capacitors in each phase. Although the authors claim that the number of diodes is reduced compared to many previous topologies, the number of semiconductor devices is still relatively high. The output phase voltage of the topology shown in **Figure 8A** can be calculated based on the switch states using (12).

$$v_{out} = (S_1\ S_2\ S_3\ S_4 - S_5\ S_6\ S_7\ S_8)\frac{v_{dc}}{2} + (S_1\ S_2\ S_4\ S_5 + S_2\ S_3\ S_4\ S_8 + S_1\ S_3\ S_4\ S_7 - S_4\ S_5\ S_7\ S_8 - S_1\ S_5\ S_6\ S_7 - S_2\ S_5\ S_6\ S_8)\frac{v_{dc}}{4} \tag{12}$$

Figure 8B depicts another five-level inverter based on a split-source supply (Aly et al., 2018). It requires fourteen switch-diode sets and four extra diodes. Although this topology requires a higher number of semiconductor devices compared to the topology proposed in Narimani et al. (2016), it has some other significant advantages including: simpler control, no flying capacitor, and fault-tolerant structure. The output voltages are $-v_{dc}$, $-v_{dc}/2$, 0, $v_{dc}/2$, and v_{dc}, which can be calculated using (13).

$$v_{out} = (S_1\ S_2\ S_7\ S_8 - S_3\ S_4\ S_5\ S_6)\, v_{dc} + (S_1\ S_2\ S_6\ S_7 + S_2\ S_3\ S_7\ S_8 - S_2\ S_3\ S_6\ S_7 - S_3\ S_4\ S_6\ S_7)\frac{v_{dc}}{2} \tag{13}$$

A bidirectional topology based on a half-bridge front-end structure and two flying-capacitor cascade structures is proposed in Naderi et al. (2015). This topology is shown in **Figure 9**. This topology has a split dc link and two flying capacitors, which represents the main disadvantage of this topology since it increases the control complexity. When compared with other topologies, this one requires a significant number of switching devices. Each of the flying capacitor cells is formed by four switching devices,

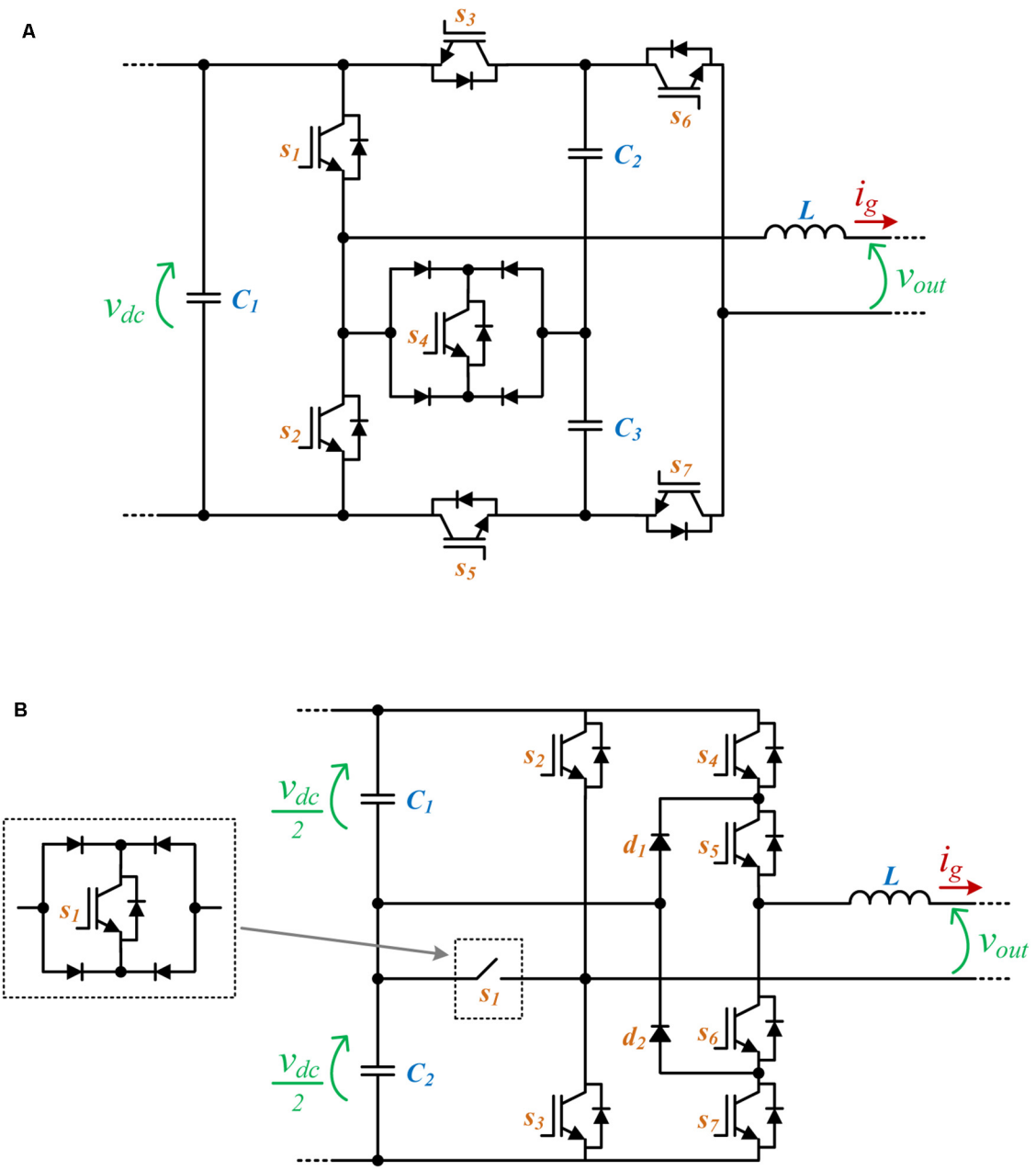

FIGURE 5 | Topologies: **(A)** proposed in Saeedian et al. (2018); **(B)** proposed in Madhukar Rao and Sivakumar (2015).

which are responsible for producing three voltage levels. The output phase voltage of the topology shown in **Figure 9** can be calculated based on the switch states defined in (14).

$$v_{out} = (S_1\ S_3\ S_4 - S_2\ S_9\ S_{10})\frac{v_{dc}}{2} + (S_1\ S_3\ S_6 + S_1\ S_4\ S_5 - S_2\ S_8\ S_9 - S_2\ S_7\ S_{10})\frac{v_{dc}}{4} \quad (14)$$

In this case, the following switches work in a complementary manner.

$$S_5 = 1 - S_3$$

$$S_4 = 1 - S_6$$

$$S_7 = 1 - S_9$$

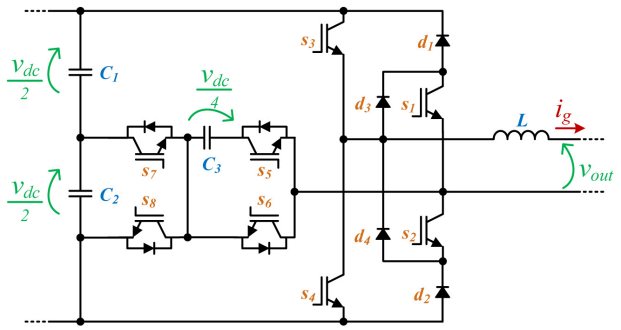

FIGURE 6 | Topology proposed in He and Cheng (2016).

$$S_8 = 1 - S_{10}$$

$$S_1 = 1 - S_2 \tag{15}$$

A bidirectional topology based on a full-bridge front-end structure and a bidirectional-bipolar cell connected between the neutral wire and a split dc link is presented in Monteiro et al. (2016). This topology is presented in **Figure 10A**. The full-bridge structure is responsible for obtaining three voltage levels ($+ v_{dc}$, 0, $-v_{dc}$), while the bidirectional-bipolar cell is responsible for obtaining the other two voltage levels ($+ v_{dc}/2$, $-v_{dc}/2$). The output phase voltage can be calculated using (16). In order to optimize the efficiency, the switching devices S_1 and S_2 can be switched at a low frequency (i.e., the frequency of the power grid voltage), while the other switching devices are switched at high frequency.

$$v_{out} = (S_2\ S_3 - S_1\ S_4)\, v_{dc} + (S_3\ S_5 - S_4\ S_5)\, \frac{v_{dc}}{2} \tag{16}$$

A bidirectional topology based on a full-bridge front-end structure and a back-end dc–dc structure with a split dc link is presented in Leite et al. (2018). This topology, shown in **Figure 10B**, operates with five voltage levels, according to the operation of the back-end dc–dc converter. The switching devices s1 and s2 are switched at a low frequency (i.e., the frequency of the power grid voltage), while the other switching devices are switched at high frequency. As claimed in the paper, this is an import aspect since it is possible to optimize the operation of the converter, reducing the switching losses. The output phase voltage of the topology shown in **Figure 10B** can be calculated based on the switch states using (17).

$$\begin{aligned} v_{out} &= (S_2\ S_3\ S_7\ S_8 - S_1\ S_4\ S_7\ S_8)\, v_{dc} \\ &+ (S_2\ S_3\ S_6\ S_7 - S_1\ S_4\ S_5\ S_8)\, \frac{v_{dc}}{2} \end{aligned} \tag{17}$$

Modular multilevel converters (MMCs) are another type of circuit that can realize five-level output voltage (Wang et al., 2019; Xu et al., 2019). In a way, MMCs are an extension of the earlier multilevel circuits based on the flying capacitors, with the exception that MMCs are much more feasible in higher voltage levels (Dekka et al., 2017). Theoretically, there is no limit to the number of voltage levels that an MMC can achieve, but the practical considerations such as controller complexity and cost would limit the number of voltage levels. Since the main advantage of the MMC topologies is in higher voltage and higher voltage levels, here only two of the more basic topologies that utilize half-bridge and full-bridge submodules are considered that are shown in **Figures 11–C**. The output voltage of the submodules shown in **Figures 11A–C** can be calculated using (18), (19), and (20), respectively.

$$v_{SM} = (S - S_2\ )\, v_C \tag{18}$$

$$v_{SM} = (S_1\ S_4 - S_2\ S_3)\, v_C \tag{19}$$

$$v_{SM} = (S_1\ S_3\ S_6\ S_8 - S_2\ S_4\ S_5\ S_7)\, v_C \tag{20}$$

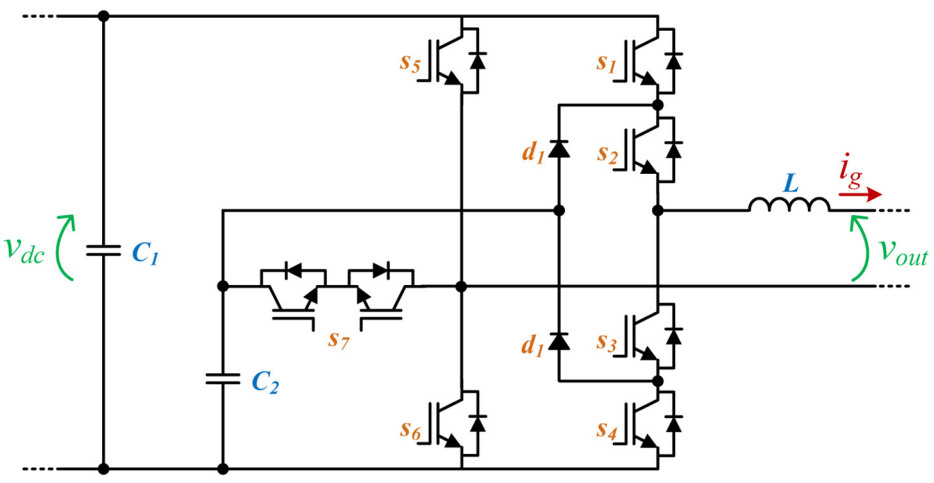

FIGURE 7 | Topology proposed in Gautam et al. (2017).

In Zhou et al. (2018), each MMC submodule has a half-bridge structure requiring two switches and two diodes. With the structure proposed in Zhou et al. (2018), eight switch-diode sets, two inductors, and four capacitors are required (Xu et al., 2018). However, it is possible to reduce the number of required modules to half, if the switching technique in Hu and Jiang (2014) is utilized. Based on the control technique proposed in Hu and Jiang (2014), four switch-diode sets, two inductors, and four capacitors are required. On the other hand, the size of the required inductor increases. The structure proposed in Hu et al. (2018) requires double switch-diode sets, than the one proposed in Zhou et al. (2018); however, because of the control proposed in Hu et al. (2018), smaller capacitors can be used while at the same time increase the output to input voltage ratio to around $0.7v_{dc}$. Another advantage of these MMCs is better fault tolerance.

There are other MMC topologies that focus on additional features such as sensorless balancing and/or parallel connection (Xu et al., 2018; Jin et al., 2019; Li et al., 2019; Xu et al., 2019). As an example, an extra half-bridge is introduced in Goetz et al. (2015, 2016) that brings about the capability to connect neighboring modules in parallel. The parallel connection decreases string impedance, reduces current ripple, and improves the balancing capability of the capacitors. The parallel connection of modules distributes load current among multiple capacitors (Zhu et al., 2018) and reduces requirements on the current rating of the switches to one half. Sizing the switches to lower current ratings compensates double the number of discrete switches of the MMCSP, and the amount of silicon needed is comparable to the MMC topology in Hu et al. (2018). The control method proposed in Li et al. (2017) reduces the complexity of the control algorithm to the level of standard MMCs. Large voltage differences and temporal imbalance might cause inrush currents between paralleled modules and reduce the feasibility of the parallel mode. Means to overcome the inrush currents are presented in Li et al. (2019).

MODULATION TECHNIQUES FOR FIVE-LEVEL FRONT-END CONVERTERS

One distinguishing aspect of the multilevel converters, when compared to the traditional two-level converters, is the wide variety of usable modulation techniques. Multilevel converters require different modulation techniques in order to synthesize all of its possible voltage levels, regardless of being three-level, five-level, or higher-level converters. Moreover, different modulation techniques can be applied to the same converter, as is the case of the most traditional techniques, but some techniques are only feasible to specific converters, as is the case of techniques that are specially developed for a given converter in order to optimize, for instance, the switching losses.

In a voltage-source inverter, the modulation technique is responsible for transforming a given reference voltage into a set of defined states of the switching devices comprising the converter, so that the desired reference voltage or current, depending on the used feedback control, is produced at its ac side. The two most common groups of modulation techniques for voltage-source inverters, regardless of the number of voltage levels, are the pulse-width modulation (PWM) and the space vector modulation (SVM). However, these two groups of modulation techniques must be properly adopted when applied to multilevel converters.

Pulse-Width Modulation (PWM)

PWM is a modulation technique widely used in two-level and three-level inverters, where a single triangular carrier and one (in two-level inverters) or two (in three-level inverters) reference voltages are used. The popularity of this technique is

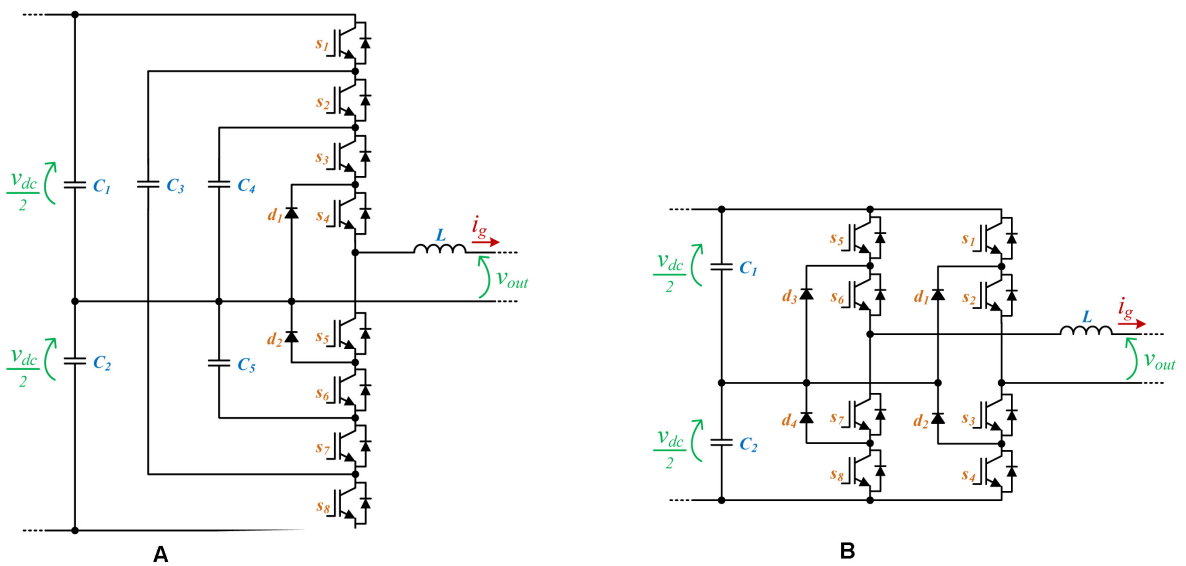

FIGURE 8 | Topologies: **(A)** proposed in Narimani et al. (2016); **(B)** proposed in Aly et al. (2018).

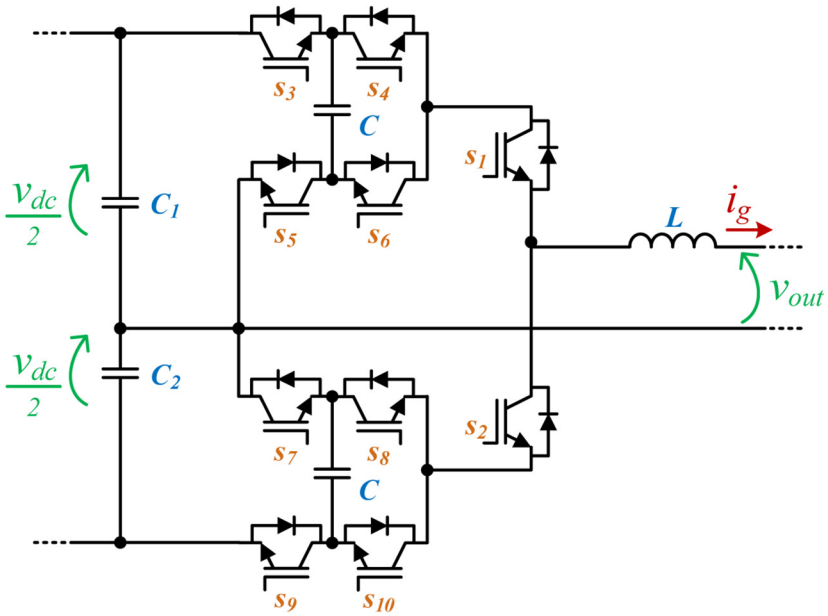

FIGURE 9 | Topology proposed in Naderi et al. (2015).

due to its ease of implementation, especially regarding digital signal processor (DSP)-based control systems, and due to the establishment of a fixed switching frequency, which is useful for sizing the output passive filters of the converter. Besides, since most inverters contain complementary pairs of active switches, one triangular carrier can be used to generate a pair of complementary signals for the switches. However, in multilevel converters, it is mandatory to use either more than one triangular carrier or more than two reference voltages in order to obtain the total number of possible voltage levels.

The classical multilevel PWM techniques consist of increasing the number of triangular carriers, which are either vertically or horizontally distributed, and the number of triangular carriers must be n-1, where n is the number of voltage levels. For the specific case of this paper, i.e., five-level inverters, four triangular carriers and one reference voltage should be used in order to attain a five-level operation with a classical multilevel PWM technique. Besides, taking into consideration the triangular carrier disposition, two main schemes can be feasible, i.e., with vertical disposition and horizontal disposition. In a vertical disposition-based PWM, all the carriers have the same amplitude and frequency but different average values, so that the maximum value of a given carrier coincides with the minimum value of the upper one, and so on. In this case, two of the carriers are only positive and the other two are only negative. In terms of phase, there are three main approaches regarding vertical-disposition PWM schemes: (a) phase disposition, where all the carriers have the same phase (**Figure 12A**); (b) phase opposition, where the positive carriers are 180° phase shifted with the negative carriers (**Figure 12B**); (c) alternative phase opposition, where the consecutive carriers are 180° phase shifted from each other (**Figure 12C**). Vertical disposition is suitable for topologies comprising a split dc link, such as NPC and flying capacitor, but can lead to power unbalances in topologies with independent dc links. Regarding horizontal distribution, this scheme is also termed as phase-shifted PWM, where all the carriers have the same amplitude, average value, and frequency but different phase angles. The phase shift between consecutive carriers should be equal to 360°/n, where n is the number of triangular carriers. Hence, in this case, each triangular carrier is 90° phase shifted from each other, as can be seen in **Figure 12D**. Another possibility is to use two reference voltages 180° phase shifted between each other (as in a unipolar PWM scheme) and only two triangular carriers obeying to a 180°/n ratio. In this case, the carriers are not evenly divided in one switching period due to the additional reference voltage, which emulates the two removed carriers, as can be seen in **Figure 12E**. Horizontal-disposition schemes have the advantage of multiplying the switching frequency (the frequency of each carrier) into the output frequency by a factor of n, (four, in this case), similarly to an interleaved converter. Compared to vertical disposition, this scheme allows a balanced power distribution in topologies such as cascaded multilevel and a natural voltage balancing in the flying-capacitor topology. Nevertheless, vertical-distribution schemes allow a lower THD in the output voltage than the horizontal distribution for the same characteristics of operation (Rodriguez et al., 2002, 2007; Kouro et al., 2010; Malinowski et al., 2010; Debnath et al., 2015; Li et al., 2015).

However, depending on the available resources, the use of multiple triangular carriers can also be an obstacle. One method to suppress this is to use a single triangular carrier but different reference voltages, also called modified reference

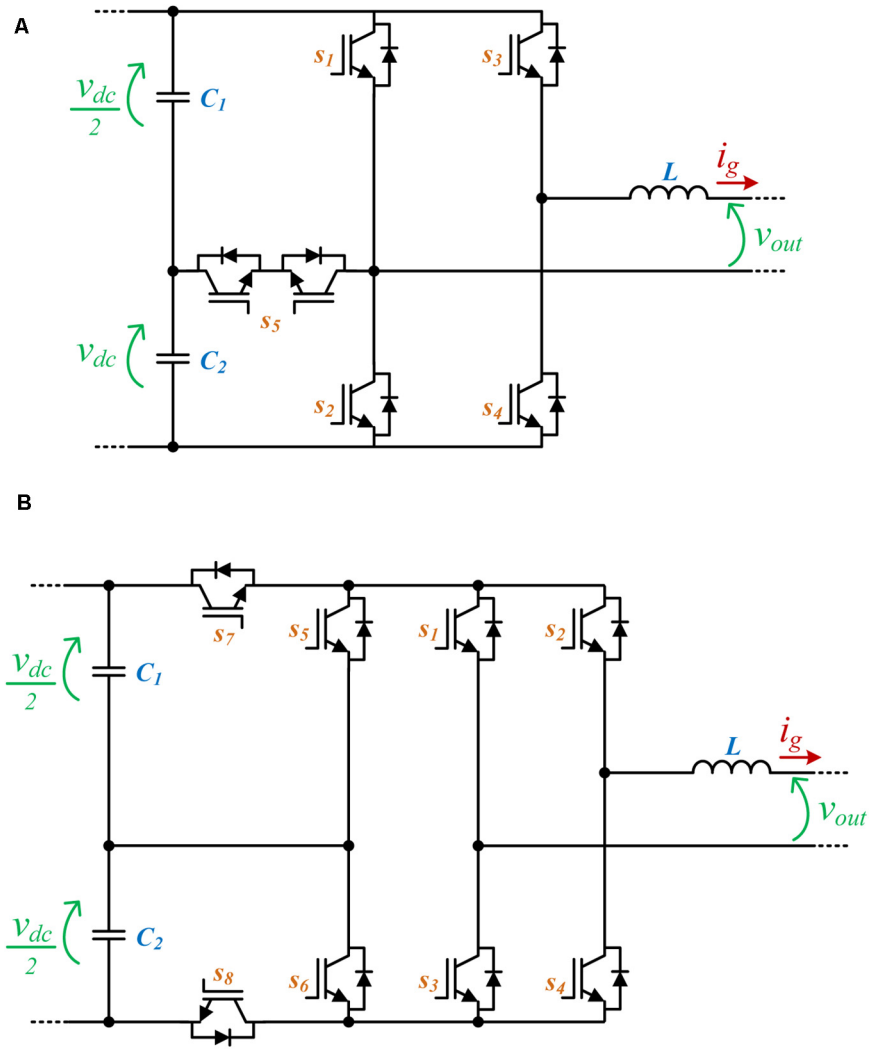

FIGURE 10 | Topologies: **(A)** proposed in Monteiro et al. (2016); **(B)** proposed in Leite et al. (2018).

voltages. Therefore, each complementary pair of signals for the active switches is achieved not from each triangular carrier but from each reference voltage. This approach can also be used to optimize the switching frequency of a multilevel converter. For instance, in Leite et al. (2018), a modulation strategy is implemented that allows an active switch pair to operate with a switching frequency equal to the low-frequency component of the output voltage, i.e., the power grid frequency. This allows reducing the switching losses of the converter or, even further, to apply a different type of power semiconductor that does not need to be fully controlled (e.g., thyristor), offering lower conduction losses and a lower cost. **Figure 12F** shows an example of this modulation scheme, where one carrier and two references can be seen, generating three pairs of switch signals.

Space Vector Modulation (SVM)

While the PWM techniques are based on the modulation of each complementary pair of active switches, the SVM technique consists of acting upon the converter as a whole. This means that, in each instant, the state of all the active switches comprising the converter is determined in order to satisfy a given reference voltage. This is achieved via a coordinate transformation from *a-b-c* to α-β, where the reference frame is divided into sectors that contain a given output voltage. In order to synthesize the desired voltage (which is contained in a given sector), two adjacent voltage vectors (which are produced by a given converter state) should be used, with the length of each one being proportional to the on-time of each converter state. Compared to PWM, SVM also allows a fixed switching frequency but reduces the total number of commutations of a given switch in each output cycle,

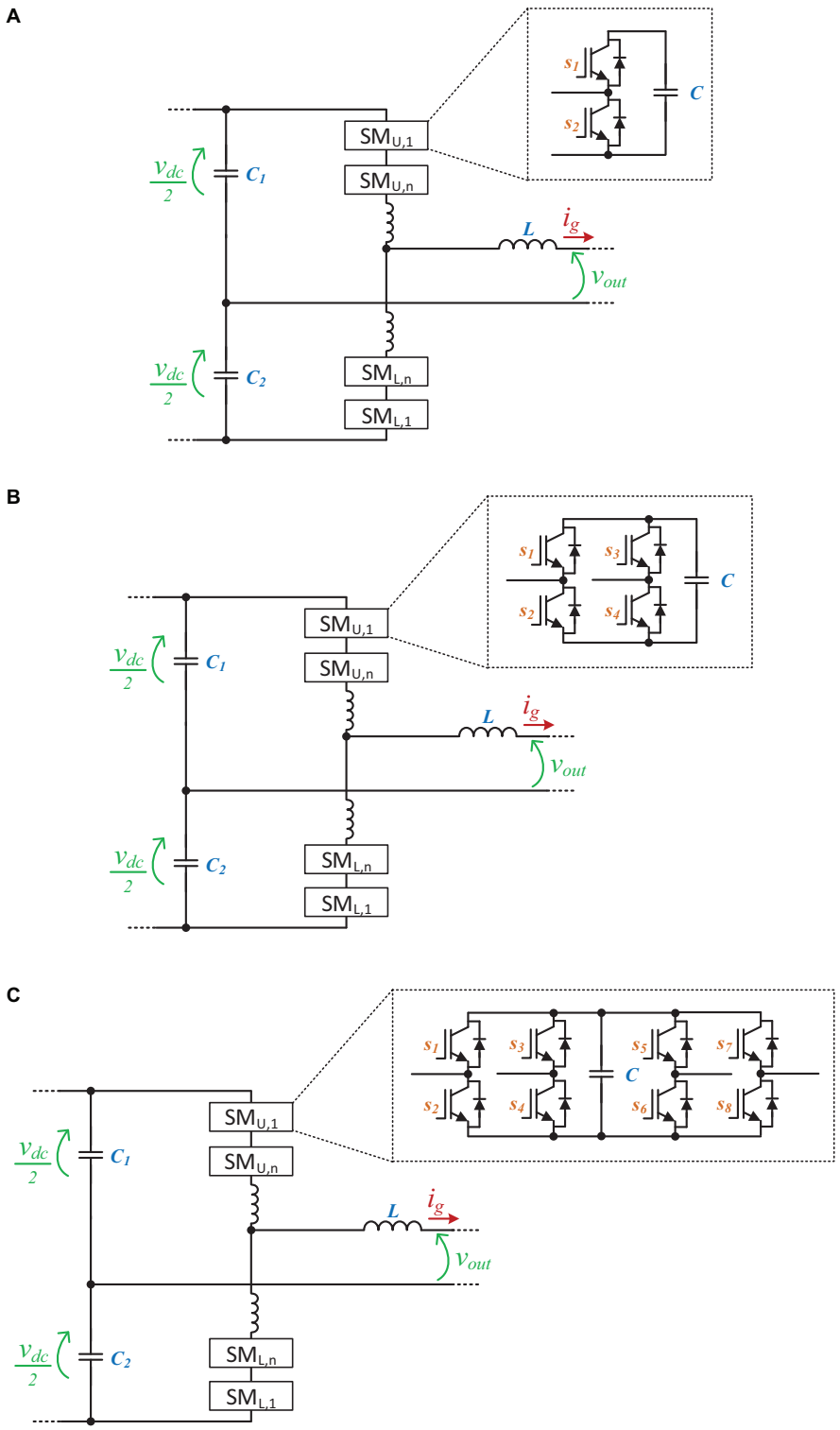

FIGURE 11 | MMC topologies: **(A)** proposed in Zhou et al. (2018); **(B)** proposed in Hu et al. (2018); **(C)** proposed in Goetz et al. (2015).

since each switch state can be assigned in a way that avoids redundant switching. A similar strategy, called pulse decoding, can be seen in Ge and Fang (2008), where only one switch pair switches at high frequency. Moreover, SVM allows a better utilization of the dc-link voltage, since it inherently comprises a third harmonic injection that allows achieving an output

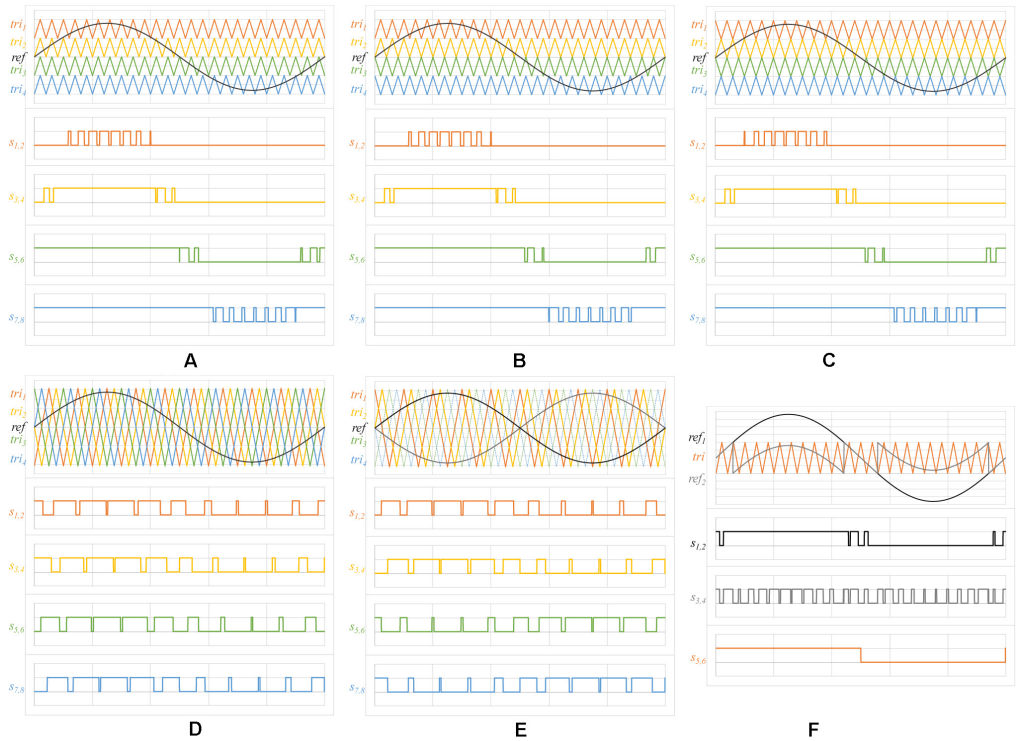

FIGURE 12 | Pulse-width modulation: **(A)** vertical phase disposition PWM carriers for five-level inverters; **(B)** vertical phase opposition PWM carriers for five-level inverters; **(C)** vertical alternative phase disposition PWM carriers for five-level inverters; **(D)** horizontal disposition PWM carriers for five-level inverters using based on four carriers and one reference voltage; **(E)** horizontal disposition PWM carriers for five-level inverters based on two carriers and two reference voltages; **(F)** horizontal-disposition PWM carriers for five-level inverters using a single carrier and a modified reference voltage.

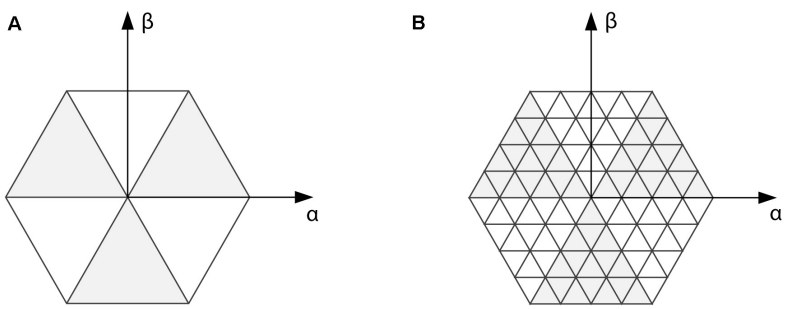

FIGURE 13 | Space vector representation for three-phase inverters: **(A)** two-level; **(B)** five-level.

voltage 15% higher than PWM for the same dc-link voltage and modulation index. Due to this reason, SVM is an interesting modulation technique to be applied in three-phase inverters for three-wire systems, as is the case of traction applications, for instance (Kanchan et al., 2005; Vinod et al., 2018). The main disadvantage of SVM compared to PWM is its complexity, requiring calculations that do not exist in PWM.

In multilevel converters, SVM is attainable through a higher number of sectors, as well as a higher number of voltage vectors. While three-phase two-level converters allow six non-null voltage vectors and six sectors, as can be seen in **Figure 13A**, three-phase five-level converters allow sixty non-null and non-redundant voltage vectors, comprising a total of ninety-six sectors, as represented in **Figure 13B**. Each triangle represents a sector, while each triangle vertex represents one voltage vector. The number of voltage vectors depends on the nature of the converter, i.e., whether it allows redundant states (multiple voltage vectors to produce the same output voltage) or not (only one voltage vector to produce a given output voltage) (Dae-Wook et al., 2003; Ahmed et al., 2016; Li et al., 2017).

TABLE 2 | Comparison between the presented topologies.

Category	References	Number of switches[a]	Number of diodes	Number of sources	Number of caps	Needs split dc link	Number of inductors	$\frac{V_{out,\,max}}{V_{in}}$	Output voltage levels	Control complexity	Fault tolerant
With flying capacitors	Korhonen et al., 2014	8n	8n	1	N	Yes	0	1/2	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	No
	Yuan, 2014	8n	6n	1	N	Yes	0	1/2	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	No
	Vahedi et al., 2016	6n	6n	1	N	No	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	**	No
	Saeedian et al., 2018	7n	10n	1	2n	No	0	2	$\pm 2v_{dc}$, $\pm v_{dc}$, 0	**	No
	He and Cheng, 2016	12n	12n	1	4n	No	0	4	$\pm 4v_{dc}$, $\pm 2v_{dc}$, 0	**	No
	Narimani et al., 2016	8n	10n	1	3n	Yes	0	1/2	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	No
	Naderi et al., 2015	10n	10n	1	2	Yes	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	***	No
Without flying capacitors	Sajadian and Santos, 2014	4n	6n	1	0	No	1	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	*	No
	Masaoud et al., 2014	4n + 4	4n + 4	2	0	Yes	0	1	$\pm v_{dc}$, $\pm 3v_{dc}/4$, $\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	*	No
	Madhukar Rao and Sivakumar, 2015	7n	10n	1	0	Yes	0	1/2	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	*	Yes
	Gautam et al., 2017	8n	8n	1	0	No	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	***	Yes
	Aly et al., 2018	14n	18n	1	0	Yes	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	***	Yes
	Monteiro et al., 2016	5n	9n	1	0	Yes	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	**	No
	Leite et al., 2018	8n	8n	1	0	Yes	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	**	No
Modular methods	Zhou et al., 2018	8n	8n	1	4	Yes	2	0.5	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	No
	Hu et al., 2018	8n	8n	1	2	Yes	2[b]	0.71	$\pm v_{dc}$, $\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	Yes
	Hu and Jiang, 2014	4n	4n	1	2	Yes	2[b]	0.5	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	No
	Goetz et al., 2015, 2016	16n	16n[c]	2	2	Yes	2	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	**	Yes

[a]*Anti-parallel diodes of the IGBTs are considered separate components, as is the case in many applications.* [b]*Relatively large inductors.* [c]*With half the rated current on each switch.* ***high; **medium; and *low.*

SVM is advantageous over PWM when the number of levels is very high, i.e., when controlling the converter as a whole is simpler to implement instead of controlling each complementary switch pair.

COMPARISON BETWEEN TOPOLOGIES

This section presents a comparison regarding the topologies identified in section "Topologies of Five-Level Front-End Converters." The comparison was performed considering three main categories: with flying capacitor, without flying capacitors, and MMCs. For all the topologies, the key parameters were considered. **Table 2** shows the comparison between the topologies. Analyzing this table in more detail, the MMC topologies (Goetz et al., 2015, 2016) requires more devices (diodes and switching devices), which can be identified as a disadvantage since it can increase the conduction and switching losses, contributing to a reduction in efficiency. Besides the MMC topologies, the topology (Masaoud et al., 2014) requires two sources and is the only topology with this requisite, which can be impeditive for applications as renewables since two independent sources are required. The topology (Sajadian and Santos, 2014) requires the use of a transformer, which can be a disadvantage, but it only requires a single source and no capacitors for obtaining the five voltage levels. Topologies (Sajadian and Santos, 2014; He and Cheng, 2016; Vahedi et al., 2016; Gautam et al., 2017; Saeedian et al., 2018) require a single dc link, i.e., a split dc link is not necessary for the operation with five levels; therefore, for applications as renewables, this is an interesting aspect. Since fault tolerance and reliability issues are not the main focus of this review, only a few examples of the more recent topologies (Madhukar Rao and Sivakumar, 2015; Gautam et al., 2017; Hu et al., 2018) were considered. Considering the fault-tolerant topologies, it is clear that higher tolerance to fault comes at the cost of a significantly higher number of active components.

The main problem in the methods based on the flying capacitors is the control complexity. When the capacitor voltage is a fraction of the supply voltage, then the controller should monitor the voltage of that capacitor and actively maintain it in a tight boundary. On the other hand, the methods based on the multiple/split sources are more expensive to implement in the end, since they require either separate power sources or keeping the split-source voltage considering all the inherent differences in the system. The capacitors of the split dc link may exhibit a difference in voltage sharing, causing a voltage ripple in the dc link. Consequently, the stabilization of the voltage ripple may require a considerably large dc-link capacitor. In addition, any imbalance in the load causes a neutral current, which causes a perturbation in the split dc-link voltage (Jasna and Anitha, 2014). Consequently, balancing the split dc-link capacitors is the subject of a proper control. Therefore, as happens always in engineering applications, here a trade-off should be maintained on the control complexity, sensor requirements, fault tolerance, and cost. Regarding the topologies based on modular structures, only a few of them are present, since the main advantage of such methods is framed in higher voltage levels. Therefore, as a five-level converter, modular multilevel methods are not very economical.

Regarding the number of semiconductors, it is commonly known that a higher number of passive semiconductors contribute to a decrease in the cost and the control complexity of the inverter but negatively affect its efficiency (Graditi et al., 2011). Consequently, the additional production of heat contributes to an increase in the requirements on system cooling, as well as to an acceleration in the aging of semiconductors (Reynolds, 1974). In this context, higher efficiency is generally achieved by trading the number of passive semiconductors (e.g., diodes) and active semiconductors (e.g., MOSFETs and IGBTs) (Kyono, 2006). Naturally, a higher overall number of components in the inverter, both passive and active, lowers its reliability, if the components do not introduce fault-tolerance itself (Zhang et al., 2014).

CONCLUSION

Worldwide, distributed renewable-energy resources are seen as absolutely fundamental to accomplish with the target to minimize environmental concerns, to obtain access to affordable energy, and to contribute to a sustainable power grid. Over the past few decades, in order to enable the increasingly effective integration of renewable-energy sources, power electronics technologies have played a leading role. In fact, even today, power electronics technologies are seen as one of the fundamental challenges for the widespread use of renewable-energy sources. Embracing this context, this paper presents a review of power electronics converters that can be used for interfacing renewable-energy sources into the power grid, concentrating on front-end converters with a voltage-source structure. More specifically, in a more attractive future perspective, this review is only focused on five-level structures. Thus, throughout the paper, the most relevant five-level topologies for the contextualization of renewable-energy sources in smart grids are presented. As a result, an effective comparison between the topologies is presented, highlighting key aspects that are useful to select a topology in detriment of others, according to the number of passive and active semiconductors, sources, capacitors, split dc links, inductors, and voltage levels. As an example, based on the established comparison, it is possible to conclude that topologies with more than one source are not advantageous and, on the other hand, topologies with a single dc link represent an interesting aspect for renewable-energy source applications. Based on the established comparison, it is possible to conclude that topologies with more than one source are not advantageous and, on the other hand, topologies with a single dc link represent an interesting aspect for renewable-energy source applications. The comparison also shows that topologies with a flying capacitor are not ideal concerning fault-tolerant characteristics, and a topology that accomplishes with the combined criteria such as being fault-tolerant, flying capacitors being unnecessary, and with reduced control complexity, which are three relevant features for obtaining reliable and high-efficiency converters to interface

renewable-energy sources with the power grid, was identified. The topologies that require lower control complexity are all based on structures independent of flying capacitors, which is understandable, since such capacitors require a dedicated control loop. Moreover, such topologies require additional hardware, such as sensors and signal conditioning circuits. On the other hand, the topologies based on modular structures require more control complexity, since these structures are based on submodules (i.e., constituted by half-bridge or full-bridge converters). Notwithstanding, it is important to emphasize that the objective of this paper is not directly related to the identification of a specific topology that complies with all the benefits under study; it has the goal of presenting the different advantages and disadvantages of each topology in order to facilitate the comparison of such topologies for different purposes.

AUTHOR CONTRIBUTIONS

VM, NT, TS, and TK contributed to writing the manuscript. JA and SG contributed to review the manuscript and to present suggestions and corrections. All authors contributed to the article and approved the submitted version.

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