



A Duty Cycle Controlled ZVS Buck Converter With Voltage Doubler Type Auxiliary Circuit

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DC–DC converters have wide applications in industries, motor drive circuits, electric vehicles, and power supplies. In traditional converters hard switching occurs due to switching losses. This imposes constraints on the converter's efficiency which results in heat dissipation and reduction in the converter's life. The proposed converter aims to encounter the hard switching problem with the provision of soft switching features. The presented topology is efficient with respect to the features of cost, compact size and durable lifetime of converter topology with the provision of low switching stresses. This research work proposes a novel stepdown converter with zero voltage switching characteristics. With the use of half bridge inverter switches and series resonant components in the auxiliary circuit, the target of zero voltage switching and reduction in switching stresses has been achieved. The proposed 500 W converter is designed to operate at frequency of 100 KHz with 300 V source input voltage. Output voltage of the converter is 150 V.

Keywords: DC–DC buck converter, hard switching, soft switching, zero voltage switching, duty cycle, stress reduction

INTRODUCTION

Nowadays, the world is facing serious environmental concerns such as global warming and environmental pollution. Many factors are responsible for these immense climatic changes. One of those factors are the emission of harmful gases from traditional transportation systems. Researchers in power electronics are putting their efforts toward providing the most effective solution to cope with these challenges by the introduction of electric transportation systems. Revolution in the transportation sector for energy efficiency is increasing in today's world. So, the development of electric vehicles has proliferated rapidly in recent years (Bose, 2010). The efficiency of electric vehicles depends upon many factors, of which the electric drive system is the most considerable one. For an efficient and optimal electric vehicles system, the electric drive system should be designed optimally to ensure fewer losses (Martinez et al., 2016). The motor drive system consists of electric motor, power converter, controller, and different sensors. The efficiency of the motor drive system mainly depends upon the power converter used in it. DC–DC converters have wide applications in industries, PC power supplies, and processor IC's (Integrated Circuits) (Marchesoni and Vacca, 2007; Batista et al., 2009). These power converters operate with hard switching which causes switching losses that result in a reduction in efficiency of the converter. Hard

switching occurs due to the presence of the current and voltage across the switch during its transition state. The researchers put their efforts toward encountering the problems of hard switching by the provision of soft switching techniques. In this paper a novel topology of DC–DC converter operating in ZVS (Zero Voltage Switching) condition is proposed. The converter is implemented in ORCAD/PSPICE (Oregon Computer Aided Design/Personal Computer Simulation Program with Integration Circuit). The result comparison was carried out with the previous research works which proves the efficiency of the proposed work in terms of cost, size and ratings of high input voltage/output voltage conversion ratio.

RELATED WORK

The demand of more efficient DC–DC power converters has increased due to their wide applications in industries. The conventional converters face the problem of hard switching during the transition state of the switches. Ideally, when the switch gets turned on, voltage across it should be zero. Similarly, at the turn off state, the current should be zero. But practically, the situation goes on differently due to the presence of voltage and current across the switches. It imposes power losses and stresses on the switch, thus causing reduction in the switch's life and leads towards a less efficient system.

Thus, the requirement of lossless and efficient dc-dc converters pushes researchers to introduce new topologies for reduction in switching losses, as the conventional dc-dc converters do not exhibit the soft switching features and techniques, so different researchers have invented new topologies to encounter hard switching. This section covers the related work on buck converter with the comparative analysis on soft switching techniques. Many researchers have used different soft switching techniques on buck converters with the introduction of new topologies.

Moschopoulos et al., (1999) introduced a stepup converter with ZVS technique for low stresses across the switches. It was designed for low power applications. Its Peak switch stresses are slightly higher than the conventional ones. It involves the use of transformer which also leads toward the complexity and core losses. Kumar et al., (2017) used a ZVS technique to improve the efficiency of the DC–DC converter for both isolated and non-isolated converters. It is a 35 W power converter working for low voltage rating. The topology has less stepdown ratio with a greater number of components used in it. Soft Switching techniques with the characteristics of losses reductions were also introduced for bidirectional buck-boost converter. Broday et al., (2016) and Hussain et al., (2019) proposed the topologies for reduction in losses and provision of soft switching characteristics for bidirectional converters. The main drawback is the factor of complexity and cost due to the use of a tapped inductor and design of magnetic core in the topologies, causing increment in cost. Lin et al., (2008) introduced a Buck-fly back converter for a ZVS operation using the topology of the active snubber circuit. This 240 W power converter with 90 kHz switching frequency provides a

large voltage stepdown between input 140 V and output 24 V. The circuit has its limitation due to the use of a greater number of components in it. Furthermore, a novel ZVS topology used by Zhao (2011) to encounter the problem of the narrow duty cycle and hard switching of the conventional converter. The prototype is 48V1V with 100 kHz switching frequency. Although the topology is simple, but its voltage conversion ratio is very low. Chauhan and Pandey (2017) put his effort into reducing switching losses and minimizing hard switching problems by comparison of the conventional buck converter with the proposed topology. The topology is simulated in PSIM with specifications of a 12 V/4.8 V DC–DC converter with a 50 MHz switching frequency. This topology is designed just for low power applications i.e battery charging applications. Striney et al., (2016) proposed a ZVS topology of Buck converter for multiloading applications. It encounters the problem of cross regulation parameters in case of multiloading applications to reduce switching losses. The circuitry is complex due to the use of the motor which leads toward the cost increment and power losses as well as rotary losses associated with motors. Marvi et al., (2016) presented a technique to improve the overall efficiency of the voltage regulator module. It also provides ZVS across the main switch in the isolated converter. In the isolated converter, with the use of the transformer, the situation leads toward the more complex and costly circuits as well as bulky size of converters. Another ZVS buck converter topology for a bidirectional buck converter is described by Song et al., (2014). It has applications in hybrid energy storage systems. The topology is capable of providing low losses with ZVS features and constant frequency. The complexity of a high stepdown operation circuit causes a reduction in efficiency and increases design difficulty and cost. A low duty cycle causes problems of insufficient PWM (Pulse Width Modulation) resolution which causes inappropriate control to the converter. Yeh et al., (2017) encounters the problem of a low duty cycle by using a tapped inductor buck converter which extends duty cycle. In contrast to the traditional converter technology, the presented converter works with a much wider duty cycle with same voltage level conversion ratio. The circuit topology is not complex and is simple, but it operates on a low power rating. Lakshminarasamma and Ramanarayanan (2007) presented Quasi resonant technology for the efficient DC–DC converter with the use of a couple inductor. It results in lossless switching across both the switches (main and auxiliary) without affecting the V/I rating of main device. A converter with 33 W and 400 kHz frequency is simulated in this paper. The limitation of this topology is that it has high voltage and current stress across the switch. The ZVS introduced in this paper works with the switch with the same VA ratings as the source voltage and load current, but it failed to overcome the problem of switching loss across the auxiliary switch in the case of the turn off state. Various researchers (Do, 2011; Kollimalla et al., 2014; Babaei and Saadatizadeh, 2019) described a bidirectional Buck–Boost technology for the operation of a ZVS DC–DC converter. In the converter the inductor L_L provides ZVS operation and increases the efficiency of the circuit. It encounters all the

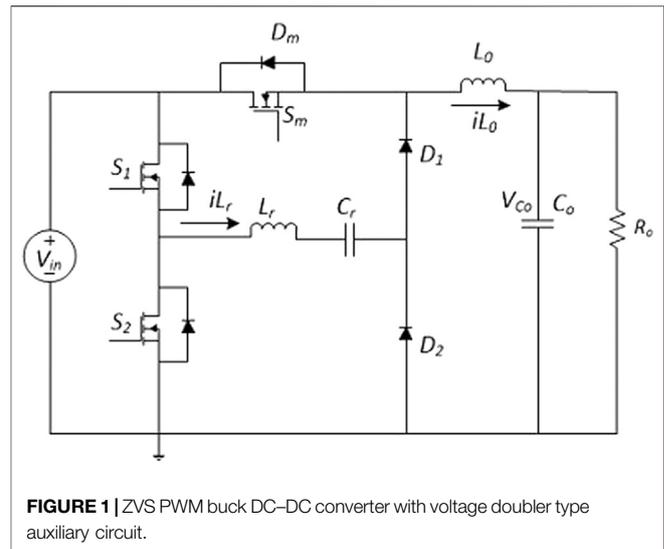
problems of the reverse recovery phenomena of body diode of the switches. These converters exhibit additional windings across the inductor which causes complexity due to the use of a greater number of components. Tsai et al., (2011) described topology as a provision of ZVS topology for an active clamp circuit in the interleaved buck converter. The topology introduced by Wang et al., (2011) encounters the problem of leakage energy and ringing voltage across the active switches including the use of the auxiliary switch and coupled inductor for ZVS operation of the PWM buck DC–DC converter. Hwan Oh, (2008) introduced ZVS topology for light load conditions for the synchronous rectifiers buck converter. In this technology the output diode gets replaced by the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) which ensures fewer conduction losses with improved efficiency. The topology consists of 12 V/5 V voltage ratings with 25 W power and switching frequency of 100 kHz. Other than the light load, it is also necessary to provide ZVS for a full load. Shao et al., (2017) proposed ZVS topology suitable for both light and full load conditions. It minimizes conduction losses in switches during a continuous conduction mode with the use of additional L and C components with a conventional buck converter. Kanamarlapudi et al., (2017) presented the ZVS full-bridge DC-DC converters. The prototype is a 2 KW power converter with voltage conversion ratings of 300 V/200 V and a switching frequency of 20 kHz. Most of the converter topologies described in this section are designed for low power applications with a lower voltage conversion ratio. So, it is very necessary to provide soft switching for high power applications with high voltage ratings. Kim et al., (2019) proposed converter which removes the problem of hard switching from the rectifier. Its main advantage is lesser component count; however, transformer incorporation may cause additional losses. An auxiliary winding turn base converter was proposed by Lin (2020). The proposed converter was designed for a wide input range of voltages. It has a high number of components and the switch undergoes a hard operation. The Research Community has exploited the topology of ZVS along with PWM in auxiliary type circuits for different applications (Kim et al., 2019; Marikkannan et al., 2019; Srivastava et al., 2019; Lin, 2020).

The limitations of research work are that the topology is presented with software simulation in PSPICE. Zero voltage switching is shown graphically. In terms of hardware implementation, the topology will be costly as it has a greater number of components used in it. The converter is limited for applications up to 500 W. The converter, due to having a greater number of components, increases its complexity and cost factor.

The proposed converter in this paper is beneficial in terms of working on high voltage ratings. All the stated topologies in the literature review have worked on low voltages. In comparison with the others, this topology provides ZVS for high voltage ratings.

It encounters the problem of hard switching by providing zero voltage switching which ensures zero power losses across the main switch.

The contributions of the research work are mentioned below:



- In switching mode, the converter provides zero losses across main switch S_m , Dynamic losses across the switch will be zero but static losses due to resistor will be there.
- With the use of an auxiliary circuit, it encounters hard switching problem by providing soft-switching across the switch.

PROPOSED ZVS DC–DC CONVERTER

The proposed Zero Voltage Switching Pulse Width Modulation DC-DC Buck converter with a Voltage Doubler Type Auxiliary Circuit is presented in **Figure 1**. The circuit consists of two parts: 1) Main circuit 2) Auxiliary circuit. The main circuit consists of the voltage source V_{in} , main switch S_m , main inductor L_0 , output capacitor C_o , and output resistor R_o . The auxiliary circuit consists of the half-bridge inverter switches i. e auxiliary switches S_1 and S_2 , two diodes D_1 and D_2 , and resonant components L_r and C_r .

The output of the half-bridge inverter is connected to the series LC resonant circuit. The output of the resonant circuit is connected to the main inductor L_0 through D_1 and D_2 . The main switch S_m is the same as the conventional Buck Converter switch. It is placed between the input voltage source and main inductor L_0 . The output capacitor C_o is connected across the output resistor R_o .

Principle of Operation Mode Analysis

The proposed converter operation is divided into six modes depending on the working of the converter. The key steady-state waveforms of the converter with the division of modes are shown in **Figure 2**. Each mode of current is explained with the help of an equivalent circuit diagram and key steady-state waveform.

Equivalent Circuits of Operation modes

The equivalent circuits of operation modes of the proposed converter are shown in **Figure 3**.

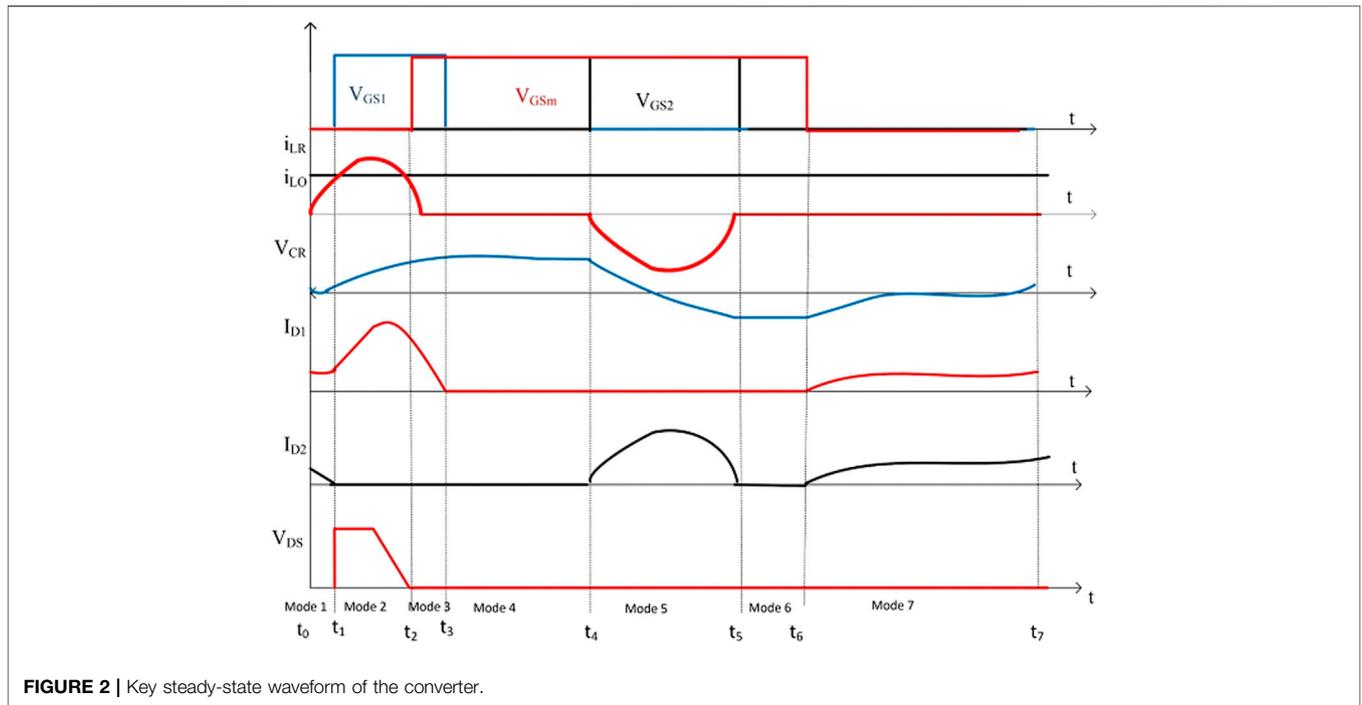


FIGURE 2 | Key steady-state waveform of the converter.

Mode 1: (Interval $t_0 < t < t_1$)

Mode 1 begins at time $t = t_0$. At this time interval, the equivalent circuit diagram of the converter is shown in Figure 3A. The switching cycle begins at time t_0 . Before t_0 the main and auxiliary switches are turned off and the main inductor is in a conduction state, thus providing energy to the circuit. This mode starts at the time t_0 when the main inductor L_o is connected with the source through the resonant path. The main inductor current i_{L_o} is rising from the minimum value. Current through resonant inductor L_r rises which causes resonant capacitor C_r to charge. Diode D_1 and D_2 are forward biased due to the previous state. Output voltage V_o is maintained through capacitor C_o .

During this mode, the resonant inductor current i_{L_r} is less than the main inductor current as it can be seen in Figure 2. Diodes are forward biased due to the energy provided by the main inductor L_o . This mode will continue until the currents of resonant and main inductor become equal.

The voltage and current across the inductor “L” will be:

$$i_{L_r}(t) = \frac{V_{in} - V_{cr(0)}}{Z_0} \sin \omega_0(t - t_0) \tag{1}$$

$$V_{cr}(t) = V_{in} - (V_{in} - V_{cr(0)}) \cos \omega_0(t) \tag{2}$$

$$i_{in} = i_{L_r} = i_{C_r} \tag{3}$$

$$i_{D2} = i_{L0} \tag{4}$$

$$i_{D1} = i_{L_r} + i_{D2} \tag{5}$$

Mode 2: ($t_1 < t < t_2$)

This mode begins at t_1 when both the currents become equal i: e resonant inductor current and main inductor current. The body diode of the main switch S_m is turned on and D_2 is turned off. The

resonant inductor current i_{L_r} keeps on swinging sinusoidally. The resonant current exceeds i_{L_o} therefore D_2 turned off and D_1 remains forward biased. Once D_m is turned on the main switch can be turned on with ZVS.

In this mode, when both currents become equal, D_m gets turned on, and the potential difference across the main switch becomes equal thus ensuring zero voltage across the main switch. It provides zero voltage switching phenomena in the converter.

The circuit diagram for mode 2 is shown in Figure 3B. The current passing through diode D_1 divides into two paths. One is from the body diode of the main switch. Another path is provided by the main inductor. Output Capacitor C_o maintains the constant output voltage V_o .

The current and voltage equations for mode 2 are as follows:

$$I = I_p \sin \omega_0 t \tag{6}$$

$$I_p = \frac{V_o}{Z_0} \tag{7}$$

$$i_{Dm} = i_{L_r} - I_0 \tag{8}$$

$$i_{D1} = i_{L_r} \tag{9}$$

$$i_{L_r}(t) = \frac{V_{in} - V_{cr}(t_1)}{Z_r} \sin \omega_0(t - t_1) \tag{10}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{11}$$

$$V_{cr} = V_{in} - (V_{in} - V_{cr}(t_1)) \cos \omega_0 t \tag{12}$$

Mode 3: ($t_2 < t < t_3$)

Figure 3C shows the equivalent circuit diagram in the case of mode 3. This mode begins when the main switch S_m is turned on.

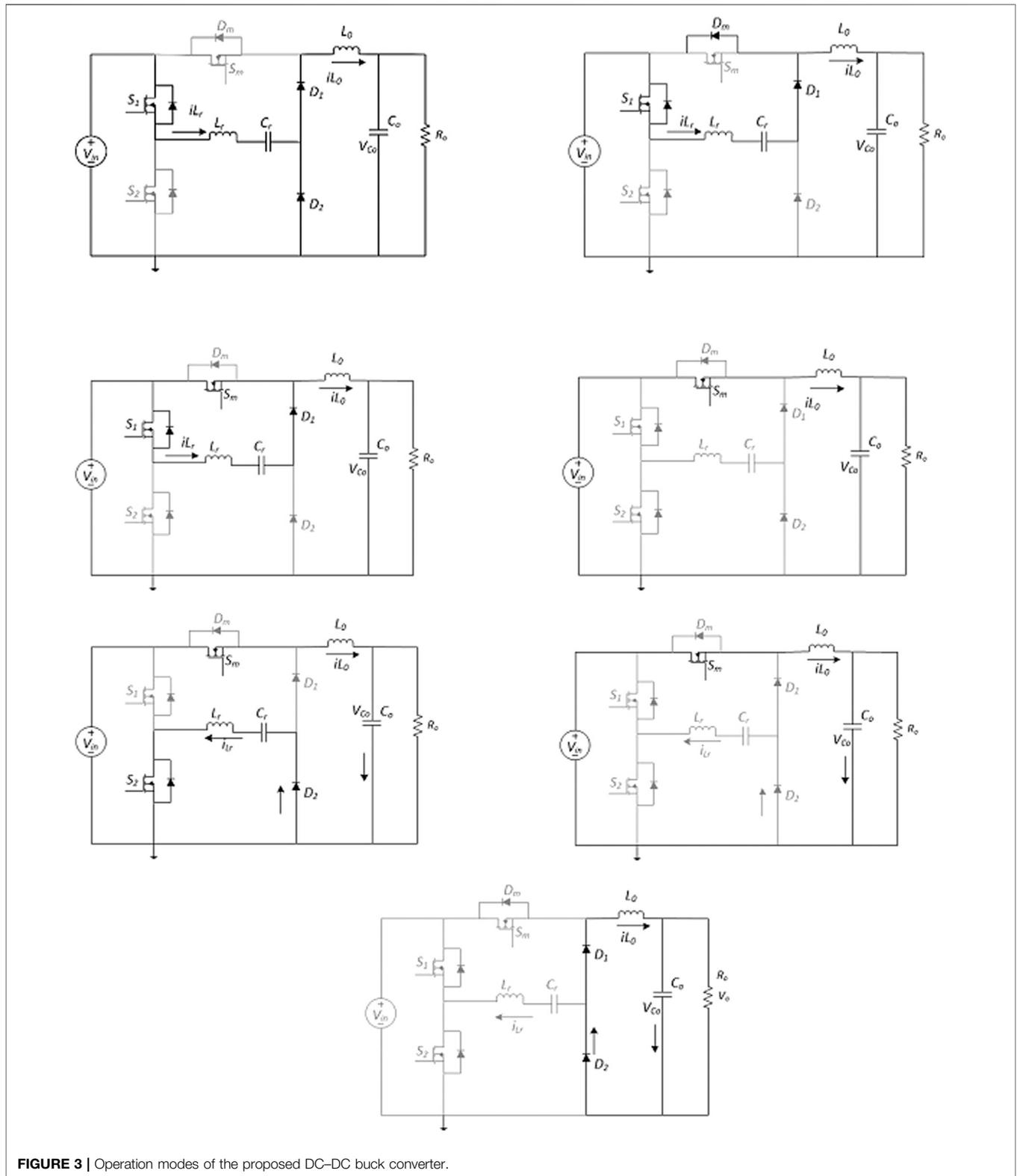


FIGURE 3 | Operation modes of the proposed DC-DC buck converter.

In this mode, S_m is turned on with ZVS. The current through the resonant path falls down linearly. The capacitor C_r is charged to the maximum value and goes to a steady state. In this mode, S_1

will also be turned off. Current through inductor L_o is increasing continuously. During the on time of S_m , the circuit behaves like a conventional buck converter. This mode ends when auxiliary

switch S_2 gets turned on. The equations for this mode are just like the conventional buck converter mode.

Mode 4: ($t_3 < t < t_4$)

This Mode begins at time $t = t_3$. In this mode when S_1 gets turned off so the main switch S_m is just in a conduction state. This time is the delay time for the auxiliary switch S_2 . The current through the resonant path is zero in this state. Both diodes are reversed biased in this mode. The source is connected to the load with the help of the main switch S_m . The equivalent circuit diagram for this mode is shown in **Figure 3D**. This mode ends at time $t = t_4$.

Mode 5: ($t_4 < t < t_5$)

In this mode the main switch S_m and auxiliary switch S_2 are turned ON. The equivalent circuit diagram showing the path of the current flows in this mode is shown in **Figure 3E**. S_m provides the conventional buck converter operation in the circuit. During this mode, the energy stored in the capacitor gets released in the closed loop followed by the auxiliary switch S_2 , diode D_2 , and resonant inductor L_r . When S_2 is turned on, the resonant capacitor C_r starts discharging due to the fall of current through the resonant inductor L_r . Diode D_2 becomes forward biased. Current flows through the resonant loop until the switch S_2 is turned off.

$$i_{L_r} = -\frac{V_{cr}(t_3)}{Z_r} \sin \omega_0 (t - t_3) \quad (13)$$

$$V_{cr}(t) = -V_{cr}(t_3) \cos \omega_0 (t - t_3) \quad (14)$$

Mode 6: ($t_5 < t < t_6$)

This mode starts at time t_5 when auxiliary switches S_1, S_2 are turned off. In this mode, only the main switch S_m is in a conduction state. The circuit in this mode acts as a conventional buck converter. The current loop consists of main switch S_m , output inductor L_o and capacitor C_o . Current through the load inductor L_o rises and provides constant output voltage through capacitor C_o . **Figure 3F** shows the equivalent circuit diagram in this mode.

$$i_{L_o} = L \frac{D(V_{in} - V_o)}{Dt} \quad (15)$$

Mode 7: ($t_6 < t < t_7$)

Figure 3G shows the equivalent circuit diagram of mode 7. This mode begins at $t = t_6$. As all the switches are in an off state in this mode. Output main inductor L_o provides energy to the circuit. The current flows through the output capacitor and two diodes D_1 and D_2 . This mode ends at time $t = t_7$ when S_1 is turned on. The equations of the current across the diodes in this mode are as follows:

$$I_{D1} = I_0; \quad I_{D2} = I_0 \quad (16)$$

Gain Analysis

The gain analysis of the converter is just similar to the conventional buck converter gain. The principle of the

TABLE 1 | Specifications of the proposed DC-DC converter.

Parameters	Values (V)
Input voltage V_{in}	300
Output voltage V_o	150
Output power P_o	500
Switching frequency f_s	100

inductor volt sec balance is used to determine the gain analysis of the converter. According to it, the average or dc component of the voltage applied across the inductor must be zero. When the main switch is closed the analysis for gain is described here.

$$(\Delta i_l)_{\text{closed}} + (\Delta i_l)_{\text{open}} = 0 \quad (17)$$

$$\frac{(V_s - V_o)}{L} DT_s + \frac{(-V_o)}{L} (1 - D)T_s = 0 \quad (18)$$

$$V_s D - V_o D - V_o + V_o D = 0 \quad (19)$$

$$V_s D - V_o = 0 \quad (20)$$

$$V_o = V_{in} D \quad (21)$$

The above equation describes the gain of the buck converter. From the equation, it is cleared that output voltage V_o depends upon the input voltage V_{in} and duty cycle D .

Duty Cycle Limitation

The output voltage of the buck converter depends upon the input voltage V_{in} and duty cycle D .

$$V_o = DV_{in} \quad (22)$$

Compared with the conventional buck converter, duty cycle D is ranging from 0 to 1. The D_{\min} for the auxiliary switch is 10% of D . So, the duty cycle range becomes

$$0.1 \leq D \leq 1 \quad (23)$$

As in the presented topology, the value of D cannot be zero so it leads toward a new duty cycle range from minimum value to 1.

$$0.1T_s \leq T_{\text{on}} \leq T_s \quad (24)$$

$$D_{\min} \leq D \leq 1 \quad (25)$$

The equation shows that the duty cycle value is ranging from its minimum value (0.1) to 1.

DESIGN AND IMPLEMENTATION

This section explains the designing and Implementation procedure of the proposed converter. The components used in the circuit implementation are selected on the basis of 500 W load operating at 150 V as listed in **Table 1**.

Referred to the data mentioned in **Table 1**, the basic parameters for the designing of the DC-DC converter are calculated here. It includes output current I_o , output resistor R_o , switching time period T_s . The value of the load resistor R_o of the DC-DC converter is calculated as:

$$R_o = \frac{V_o^2}{P_o} \quad (26)$$

$$R_o = \frac{(150)^2}{500} \quad (27)$$

$$R_o = 45 \Omega \quad (28)$$

The conventional buck converter has filter inductor L_o at the output side. It provides the continuous and smooth output current waveform at the output load terminal of the converter. The output inductor current is determined as:

$$I_o = \frac{P_o}{V_o} \quad (29)$$

$$I_o = \frac{500}{150} \quad (30)$$

$$I_o = 3.33 \text{ A} \quad (31)$$

From the given switching frequency, the total time period of the circuit can be found out. The time period and frequency are inversely proportional to each other. With the known information of one parameter, we can find out the value of the other.

$$T_s = \frac{1}{f_s} \quad (32)$$

$$f_s = 100 \text{ kHz} \quad (33)$$

$$T_s = \frac{1}{100 \times 10^3} \quad (34)$$

$$T_s = 10 \mu\text{s} \quad (35)$$

Design of the Converter

This section covers the designing of the parameters of DC-DC converter topology. The DC-DC converter with the ZVS technique is designed for a practical application of 500 W. The topology consists of two sub-circuits, the main and auxiliary circuit. The parameters to be designed in the main circuit includes the main inductor L_o and output capacitor C_o . The designing of the auxiliary circuit includes resonant inductor L_r and resonant capacitor C_r . The converter is operating in continuous conduction mode.

Determination of the Duty Cycle

The output voltage of the buck converter depends upon the input voltage V_{in} and duty cycle D .

$$V_o = DV_{in} \quad (36)$$

From the output and input voltage values the duty cycle of the circuit can be found as:

$$D = \frac{v_o}{v_{in}} = \frac{150}{300} \quad (37)$$

$$D = 0.5; \quad 50\% \quad (38)$$

Output Inductance L_o

The next step is to determine the size of the main inductor L_o of the converter. The inductor is a wire wrapped around the

ferromagnetic material known as the core. L_{min} is the minimum value of the inductor at which the converter operates for continuous conduction mode. In the design process, such value of the inductor should be chosen which is greater than the L_{min} .

$$L_{min} \geq \frac{(1-D)(R)}{2f} \quad (39)$$

$$L_{min} \geq \frac{(1-0.5)(45)}{(2 \times 100 \times 10^3)} \quad (40)$$

$$L_{min} \geq 112.5 \mu\text{H} \quad (41)$$

L_{min} is the minimum inductance value required for continuous current. For the converter's design, the value of inductor L_o should be greater than or equal to L_{min} . The value of inductor L_o depends upon the switching frequency, output and input voltages V_{in} and V_{out} , duty cycle D , and peak to peak variation in the inductor current. The formula of determination of inductor value L is:

$$L_o = \left(\frac{V_s - V_o}{\Delta i_L f} \right) D \quad (42)$$

Assume that Δi_L is 20% of load current.

$$\Delta i_L = 20\% \text{ of } I_o \quad (43)$$

$$\Delta i_L = \frac{20}{100} \times 3.33 = 0.66 \text{ A} \quad (44)$$

Putting this value in above equation.

$$L_o = \frac{(300 - 150)}{(0.66)(100K)} (0.5) \quad (45)$$

$$L_o = 1136 \mu\text{H} \quad (46)$$

The above equation describes the value of main inductance L_o for a specified peak to peak inductor current for continuous-current operation of the converter.

Output Capacitance C_o

The value of output capacitance C_o can be found out by the following formula.

$$C_o = \frac{1-D}{8L \left(\frac{\Delta V_o}{V_o} \right) f^2} \quad (47)$$

Assume that ΔV_o is 0.1% of V_o , where ΔV_o is the output voltage ripples then, the value of output capacitor is calculated as:

Putting the value of $\frac{\Delta V_o}{V_o}$ in C_o equation.

$$C_o = 8.2 \mu\text{F} \quad (48)$$

The above equation shows the values of output capacitor C_o to be used in the converter. Capacitor C_o provides the continuous output voltage value. The high value of capacitance minimizes the output voltage ripples.

Resonant Inductor L_r and Capacitor C_r

The selection of resonant capacitance C_r and inductance L_r is the most important step in the designing of the power converter. As, both the auxiliary switches turned on for a time of less than 1 μs

so, from total time $T_s = 10 \mu\text{s}$, assume that 10% of the total is dedicated to two auxiliary switches.

$$\frac{T_r}{2} \leq 1 \mu\text{s} \quad (49)$$

$$\omega = \frac{1}{\sqrt{L_r C_r}}; \quad \omega = 2\pi f_r \quad (50)$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (51)$$

$$\frac{T_r}{2} \leq \frac{2\pi\sqrt{L_r C_r}}{2} \leq 1 \mu\text{s} \quad (52)$$

$$\pi\sqrt{L_r C_r} \leq 1 \mu\text{s} \quad (53)$$

$$\sqrt{L_r C_r} \leq \frac{1\mu}{3.14} \quad (54)$$

In the above equation, assume the value of resonant capacitor $C_r = 10 \text{ nF}$ and, simplifying the above equation, the value of resonant inductor L_r can be found.

$$L_r \leq 10 \mu\text{H} \quad (55)$$

Equation (56) defines the range of values for the resonant inductor. By adjusting the values of resonant inductor and capacitor values the required behavior of the resonant current can be achieved. From the above values of the resonant inductor L_r and resonant capacitor C_r , resonant frequency f_r of the auxiliary circuit can be found as:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (56)$$

$$f_r = \frac{1}{2\pi\sqrt{(2\mu)(10\text{n})}} = 1 \text{ MHz} \quad (57)$$

f_r can also be found through using the relationship with the switching frequency f_s .

$$\frac{T_r}{2} = 0.1 T_s \quad (58)$$

$$\frac{1}{2f_r} = \frac{0.1}{f_s} \quad (59)$$

$$f_r = \frac{f_s}{0.2} \quad (60)$$

$$f_r = \frac{100 \times 10^3}{0.2}; \quad f_r = 500 \text{ kHz} \quad (61)$$

The impedance of the auxiliary circuit Z_r , can also be found as.

$$z_r = \sqrt{\frac{L_r}{C_r}} \quad (62)$$

By putting values:

$$z_r = \sqrt{\frac{2 \times 10^{-6}}{10 \times 10^{-9}}}; \quad z_r = 14.14 \quad (63)$$

Power Loss Analysis

In the proposed converter, due to zero voltage switching during the transition state of the switches, switching losses goes to zero,

as the drain to the source voltage of the main switch S_m is zero in this converter. So, power loss across the switch goes to zero. Dynamic losses across the switch are zero. But static losses exist due to the resistance factor.

Power losses across the switch can be calculated as,

$$P = \frac{V_{ds}^2}{R_{don}} \quad (64)$$

where p = power, V_{ds} = drain to source voltage, R_{don} = Static drain to source on resistance.

From the datasheet of used MOSFET in the designing of converter the value of R_{don} is found as 0.55Ω . As V_{ds} is zero at the transition state of the switch so, power loss across the switch goes to zero. Thus, verifying zero voltage characteristics of the converter.

SIMULATION RESULTS

The simulation results of the soft-switching topology are discussed in this section. The ZVS operation of the PWM Buck converter can be verified with a voltage waveform across the main switch. The circuit diagram of the proposed converter which was presented in the previous section is simulated in PSPICE. In **Figure 4** the software simulated circuit is shown.

The results verify the gain analysis of the step-down converter. It also verifies the ZVS characteristics of the proposed topology. The simulation results of current and voltage of resonant components, main inductor current, main capacitor voltages, and diode currents are also discussed in this section.

The simulated converter is 500 W with an input voltage of 300 V. The switching frequency is 100 kHz.

Voltage Gain Analysis

Figure 5 is the output voltage simulated result graph operating with a 50% duty cycle. It can be seen in the figure that it has two plots in it. Blue colored waveform shows the plot for an input voltage of 300 V. The output voltage plot verifies the derived relation from **Eq (22)** which is 150 V is shown with pink colored waveform. Switching frequency directly affects the output voltage. Changing the switching frequency effects D thus result in a change of the output voltage.

Gate Signals of the Power Switches

Gate signals provided to the converter are shown in **Figure 6**.

Gate pulses are fed as input to the half-bridge inverter switches and the main switch at the gate to the source terminal of the switches. The Pulse Width Modulation technique is used to control the load voltage. The converter is operating with a 50% duty cycle. In the presented topology, three power switches are used. One main switch and two auxiliary switches. Gate signals are provided to the switches for controlling their on/off states. A V pulse is used in the circuit for pulse generation in PSPICE. It involves different parameters that need to be set for the required output. Before the on state of the main switch, S_l of the auxiliary circuit gets turned on. S_m

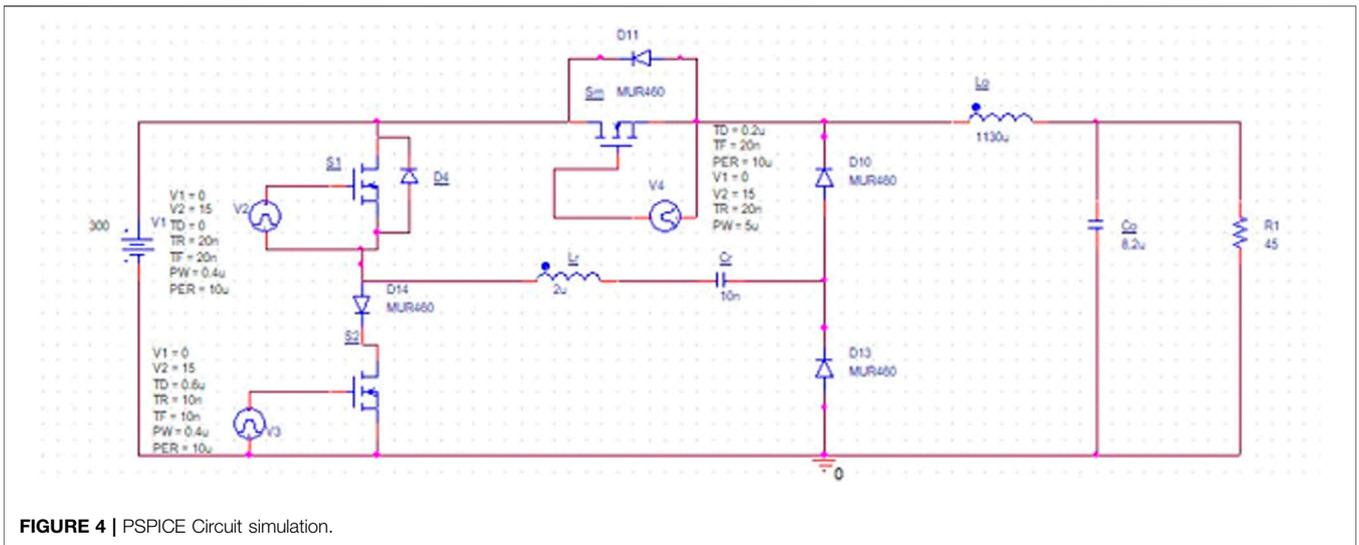


FIGURE 4 | PSPICE Circuit simulation.

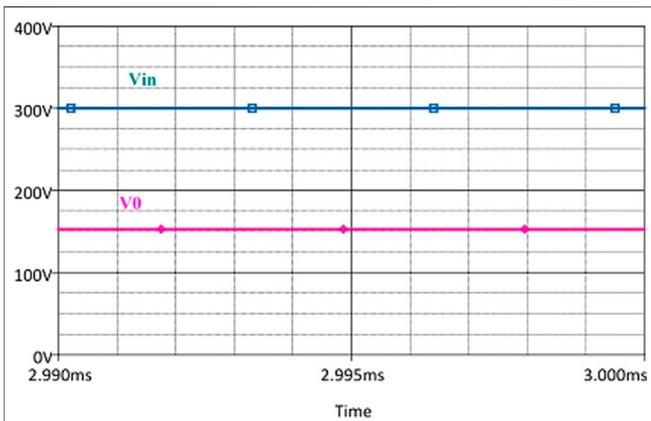


FIGURE 5 | Input and Output Voltage Waveform of Converter. simulation result verifies the operation of the buck converter with the magnitude less than the input voltage. It converts 300–150 V.

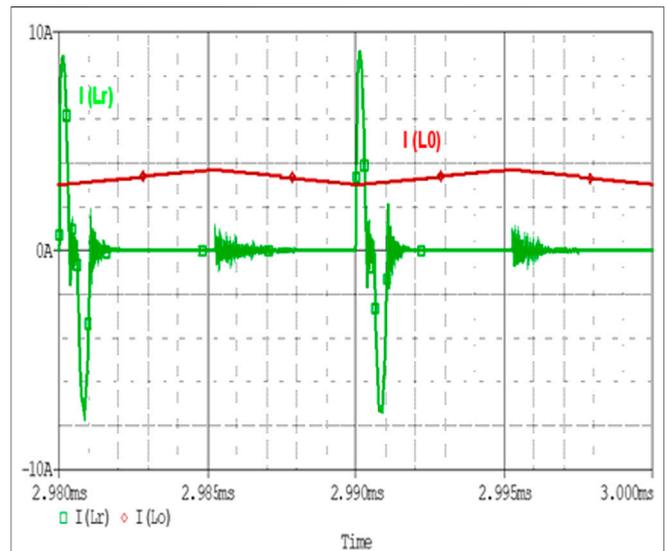


FIGURE 7 | Current waveform of I_{Lr} and I_o .

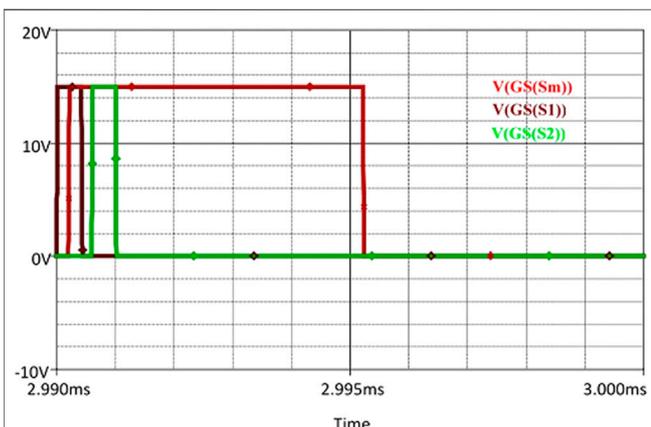


FIGURE 6 | Gate Signals of Power Switches used in Converter.

turned on with a delay of 0.2 μ s. In **Figure 6**, Maron colored waveform is the gate pulse for S_1 . After a delay of 0.6 μ s, the auxiliary switch S_2 gets turned on. It is shown as a green-colored waveform. Both the auxiliary switch remains turned on for 2 μ s. The red-colored waveform is the gate pulse of the main switch S_m . It remains turned on for 5 μ s. The duty cycle of the converter will remain the same throughout the operation of the converter for the respective value of input and load voltage.

Analysis of the Currents of Resonant I_{Lr} and Main Inductor I_o

The simulation waveform for the resonant inductor current I_{Lr} and the main inductor current I_o is illustrated in **Figure 7**.

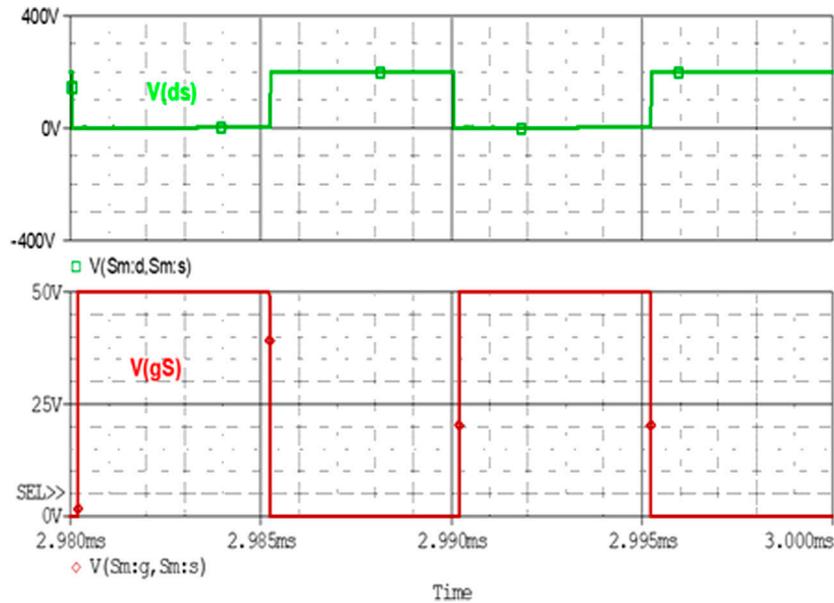


FIGURE 8 | Zero voltage switching graph.

From **Figure 7**, the behavior of resonant inductor current can be seen as sinusoidal in nature. While the DC current flows through L_o . **Equation (65)** describes the average dc current through the main inductor which is also the output current of the converter.

$$I_0 = 3.33 \text{ A} \quad (65)$$

I_{Lr} flows through the auxiliary circuit. The behavior of I_{Lr} can be explained through two cycles. In positive half cycle switch S_1 gets turned on, I_{Lr} rises linearly from 0 to peak value. Both I_{Lr} and I_o become equal at $I_o = 3 \text{ A}$. After this zero crossing, the main diode D_m gets turned on. During this interval, the main switch S_m can be made to turn on in that portion at any time before the second crossing of both currents. This enables the ZVS of the converter across the main switch. After the second crossing of both currents again I_{Lr} becomes less than I_o . When I_{Lr} reaches zero it stops the flow of current.

$$I_{Lr}(\text{peak}) = 9 \text{ A} \quad (66)$$

$$I_{Lr}(\text{rms}) = 2.148 \text{ A} \quad (67)$$

In the negative half cycle, as shown in the above waveform, I_{Lr} flows through the resonant tank followed by the D_2 , S_2 , and resonant capacitor. The peak and rms value of the resonant current is described in **Equations (66)** and **(67)**. The Resonant Inductor current has its peak value in the case of a negative half cycle of -7 A .

As the resonant inductor current waveform is sinusoidal in nature, the total area of the waveform remains the same in both the cycles. In the first half cycle, the waveform is steeper and narrower. In comparison with the negative half cycle, the waveform is wider with a low peak. According to the volt sec balance of inductor, the area under the curve in both half cycles

must be equal. **Figure 8** is in accordance with the volt sec balance of the inductor.

The ringing effects shown in the waveform of **Figure 8** are unwanted parts. These are due to parasitic effects. Due to the reverse recovery effects of diodes, these portions emerge in the waveform. These unwanted effects can be removed by using the best quality diodes and components in hardware implementation. In software designing, the converters face this type of problem.

Analysis of Zero Voltage Switching Operation of the Converter

Achievement of zero voltage switching is the focus of this topology. It can be viewed and verified in **Figure 9**. As for ZVS operation, the most necessary parameter is that the drain to source voltage V_{DS} should be zero across the switch before the gate pulse is applied. So, **Figure 9** verifies this operation by seeing that when the gate pulse is applied across the main switch S_m , V_{DS} is zero across the switch. In the above diagram, the green-colored waveform shows the V_{DS} across the main switch. During the positive half cycle when i_{Lr} becomes equal to I_o , then i_{Lr} flows through the body diode D_m of main switch S_m . It makes diode D_m forward biased. **Figure 10** shows the current across the main diode.

Analysis of Zero Voltage Switching Operation of the Converter

As shown in **Figure 8**, the combined effect of the main inductor current and resonant inductor current flows across the body diode of the main switch. It has a peak value of 5.283 A .

When the current through diode D_m goes to zero then V_{DS} also reaches zero. Switch S_m becomes active through gate pulse V_{GS}

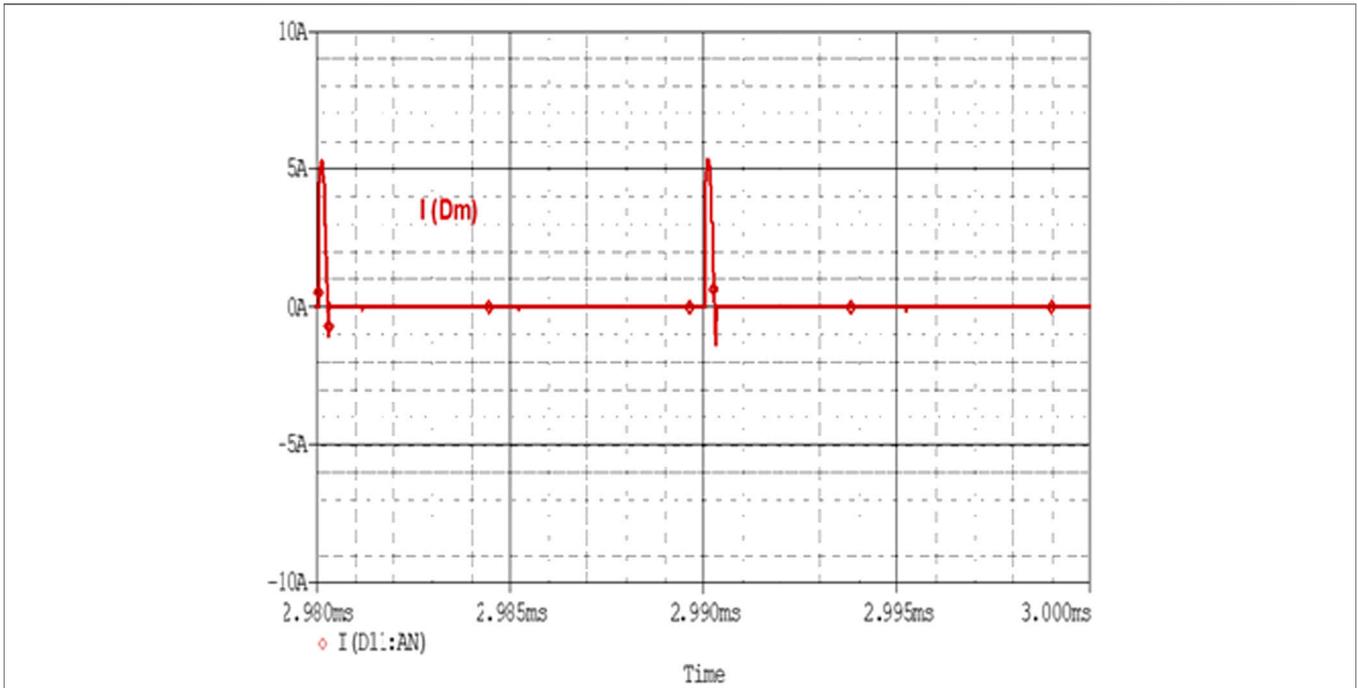


FIGURE 9 | Current through the body diode of the main switch.

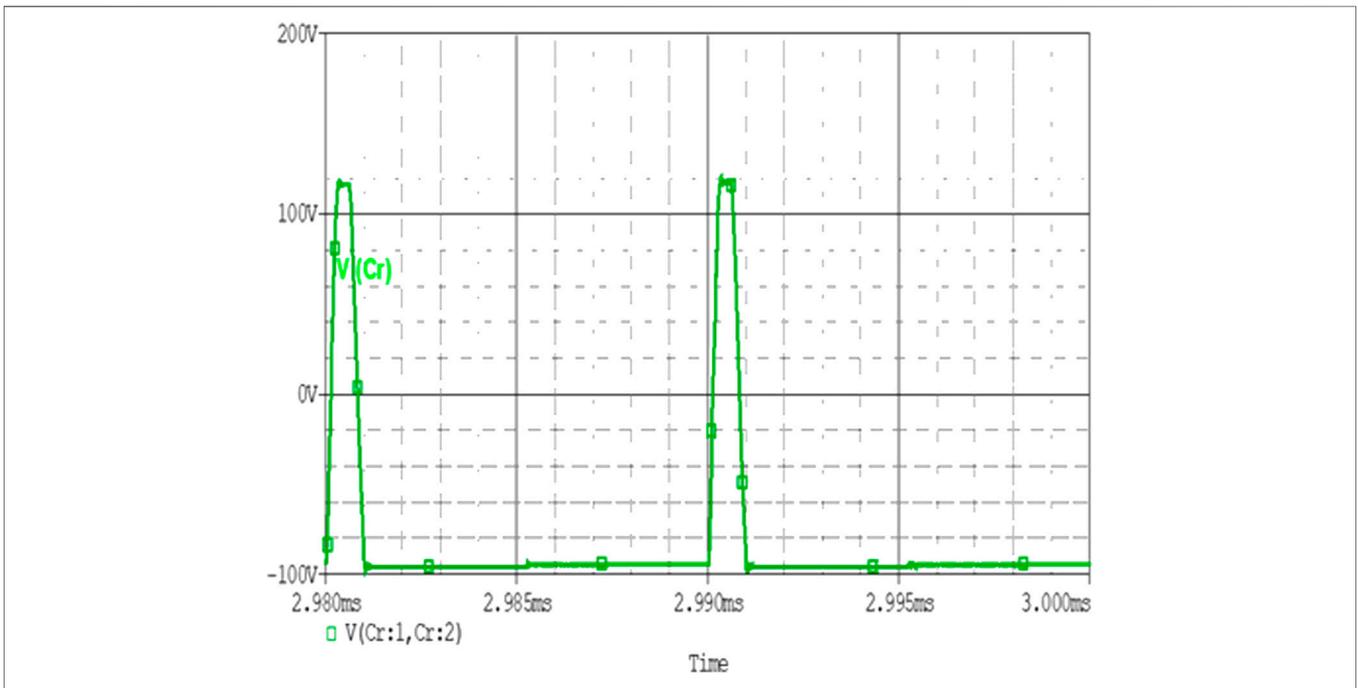


FIGURE 10 | Voltage waveform across the resonant capacitor.

with no power loss across the switch. The nature of I_{Dm} is also sinusoidal as iL_r flows across it.

$$I_{Dm} = 4.156 \text{ A} \tag{68}$$

Conventionally, power is absorbed across the switching devices during their turn on or turn off time. This is due to the fact that current or voltages across it is non-zero during the transition. These transitions occurred rapidly when working with

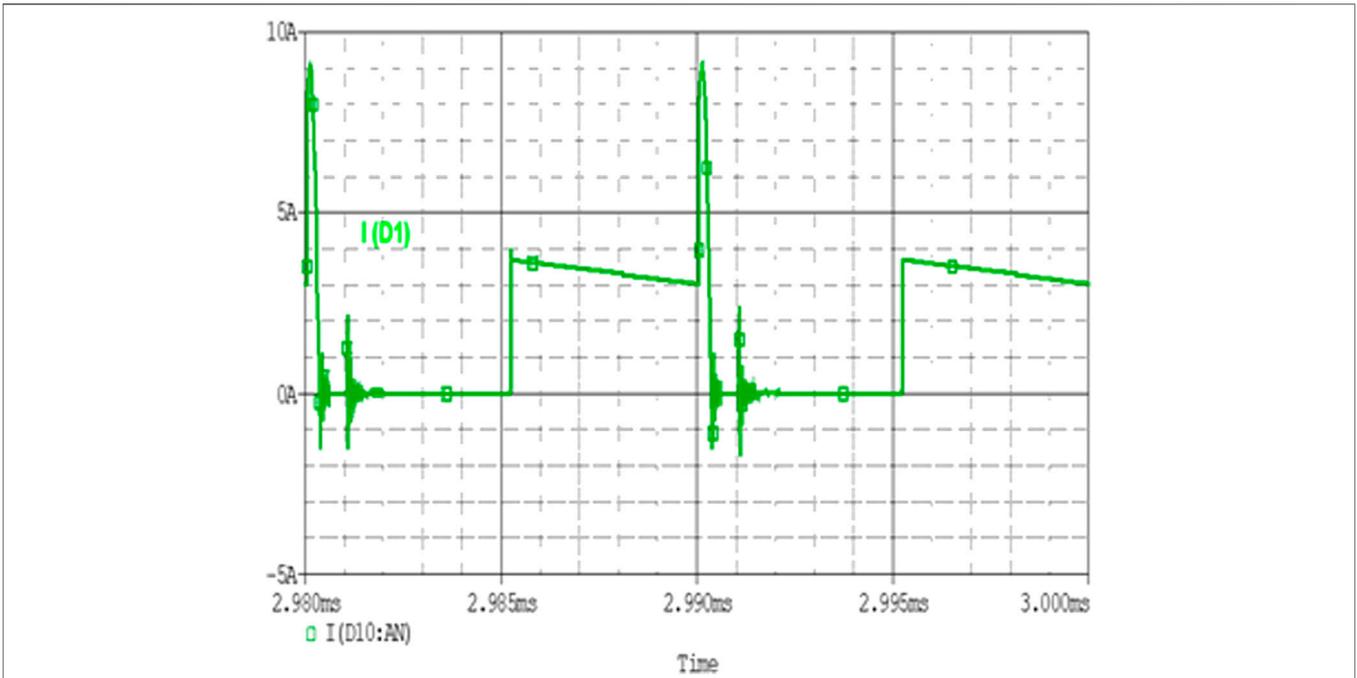


FIGURE 11 | Diode D_1 Current Waveform. When S_2 turned on then diode D_1 gets reversed biased and D_2 gets forward biased. **Figure 12** shows the current through diode D_2 .

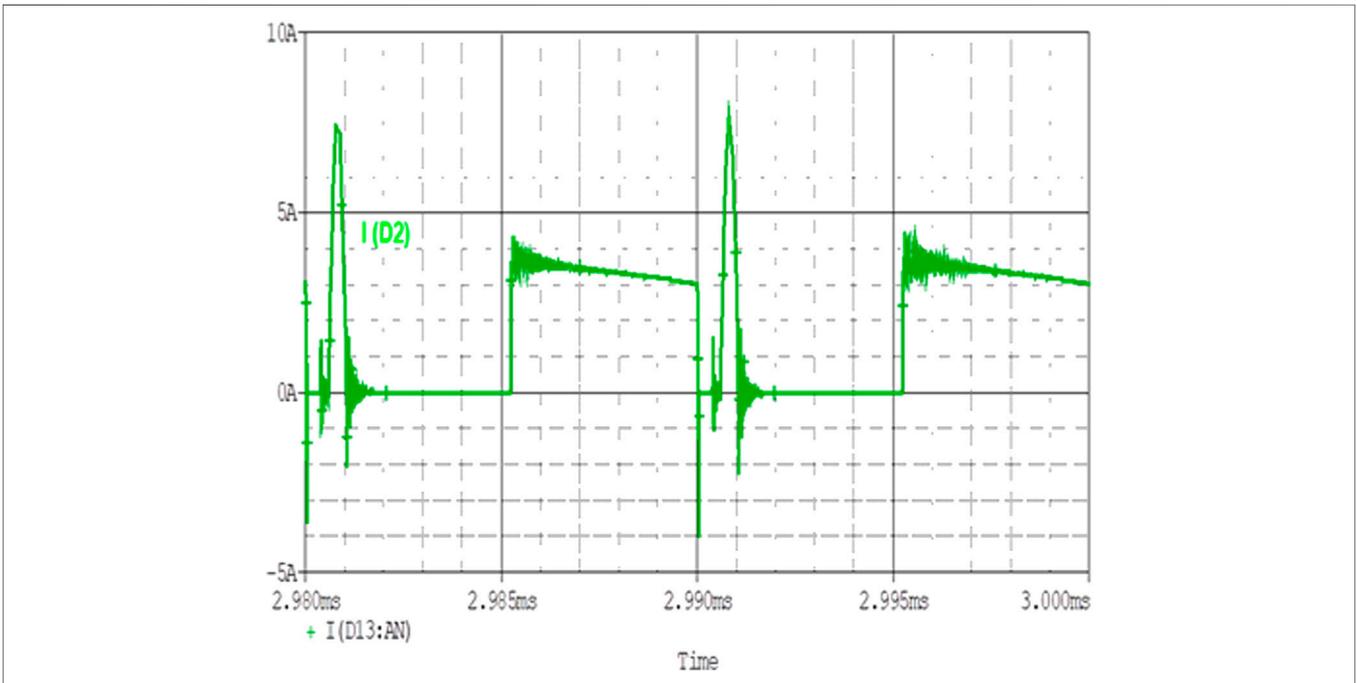
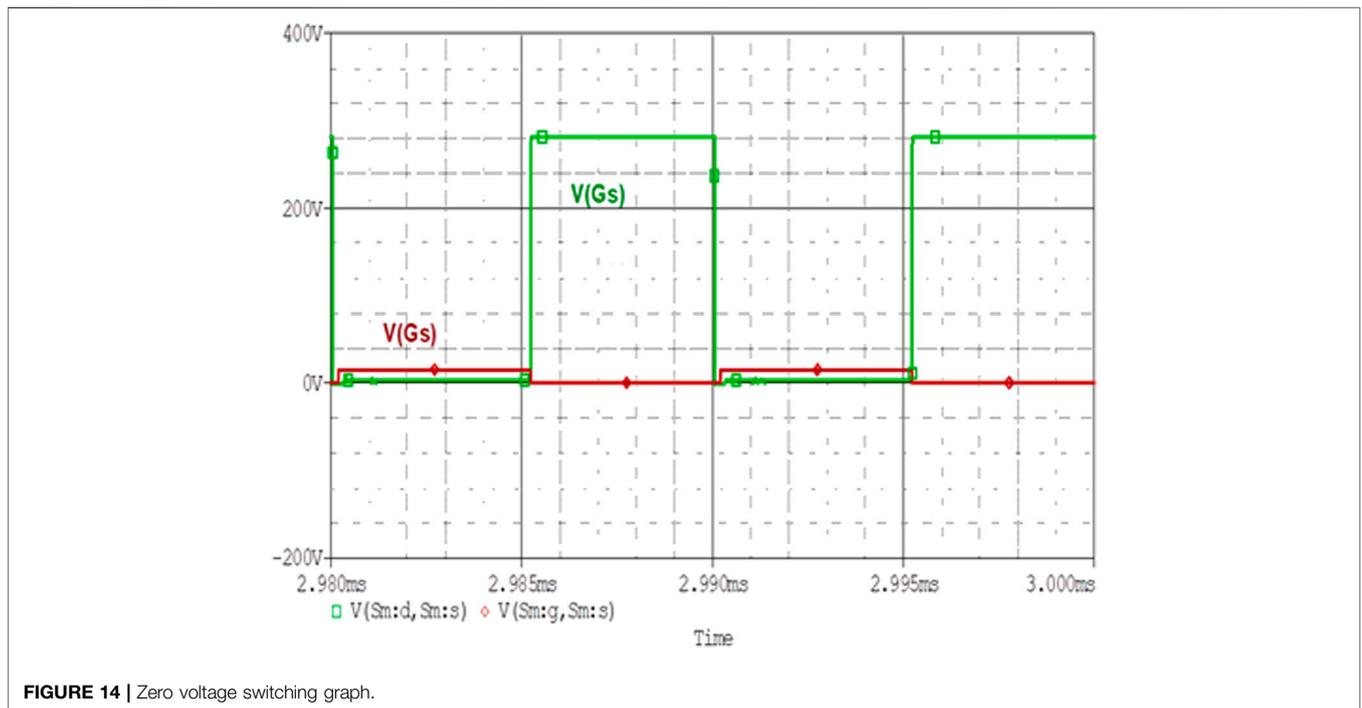
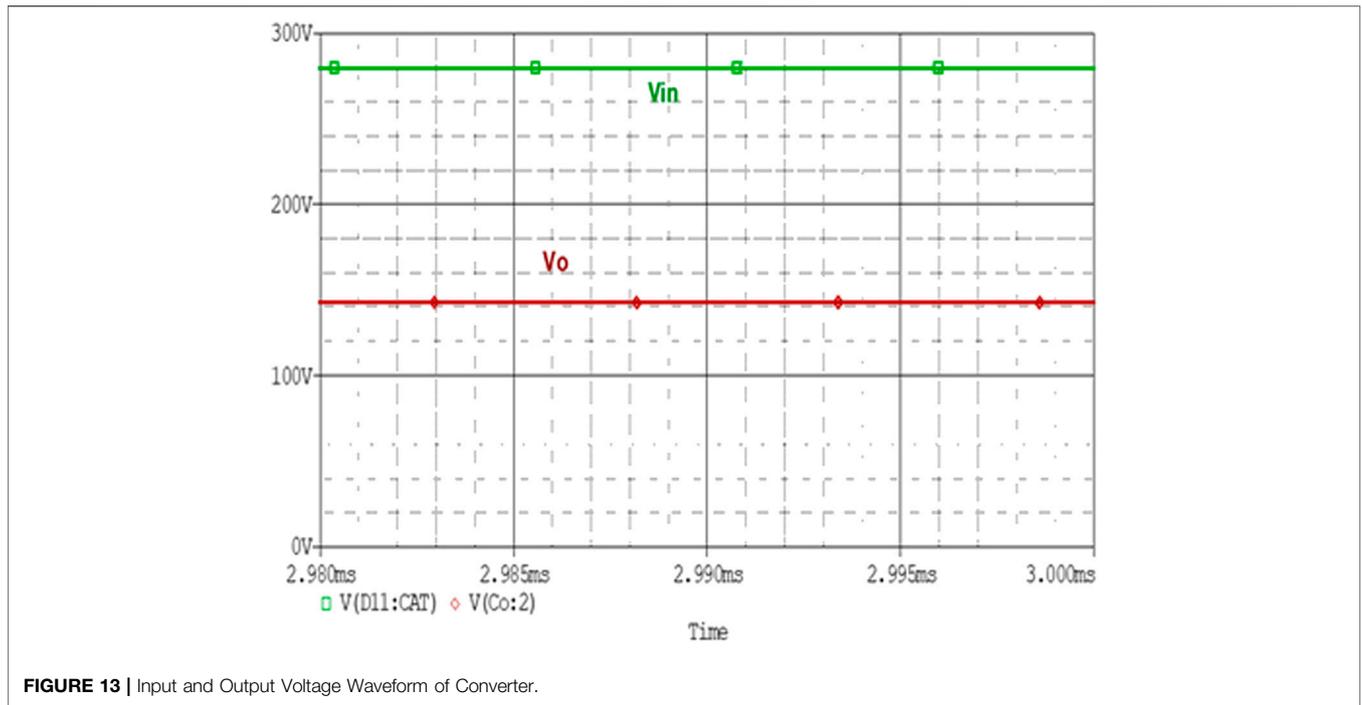


FIGURE 12 | Diode D_2 current Waveform.

high frequency. To eliminate these losses resonant converters are used. They provide soft-switching across the switches during their transition. During turn on/turn off the switches, voltage, and

current become zero. It results in zero power absorption across the switches. In ZVS operation when the switch gets turned on, the voltage across the switch reaches zero. Thus, ensuring zero



power loss. From the given waveforms, it can be clearly verified that the proposed converter ensures zero voltage switching.

Analysis of Resonant Capacitor Voltage V_{Cr}

The analysis of the behavior of voltage across the resonant capacitor is explained in this section. In the resonant tank, the

capacitor and inductor both are in series. The waveform of voltage across the capacitor is shown in **Figure 10**. The resonant inductor current I_{Lr} affects the behavior of voltage across the resonant capacitor C_r . In the positive half cycle of the sinusoidal current waveform, when the resonant inductor current I_{Lr} rises linearly, the positive voltage builds up across the capacitor. The capacitor

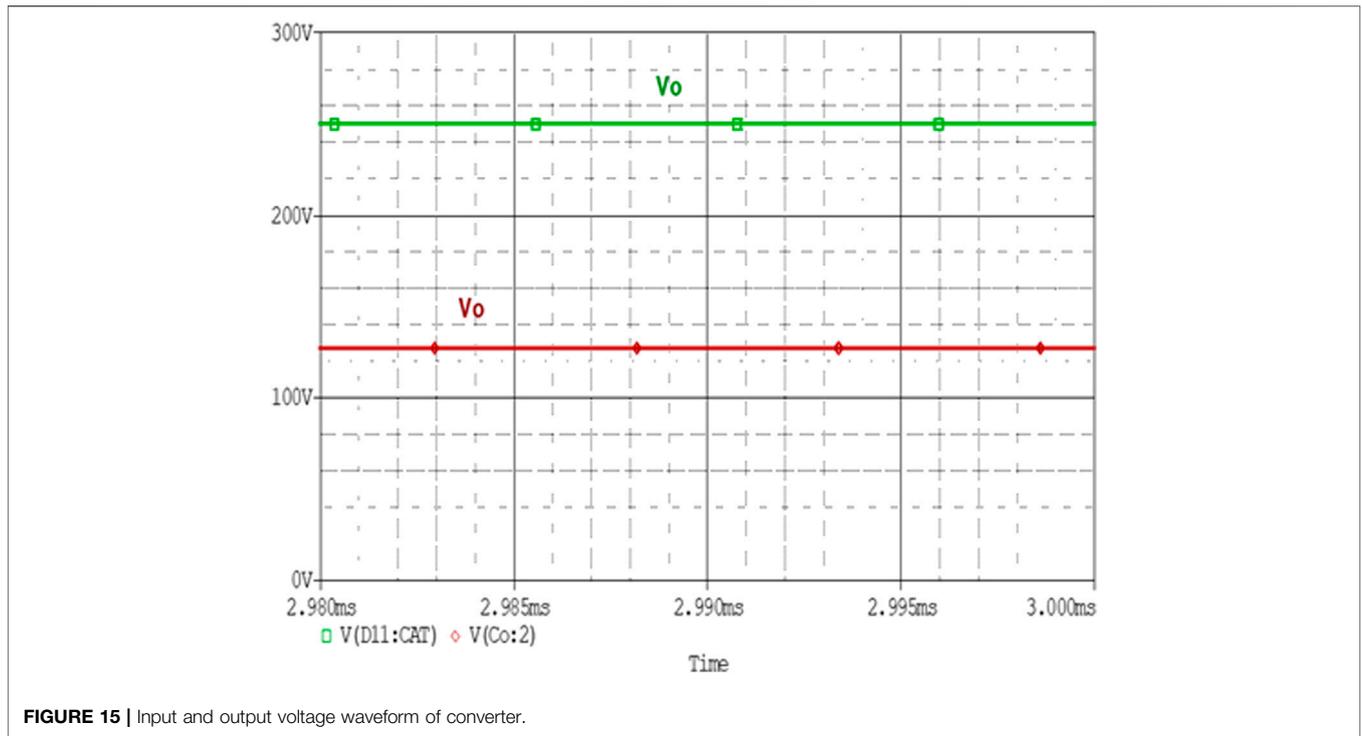


FIGURE 15 | Input and output voltage waveform of converter.

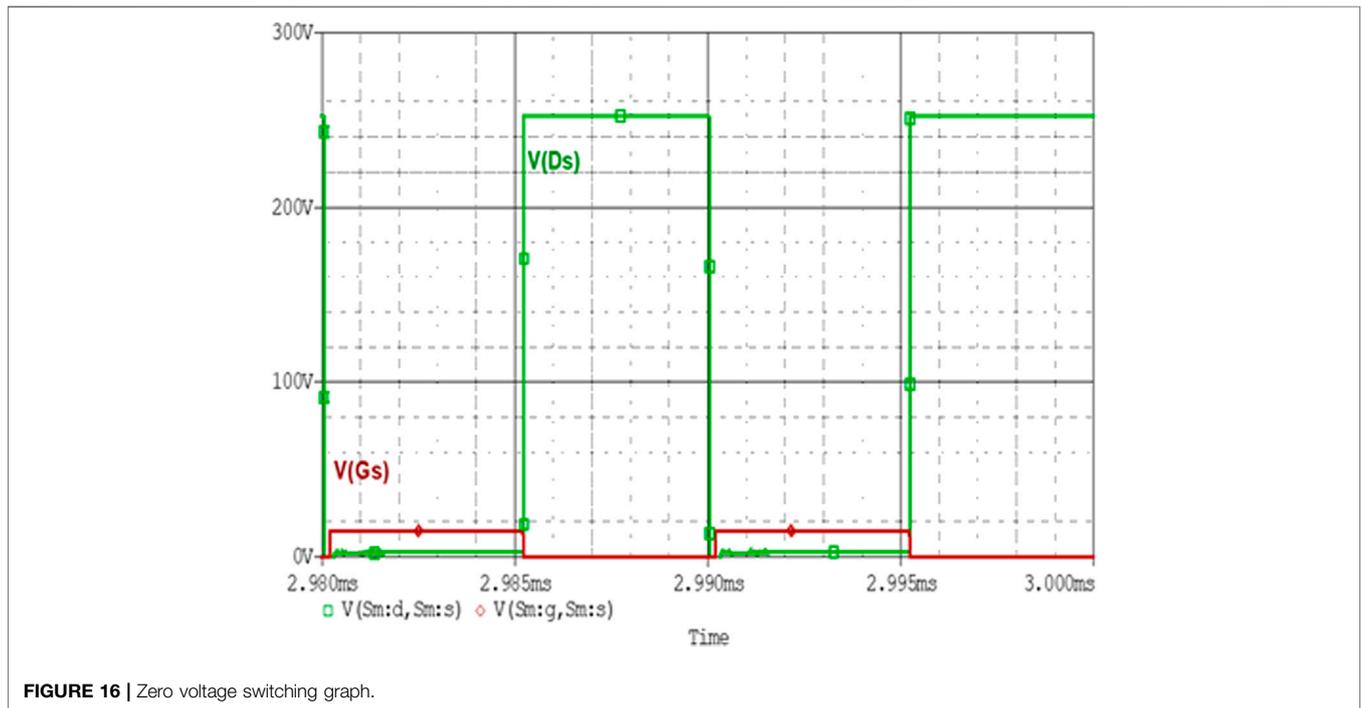


FIGURE 16 | Zero voltage switching graph.

voltages start building up from the previous value that is from -98 A. Voltages go on increasing until its peak value 118 V. Until this point, the resonant inductor current falls down to zero due to the turned off state of S_1 . The capacitor goes on to a steady state for the shortest time period of delay for S_2 .

As soon as S_2 is turned on, the capacitor starts releasing energy to the auxiliary circuit thus at the turned-off time of S_2 , all the energy gets released thus flowing current in the closed loop. The capacitor voltage increases until I_{Lr} flows through it. As soon as I_{Lr} becomes less than I_o the resonant current stops flowing the

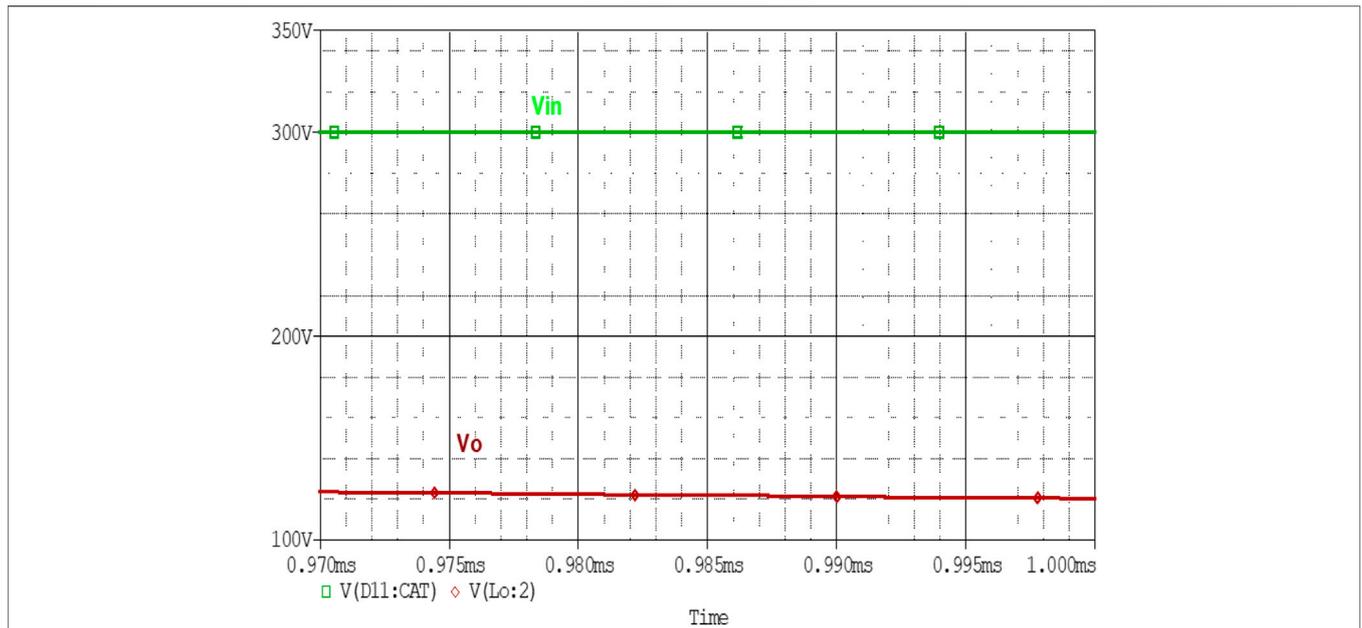


FIGURE 17 | Input and output voltage waveform of converter.

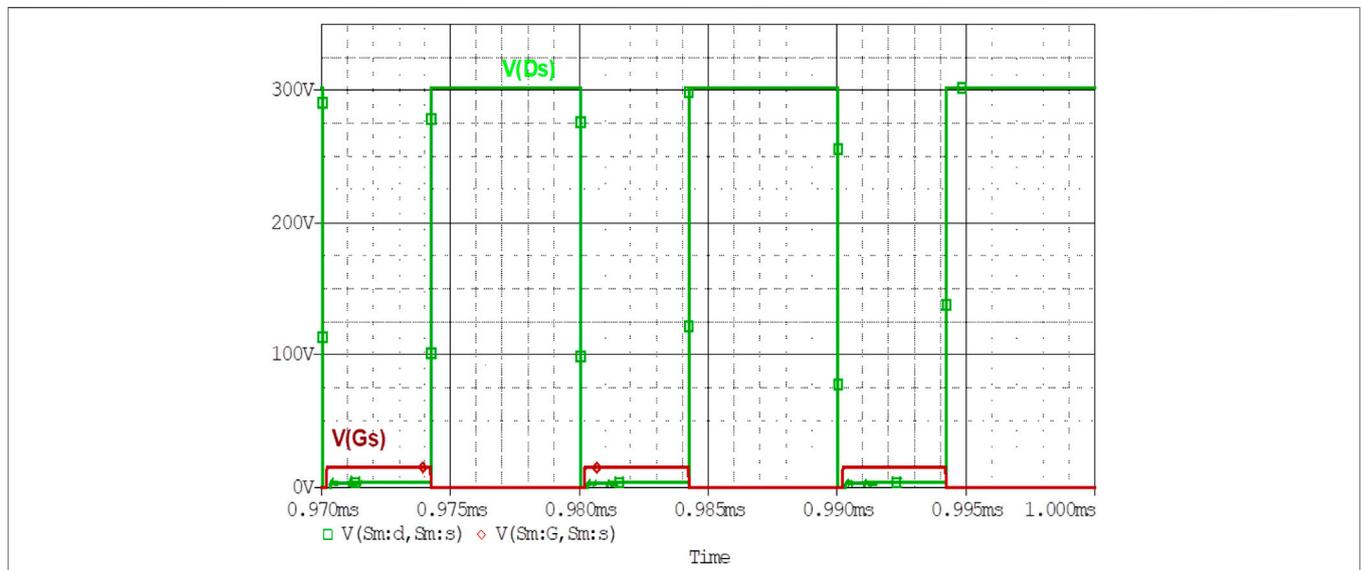


FIGURE 18 | Zero voltage switching graph.

loop. At that point, the capacitor voltage reaches its maximum value.

In the negative half cycle of the resonant current, the capacitor acts as a source releasing its energy in this loop. When I_{Lr} reaches zero crossing the capacitor discharges at its negative maximum value and goes to a steady state.

Analysis of Current Across Diode D_1 and D_2

The waveform of the current across the diode D_1 and D_2 are shown in Figures 11 and 12. The currents across diodes D_1 and

D_2 are explained in accordance with the resonant and main inductor current. When all switches are turned off, I_o is greater than I_{Lr} so, I_o flow through diodes D_1 and D_2 . At this time 3.072 A current flows across both diodes.

When S_1 is turned on, I_{Lr} rises linearly. After the point when I_o and I_{Lr} become equal, I_{Lr} flows through the diode D_1 . D_2 is reversed biased. Peak and rms values of current flowing through diode are described in Eq (69).

$$I_{D1} (peak) = 7.26A, \quad I_{D1} (rms) = 3.65 A \quad (69)$$

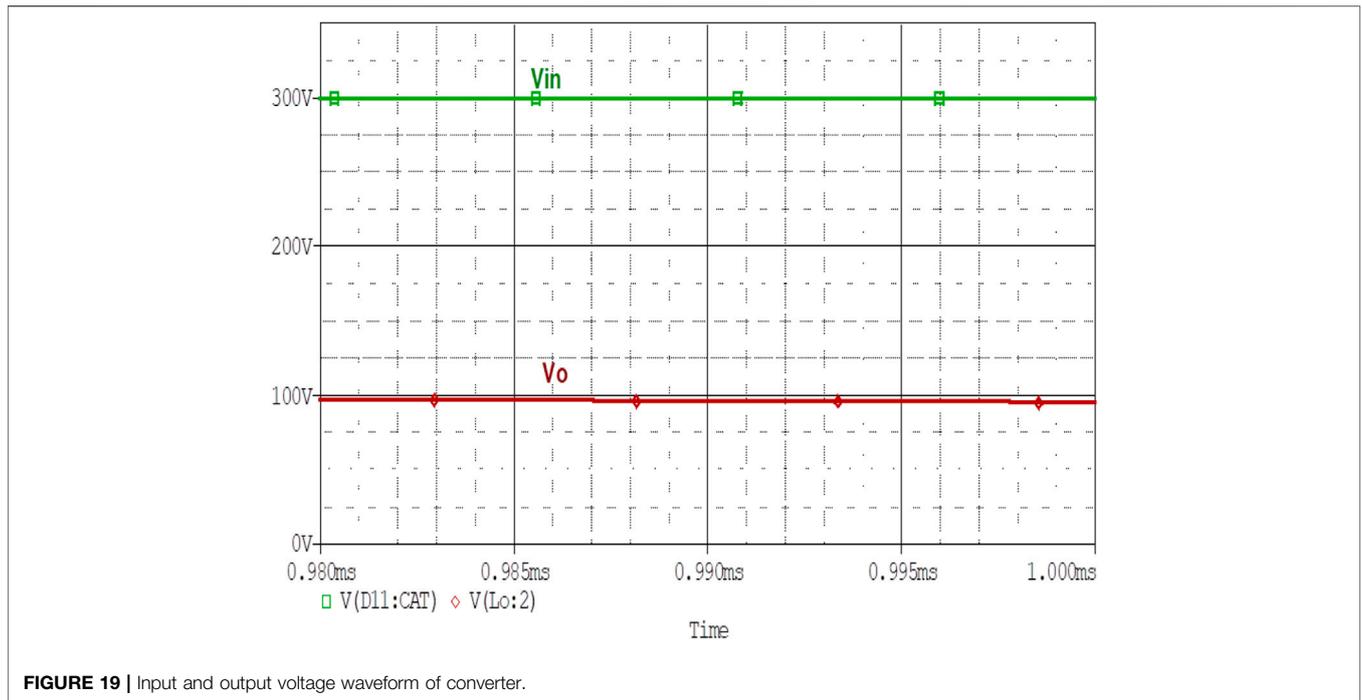


FIGURE 19 | Input and output voltage waveform of converter.

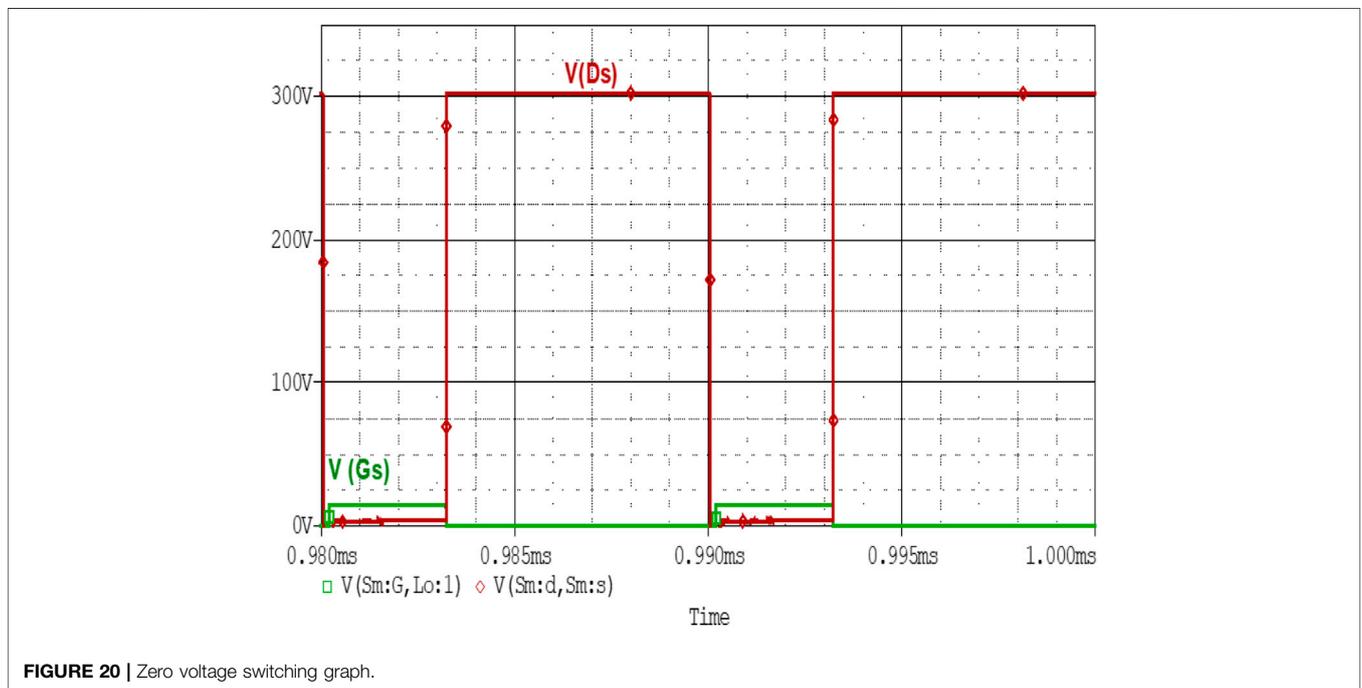


FIGURE 20 | Zero voltage switching graph.

I_{Lr} flows through the diode D_2 , which has a peak value of 7.5 A. The nature of the waveform is sinusoidal with just a positive cycle. It has an rms value of 3.6640 A.

When all switches get turned off, then output inductor L_o releases energy in the form of current I_o . Diodes D_1 and D_2 provide a path to the current. At this time average current of 3.57 A flows through both diodes. So, during the conduction period of switches I_{Lr} flows through diodes, and during the off period, I_o flows through diodes.

Analysis of Zero Voltage Switching for Different Input and Output Values

The topology is efficient and provides zero voltage switching for different values of input and output voltage. Here is the analysis of ZVS achievement for different values. More results in Figures 13–20 are presented in this section with the help of simulated waveforms.

TABLE 2 | Result comparison of proposed topology with previous circuits.

Parameters	An improved ZVS-PWM buck converter with ZCS auxiliary circuit (Kumar et al., 2017)	A low stress ZCS technique for power converter (Shao et al., 2017)	An efficient ZVS synchronous buck converter (Marvi et al., 2016)	Proposed ZVS buck converter
Switching frequency	20 kHz	200 kHz	100 kHz	100 kHz
V_{in}	24 V	300 V	12 V	300 V
V_{out}	12.6 V	200 V	1 V	150 V
Power	35 W	2 KW	20 W	500 W
Duty cycle	50%	60%	50%	50%
Modes of operation	7	10	6	7
Features	ZVS and ZCS	ZCS	ZVS	ZVS
Size	Large	Small	Large	Small
Cost	High	Low	High	High
Magnetizing inductor	No	No	4	No
Controlled switches	2	2	4	3
No. of resonant components	2	2	No	2
No. of diode	4	4	4	3
Overall components	13	10	15	10

ZVS for $V_{in} = 280$ V, $V_{out} = 140$ V, $D = 50\%$

The converter provides ZVS for the above values too. The figure describes the ZVS achievement of the converter for these values with a duty cycle of 50%.

ZVS for $V_{in} = 250$ V, $V_{out} = 125$ V, $D = 50\%$

ZVS for $V_{in} = 300$ V, $V_{out} = 120$ V, $D = 40\%$

ZVS for $V_{in} = 300$ V, $V_{out} = 100$ V, $D = 33\%$

The above simulated results clearly verify the achievement of ZVS for different input-output voltage values and duty cycles. It can be seen that in all cases the circuit provides zero voltage switching. It provides zero switching losses across the switch during the transition state.

A comparison of the proposed research topology can be clearly illustrated from **Table 2**.

CONCLUSION

A novel ZVS based DC–DC converter with an auxiliary circuit has been proposed in this work. The proposed converter encounters the hard-switching problems of the conventional converter during its transition modes. To keep away the dynamic power losses across solid-state devices an auxiliary circuit consists of MOSFET and resonant components is incorporated with the conventional buck converter. Keeping in view for the application of the 500 W system the parameters and components have been designed optimally. The verification of the design has been made in PSPICE/ORCAD. The novel

REFERENCES

Babaei, E., and Saadatizadeh, Z. (2019). A new interleaved high voltage gain bidirectional buck-boost DC/DC converter with capability of zero voltage

topology is simulated with voltage ratings 300/150 V, a duty cycle of 50%, and 100 kHz frequency. ZVS across the main switch S_m has been achieved during the transition mode of the converter and is shown graphically. Thus, the converter provides zero voltage switching for high voltage ratings. The reduction of stresses in the research work is shown graphically with the help of zero voltage switching waveform across main switch S_m .

In the future this work can be extended to be designed for electric vehicles to interface the elements for a power train. As the converter works for high voltage ratings, it can also be implemented in dc motor drives of electric vehicles.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

AUTHOR CONTRIBUTIONS

All authors listed have made a substantial, direct and intellectual contribution to the work, and approved it for publication.

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switching. *Elec. Power Compon. Syst.* 47 (13), 1180–1195. doi:10.1080/15325008.2018.1472151

Batista, F. A., Petry, C. A., Santos, E. L., and Almeida, B. R. (2009). September). Didactic system for digital control of power electronics applications. in 2009 Brazilian Power Electronics Conference.

- Bonito-Mato Grosso do Sul, 2009, IEEE, 1093–1098. doi:10.1109/COBEP.2009.5347672
- Bose, B. (2010). Global warming: energy, environmental pollution, and the impact of power electronics. *EEE Ind. Electron. Mag.* 4 (01), 6–17. doi:10.1109/mie.2010.935860
- Brodady, G. R., Nascimento, C. B., Lopes, L. A., and Agostini, E. (2016, November). Analysis and simulation of a buck-boost operation in a bidirectional ZVS DC-DC converter. In 2016 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), Toulouse, 2016, IEEE, 1–7. doi:10.1109/ESARS-ITEC.2016.7841431
- Chauhan, S., and Pandey, A. K. (2017, March). Simulation of ZVS buck converter for charging application using PSIM simulator. In 2017 International Conference on Computation of Power. Melmaruvathur, 2017, Energy Information and Communication (ICCPEIC) IEEE, 809–814. doi:10.1109/ICCPEIC.2017.8290478
- Do, H.-L. (2011). Nonisolated bidirectional zero-voltage-switching DC-DC converter. *IEEE Trans. Power Electron.* 26 (09), 2563–2569. doi:10.1109/tpe.2011.2111387
- Hussain, A., Akhtar, R., Ali, B., Awan, S. E., and Iqbal, S. (2019). A novel bidirectional DC-DC converter with low stress and low magnitude ripples for stand-alone photovoltaic power systems. *Energies* 12 (15), 2884. doi:10.3390/en12152884
- Kanamarlapudi, V. R. K., Wang, B., Kandasamy, N. K., and So, P. L. (2017). A new ZVS full-bridge dc-dc converter for battery charging with reduced losses over full-load range. *IEEE Trans. Ind. Appl.* 54 (1), 571–579.
- Kim, J. W., Park, M. H., Han, J. K., Lee, M., and Lai, J. S. (2019). PWM resonant converter with asymmetric modulation for ZVS active voltage doubler rectifier and forced half resonance in PV application. *IEEE Trans. Power Electron.* 35 (01), 508–521.
- Kollimala, S. K., Mishra, M. K., and Narasamma, N. L. (2014). Design and analysis of novel control strategy for battery and supercapacitor storage system. *IEEE Trans. Sustain. Energy* 5 (04), 1137–1144. doi:10.1109/tste.2014.2336896
- Kumar, M., Pattnaik, M., and Mishra, J. (2017, November). An improved ZVS-PWM buck converter with ZCS auxiliary circuit. In TENCON 2017-2017 IEEE Region 10 Conference, Penang, 2017, IEEE, 1279–1284. doi:10.1109/TENCON.2017.8228054
- Lakshminarasamma, N., and Ramanarayanan, V. (2007). A family of auxiliary switch ZVS-PWM DC-DC converters with coupled inductor. *IEEE Trans. Power Electron.* 22 (05), 2008–2017. doi:10.1109/tpe.2007.904225
- Lin, B.-R. (2020). Analysis and implementation of a phase-shift pulse-width modulation converter with auxiliary winding turns. *Energies* 13 (01), 222. doi:10.3390/en13010222
- Lin, B. R., Chen, J. J., Huang, C. L., and Chiang, H. K. (2008). Analysis of integrated Buck-flyback ZVS converter. In 2008 3rd IEEE Conference on Industrial Electronics and Applications, Singapore, 2008, IEEE, 388–393. doi:10.1109/ICIEA.2008.4582545
- Marchesoni, M., and Vacca, C. (2007). New DC-DC converter for energy storage system interfacing in fuel cell hybrid electric vehicles. *IEEE Trans. Power Electron.* 22 (01), 301–308. doi:10.1109/tpe.2006.886650
- Mariikkannan, A., Manikandan, B. V., and Kumar, M. (2019). ZVS asymmetrical PWM full-bridge high voltage gain DC-DC converter controlled by ANFIS for energy harvesting applications. *Journal of Control Engineering and Applied Informatics* 21 (04), 51–58.
- Martinez, C. M., Hu, X., Cao, D., Velenis, E., Gao, B., and Wellers, M. (2016). Energy management in plug-in hybrid electric vehicles: recent progress and a connected vehicles perspective. *IEEE Trans. Veh. Technol.* 66 (06), 4534–4549.
- Marvi, F., Adib, E., and Farzanehfard, H. (2016). Efficient ZVS synchronous buck converter with extended duty cycle and low-current ripple. *IEEE Trans. Ind. Electron.* 63 (09), 5403–5409. doi:10.1109/tie.2016.2558483
- Moschopoulos, G., Jain, P. K., Yan-Fei Liu, Y. F., and Joos, G. (1999). A zero-voltage-switched PWM boost converter with an energy feedforward auxiliary circuit. *IEEE Trans. Power Electron.* 14 (04), 653–662. doi:10.1109/63.774202
- Oh, I. H. (2008, February). A soft-switching synchronous buck converter for zero voltage switching (ZVS) in light and full load conditions. In 2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, Austin, TX, 2008, IEEE, 1460–1464. doi:10.1109/APEC.2008.4522916
- Shao, T., Zheng, P., Li, H., Xue, Y., Wang, J., and Zheng, T. Q. (2017). A low-stress zero-current switching technique for power converters. *IEEE Trans. Power Electron.* 33 (06), 5087–5096.
- Song, C., Yingchao, Z., Jiaxin, L., Tianwen, Z., Long, L., and Xisen, Q. (2014). A ZVS bidirectional buck converter applied to hybrid energy storage system. In 2014 IEEE Conference and Expo Transportation Electrification Asia-Pacific (ITEC Asia-Pacific), Beijing, 2014, IEEE. doi:10.1109/ITEC-AP.2014.6940828
- Srivastava, M., Verma, A. K., and Singh Tomar, P. (2019). Design and implementation of a novel auxiliary network based ZVS DC/DC converter topology with MPWM: an application to electric vehicle battery charging. *IET Power Electron.* 12 (13), 3340–3350. doi:10.1049/iet-pel.2019.0258
- Striney, J. A., Anuja, V., and Ananth, M. B. J. (2016, March). Design of integrated zvs single-inductor synchronous buck converter for multiloading applications. In 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, 2016, IEEE, 4835–4840. doi:10.1109/ICEEOT.2016.7755639
- Tsai, C. T., Shen, C. L., Su, J. C., and Kuo, Y. C. (2011). Analysis and implementation of an interleaved ZVS buck converter with coupled-inductors. In 2011 6th IEEE Conference on Industrial Electronics and Applications, Beijing, 2011, IEEE, 1392–1397. doi:10.1109/ICIEA.2011.5975805
- Wang, J.-M., Wu, S.-T., and Jane, G.-C. (2011). A novel control scheme of synchronous buck converter for ZVS in light-load condition. *IEEE Trans. Power Electron.* 26 (11), 3265–3273. doi:10.1109/tpe.2011.2142324
- Yeh, C. S., Zhao, X., and Lai, J. S. (2017). A MHz zero voltage switching (ZVS) tapped-inductor buck converter for wide-input high step-down low-power applications. In 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia), Kaohsiung, 2017, IEEE, 494–499. doi:10.1109/IFEEC.2017.7992088
- Zhao, J. (2011). A novel ZVS buck converter topology for VRM applications. In 2011 6th IEEE Conference on Industrial Electronics and Applications, Beijing, 2011, IEEE, 2374–2379. doi:10.1109/ICIEA.2011.5975990

Conflict of Interest: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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NOMENCLATURE

C_o : output capacitor

C_r : resonant capacitor

D : duty cycle

D_1 : diode 1

D_2 : diode 2

D_m : main diode

D_{min} : minimum value of duty cycle

f : frequency

H : henry

I_{D1} : current across diode 1

I_{D2} : current across diode 2

I_{in} : input current

i_{LO} : main inductor current

i_{LR} : resonant inductor current

I_p : peak current

L_o : main inductor

L_r : resonant inductor

R_o : output resistor

S_1 : switch 1

S_2 : switch 2

S_m : main switch

t : time

T_r : resonant time

T_s : switching time

V : voltage

V_{CO} : capacitor output voltage

V_{CR} : resonant capacitor voltage

V_{DS} : drain to source voltage

V_{GS1} : gate pulse voltage of S_1

V_{GS2} : gate pulse voltage of S_2

V_{GSm} : gate pulse voltage of main switch

V_{in} : input voltage

V_o : output voltage

ω_o : output frequency

Z_o : output impedance

Z_r : resonant impedance