Performance Improvement Strategies for Discrete Wide Bandgap Devices: A Systematic Review

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Wide bandgap (WBG) devices are becoming increasingly popular due to their excellent material properties. WBG devices are commercially available in discrete and module packages. Many studies have investigated the design, structure and benefits of module packages. However, a comprehensive and in-depth overview of the discrete package is lacking. Discrete package has the advantages of flexibility, scalability and reduced cost; however, challenges of severe switching oscillations and limited current capacity are associated with it. This review encompasses the switching oscillations and limited current capacity issues of discrete devices. Switching oscillations are categorized in terms of voltage. The underlying oscillation mechanisms are explored in detail. For the current imbalance, the types, root causes and adverse effects in parallel-connected discrete devices application are reviewed. Besides, the most recent techniques to extract stray parameters are also explored. Finally, state-of-the-art methods to mitigate the switching oscillations and the current imbalance are summarized and evaluated. The performance improvement strategies discussed in this paper can assist researchers to better use the discrete package and can stimulate them to come up with new solutions.

Keywords: WBG devices, discrete package, switching oscillations, paralleling discrete devices, silicon carbide (SiC), gallium nitride (GaN)

1 INTRODUCTION

1.1 Overview of Discrete Package

Excellent material characteristics of WBG devices enable the high efficiency, high frequency and high power density design of power converters. They are commercially available in both discrete and module packages (CREE, 2021b; Infineon, 2021a; Infineon, 2021b; Rohm, 2021). Discrete and module packages are commonly used in low and high power applications, respectively. In medium power applications such as an electric vehicle (EV), both packages can be employed (Bertelshofer et al., 2019; Lu, 2020; Infineon, 2021c). Module packages have advantages of high current ratings and low package inductance (Chen et al., 2017; Hou et al., 2020; Lee et al., 2020). However, they are expensive and lack design flexibility (Jahns and Dai, 2017; Bertelshofer et al., 2019; Lu, 2020). The discrete package features a cost-optimized solution and enables quick prototyping of available convert designs at different power levels (Bertelshofer et al., 2019; Lee et al., 2020). The flexibility facilitates the converter manufacturers to fulfill specific requirements. For instant, the discrete package is a good fit for the data center uninterruptible power supply (UPS) (Infineon, 2021c) and integrated motor drive inverters as it assists full integration (Jahns and Dai, 2017). Generally, for the same chip size, the available cooling area is larger in discrete package compared with module package as illustrated in **Figure 1**, which enables the device to better handle the fleeting overloading condition

FIGURE 1 | Comparison of available cooling area in module vs discrete package.
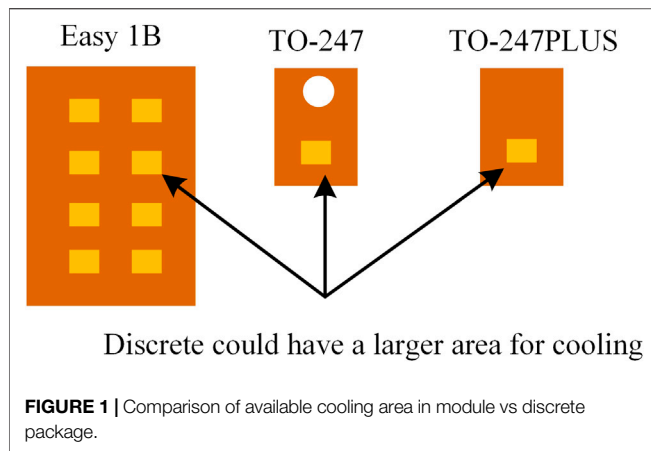
and can simplify the thermal design (Infineon, 2021c). With the advancements in packaging technology, new discrete packages such as TO-247PLUS offer higher power ratings and better thermal performance thanks to the bigger backside active thermal pad (Infineon, 2017; Infineon, 2021b; Sobe et al., 2020; IXYS, 2021). Finally, the discrete package is offered by more number of suppliers and it enables the designers to choose their preferred supplier based on price, region and customer support. The simple manufacturing process of discrete packages encourages the second sourcing strategies; thus, promoting the competition and as result, the price of discrete packages is expected to drop faster than that of module package. A 150 kW EV inverter with parallel-connected discrete (TO-247) SiC MOSFETs achieved a longer lifetime and similar power density compared to the Si module package (Bertelshofer et al., 2019). In addition, Tesla has also used discrete devices in parallel to push up the current ratings to achieve a cost-effective solution for EV inverters (Jahns and Dai, 2017; Jahns and Dai, 2018).

The discrete packages own the advantages of flexibility, scalability and reduced cost; though, challenges of severe switching oscillations and limited current capacity are associated with them. This review provides a comprehensive and in-depth overview of advanced performance improvement strategies to overcome these challenges.

1.2 Switching Oscillation Challenge

The high-frequency operation of WBG devices enables higher power density design by reducing the size of passive components. However, fast switching speed inevitably increases di/dt and dv/dt, inducing switching oscillations. The dv/dt of Silicon (Si) devices is typically around 3 V/ns (Ji et al., 2017) whereas that of Silicon Carbide (SiC) MOSFETs and Gallium Nitride (GaN) HEMT can reach 50 V/ns (Ji et al., 2017) and 80 V/ns (Hughes et al., 2012), respectively. Besides, low stray capacitance and the smaller R_{DSon} of WBG devices aggravate the oscillations (Zhang W. et al., 2014; Huang et al., 2017; Wang et al., 2018). Oscillations get more severe in the discrete package due to the high parasitic inductance of the package and printed circuit board (PCB). These oscillations have adverse effects on the convert performance such as additional power losses (Abou-Alfotouh et al., 2006; Chen,

2009; Mermet-Guyennet et al., 2012; Chen, 2014; Nayak et al., 2014; Dong et al., 2015; Jahdi et al., 2015; Liang et al., 2019; Meng et al., 2019), increased EMI noise (Gong et al., 2013; Tsai et al., 2013; Zare et al., 2015; Fang et al., 2017; Zhang et al., 2019; Zhang and Wang, 2020), shoot through (Elbanhawy, 2005; Watanabe and Itoh, 2011; Xu et al., 2013; Yanagi et al., 2014; Zhang Z. et al., 2014; Ishibashi et al., 2015; Yin et al., 2016; Wang et al., 2018) and overshoots in current and voltage (Gamand et al., 2012; Joko et al., 2015; Ando and Wada, 2017; Liang et al., 2017).

1.3 Uneven Current Distribution Concern

High-power applications require high current ratings switching devices; however, the maximum current of a commercially available discrete SiC MOSFET is limited to 115A (CREE, 2021b; Infineon, 2021a; Rohm, 2021). To increase the current ratings, discrete devices are usually used in parallel for high-power applications (Bertelshofer et al., 2019). Due to a mismatch in the parameters of the devices (Wang G. et al., 2014; Ke et al., 2018; Zhao et al., 2021a; Zhao et al., 2021b) and asymmetrical layout design (Li et al., 2014a; Tiwari et al., 2015; La Mantia et al., 2017), the current distribution among parallel-connected discrete devices is uneven, leading to imbalanced power loss distribution, uneven temperature rise and risk of device thermal runaway.

Recently, several studies have been reported to address above mentioned issues, but a comprehensive overview of the discrete package is lacking. Previously published survey articles focus on different aspects (Millán et al., 2014; Wang and Zhang, 2016; She et al., 2017); analyze the performance and applications of WBG devices. Commercialization, design challenges and fabrication methods are discussed in Jones et al. (2016) and Zhao S. et al. (2021), active driving solutions for module packages are discussed in Zhao S. et al. (2021), packaging technology and progress of module packages are presented (Hou et al., 2020; Lee et al., 2020; Alizadeh and Alan Mantooth, 2021). A systematic overview of the discrete package offering performance improvement strategies is required to unleash its potential. This survey comprehends switching oscillations and uneven current distribution issues of discrete packages. Oscillations are classified in terms of drain to source voltage (V_{ds}) and gate to source voltage (V_{gs}) and the underlying oscillation mechanism is explored in depth. In addition, the uneven current distribution is categorized into static current imbalance and dynamic current imbalance. Root causes and adverse effects of the current imbalance are also included. Furthermore, stray parameters extraction techniques are also discussed. In the end, the latest oscillation attenuation methods and current imbalance solutions are systematically summarized which can assist readers to fully leverage the benefits of the discrete packages.

2 CATEGORIES OF SWITCHING OSCILLATIONS

Switching oscillations have been reported in Si-based power converters (Idir et al., 2006; Makaran, 2009; Chen and Amaro, 2012; Filadelfo Fusillo, 2012; Taylor and Manack, 2012; Wang B. et al., 2014) which become even more severe in WBG devices

FIGURE 2 | (A) Types of switching oscillatins **(B)** Damped oscillation **(C)** Sustained oscillation (Umetani et al., 2019).
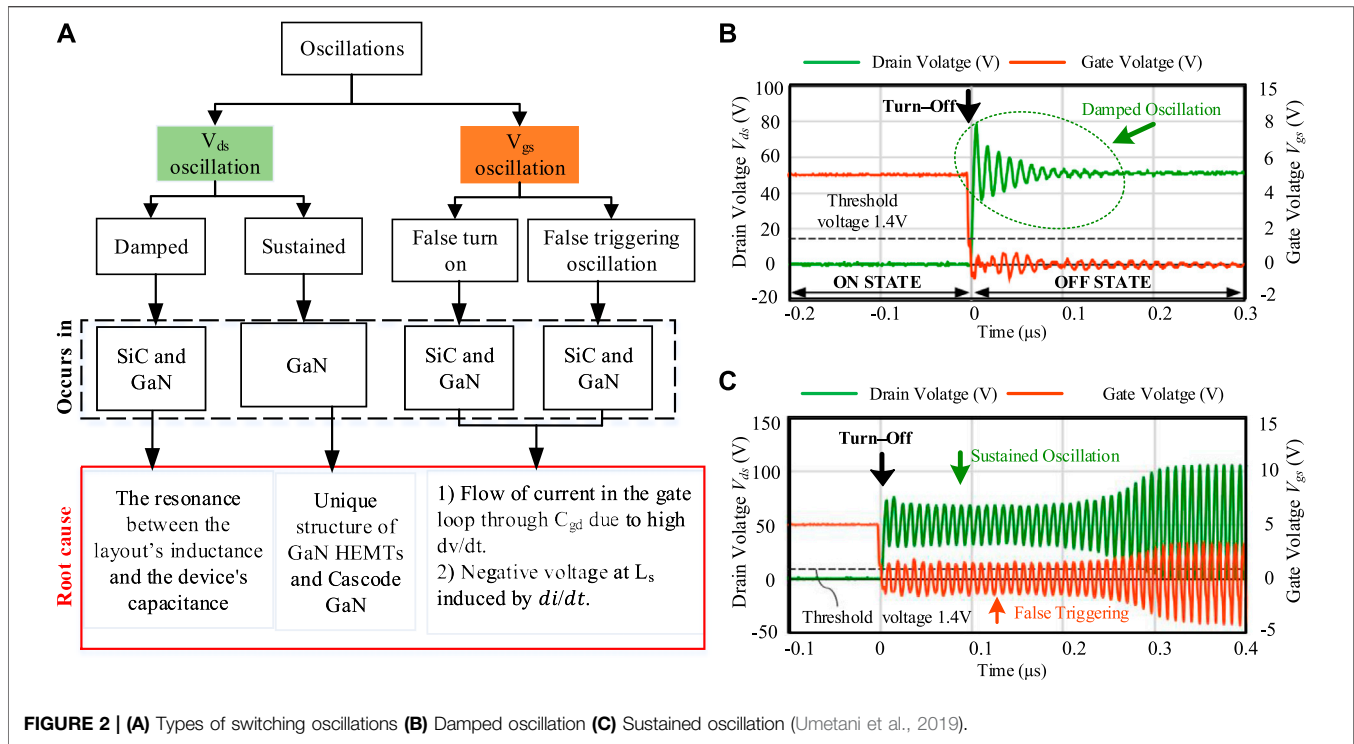
because of their extremely low parasitic capacitances and fast switching speed. As shown in **Figure 2A**, all oscillation types along with their root cause are discussed in this section. Oscillations in V_{ds} are organized as damped and sustained oscillation. Furthermore, oscillations in V_{gs} are discussed in terms of false turn-on and false triggering.

2.1 Drain to Source Voltage Oscillations and Underlying Mechanism
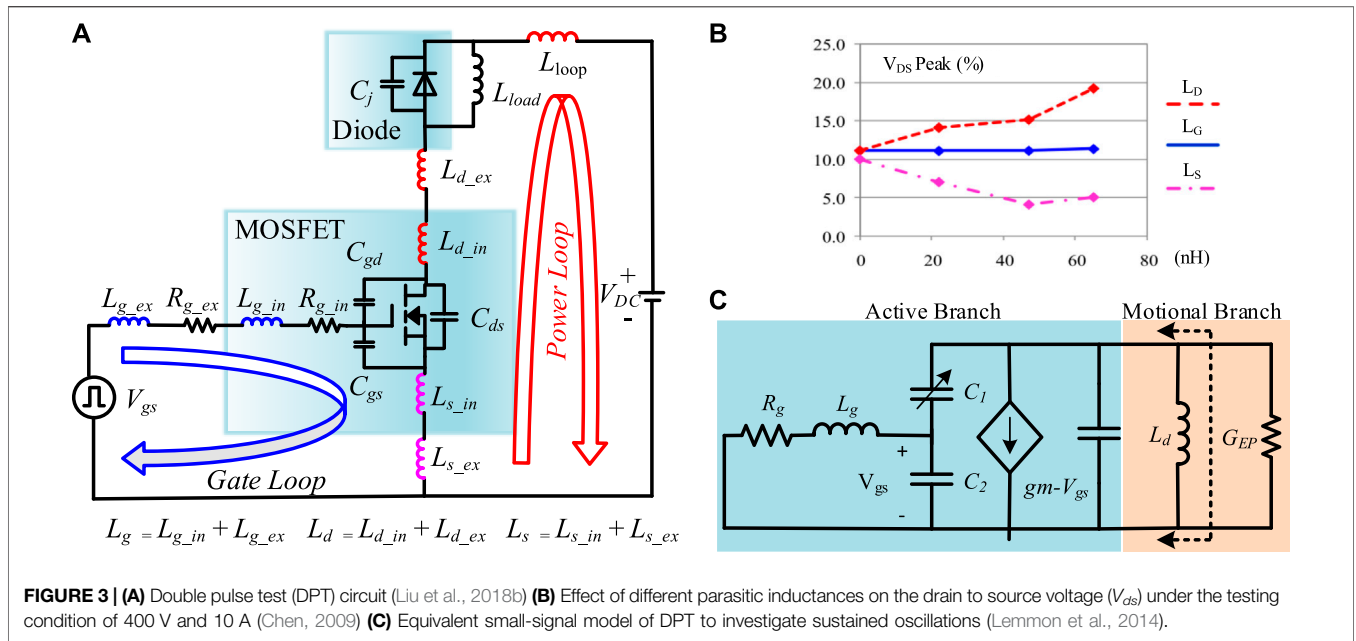### 2.1.1 Damped Oscillations in V_{ds}
The resonance between the inductance and capacitance in the power loop is a root cause of oscillation in V_{ds} (Gamand et al., 2012; Nayak et al., 2014; Joko et al., 2015; Ando and Wada, 2017; Liang et al., 2017). A double pulse test (DPT) circuit is shown in **Figure 3A**, which is made up of a freewheeling diode and SiC MOSFET. The parasitic inductances in the circuit include; drain inductance (L_d), gate inductance (L_g), common source inductance (L_s) and loop inductance (L_{loop}). Besides, the parasitic capacitances include; drain to source capacitance (C_{ds}), gate to drain capacitance (C_{gd}) and gate to source capacitance (C_{gs}). Parasitic capacitors and inductors might form an LC resonant circuit, then the energy transferred between them appears as an oscillation (Platania et al., 2011; Liu et al., 2016a). The oscillation gets damped over time as depicted in **Figure 2B** due to the small amount of resistance in the LC circuit which dissipates the energy in terms of heat. Damped oscillation is the most common type of oscillation and has been well documented in the literature. It has been reported in synchronous buck converters (Taylor and Manack, 2012), inverters (Chuai et al., 2019) and matrix converters (Safari et al., 2013). Oscillation can be modeled

using RLC equivalent circuits (Kassakian and Lau, 1984; Teulings et al., 1996; Githiari and Palmer, 1998; Ogura et al., 2003; Palmer and Joyce, 2003; Fujihira et al., 2008; Makaran, 2009; Alatise et al., 2012; Chen and Amaro, 2012; Liu et al., 2016b; Ren et al., 2017; Ding et al., 2017). The turn-off equivalent RLC circuit for the inductive load testing circuit is studied in Liu et al. (2016a) and a mathematical model is provided for designing oscillation mitigation solutions.

In a complicated resonance process, the impact of individual inductances (L_d, L_g, L_s) on the oscillation is different. Analytical (Xiao et al., 2004; Ren et al., 2006; Zhang et al., 2008; Li et al., 2011; Wang et al., 2012; Alexakis et al., 2013; Raee et al., 2013; Takao and Ohashi, 2013; Azizouglu and Karaca, 2014; Nayak and Hatua, 2016; Xie et al., 2016) and empirical methods (Chen, 2009; Chen et al., 2010; Zhang et al., 2012; Chen et al., 2013a; Stewart et al., 2013; Wada et al., 2013; Anthon et al., 2014; Li and Munk-Nielsen, 2014; Noppakunkajorn et al., 2014; Noppakunkajorn et al., 2015; Walder and Yuan, 2015; Wang X. et al., 2017) have been reported that investigated the impact of different parasitic inductance on oscillation. As shown in **Figure 3B**, it is concluded that the impact of L_g on damped oscillation is negligible and the main contributor is L_d (Chen, 2009; Khanna et al., 2013). Larger L_d enables fast speed and reduced switching losses but elevates the oscillation in V_{ds}. In addition, damped oscillation induced by the resonance of L_d and C_{gd} can be alleviated with increased L_s as it slows down the drain current. Larger L_s offers reduced oscillation and overshoots at the cost of increased switching losses.

2.1.2 Sustained Oscillations in V_{ds}
Sustained oscillation in V_{ds} stems out either from the structure of the device or sweep from the false triggering (Wang et al., 2009;

FIGURE 3 | (A) Double pulse test (DPT) circuit (Liu et al., 2018b) **(B)** Effect of different parasitic inductances on the drain to source voltage (V_{ds}) under the testing condition of 400 V and 10 A (Chen, 2009) **(C)** Equivalent small-signal model of DPT to investigate sustained oscillations (Lemmon et al., 2014).
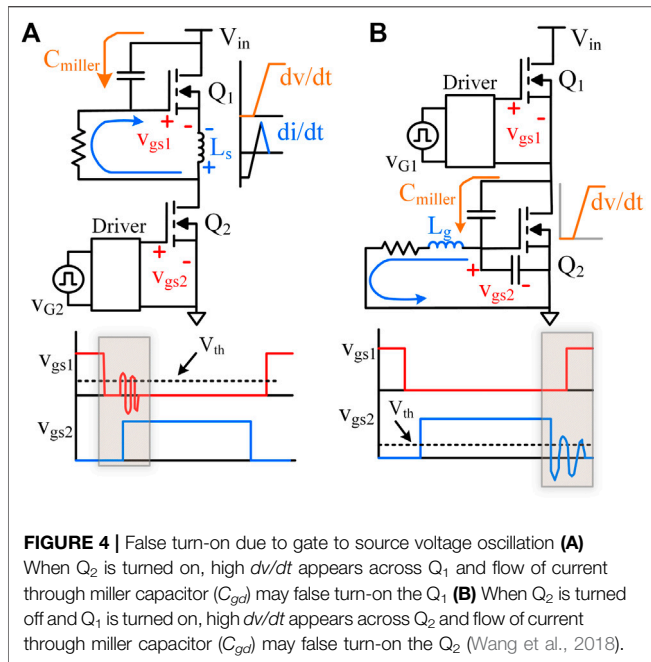
Adamowicz et al., 2011; Xu et al., 2011; Chen et al., 2014; Arribas et al., 2015; Lemmon et al., 2015; Wang et al., 2018; Umetani et al., 2019). Sustained oscillations are commonly observed in GaN (Wang et al., 2018; Umetani et al., 2019) and less likely to occur in SiC devices thanks to their relatively higher V_{th}. Among GaN devices, the structure of normally-off GaN HEMT and cascode GaN can instigate sustained oscillation whereas the structure of SiC MOSFETs is not observed to have any contribution in sustained oscillations. For example, normally-off GaN HEMTs have a unique bidirectional channel in contrast to SiC MOSFET. One phase leg usually consists of a lower switch and an upper one. In the case of Si/SiC-based switches, when the lower switch is turned off, the current flows through the body diode of the upper switch (Wang et al., 2019). But in GaN HEMTs, when the lower switch is turned off, the reverse current flows through the channel of the upper switch due to the absence of the body diode. The reverse channel current in GaN HEMTs is governed by the source current and the device can draw energy from the source leading to a sustained oscillation (Wang et al., 2018). The condition for reverse conduction in GaN HEMTs is; $V_{gd} > V_{gd(th)}$ or $V_{gs} > V_{gs(th)}$, which implies that the device would conduct in the reverse direction when either V_{gs} or V_{gd} exceed their corresponding threshold voltage (Wang et al., 2018). Apart from normally-off GaN HEMTs, turn-off sustained oscillation also occurs in the cascode GaN devices. Cascode GaN is made up of a low resistance silicon MOSFET placed in series with a normally-on GaN HEMT to make it a normally-off device. The junction capacitance discrepancy between the two components causes sustained oscillation. Detailed analysis of sustained oscillation in the cascode GaN is presented in Huang et al. (2017) and authors have concluded that during the turn-off, the rise in the V_{ds} of Si MOSFET might be caused by current oscillations. Then, a false turn on might occur in the internal GaN HEMT. This false turn-on of GaN HEMT causes sustained in the cascode GaN structure (Huang et al., 2017).

The susceptibility of sustained oscillation gets increased with larger transconductance and lower on-sate resistance of the device (Lemmon et al., 2014). Instead of using the hit and trial method, engineers usually predict sustained oscillation using the Barkhausen criterion and the small-signal models (Kazimierczuk, 2014; Lemmon et al., 2014; Umetani et al., 2019). Sustained oscillation would occur when the Barkhausen criterion is satisfied. A zero loop gain and the specified phase shift are required to fulfill the criterion (Unkrich and Meyer, 1982; Vittoz et al., 1988). To investigate the characteristics of the sustained oscillation, a small-signal model for the double pulse test (DPT) is presented in **Figure 3C**. The gate loop of the DPT act as the active branch and the power loop act as a motional branch (Lemmon et al., 2014). Sustained oscillations will occur if the resistance of the active branch is canceled out by the passive branch's resistance and reactive parts counterbalance each other. It performs like a negative resistance case. Different methods to mitigate the oscillation are discussed in **Section 4**.

2.2 Gate to Source Voltage Oscillations and Underlying Mechanism

Gate to source voltage (V_{gs}) oscillation may cause false action like false turn-on or false triggering as shown in **Figure 2A**. Both of them may lead to a shoot-through issue. The shoot-through current deteriorates the performance, increases switching losses, and can even damage the devices (Elbanhawy, 2005; Watanabe and Itoh, 2011; Xu et al., 2013; Yanagi et al., 2014; Zhang Z. et al., 2014; Ishibashi et al., 2015; Fan et al., 2016; Yin et al., 2016; Wang et al., 2018). The difference between false turn-on and false triggering lies in single and repeated trigger action. The false turn-on is mainly related with the high dv/dt and di/dt in WBG devices (Khanna et al., 2013; Wang and Chung, 2014; Yanagi et al., 2014; Ishibashi et al., 2015; Jahdi et al., 2015; Wang

FIGURE 4 | False turn-on due to gate to source voltage oscillation **(A)** When Q_2 is turned on, high *dv/dt* appears across Q_1 and flow of current through miller capacitor (C_{gd}) may false turn-on the Q_1 **(B)** When Q_2 is turned off and Q_1 is turned on, high *dv/dt* appears across Q_2 and flow of current through miller capacitor (C_{gd}) may false turn-on the Q_2 (Wang et al., 2018).

et al., 2018; Li R. et al., 2019). When one of two MOSFETs in a phase leg configuration turns on, a fast-rising voltage appears across the off-state MOSFET, as shown in **Figure 4**. As a result, a current flow in the gate loop through C_{gd} causing a voltage drop. If the voltage drop is higher than the device threshold voltage, a false turn-on event would occur leading to shoot-through. Typically, the duration for a false turn-on is between 10 and 100 nsec (Yin et al., 2016) and the value of current can reach up to 150 A (Yanagi et al., 2014). As shown in **Figure 3A**, L_s stays in both gate loop and power loop. It indicates that a negative gate voltage would be introduced by high *di/dt* from power loop which can worsen the oscillation leading to false triggering. False triggering is reported in both SiC (Lemmon et al., 2013, 2014; Sugihara et al., 2017) and GaN (Umetani et al., 2016, 2019; Matsumoto et al., 2017) devices, though, the latter one is more susceptible to false triggering owing to its low threshold voltage. A comprehensive analysis of false triggering oscillations is provided in Umetani et al. (2016) and it is concluded that in order to avoid the false triggering oscillation the resonance frequency of the power loop and that of the gate loop should be decoupled. Besides, an optimum device selection and proper circuit layout design are important for depressing the gate oscillations by minimizing C_{gd} and L_s.

3 CATEGORIES OF CURRENT IMBALANCE AND CAUSES

Parameters of semiconductor devices vary even when they are from the same wafer. This variance is especially noticeable in WBG devices since technology is not yet mature. In Wang G. et al. (2014), thirty samples of SiC MOSFET (C2M0160120DA) from the same vendor under room temperature are evaluated and it has been

reported that the difference of R_{DSon} can reach up to 20% and the difference of V_{th} can reach up to 24% (Wang G. et al., 2014). The variation in the parameters of devices, called device mismatch, causes unequal current distribution (Wen et al., 2021; Zhao et al., 2021a; Zhao et al., 2021b). In addition, due to asymmetrical layout design, the discrepancy in the parasitic inductances of the circuit also causes uneven current distribution (Li et al., 2014a; Tiwari et al., 2015; La Mantia et al., 2017; Hu and Shao, 2021). During unequal current sharing, one device carries more current than the others, which not only stresses the device but may also lead to thermal runaway if it operates outside of its safe operating area (SOA).

3.1 Static Current Imbalance

Static current imbalance is due to the variation in R_{DSon} of parallel-connected devices. During the on state, MOSFETs behave like a small resistor and a group of MOSFETs connected in parallel has the advantage of reduced resistance current path. Due to R_{DSon} variation, the device with the lowest resistance conducts more current and has relatively higher conduction losses, as a result, its resistance increases. In Si MOSFETs, owing to the positive temperature coefficient (PTC) of R_{DSon}, the static current imbalance naturally gets reduced (Xue et al., 2013; Mao et al., 2017a; Mukunoki and Horiguchi, 2018; Zeng et al., 2020). As shown in **Figure 5E**, the TO-247 package of Si, SiC and GaN MOSFETs with similar ratings have been tested. It is concluded that when the temperature is raised from 25°C to 175°C, the R_{DSon} of Si, SiC and GaN increases by 3×, 1.5× and 2×, respectively. Hence, the intrinsic current sharing capability of WBG MOSFETs is not as prominent as that of Si counterparts (Wang G. et al., 2014; Xue et al., 2014a; Ke et al., 2018; Zeng et al., 2020; Zhao et al., 2021a; Zhao et al., 2021b). In addition, the value of gate to source voltage (V_{gs}) also influences the R_{DSon} (Wang G. et al., 2014).
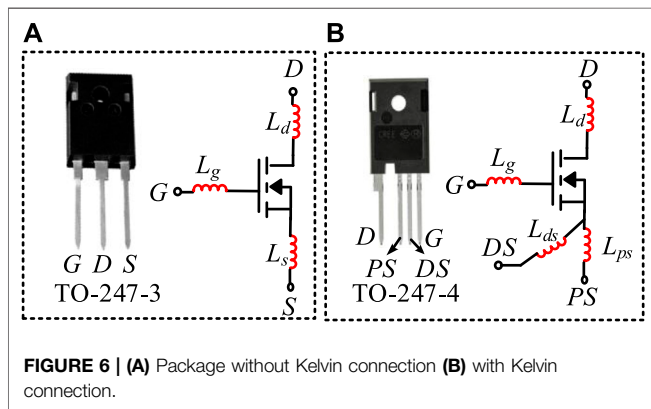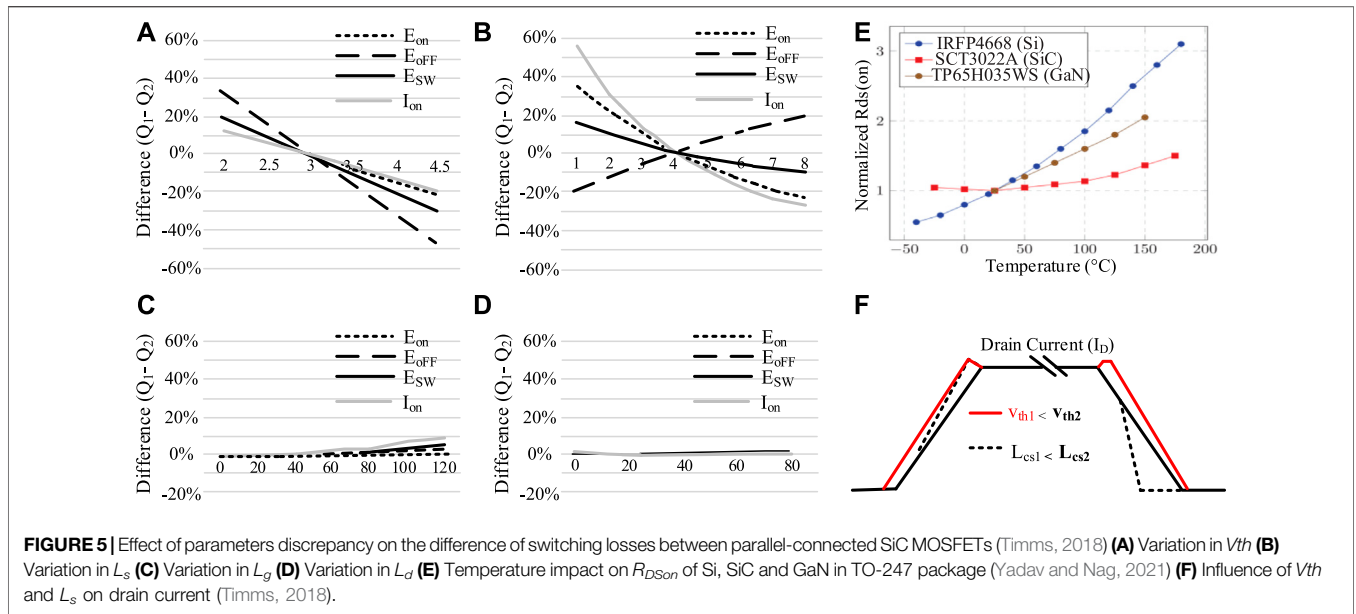
3.2 Dynamic Current Imbalance

The dynamic current of a device depends on its threshold voltage (V_{th}), gate to source voltage (V_{gs}) and transconductance (g_{fs}) as depicted in **Eq. 1**. Among parallel-connected devices, the device with lower V_{th} or higher g_{fs} conducts more dynamic current leading to dynamic current unbalance. Furthermore, dynamic current imbalance increases with a rise in temperature due to the negative temperature coefficient (NTC) of threshold voltage (V_{th}). At higher frequency, even a slight discrepancy in L_s of parallel-connected MOSFETs will induce negative feedback to gate voltage as revealed in **Eq. 2**, and the change in V_{gs} will directly impact the drain current as shown in **Eq. 1**.

$$I_d = g_{fs}\left(v_{gs} - V_{th}\right) \tag{1}$$

$$v_{gs} = V_{driver} - i_g R_g - L_s \frac{di_s}{dt} \tag{2}$$

Dynamic current imbalance leads to unequal distribution of switching losses among parallel connected devices. The impact on switching losses variation from the current imbalance is illustrated in **Figures 5A–D** (Timms, 2018). It shows that the dynamic current and switching losses distribution are mainly

FIGURE 5 | Effect of parameters discrepancy on the difference of switching losses between parallel-connected SiC MOSFETs (Timms, 2018) **(A)** Variation in V_{th} **(B)** Variation in L_s **(C)** Variation in L_g **(D)** Variation in L_d **(E)** Temperature impact on R_{DSon} of Si, SiC and GaN in TO-247 package (Yadav and Nag, 2021) **(F)** Influence of V_{th} and L_s on drain current (Timms, 2018).

FIGURE 6 | (A) Package without Kelvin connection **(B)** with Kelvin connection.

affected by the V_{th} and L_s. As demonstrated in **Figure 5F** (Timms, 2018), a lower L_s means a faster switching speed. In addition, a lower V_{th} means faster turns on but slower turns off. Hence, matching the V_{th} and L_s of parallel-connected devices is crucial to suppress the dynamic current imbalance.

In summary, the prominent root cause of static current imbalance is R_{DSon} whereas the mismatch in V_{th}, L_s or g_{fs} instigates the dynamic current imbalance. The adverse effects of the current imbalance include uneven power loss distribution, increased stress to a single device, higher current overshoots, uneven temperature rise and all contribute to reduced reliability.

4 METHODS TO MITIGATE OSCILLATIONS

4.1 Parasitic Elements Minimization

4.1.1 Impact of the Package
Parasitic elements causing switching oscillations are related to the device package and PCB layout. It is challenging to switch SiC MOSFET faster than 10 ns without ringing in the TO-247-3

package (Li and Munk-nielsen, 2014) as it has 8 nH inevitable common source inductance (L_s) (Aikawa et al., 2017). By using a package with a kelvin source, the oscillations and overshoots can be reduced since the L_s can be bypassed as shown in **Figure 6** (Li and Munk-nielsen, 2014; Lemmon et al., 2016). TO-247-4, TO-247PLUS-4 and TO-263-7 are the common commercialized package with a kelvin source. The TO-247PLUS-4 (CREE, 2021a) package offers a higher breakdown voltage (1,700 V) with superior thermal performance and increased current ratings. The TO-263 package offers 32% less package inductance than the TO-247 package and achieved 29% reduction in switching losses per cycle and reduced the current overshoot by 10 A in Lemmon et al. (2016). Hence, low package inductance and Kelvin source connection facilitate the oscillation mitigation.

4.1.2 Impact of the Layout Design
Parasitic elements in the circuit also induce switching oscillations. An optimized layout design with respect to the loop size and geometry can reduce the overshoots and improves efficiency (Reusch and Strydom, 2014; Wang K. et al., 2017; Letellier et al., 2019; Sun et al., 2021). Parasitic inductances in the power and gate loops should be kept as low as possible to reduce switching oscillation. A comparison of different PCB layouts to minimize the power loop and drive loop inductances is presented in Wang K. et al. (2017). It is concluded that the double side layout achieves minimum power loop and drive loop inductance along with low voltage overshoot. A buck converter with a double-layer design achieves a 50% reduction in driver loop inductance, resulting in 0.6% increase in peak efficiency and 8.3% drop in drain-source voltage overshoot (Wang K. et al., 2017). To obtain an optimized layout design with minimized stray inductance, in-depth investigation has been carried out in Shtargot et al. (2012), Reusch and Strydom (2014), Meng et al. (2021), and Pace et al. (2021).

4.2 Gate Resistor Adjustment

The external gate resistor plays a critical role in the device's performance. The dv/dt or di/dt of a device can be decreased by increasing the gate resistor (R_g), leading to a reduced oscillation and overshoots (Liu et al., 2016b) at the cost of increased switching losses. A detailed gate resistor effect demonstration is shown in Liu et al. (2018b), where an additional 10 Ω gate resistor brings a reduction of about 15 and 4% in voltage overshoot and oscillation duration, respectively. In another aspect, a significant increase in turn-on and turn-off times is resulted and the turn-on energy (E_{on}) and turn-off energy (E_{off}) get increased by 64 and 80%, respectively. Gate resistor also impacts the false triggering oscillation and parasitic ringing, as reported in Gafford et al. (2013), Li and Munk-Nielsen (2014a), and Liu et al. (2018b). The gate resistor can be viewed as the tradeoff between switching losses and switching oscillations. To determine an optimum value of R_g, equivalent circuits, the analysis and validation are provided in Chen and Amaro (2012), Liu et al. (2016a), and Paredes et al. (2017).

4.3 Gate Driver Design

Adjustment of gate resistance can be viewed as a simple and specified way in gate driver to mitigate oscillations. Many well-designed gate drivers for oscillation and crosstalk depression are reported in the literature (Paredes Camacho et al., 2017; Paredes et al., 2017; Zhang et al., 2017). Gate drivers can be categorized as open loop gate drivers, active gate drivers and multi-level gate drivers.

4.3.1 Open Loop Gate Drivers

Conventional gate drivers (CGDs) are simple and work in the open loop. The cross-talk effect and oscillation caused by dv/dt or di/dt can be attenuated by employing negative voltage gate drivers (Kelley et al., 2009; Chen et al., 2011; CREE, 2011; Semiconductor, 2013; Li et al., 2020a). Nevertheless, negative voltage gate drivers induce negative overshoot in the V_{gs} and corresponding overshoot would affect the device reliability since the negative gate voltage withstand ability of WBG devices is low. Negative voltage spikes can be diminished using gate drivers with auxiliary transistors (Zhou and Gao, 2016; Gao et al., 2018). Reshaping the gate loop of conventional gate drivers with the implementation of two extra capacitors is another way to mitigate the cross-talk which achieved 0.6% increase in the converter's efficiency by avoiding the L_s (Li Y. et al., 2019). An intelligent gate driver (IGD) adopting two auxiliary transistors and two diodes is reported in Zhang et al. (2017). Compared with conventional gate drivers, the intelligent gate driver offers similar oscillations attenuation with reduced energy losses and lower V_{gs_peak}, as shown in **Figures 7A,B**.

4.3.2 Active Gate Drivers

Active gate drivers mitigate the oscillation by actively controlling the gate voltage to regulate the slew rate of voltage/current. They employ a closed-loop to fully exploit the potential of WBG devices (Shahverdi et al., 2013; Dymond et al., 2018; Cao et al., 2021). The active gate driver proposed in Nayak and Hatua (2017) utilized stray inductance and capacitance to achieve quasi zero switching leading to reduced switching losses. To suppress the cross-talk, active gate drivers generally regulate the gate impedance and gate voltage. An active gate driver with gate assist circuits featured a fast turn-on by adjusting the gate loop resistance and gate voltage. It achieved up to 17% reduction in turn-on switching losses with an effectively suppressed cross-talk (Zhang Z. et al., 2014). Two gate assist circuits, gate impedance regulation and gate voltage control have been studied in Zhang Z. et al. (2014). Gate impedance regulation circuit is simple since it employs one transistor and one capacitor compared to gate voltage control circuit, which adopts two transistors and one diode (Zhang Z. et al., 2014). The former one is suitable for board-level integration and the latter one is a better fit for chip-level integration. Other active gate drivers that target V_{ds} overshoot, EMI noise and parasitic ringing have been reported in Nayak and Hatua (2017), Paredes Camacho et al. (2017), Nayak and Hatua (2018), and Yang et al. (2019).
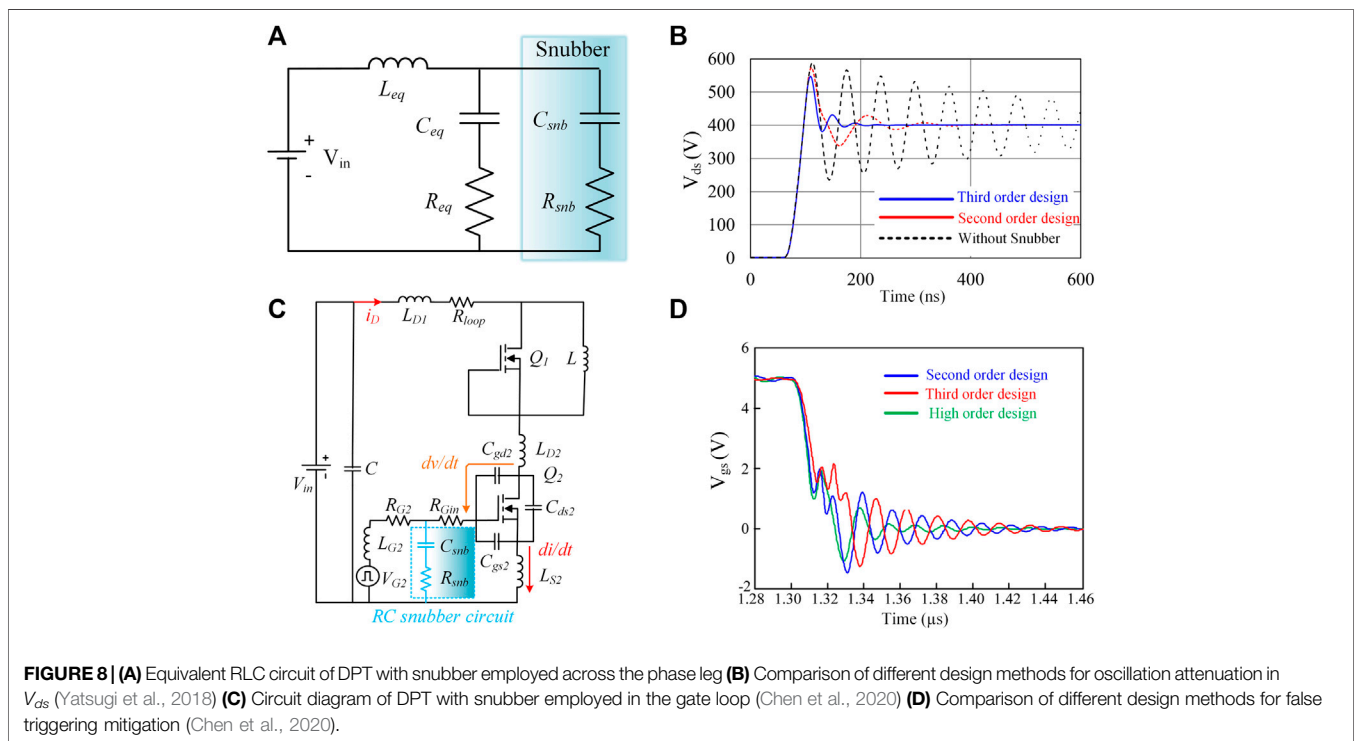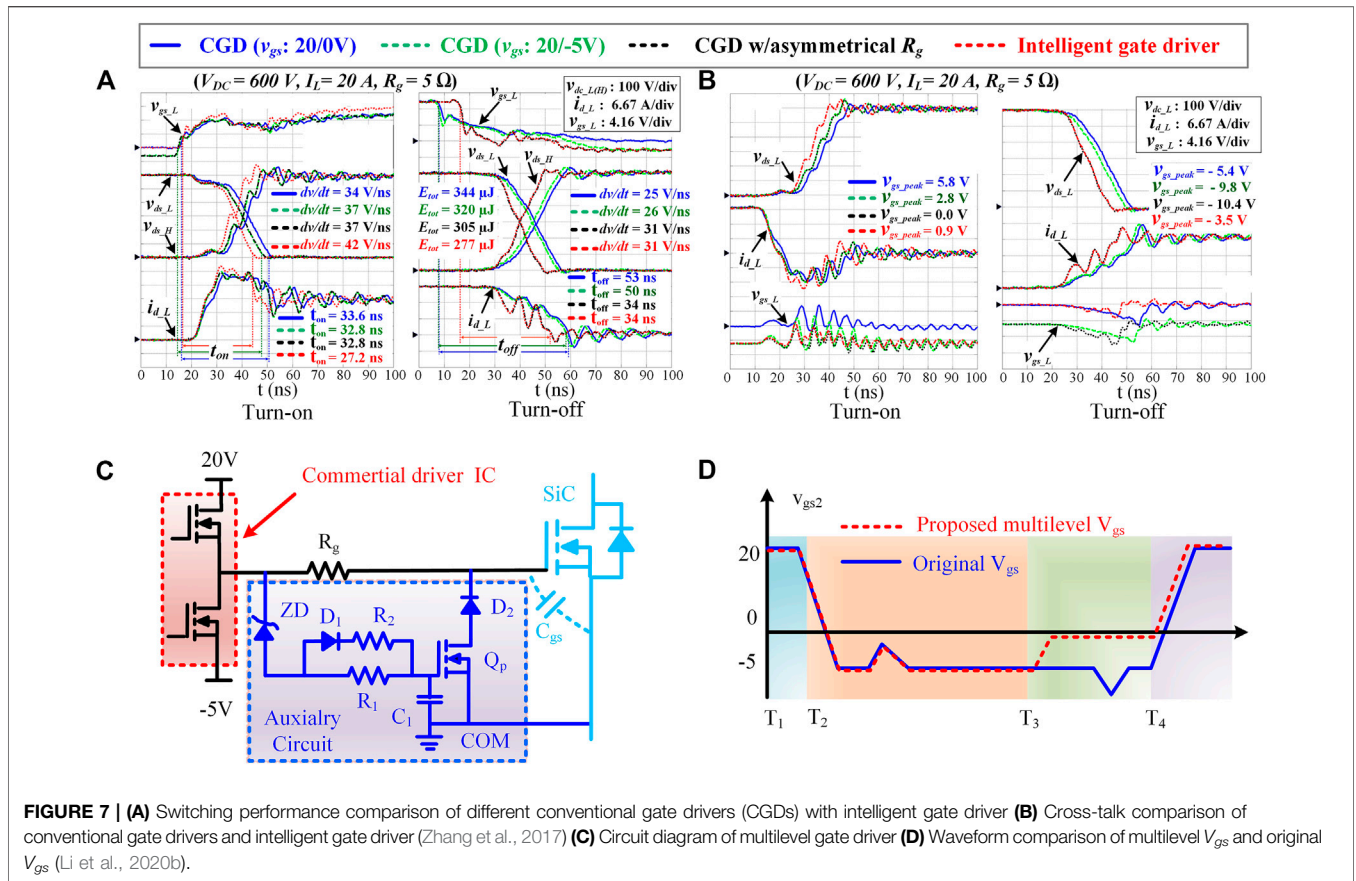
4.3.3 Multilevel Gate Drivers

Multilevel gate drivers are effective to mitigate crosstalk (Li et al., 2020b; Wu et al., 2020) and offer reduced energy losses and increased safety and reliability (Zhao et al., 2019; Li et al., 2020b). To introduce additional levels in gate voltage, multilevel gate drivers employ either auxiliary circuits or an active driving approach. A multilevel gate driver adopted an auxiliary circuit that is suitable to suppress false triggering oscillations and negative gate overvoltage (Li et al., 2020b). The auxiliary circuit is shown in **Figure 7C** which can easily be implemented on the conventional gate driver (Li et al., 2020b), as it does not require any additional dc power, isolation stage, or control signals. As shown in **Figure 7D**, during the V_{gs} positive peak event, the multilevel gate driver (Li et al., 2020b) keeps the voltage to a specific negative level so that false triggering can be avoided. Afterward, it shifts the voltage to zero or less negative level just before the positive peak event to prevent the negative voltage breakdown. Negative overshoot in the gate to source voltage is reduced from −9.9 V to −1.6 V (Li et al., 2020b). For desaturation protection, the multi-level turn-off strategy is widely used in the industry. In Zhao et al. (2019) an adaptive multi-level active gate driver is investigated that used a three-level turn-off strategy. It enables a shorter turn-off delay than conventional gate drivers and two-level gate drivers (Zhao et al., 2019). It employed a behavioral model and adaptive optimization to accommodate the variation in turn-off delay due to varying load currents and bus voltages.

To sum up, open loop gate drivers are relatively simple and their mitigation effect can be improved by employing additional components but still, they do not consider load variations. Active gate drivers and adaptive multi-level active gate drivers consider the load variation and provide effective oscillations mitigation, but have increased cost and design complexity (Paredes Camacho et al., 2017; Dymond et al., 2018; Zhao et al., 2019).

4.4 RC Snubbers

To suppress the oscillation, the large gate resistance increases the energy losses and the active gate driver approach demands complex feedback control. RC snubber offers reduced cost and complexity compared with the active gate driver and slightly less

FIGURE 7 | (A) Switching performance comparison of different conventional gate drivers (CGDs) with intelligent gate driver **(B)** Cross-talk comparison of conventional gate drivers and intelligent gate driver (Zhang et al., 2017) **(C)** Circuit diagram of multilevel gate driver **(D)** Waveform comparison of multilevel V_{gs} and original V_{gs} (Li et al., 2020b).

FIGURE 8 | (A) Equivalent RLC circuit of DPT with snubber employed across the phase leg **(B)** Comparison of different design methods for oscillation attenuation in V_{ds} (Yatsugi et al., 2018) **(C)** Circuit diagram of DPT with snubber employed in the gate loop (Chen et al., 2020) **(D)** Comparison of different design methods for false triggering mitigation (Chen et al., 2020).

energy losses compared with the gate resistance method. RC snubber is a widely adopted solution for oscillation attenuation (McMurray, 1972; Josifović et al., 2011; Josifovic et al., 2012; Salem and Wood, 2014; Vaculik, 2014; Joko et al., 2015; Liu et al., 2016a; Liu et al., 2016b; Torsæter et al., 2016; Chen et al., 2021; Yang et al., 2021). Choosing optimum values of snubber for effective oscillation suppression is essential. An efficient way to design these parameters is to simplify the switching circuit into an equivalent RLC circuit incorporating all circuit parasitic. Then switching oscillations can be modeled using the RLC equivalent circuit and theoretical analysis of models can provide the guidelines for designing RC snubber. The equivalent RLC circuit of DPT including snubber is shown in **Figure 8A**. Snubber design methods can be categorized into second order, third order and higher order. Compared with the second order method, third order and higher order design methods enable better oscillation mitigation in both V_{ds} and V_{gs} as depicted in **Figures 8B,D** at the cost of increased design complexity (Chen et al., 2020). Detailed guidelines to design snubber using second order approach are provided in Josifović et al. (2011), Josifovic et al. (2012), Salem and Wood (2014), Vaculik (2014), Joko et al. (2015), and Torsæter et al. (2016) and those for third order and higher order methods are discussed in Yatsugi et al. (2018) and Chen et al. (2020).

4.5 Soft Switching Strategy

Switching oscillation and switching losses can also be mitigated by implementing either the zero voltage switching or zero current switching or both (Hua et al., 1994; Watson et al., 1996; Lai, 1997; Tang et al., 1998; Zhang et al., 2007; Chen et al., 2013b; Chen et al., 2013c; Ahmed et al., 2017). Usually, an additional capacitor/inductor or their combination is implemented in the topology to realize resonance for achieving soft switching. Researchers (Ahmed et al., 2017) illustrated that soft switching can significantly reduce the oscillation with 86% drop in dv/dt. Soft switching also has certain drawbacks, such as increasing part count and making the control system more complex (Toshiba, 2019). Therefore, it is important to determine if soft switching is suitable for the required application. Since soft switching is valuable to minimize diode recovery loss and transformer leakage inductance loss (Toshiba, 2019), it is widely adopted in isolated dc-dc converters such as LLC, CLLC and Flyback converts (Hua et al., 1994; Watson et al., 1996; Lai, 1997; Tang et al., 1998; Zhang et al., 2007; Lu et al., 2021; Spiazzi and Buso, 2021).

4.6 Ferrite Beads

Ferrite beads are effective to mitigate the oscillation as reported in Dodge (2004), Josifović et al. (2011), Josifovic et al. (2012), Zhao et al. (2017), and Liu et al. (2018b). These beads work based on Faraday's law; when a high frequency oscillation passes through the ferrite bead, a back emf is induced in the core of the bead that attenuates the oscillation. Ferrite bead can be employed in the power loop to reduce oscillation in V_{ds} or in the gate loop to reduce oscillation in the V_{gs}. A ferrite bead implemented in the power loop is illustrated in **Figure 9A**. The characteristics graph of a ferrite bead is shown in **Figure 9B** (Liu et al., 2018b). For effective oscillation mitigation, the undesired frequencies must be in the resistive band

of the ferrite bead. The oscillation frequency (f_{osc}) can be determined using **Eq. 3**, where C_{eq} is equivalent stray capacitance and the sum of ferrite beat inductance along with equivalent circuit's inductance is represented by L_{eq}. In addition, the damping coefficient (m) can be calculated using **Eq. 4** where the resistive impedance of the bead is denoted by R_{seq}. As ferrite bead's inductance and capacitance are frequency dependent, the following conditions must be satisfied to achieve effective oscillation suppression.

$$f_{oscillation} = \frac{1}{2\pi\sqrt{C_{eq} \times L_{eq}}} \qquad (3)$$

$$m = R_{seq} / \left[2 \times \left(\sqrt{\frac{L_{eq}}{C_{eq}}} \right) \right] \qquad (4)$$

1) The damping coefficient must be greater than one ($m > 1$), for selected values of resistor and inductor of the bead.
2) At oscillation frequency (f_{osc}), ferrite bead must have resistive dominant impedance with $m > 1$.
3) To reduce the overall power losses, dc power losses in the bead should be kept to a minimum possible level.

As the characteristics of ferrite beads vary with load current, therefore, impedance vs load current curves should be referred to select the right ferrite bead. **Figure 9C** reveals the influence of ferrite bead on voltage oscillation of SiC MOSFET (Kim et al., 2017). Ferrite beads are effective for EMI reduction and at 15 MHz oscillation frequency, a noise reduction of 15 dB has been achieved in a SiC-based boost (Kim et al., 2017). By employing ferrite bead, 3.8% reduction in voltage overshoot and 78.45% reduction in oscillation duration of SiC MOSFET were achieved by Liu et al. (2018b). No matter how precisely parameters of ferrite are selected, a small amount of dc resistance is inevitable, which causes a slight increase in the conduction losses. Comprehensive design guidelines for ferrite beads can be found in Josifović et al. (2011), Josifovic et al. (2012), and Liu et al. (2018b).

To summarize, careful selection of a device with low package inductance and kelvin source can alleviate the oscillation. In addition, an optimized PCB layout offers reduced oscillation by diminishing the power loop and gate loop inductances. Increasing external gate resistance reduces the oscillation but slows down the switching speed leading to increased switching losses. Active gate driver can reduce the overshoots and cross-talk by controlling the di/dt and dv/dt, but increases the circuit cost and design complexity. The RC snubber method offers effective oscillation mitigation but slightly increases switching losses. Ferrite beads perform better to suppress high-frequency oscillations at the cost of slightly increased conduction loss. All oscillation mitigation methods have their pros and cons that are outlined in **Table 1**.

5 METHODS TO MITIGATE CURRENT IMBALANCE

5.1 Symmetrical Layout Method

The mismatch of parasitic parameters in the circuit is due to asymmetrical layout design (Graovac, 2009; Wang G. et al., 2014;
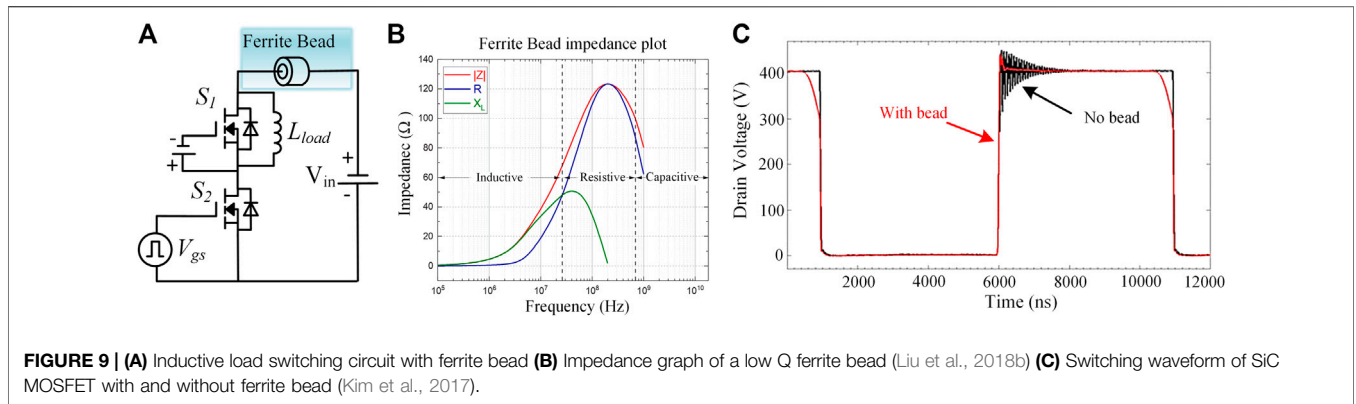
FIGURE 9 | (A) Inductive load switching circuit with ferrite bead **(B)** Impedance graph of a low Q ferrite bead (Liu et al., 2018b) **(C)** Switching waveform of SiC MOSFET with and without ferrite bead (Kim et al., 2017).

TABLE 1 | Summary of methods for oscillation alleviation.

Method	Benefits	Drawbacks	Remarks
Package selection	• Easy to implement • No additional component required	• Limited oscillation mitigation	Select either TO-247-4 package or TO-263-7 package. Both packages have kelvin source connection which provides a shorter path to the gate loop and assist the oscillation attenuation. TO-247-4 has higher current capacity while TO-263 offers 32% less package inductance compared to TO-247
Layout optimization	• No additional component required • No increase in losses	• Increase design effort • Difficult to implement • Limited oscillation mitigation	Minimize the power loop and drive loop inductances as much as possible. Double layout design method can be adopted which reduced voltage overshot by 8.3% and increased efficiency by 0.6% (Wang et al., 2017a)
External gate resistor	• Good oscillation mitigation • Easy to implement	• Slow turn-on and off • Increase switching losses	Since the higher resistor value leads to increased switching losses, choose an optimum value of resistance that keeps the oscillation under control without a substantial increase in switching losses
Gate driver design	• Mitigates specific oscillations • Maintains fast switching speed • Suppress oscillation regardless of its cause	• Require auxiliary circuit • Increase cost • Increase design complexity	Different gate driver design strategies aim to suppress different oscillations. By controlling gate impedance and gate voltage, cross-talk can be reduced. The benefits of active gate drivers should be weight against the complexity
RC snubbers	• Good oscillation mitigation • Easy to implement	• Require additional components • Minor increase in switching losses • Complex design method for higher order circuits	The key is to carefully design the snubber parameters. To achieve a good damping effect, damping ratio should be as high as possible for all solutions. Higher order design offers better oscillation mitigation, but its design method is extremely complicated
Soft switching strategy	• Good oscillation mitigation • Reduce switching losses • No reduction in switching speed	• Require careful design • Increase control complexity • Increase part count	It is an effective method to suppress oscillation and losses, though cannot be adopted for all applications. Usually suitable for DC-DC converts (LLC, DAB, Flyback, etc)
Ferrite beads	• High-frequency damping ability • Effective oscillation mitigation • Easy to Implement	• Require additional ferrite bead • Slightly increase conduction losses	Ferrite beads are good for EMI reduction and can reduce the EMI noise by 15 dB at 15 MHz oscillation frequency (Kim et al., 2017). The damping coefficient must be greater than one. Ferrite beads can reduce the voltage overshoot and the duration of oscillations by 3.8 and 78.45%, respectively (Liu et al., 2018b)

Colmenares et al., 2015; Li et al., 2016; Haihong et al., 2017). This mismatch is the reason for the current imbalance which can be mitigated by realizing the symmetrical layout (Sadik et al., 2013). As mentioned earlier, the impact of L_s mismatch on current sharing is more prominent than that of L_d or L_g. Therefore, it is paramount to minimize discrepancy in L_s to reduce the current imbalance (La Mantia et al., 2017). Nevertheless, in many applications, due to layout constraints, it is extremely hard to achieve exactly symmetrical layout design. In such cases, a four-pin device that offers a kelvin connection can be adopted which provides a shorter path to the gate loop and bypass the L_s as

shown in **Figure 6B**. Kelvin connection does not guarantee equal current distribution, yet it offers an opportunity to designers to achieve a better layout design, leading to improved current sharing.

This method can reduce the dynamic current imbalance and can provide a slight reduction in static current imbalance. For effective reduction of current imbalance, just realizing the symmetrical layout is not enough as it does not address the device mismatch. Generally, symmetrical layout design is a prerequisite for advanced current balancing methods. Besides, it does not offer increased switching speed, and energy losses cannot

be minimized. Moreover, this method is difficult to adopt for more parallel-connected devices as the symmetrical layout is practically difficult to achieve for a higher number of devices.

5.2 Imbalance Mitigation via Source or Gate Resistors

Adjustment of gate or source resistor is a simple way to mitigate the current imbalance without adding any sensing or control circuit. One of the reasons for dynamic current imbalance is; a device with a lower V_{th} turns on earlier than the device with a higher V_{th}. There are two ways to reduce the effect of V_{th} mismatch using a gate resistor. First, the current imbalance can be suppressed by reducing the value of gate resistance if the same gate resistor is shared by the parallel-connected devices. Authors in Wang G. et al. (2014) achieved an effective reduction in current imbalance by reducing the gate resistance from 41 to 5.1 Ω at the cost of increased overshoot. The reason behind improved current sharing is; at a lower gate resistance, the switching speed increases and the effect of V_{th} mismatch become less significant. Another way is to add a suitable resistance only to the gate of the fast device with the lower V_{th} (Du et al., 2014). The fundamental principle behind adding the resistance is to delay the driving signal of the fast device (Du et al., 2014). Symmetrical layout is requisite for achieving promising results for both methods. Gate resistance adjustment can improve the dynamic current sharing and may offer a slight improvement in the current ratings. Nevertheless, it does not provide static current balancing since the V_{th} is the only parameter addressed in the strategy.

Employing additional source resistors in the parallel branches can suppress static current imbalance by reducing the R_{DSon} mismatch. As the source resistors can only reduce the R_{DSon} mismatch; therefore, no improvement in the dynamic current sharing can be attained and additional resistors cause extra power losses. Moreover, source resistors do not offer any reduction in voltage overshoot and gate oscillation (Zeng et al., 2020). Nonetheless, the cost, size and volume of gate and source resistance solutions are low and they can be employed for more than two devices.

5.3 Transfer Curve Screening Method

This method aims to reduce the device mismatch using the transfer curve screening method to select the devices with similar characteristics to improve the current distribution. As mentioned earlier, the dynamic current balance is influenced by the threshold voltage (V_{th}) and transconductance (g_{fs}). Researchers in Fuji Electric (2016) screened the devices based on only V_{th}, and limited reduction in current imbalance was achieved since the effect of g_{fs} was ignored (Lim et al., 2014; Wang G. et al., 2014; Kokosis et al., 2017). The scanning method adopted in Ke et al. (2018) takes into account both V_{th} and g_{fs} for screening the devices. The g_{fs} and V_{th} have the contrary effect on the current sharing as during turn-on transition, the device with larger g_{fs} carries a more current, and the device with larger V_{th} carries a less current as can be seen in **Eq. 1** (Ke et al., 2018).

$$\varepsilon = \frac{|x_1 - x_2|}{(x_1 - x_2)/2} \tag{5}$$

$$\mu_\varepsilon = \frac{1}{n} \times \sum_{k=1}^{n} \varepsilon_k \tag{6}$$

In this method, first of all, the transfer curves of all devices are drawn and a particular procedure, as demonstrated in **Figure 10A**, is used to select the curves. Subsequently, selected curves are discretized and corresponding points of curves are compared under the equal drain current to get the V_{gs} difference. Under the equal drain current, x_1 and x_2 are abscissa values of the two curves that are used to measure the relative difference ε by using **Eq. 5**. The average of the relative difference (μ_ε), which represents the curve's proximity, is then determined using **Eq. 6**, where n is the total number of sampling points and k is the serial number. The dominance of the transfer curve scanning method over the conventional counterpart is shown in **Figure 10B**, where among thirty tested devices, the devices with the lowest μ_ε (No. 20 and No. 27) accomplish better current sharing as compared to the devices with the smallest ΔV_{th} (No. 15 and No. 17).

This method provides effective dynamic current sharing along with improved current rating. It can be used for more than two devices. Achieving a symmetrical layout is essential to adopt this method, as the effect of circuit discrepancies is avoided in the results by accomplishing a symmetrical layout. Nevertheless, the gate oscillation, voltage overshoot and energy losses cannot be reduced. This method does not provide increased switching speed, and static current imbalance cannot be minimized since R_{DSon} is not considered. Furthermore, screening procedures are generally expensive and time-consuming (Graovac, 2009).

5.4 Active Current Balancing Method

An Active Current Balancing (ACB) technique has been presented in Xue et al. (2014b), where an active gate driver is used to accomplish equal current sharing among parallel-connected SiC MOSFETs. The current imbalance occurs due to several reasons and it is hard to anticipate until the circuit is fabricated. ACB technique diminishes the current imbalance regardless of its cause (Xue et al., 2013). This method immediately detects a current imbalance, using a differential current transformer (DTC) employed at the drain of the parallel-connected devices as shown in **Figure 11B**. The current imbalance is suppressed by using the current balancing controller that actively adjusts the gate current with gate delay (Xue et al., 2014b). The system block diagram is illustrated in **Figure 11A**. There are three subsystem blocks: current sensing block (CSB), current balancing controller (CBC), and active gate control (AGC). The CSB detects the current using DTC whereas CBC takes the DCT's current difference signal and extracts the imbalance during turn-on and turn-off events. CBC generates the appropriate signal for AGC to eliminate the imbalance. Finally, the AGC uses the instructions from the CBC to adjust the gate signals using a variable gate delay (VGD) circuit during turn-on and turn-off events. In this way, three blocks work together to reduce the current imbalance.
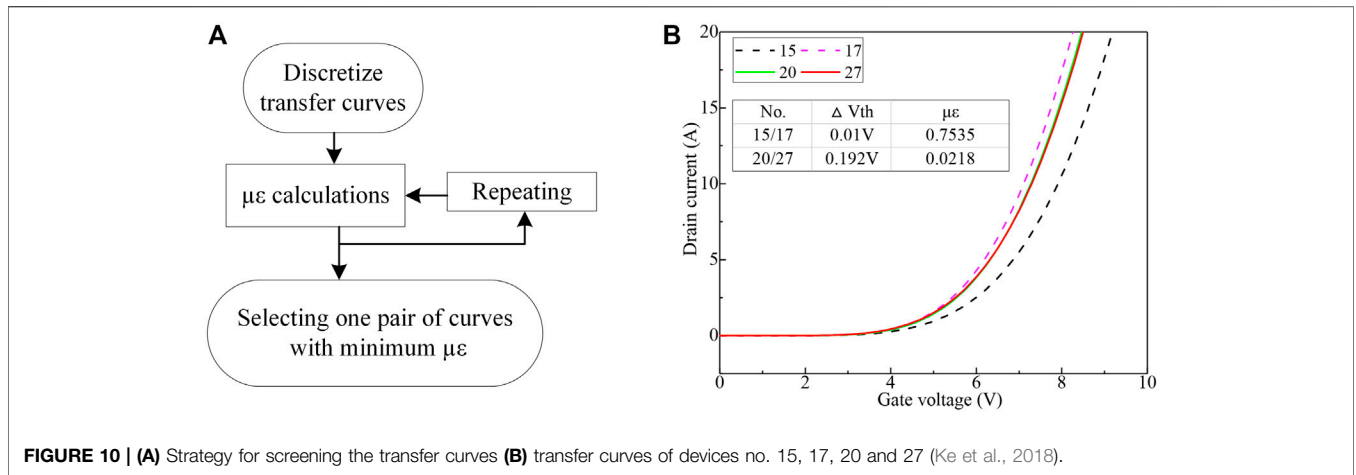
FIGURE 10 | (A) Strategy for screening the transfer curves **(B)** transfer curves of devices no. 15, 17, 20 and 27 (Ke et al., 2018).
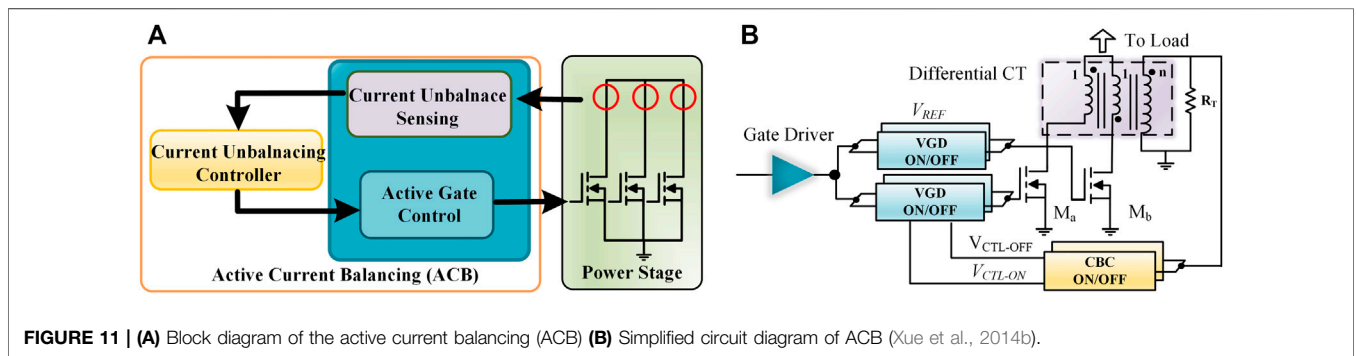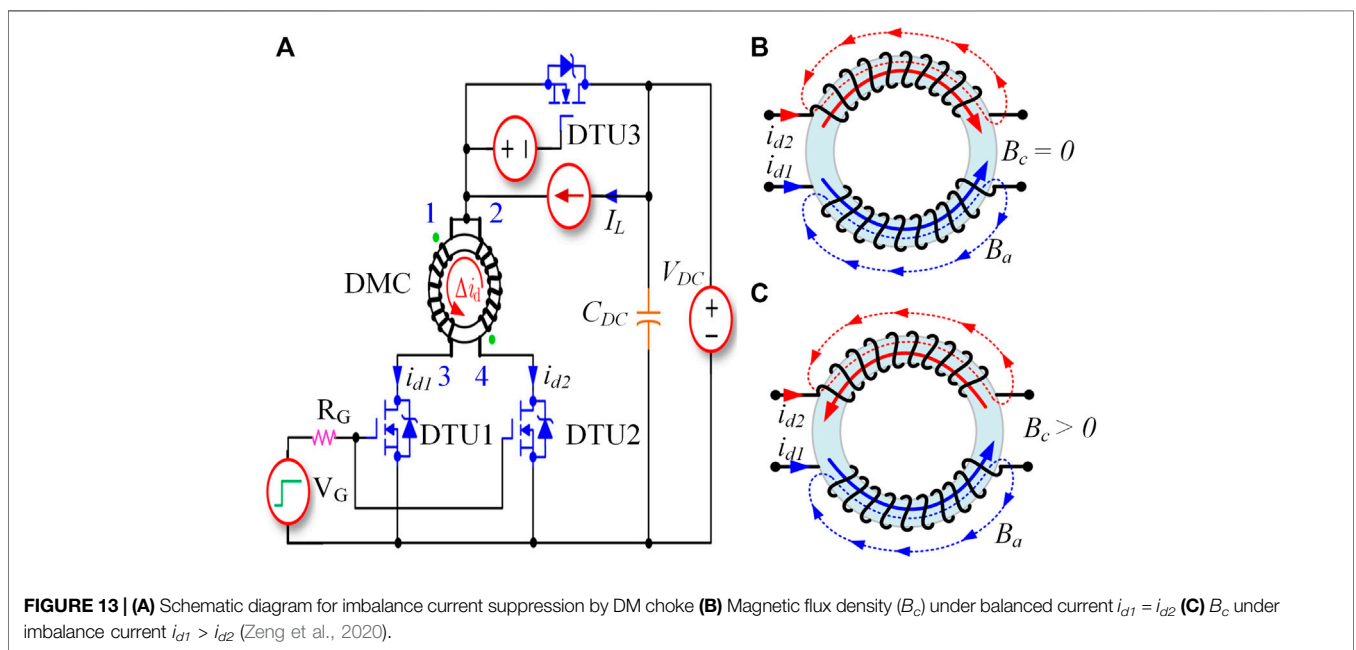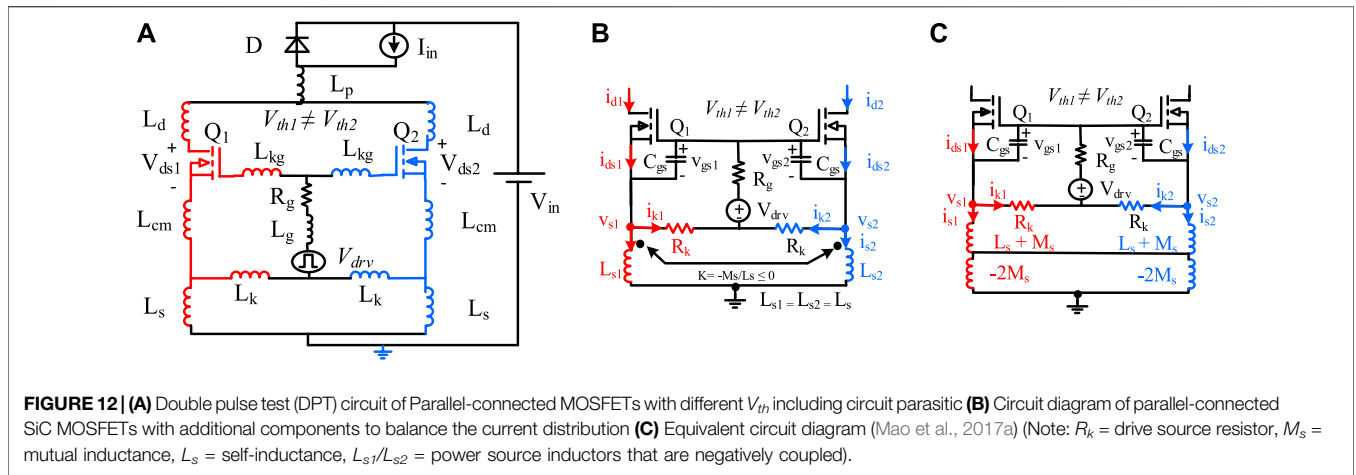

FIGURE 11 | (A) Block diagram of the active current balancing (ACB) **(B)** Simplified circuit diagram of ACB (Xue et al., 2014b).

This method offers excellent dynamic current balancing and slightly improves the static current balance (Xue et al., 2014b). Moreover, this technique ensures small gate oscillation and low voltage overshoot. Although it does not improve the switching speed and no reduction in the energy losses was achieved. The complexity and cost of active current balancing are relatively higher due to additional sensing and control circuits. Besides, it does not ensure a small size and volume. In addition, the effective current balancing does not start from the first cycle; it takes more than ten cycles (Xue et al., 2014b). The high-bandwidth multi-channel current sensor requirement limits the adoption of this technique to two devices (Xue et al., 2014a). To address the current sensing issue, (Xue et al., 2014a) proposed a solution to measure the device's current by using a PCB Rogowski coil current sensor. The design of the Rogowski coil is compact and planar along with high bandwidth, which allows accurate current measurement even with its dc component (Xue et al., 2014a). This method provides effective current sharing; however, the complexity of this method makes the integration tough.

5.5 Resistors and Coupled Power-Source Inductor Scheme

Current distribution can be improved by incorporating additional coupled power-source inductors and drive-source resistors as shown in **Figure 12**. This is an innovative passive current balancing solution that applied one gate driver to parallel-connected MOSFETS without requiring any sensors or feedback system. The circuit diagram of parallel-connected SiC MOSFETs is shown in **Figure 12A** along with the parasitic parameters. The authors assumed the layout to be exactly symmetrical and ignored the effect of all layout stray inductances including the common source inductance (L_{cm}) and the reduced diagram with compensating components as demonstrated in **Figure 12B**. The gate-source instance (L_k) assists current balancing without causing voltage stress. The resistor (R_k) enables voltage drop across the L_k. The loss impact of R_k in the gate loop is negligible as its size is extremely small compared with L_k. The power source inductor (L_s) also assists the current balancing but increases the voltage stress as well. To avoid the voltage stress caused by the L_s, they are negatively coupled as clarified in **Figure 12B**. The equivalent circuit diagram is shown in **Figure 12C** where coupled inductors are substituted as mutual inductance (M_s) and self-inductance (L_s). With the implementation of these additional components the power-source inductance gets amplified from L_s to $L_s + M_s$ and gets diminished from L_s to $L_s - M_s$ during differential-mode and common-mode path, respectively, enabling improved current distribution along with reduced voltage overshoot, ringing, and EMI noise. By using this passive solution, the peak current difference of parallel-connected SiC MOSFETs is reduced from 15 to 3% without any additional voltage stress or switching loss. In-depth analysis and equations to determine the values of different parameters

FIGURE 12 | (A) Double pulse test (DPT) circuit of Parallel-connected MOSFETs with different V_{th} including circuit parasitic **(B)** Circuit diagram of parallel-connected SiC MOSFETs with additional components to balance the current distribution **(C)** Equivalent circuit diagram (Mao et al., 2017a) (Note: R_k = drive source resistor, M_s = mutual inductance, L_s = self-inductance, L_{s1}/L_{s2} = power source inductors that are negatively coupled).

FIGURE 13 | (A) Schematic diagram for imbalance current suppression by DM choke **(B)** Magnetic flux density (B_c) under balanced current $i_{d1} = i_{d2}$ **(C)** B_c under imbalance current $i_{d1} > i_{d2}$ (Zeng et al., 2020).

such as mutual inductance, self-inductance and resistance are presented in Mao et al. (2017a). Based on this technique, new passive current balancing solutions can also be explored by replacing the R_k with an inductor or with the combination of resistor and inductor.

This innovative approach reduces the static and dynamic current imbalance and improves the overall current rating (Mao et al., 2017a). In addition, this method limits the gate oscillations, ringing, EMI issues and it is a low-cost solution. The effect of layout mismatch is excluded by realizing the symmetrical design in this method. Although the integration is not easy, this method can be implemented for more than two devices.

5.6 Differential Mode Choke Method

Inspired by the common-mode choke's success to mitigate common mode current in high frequency switching mode power supplies, authors in Zeng et al. (2020) employed a differential mode (DM) choke to suppress current imbalance among parallel-connected SiC MOSFETs, as the nature of imbalance current is a kind of differential mode. The implementation of DM choke for the current balancing between parallel-connected SiC MOSFETs is demonstrated in **Figure 13A**. The basic operation of the DM choke is illustrated in **Figures 13B,C**, which shows that there is no magnetic flux density (B_c) in the case of balanced current ($i_{d1} = i_{d2}$) and it is initiated by the imbalance current ($i_{d1} > i_{d2}$) as shown in **Figure 13C** (Zeng et al., 2020). From the impedance perspective, imbalance current is shown in **Eq. 7** where drain-source voltage is denoted by u_{ds} and Δi_d is the current difference. The impedances of parallel branches are represented by Z_1 and Z_2. The difference of current flows through the DM choke windings when the impedance of parallel branches is not equal. The current imbalance gets reduced by the induced voltage (v_m) shown in **Eq. 8** where L_m is magnetic inductance.

TABLE 2 | Evaluation of advanced current imbalance mitigation methods.

Features/Methods	Transfer Curve Screening Method	Resistors and Coupled Power-Source Inductor Method	Active Current Balancing Method	Differential Mode Choke Method
Static Current Imbalance Mitigation	☐ (white)	■ (dark green)	■ (light green)	■ (dark green)
Dynamic Current Imbalance Mitigation	■ (light green)	■ (dark green)	■ (dark green)	■ (dark green)
Current Rating Improvement	☐ (white)	■ (dark green)	■ (dark green)	■ (dark green)
Energy Losses	☐ (white)	■ (salmon)	☐ (white)	■ (salmon)
Voltage Overshoot	☐ (white)	☐ (white)	■ (light green)	☐ (white)
Gate Oscillation	☐ (white)	■ (light green)	■ (light green)	☐ (white)
Size and Volume	☐ (white)	■ (salmon)	■ (red)	■ (red)
Cost	■ (red)	■ (salmon)	■ (red)	■ (red)
Acceptance for more than two devices	■ (dark green)	■ (light green)	■ (red)	■ (light green)

■ ■ ■ ☐ ■ ■ ■

←————————————→

Worse   Better

During imbalance current suppression, one winding of DM choke senses energy ($P_{in} = v_m \Delta i_d$) and transforms electric energy into magnetic. Meanwhile, the other winding energy produces energy ($P_{in} = -v_m \Delta i_d$) and transforms magnetic energy into electrical energy (Zeng et al., 2020). In this way, DM choke uses magnetic flux as a medium to transmit current between parallel branches. In ideal conditions, it enables current imbalance suppression without any energy loss. Detailed guidelines to design the DM choke are presented in Zeng et al. (2020).

$$\Delta i_d = \frac{u_{ds}}{Z_1} - \frac{u_{ds}}{Z_2} = u_{ds} \frac{Z_1 - Z_2}{Z_1 Z_2} \qquad (7)$$

$$v_m = L_m (d\Delta i_d / dt) \qquad (8)$$

DM choke can effectively suppress both static and dynamic current imbalance even when different gate resistances are employed. In Zeng et al. (2020), parallel-connected SiC MOSFETs showed nearly identical current waveforms, including current rise and fall time and current peak value by employing DM choke. The DM choke improves the current ratings and reduces *dv/dt* which slightly diminishes the V_{ds} overshoot. Though the switching losses slightly increase, the turn-on and turn-off losses (E_{on} and E_{off}) of parallel-connected devices are nearly the same. It is recommended to use the bifilar winding for the DM choke since it minimizes leakage inductance and equivalent parallel capacitance (EPC) (Zeng et al., 2020). This method can be extended to more than two devices. Mechanisms of interaction between DM choke and SiC MOSFETs need further research to explore cross-talk, short-circuit, etc. (Zeng et al., 2020). The cost and design effort of the DM choke method are lower than ACB because the former one does not require any complex control scheme

and feedback. A comparison of the different methods is presented in **Table 2**.

6 STRAY PARAMETER EXTRACTION METHODS

The stray parameters in the circuit are the reason behind oscillations and also impact the current distribution. Their accurate estimation can provide necessary guidance to analyze and mitigate the oscillation and current imbalance. In the literature, simulation and experimental based studies have been carried out to extract the stray inductance. In simulation-based studies, different software like FastHenry, ANSYS Q3D, FastCap, finite-element analysis (FEA) have been reported to extract the stray inductance (Lianghua et al., 2006; Chen et al., 2009; Fu et al., 2013; Liu et al., 2014). Software-based extraction is complex and demands precise molding; however, complete information of structure, material, dimensions and interconnections of commercialized devices is usually not available. Besides, it is time-consuming and convergence is poor for complex packages. On the other hand, experimental methods are relatively simple and can be divided into time domain and frequency domain methods. Time-domain methods (Ariga et al., 2012; Li S. et al., 2014; Kexin et al., 2014) calculate the stray inductance by measuring the voltage U, rate of change of current *di/dt,* and then using the expression $U = L(di/dt)$. The accuracy of time-domain methods highly depends on the measuring probe's sensitivity and data processing technique. In addition, they extract the total inductance of the device and the power loop and individual inductances cannot be extracted; though, (Umetani et al., 2017) suggested a way to

calculate common source inductance. In high frequency/power applications, extraction of equivalent series inductance (ESL) of a dc-link capacitor, internal package inductance of device and stray inductance of busbar is crucial to anticipate and optimize the switching performance. Frequency domain methods reported in Sadik et al. (2016) and Liu et al. (2020) overcame some limitations of the time domain methods by exploiting the relationship of power loop parameters with underdamped frequency to calculate the stray inductance. Nonetheless, the discussed time domain and frequency domain methods only extract the stray inductance and the contribution of stray capacitance and package inductance remained obscure. New methods have been reported in Wang et al. (2020), Hu et al. (2021b), and Hu et al. (2021a) which can extract both stray inductance and stray capacitance by leveraging the parasitic ringing of the device and the impact on DC-link is explored in Krishna Moorthy et al. (2020), Meng et al. (2020), and Liang et al. (2021). Package inductance extraction of discrete devices is investigated in Liu et al. (2014), Liu et al. (2018a), and Xie et al. (2019) where two port extraction strategy outperforms the single port method (Liu et al., 2018a). Other researches have explored the techniques to minimize the stray parameters and in-depth investigation has been provided in Shtargot et al. (2012), Reusch and Strydom (2014), Meng et al. (2021), and Pace et al. (2021). Research on the extraction methods is still limited especially for extracting ESL of a dc-link capacitor and package inductance of discrete devices, bringing new research opportunities for young researchers.

7 CONCLUSION

Discrete package offers a cost-effective solution with design flexibility and scalability. Severe switching oscillations and limited current ratings are the main challenges faced by discrete packages. This paper organized the oscillations with respect to voltage and their underlying oscillations mechanisms are presented. Current distribution among parallel-connected discrete devices is categorized into static current imbalance and dynamic current imbalance. In addition, the root causes and negative impacts of the current imbalance are discussed. Furthermore, newly reported stray parameter extraction methods are also reviewed. Finally, state-of-the-art solutions to mitigate the oscillations and current imbalance are summarized. To fully leverage the potential of the discrete WBG devices, guidelines are given below:

1) Select a package with kelvin source. Among kelvin source packages, TO-263-7 offers low package inductance and TO-247-4 offers relatively high current ratings.
2) During layout design, the power loop and drive loop inductance should be kept as small as possible. A double layout design method can be adopted which can reduce voltage overshot by 8.3% and increase efficiency by 0.6% (Wang K. et al., 2017).
3) While selecting the gate resistor, a trade-off should be made between switching oscillations and switching losses. Careful selection of gate resistor should be made in such a way that it keeps the switching oscillations within safe limits without a substantial increase in the switching losses.
4) Compared to the gate resistor technique, the RC snubber has a minor increase in switching losses. Active gate driver can reduce the voltage overshoot and cross-talk by controlling the di/dt and dv/dt, but increases the circuit cost and design complexity. Ferrite bead is a good choice to mitigate high-frequency oscillation though it cost a slight increase in conduction losses. The benefits and drawbacks of different methods are summarized in **Table 1.**
5) To increase the current ratings, discrete devices are used in parallel. The devices with a minimum difference of R_{DSon} and Vth should be selected using the screening process to achieve better performance. Yet the benefits of the screening method should be weighed against the cost.
6) In parallel design layout, matching of common source inductance (L_s) is paramount to reduce the dynamic current imbalance and kelvin source packages can assist the design.
7) The reduction of gate resistance can improve the dynamic current sharing but does not improve the static current sharing. Implementation of additional source resistors can mitigate the static current imbalance but increase the energy losses and no improvement in the dynamic current sharing is obtainable. The active current balancing method is effective for mitigating both static and dynamic current imbalance, ensuring small gate oscillation and low voltage overshoot; however, it is hard to adopt for a higher number of devices. Among current sharing solutions, coupled power-source inductor method and differential mode choke method offer excellent current sharing features. The comparison of advanced methods is presented in **Table 2.**
8) Newly reported stray parameters extraction methods should be leveraged since they provide accurate estimation which can offer necessary guidance to analyze and design innovative solutions to mitigate the switching oscillation and current imbalance.

This work will assist the readers in the following ways:

1) It provides clear comprehension of the oscillation and current imbalance challenges associated with discrete devices along with their underlying mechanisms.
2) It offers the clear recognition of exciting solutions including their benefits and drawbacks.
3) To fully unleash the potential of discrete devices, guidelines are also provided.
4) The solutions are the guidelines illustrated in this survey can easily be extended to module packages and silicon-based devices.
5) The limited research on stray parameters extraction methods is also pointed out which reveals new research opportunities for young researchers.
6) The in-depth and comprehensive outline of challenges and their root causes provided in this work can stimulate the readers to come up with new solutions.

Research on discrete packages is still evolving and there will be methods in the future.

AUTHOR CONTRIBUTIONS

MT and SH conceptualized and performed the review process. MT was responsible for the main writing of the paper, while SH was responsible for the revision of the paper. XH provided the ideas and revised the manuscript based on his extensive knowledge and experience in power electronics. All authors contributed to the article and approved the submitted version.

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