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Study of Voltage Sag Detection and Dual-Loop Control of Dynamic Voltage Restorer

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Voltages sags have become the major issue that prevents the customers from getting high-quality power supply, and the dynamic voltage restorer (DVR) is considered an effective way to solve this issue. In this work, a method for voltage sag detection implemented in the time-domain is firstly addressed, which features highly accurate and fast response. Then, the dual-loop voltage–current control for the DVR is intensively investigated. Specifically, the optimal tuning of the inner current loop to achieve the maximum active damping is approached, and the voltage controller implemented in the discrete-time is developed. Tuning of the voltage loop based on critical damping is also approached, which features reduced settling time and avoidance of overshoot. The simulation and experimental results have verified the effectiveness of the proposed method for detection and management of voltage sags.

Keywords: voltage sags, dual-loop control strategy, active damping, critical damping, discrete-time domain

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1 INTRODUCTION

It has been reported that according to the statistics, voltage sags, which can cause enormous economic loss every year, account for over 70% of the cases that give rise to the power-supply deterioration, resulting in severe complaints from the customers (Nagata et al., 2017; Parreño Torres et al., 2019; Han et al., 2020). In other words, voltage sags have become the major issue that prevents consumers from getting the uninterrupted and high-quality power supply.

Many literature studies have been devoted to the control and management of voltage sags for a long period of time (Jowder, 2009; Nagata et al., 2017; Parreño Torres et al., 2019; Gontijo et al., 2020; Han et al., 2020). Presently, among the proposed methods, the dynamic voltage restorer (DVR), which is connected between the grid and the load, has been commonly considered an effective and economical way to solve the issue of voltage sags, and a high-quality power supply can be expected. The basic idea of DVR is to generate the compensation voltage through the power-electronics–based converter, so as to keep the load-side voltage unaffected when sags occur on the grid-side voltage. Consequently, the fast and accurate voltage sag detection and the effective voltage regulation strategy are of almost importance to the DVR to achieve a high level of performance.

With regard to sag detection, many methods have been developed from either the time- or frequency-domain, such as the Kalman filter (Cisneros-Magaña et al., 2018), fast Fourier transform (Wang Y et al., 2019), wavelet transform (Hu et al., 2020), and approaches based on instantaneous reactive power theory (Pradhan and Mishra, 2019; Tu et al., 2020; He et al., 2021). Specifically, it has been proved that both the output speed and the accuracy of the Kalman filter are related to the system model, and there is also convergence issue which can result in an unstable response. Alternatively, methods based on the Fourier or wavelet transforms require historical data, resulting in heavy

computation burden which is, therefore, unacceptable for real-time signal implementation with a commercial digital signal processor (DSP) or microcontroller unit (MCU). Although this issue can be avoided with the employment of a sliding window as addressed by Wang J et al. (2019), it has, however, been proved that there are also stability and high-frequency noise amplification issues, which need careful considerations for the practical implementation with a DSP or MCU. The method based on instantaneous reactive power theory is suitable for a three-phase system and has, in fact, been studied and implemented in a lot of literature studies, such as He et al. (2021) and Pradhan and Mishra (2019). This kind of method, however, has a blind zone for the detection of unbalanced voltage drops.

On the contrary, for the DVR, the LC filter is commonly employed at the output terminal of the converter. This can put a great challenge to the system's overall control since the LC filter has resonance phenomenon and causes stability problem (Wang J et al., 2019; Naidu et al., 2019; Bajaj, 2020; Xiong et al., 2020). Although various passive methods, for instance, connecting resisters in parallel or series with the capacitor, have been developed and can be employed to increase the system's physical damping, this kind of method is however not preferred, since it can further cause other issues, such as increase in power loss and deteriorated filter effectiveness for high-frequency voltage harmonics (Pal and Gupta, 2020; Vo Tien et al., 2018). On the contrary, the counterpart, i.e., active damping methods, is realized by modifying the control structure, which can avoid the aforementioned issues faced by the passive methods, and has therefore been intensively investigated in recent years (Suppioni et al., 2017; Liu et al., 2018; Roldán-Pérez et al., 2019; Liu et al., 2021; Xiong et al., 2021). Specifically, the following two types of control strategies: 1) single-loop voltage and 2) dual-loop voltage–current control, can be employed to achieve enhanced active damping. Nevertheless, it has been addressed that the single-loop voltage control method suffers from the issues of poor stability and constrained loop-bandwidth, which can result in an oscillatory and slow transient response of the output voltage. Hence, this approach is not preferred for high-performance applications, although it has the merits of simple structure and easy implementation.

Alternatively, the dual-loop control method, in which additional active damping can be achieved by incorporating the current loop, has been proved to have improved performance compared to that of the single-loop control method. Hence, numerous studies have been dedicated to the analysis and tuning of the current loop. Commonly, the frequency response analysis is employed in these studies, where the bandwidth of the voltage loop is tuned to be one-fifth to one-tenth of that of the current loop, which is a rule of thumb for a common dual- or multi-loop control structure for grid-following converters. This rule is however not applicable for the dual-loop regulated DVR, since the objective of the current loop is to improve damping, instead of signal tracking where bandwidth is concerned. Hence, the explicit guidance for tuning of the current loop needs to be clarified, which is approached in this work. Also, based on the equivalent plant which is damped with the current loop, a voltage controller implemented in the discrete-time domain is developed, which features fast response and avoidance of overshoot.

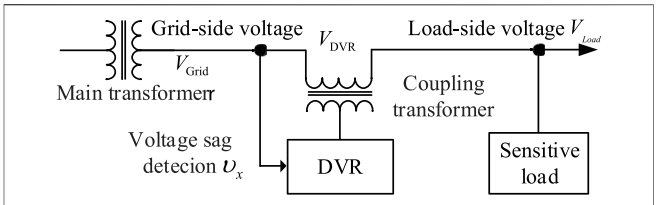

FIGURE 1 | Voltage sag compensation of the DVR.

To do that systematically, the rest of this work is organized as follows: **Section 2** begins with the description of the basic principle of DVR succinctly, and then based on signal reconstruction, a method for voltage sag detection in the time-domain is developed, which features low settling time, high accuracy, and frequency adaptive characteristic. The inner current loop is addressed in **Section 3**, with the objective of obtaining the maximum active damping. The developed discrete voltage controller is addressed in **Section 4**, in which the tuning of the voltage loop based on optimization of settling time and overshoot is also addressed. The simulation and experimental verifications are presented in **Section 5**, before concluding the findings in **Section 6**.

2 PRINCIPLE OF DVR AND VOLTAGE DROP DETECTION

As shown in **Figure 1**, the load-side voltage V_{Load} can be expressed as the superposition of the grid-side voltage V_{Grid} and the compensation voltage V_{DVR}, which can be expressed as follows:

$$V_{\mathrm{Load}} = V_{\mathrm{Grid}} + V_{\mathrm{DVR}}. \tag{1}$$

In this manner, when a fault occurs in the main grid or adjacent transmission line, the voltage drop can occur on the grid-side voltage V_{Grid}. The DVR detects the voltage sag and injects the compensation voltage V_{DVR} to the grid through the coupling transformer. In this manner, the load-side voltage V_{Load} remains stable and the voltage supply for the sensitive load is unaffected.

According to the Fourier theory, the periodic grid voltage can be expressed as the sum of different frequency signals, which can be expressed as follows:

$$\begin{aligned} \upsilon_x &= \sum_{h=1}^{\infty} \upsilon_x^h \\ &= \underbrace{A_1 \sin(\omega_1 t + \theta_{l1})}_{\upsilon_x^1} + \underbrace{A_2 \sin(2\omega_1 t + \theta_{l2})}_{\upsilon_x^2} + \cdots, \end{aligned} \tag{2}$$

where ω_1 is the grid frequency and A_h, θ_{lh} are the amplitude and initial phase of υ_x^h, respectively. Also, the fundamental voltage υ_x^1

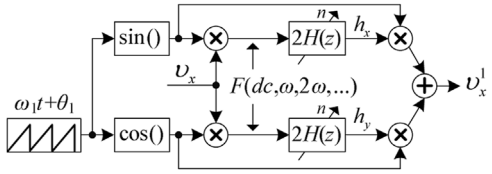

FIGURE 2 | Detection of the fundamental voltage.

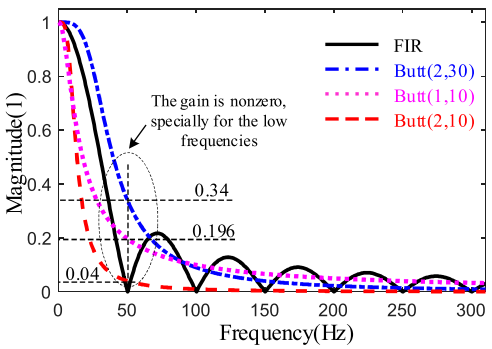

FIGURE 3 | Frequency response of the LPFs.

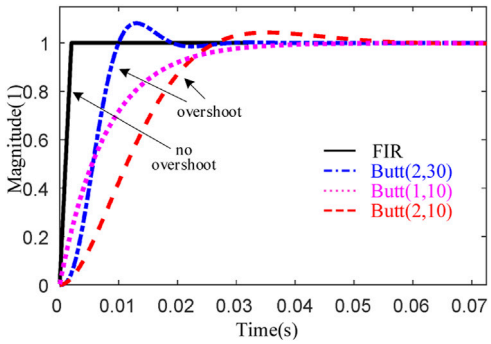

FIGURE 4 | Step response of the LPFs.

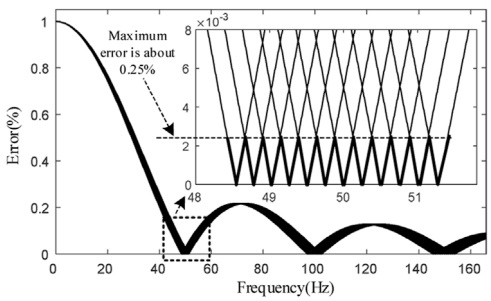

FIGURE 5 | Frequency adaption for the FIR filter.

can be expressed as the sum of two orthogonal signals, which is shown as follows:

$$v_x^1 = h_x \sin(\omega_1 t + \theta_1) + h_y \cos(\omega_1 t + \theta_1), \tag{3}$$

where θ_1 is the initial value of the phase for implementation, which has no impact on the output value of v_x^1, while the expressions of h_x and h_y are expressed as follows:

$$\begin{aligned} h_x &= A_1 \cos(\theta_{l1} - \theta_1), \\ h_y &= A_1 \sin(\theta_{l1} - \theta_1). \end{aligned} \tag{4}$$

It can be noted that θ_{l1}, θ_1, and A_h are constant; hence, h_x and h_y are dc signals. In order to obtain their values, the following derivations are performed:

$$\begin{aligned} &v_x \times \sin(\omega_1 t + \theta_1) = \\ &\frac{1}{2}\left[\underbrace{A_1 \cos(\theta_{l1} - \theta_1)}_{h_x} + F(\omega_1, 2\omega_1, 3\omega_1, \cdots)\right], \end{aligned} \tag{5}$$

$$\begin{aligned} &v_x \times \cos(\omega_1 t + \theta_1) = \\ &\frac{1}{2}\left[\underbrace{A_1 \sin(\theta_{l1} - \theta_1)}_{h_y} + F(\omega_1, 2\omega_1, 3\omega_1, \cdots)\right]. \end{aligned} \tag{6}$$

Combining **Eqs 2–5**, the structure for the detection of the fundamental voltage v_x^1 can be obtained, which is shown in **Figure 2**, where H(z) is the low-pass filter.

From **Eqs 4, 5**, it can be observed that the frequency of the alternating signals is multiple of the fundamental frequency. Therefore, in this work, a finite impulse response (FIR) filter is employed, whose expression is shown as follows:

$$H(z) = \frac{1}{n} \cdot \frac{1 - z^{-n}}{1 - z^{-1}}, \tag{7}$$

where n is the number of sampling points within a period of the grid voltage. For comparison, the magnitude responses of the FIR filter and Butterworth filter Butt(a, b) are illustrated in **Figure 3**, noting that a is the order and b is the cutoff frequency of the filter. It can be noted that the amplitude of the FIR filter at the fundamental frequency ω_1 as well as the high frequencies $h\omega_1$ is zero. Hence, the alternating signal in **Eqs 4, 5** can be canceled completely with the FIR filter of **Eq. 7**. On the contrary, the magnitude response of Butt(a, b) presents a monotonic characteristic. However, it can be observed that the gains at the lower frequencies are non-zero, which can further result in poor accuracy of dc signal detection in **Eqs 4, 5**.

It should be mentioned that the output accuracy of Butt(a, b) can be improved by reducing the cutoff frequency b. This is, however, at the cost of the reduction of the bandwidth for the filter, leading to a slow transient response. As shown in **Figure 4** where the step response of different filters is illustrated, comparing Butt(2,30), the settling time is much extended for the case of Butt(1,10) and Butt(2,10). Alternatively, the fastest response can be obtained with the employment of FIR filter, and no overshoot can be observed.

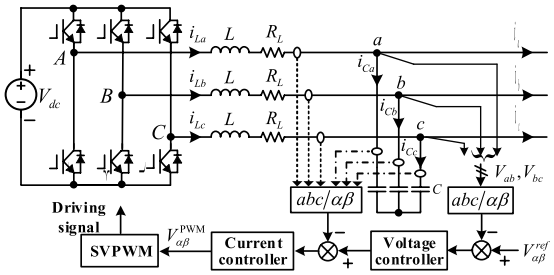

FIGURE 6 | Main circuit of the DVR and the related dual-loop control method.

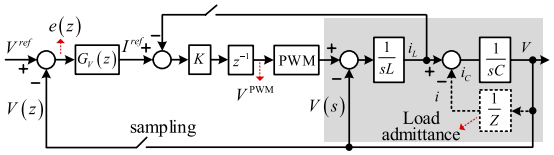

FIGURE 7 | Block diagram of the dual-loop control method.

From the above analysis, it can be concluded that, from the viewpoint of accuracy and speed of detection of h_x and h_y in **Eqs 4, 5**, the performance of FIR filter is superior to that of Butt(a, b). The main shortcoming of employing the FIR filter (7) is the storage requirement, which is, commonly, RAM for microprocessors. The next step is to achieve frequency adaption for the FIR filter, since the grid voltage ω_1 can vary within a certain range. In this work, the order n of FIR is dynamically adjusted according to the real value of ω_1 which is obtained with a frequency locked loop. As shown in **Figure 5**, the maximum error is 0.25% approximately.

In this manner, with the developed method illustrated in **Figure 2**, the fundamental grid voltage can finally be obtained, whose amplitude and phase are employed for voltage sag identification. It should be noted that the developed method can be employed for either three- or single-phase configuration, although only the three-phase one is taken as an example for analysis in this work.

3 OPTIMAL ACTIVE DAMPING TUNING OF THE INNER CURRENT LOOP

In **Figure 6**, the main circuit and the corresponding dual-loop control method of the three-phase DVR are both illustrated. The dc bus voltage can be supplied by either a rectifier or an energy storage system. Hence, a dc source Vdc can be assumed for simplicity here. The output of the converter is connected to the LC filter, where L is the inductor, C is the capacitor, and R_L is the equivalent resistor which is employed for emulating the power loss of the converter. After the filter, the voltage is fed to the coupling transformer shown in **Figure 1**. The reference voltage $V_{\alpha\beta}^{ref}$ is the detected voltage sag, which is compared with the measured capacitor voltage. The error signal is fed to the voltage controller, whose output is the reference of the inner current loop. It should be noted that either the capacitor current i_C or the inductor current i_L can be measured and fed back for regulation. The difference of feeding back of i_C and i_L lies in that i_L can be employed for the overcurrent protection of the converter. In this work, the inductor current is employed since it can be adopted for overcurrent protection of the converter.

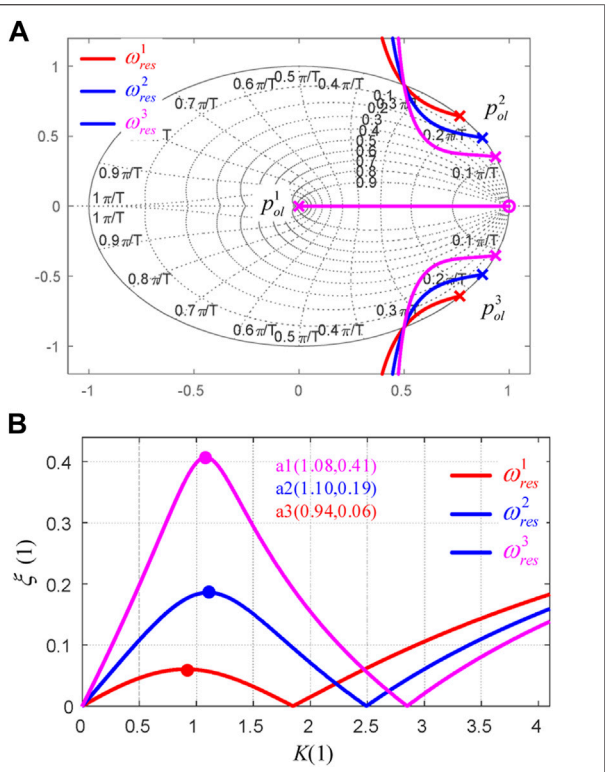

FIGURE 8 | Root locus and active damping of the plant when K varies, where **(A)** shows the root locus and **(B)** shows the plot of K vs ξ.

For better illustration, the dual-loop control method is further depicted in **Figure 7**, where V^{ref} represents the reference voltage (either V_α^{ref} or V_β^{ref}), $G_V(z)$ is the voltage controller, K is the current loop proportional gain, z^{-1} is the one-sampling delay, and V^{PWM} is the modulation signal. It should be noted that the case of $R_L = 0$ is employed here, in order to emulate the worst case without any physical damping.

The modulation signal V^{PWM} is updated at each sampling point and kept constant during the sampling period. Hence, the zero-order holding method is employed for discretization here. Combining **Figure 7**, the transfer function of the output voltage V related to the current reference I^{ref} can be derived as follows:

$$G_{\mathrm{PL}}^{V}(z) = \frac{V(z)}{I^{ref}(z)} = \frac{K \cdot [1 - \cos(\omega_{res} \cdot T_s)] \cdot (z+1)}{z^3 - 2z^2\cos(\omega_{res}T_s) + b_1 \cdot z - \dfrac{K}{\omega_{res}L}\sin(\omega_{res}T_s)}, \tag{8}$$

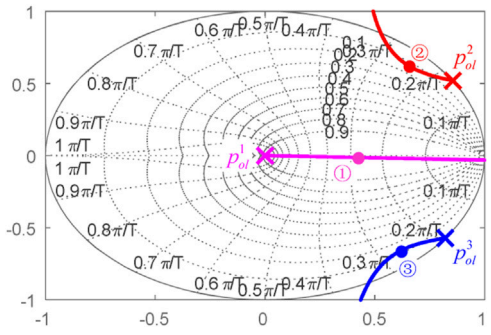

FIGURE 9 | Pole distribution of the equivalent plant in the SRF for K=K_{opt}.

where $b_1 = 1 + K/(\omega_{res}L) \cdot \sin(\omega_{res}T_s)$, T_s is the sampling period, and $\omega_{res} = \sqrt{1/(LC)}$ is the LC resonance frequency.

Recalling **Figure 7**, it can be observed that **Eq. 8** is actually the equivalent plant of the voltage controller. Since the inclusion of the current loop is for active damping, the damping characteristic of **Eq. 8** is investigated. As shown in **Figure 8A**, with the increase of K, the conjugate poles $p_{ol}^{2,3}$ which are located on the unit circle and related to the filter resonance move inside of the unit circle, and the damping ξ increases gradually, as shown in **Figure 8B**. For the case of K=K_{opt} = 1.1 of ω_{res}^2, the active damping ξ reaches the maximum value of 0.19. With the further increase of K, the pole moves to the unit circle, and the active damping ξ decreases instead. When K=K_{max} = 2.5, the poles cross the unit circle, resulting in a non-minimum phase system. This certainly should be avoided. From the above analysis, it can be concluded that, for the optimal gain of K=K_{opt} = 1.1, the maximum active damping can be achieved for the equivalent plant.

4 THE DEVELOPMENT OF VOLTAGE CONTROLLER IN THE DISCRETE-TIME DOMAIN

In order to have zero steady-state error signal tracking of the sinusoidal waveform, the following analysis is performed in the synchronous reference frame (SRF). Hence, with the replacement of z with $z = ze^{j\omega_1 T_s}$ in **Eq. 8**, the equivalence of the voltage controller in the SRF can be obtained. With the substitute of the optimal gain K_{opt} for (8), the distribution of poles of the equivalent plant for the case of ω_{res}^2 is depicted in **Figure 9**, as illustrated with the solid circle "●."

Observing **Figure 9**, it can be noted that, with the optimal damping of K_{opt}, the damping ξ of the poles on branch ① is unity; however, the damping of the other poles $p_{ol}^{2,3}$ located on branches ② and ③ is only 0.19, which can be observed from **Figure 8B**. Therefore, the equivalent plant actually features a weak damping characteristic, even with the optimal active damping gain K_{opt} employed.

With the objective of canceling the above weak damping poles, in this work, a voltage controller is developed, whose transfer function is shown as follows:

$$G_V^{\mathrm{SRF}}(z) = K_V \cdot \frac{z^3 e^{-j3\omega_1 T_s} - 2z^2 e^{-j2\omega_1 T_s} \cdot c + (1+a) z e^{-j\omega_1 T_s} - a}{z^2 \cdot (z-1)}, \quad (9)$$

where $c = 2e^{-j2\omega_1 T_s}\cos(\omega_{res}T_s)$, $a = K\sin(\omega_{res}T_s)/(\omega_{res}T_s)$, and K_V is the controller gain. It can be noted that **Eq. 9** achieves the pole zero cancellation with the equivalent plant (8), and the denominator of **Eq. 9** provides infinite open-loop gain for the dc signal in the SRF, which equivalently achieves infinite gain for the ac signal alternating at ω_1 in the stationary reference frame, resulting in zero steady-state tracking error for the sinusoidal signal.

5 TUNING OF THE VOLTAGE LOOP WITH THE EMPLOYMENT OF THE DEVELOPED CONTROLLER BASED ON CRITICAL DAMPING

Combining (8), (9), and **Figure 7**, the open-loop transfer function of the voltage loop can be derived. Then, by varying the controller gain K_V from zero to infinity, the root locus of the voltage loop can be obtained, as shown in **Figure 10**. It can be noted that, for lower values of K_V, the closed-loop poles on branches ① and ② are initially on the real axis and move toward the unit circle with the further increase of K_V, while for higher values of K_V, the poles on both ① and ② can move outside of the circle, resulting in an unstable response of the voltage loop.

Nevertheless, the damping and magnitude of the poles obtained from the discrete root locus analysis are not straightforward as those derived in the continuous-time domain. Hence, the damping and magnitude of the equivalence of the poles in the continuous-time domain are employed for analysis, which can be expressed as follows:

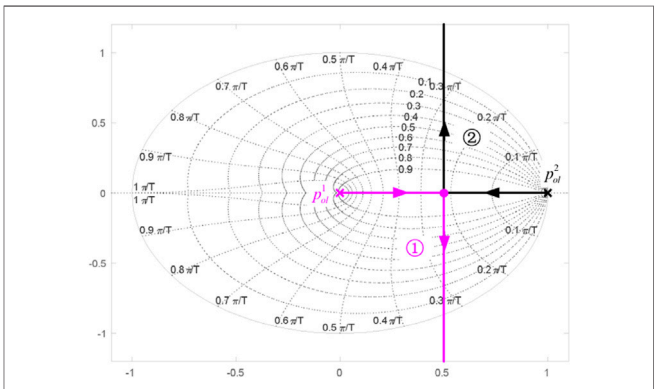

FIGURE 10 | Root locus diagram of the voltage loop with the employment of the developed controller.

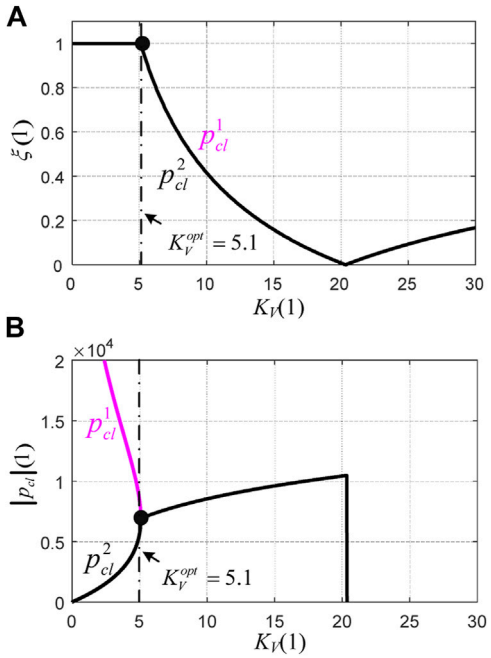

FIGURE 11 | Curve of **(A)** Kv vs ξ and **(B)** Kv vs $|p|$.

$$\xi = \sqrt{\frac{1}{\left\{\arctan\left(\frac{\mathrm{Im}\left(p_{cl}^{z}\right)}{\mathrm{Re}\left(p_{cl}^{z}\right)}\right)\cdot\frac{1}{\ln\left|p_{cl}^{z}\right|}\right\}^{2}+1}} \tag{10}$$

and

$$\left|p_{cl}\right| = \frac{\ln\left|p_{cl}^{z}\right|}{T_s}, \tag{11}$$

where p_{cl}^z is the pole in the z-domain, ξ is the damping, and $|p_{cl}|$ is the equivalent magnitude in the s-domain.

For better illustration, the damping ξ and magnitude $|p_{cl}|$ of the poles in **Figure 10** are further calculated, and the plots of Kv vs ξ and Kv vs $|p_{cl}|$ are depicted in **Figures 11A,B**, respectively. To begin with, as shown in **Figure 11A**, for K_V<*Kopt V*, unity damping is achieved for both poles $p_{cl}^{1,2}$, and the magnitude of p_{cl}^2 is much lower than that of $|p_{cl}^1|$. As a result, p_{cl}^2 is the dominant pole, and the voltage loop is overdamped in this case. As a result, a monotonically rising step response can be expected. In particular, for K_V = *Kopt V*, it can be noted that $|p_{cl}^1| = |p_{cl}^2|$ from **Figure 11B**, and unity damping is valid for both poles. With the further increase of K_V, the damping of $p_{cl}^{1,2}$ decreases sharply, resulting in overshoot in the step response. Therefore, the voltage loop is critically damped for the case of K_V = *Kopt V*.

However, for K_V>*Kopt V*, the magnitude of $|p_{cl}^{1,2}|$ increases overall, while the added value is relatively limited. However, in this case, the damping ξ of both poles $p_{cl}^{1,2}$ decreases sharply, resulting in deteriorated performance, which is certainly undesired.

Form the above analysis, it can be concluded that, for K_V = *Kopt V*, the possible maximum magnitude of both $p_{cl}^{1,2}$ can be achieved. Besides, in this case, the unity damping for $p_{cl}^{1,2}$ is valid. Consequently, the voltage loop is critically damped, which means minimum settling time with the avoidance of overshoot for the step response can be expected.

6 SIMULATION AND EXPERIMENTAL RESULTS

To verify the effectiveness of the developed method for voltage sag detection and the controller for voltage regulation of DVR, the simulation is performed in Matlab/Simulink. In particular, the parameters are shown as follows: the filter inductance of 0.4 mH, the filter capacitor of 180 uF, the switching frequency of i5 kHz, the sampling frequency of 10 kHz, and the grid line voltage of 380 V.

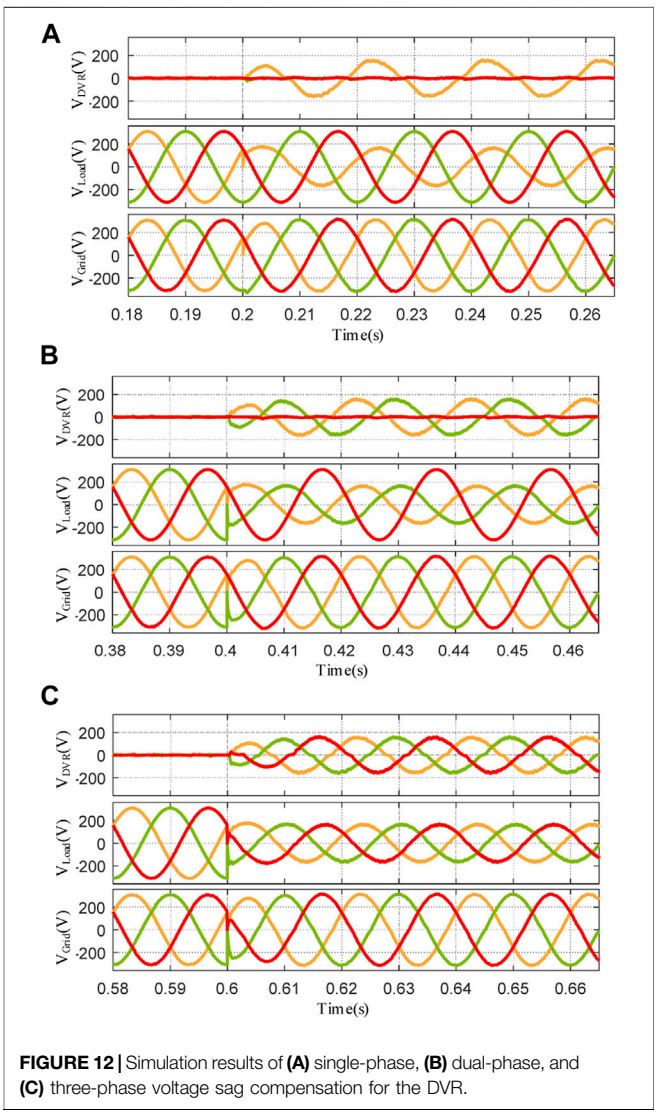

FIGURE 12 | Simulation results of **(A)** single-phase, **(B)** dual-phase, and **(C)** three-phase voltage sag compensation for the DVR.

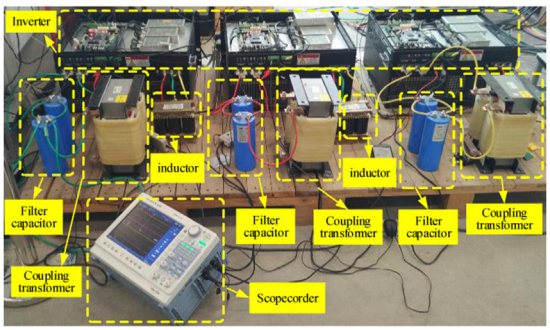

FIGURE 13 | Experimental setup for voltage sag compensation.

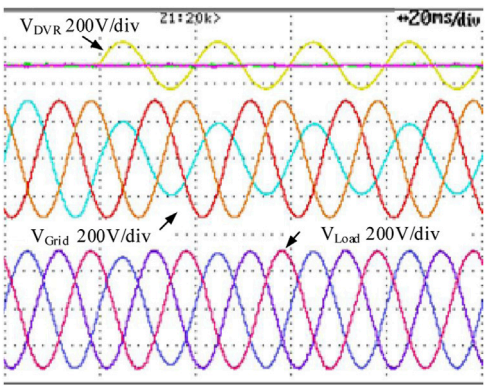

FIGURE 14 | Experimental results of single-phase voltage sag compensation.

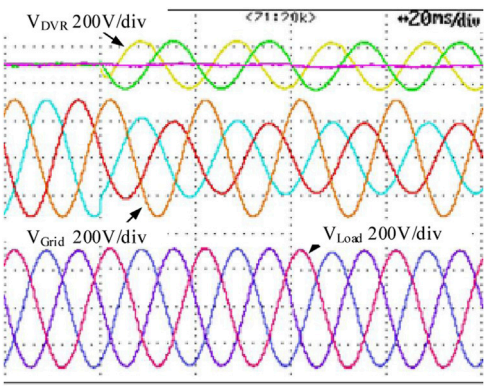

FIGURE 15 | Experimental results of dual-phase voltage sag compensation.

In **Figure 12**, the simulation results for the single-phase, dual-phase, and three-phase voltage sags of 40% are illustrated, where the grid-side voltage, the load-side voltage, and the DVR voltage are represented as V_{Grid}, V_{Load}, and V_{DVR}, respectively. It can be noted

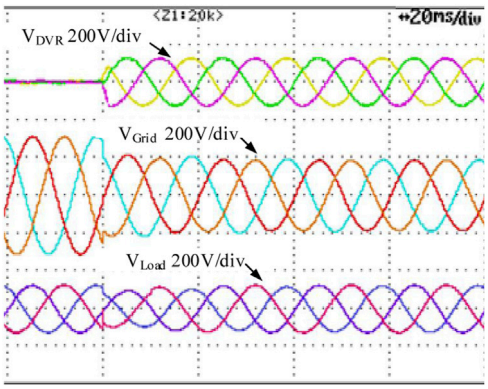

FIGURE 16 | Experimental results of three-phase voltage sag compensation.

that, for the three evaluated cases, the DVR can generate the required voltage within 2 ms approximately, and no overshoot can be observed. In this manner, the load-side voltage remains unaffected and a high-quality power supply can be guaranteed.

The experimental setup is shown in **Figure 13**, whose parameters are the same as those addressed for simulation. The rated capacity of the setup is 100 kVA. The digital controller is a TMS320F28346 DSP and a EP3C25 FPGA, and the DSP is responsible for the calculation and data process, while the FPGA is employed for logic management and protection. Also, the measuring equipment includes a DL850 ScopeCorder and several P5200 differential probes.

The experiment is performed for different voltage sag sceneries. To begin with, the single-phase voltage sag of 40% is investigated. As shown in **Figure 14**, it can be noted that the DVR compensation voltage has a fast response with no overshoot, which is in good agreement with the theoretical findings addressed before. In this manner, the load-side voltage is stable regardless of the sag on the grid-side voltage.

Also, the case of dual-phase voltage sag of 40% is addressed. The experimental result is shown in **Figure 15**, where it can be observed the settling time is about 2 ms with no overshoot, which agrees with the analytical findings addressed before.

Finally, the case of voltage sag for the three-phase voltage is investigated. As shown in **Figure 16**, the amplitude of the three-phase voltage sag is 40% simultaneously, and the compensation voltage is fast and accurate, and a similar conclusion to that of the single- and dual-phase voltage drops can be drawn, i.e., reduced settling time and avoidance of overshoot. It should be emphasized that if non-linear loads are considered, the load-side voltage can be distorted by the high-frequency harmonic currents, since the voltage controller developed in this work is employed for handling the fundamental frequency voltage.

7 CONCLUSION

In this work, the DVR for voltage sag compensation is intensively addressed. A method implemented in the time-domain for voltage sag

identification is developed, which features fast response, high accuracy, and frequency adaptive characteristic. Then, the dual-loop voltage–current regulation for the DVR is approached, where the optimal tuning of the current loop to achieve the maximum active damping is addressed. Also, a discrete voltage controller is developed, and tuning of the voltage loop based on critical damping is lastly addressed, which can be employed to achieve a fast response and avoidance of overshoot for output voltage regulation.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/supplementary material, and further inquiries can be directed to the corresponding author.

AUTHOR CONTRIBUTIONS

All authors listed have made a substantial, direct, and intellectual contribution to the work and approved it for publication.

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