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A capacitor-based DC circuit breaker for HVDC power grid

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DC circuit breakers (DCCBs) are the critical equipment to isolate faults in high-voltage DC grids. The improvement of interruption performances of capacitor-based DCCBs (C-DCCBs) has been widely researched. However, in previous papers, the adaptive reclosing of C-DCCBs is less considered and requires further research. In this paper, a novel C-DCCB with adaptive reclosing ability is proposed. The interruption and adaptive reclosing processes of the proposed C-DCCB are presented. The fault current is interrupted by charging the internal capacitor to a voltage higher than the system voltage. The fault property identification is key to adaptive reclosing and is achieved using the capacitor discharge characteristic. The parameter designs are analyzed to guarantee successful interruptions, and the identification criteria are proposed to serve the adaptive reclosing. On the one hand, the proposed C-DCCB has good interruption performances; on the other hand, an adaptive reclosing strategy is designed for the proposed C-DCCB to restore the power transmission whereas avoiding a second fault shock, which is the main contribution of this paper. Finally, the interruption and adaptive reclosing performances of the proposed C-DCCB are validated using PSCAD/EMTDC simulations.

KEYWORDS

adaptive reclosing, dc circuit breaker, fault property identification, HVDC grid, thevenin equivalent circuits

1 Introduction

High-voltage DC (HVDC) grids have great application potential in renewable energy integration, island power supply and AC grid interconnection (Hertem and Ghandhari, 2010)- (An et al., 2017). However, after a DC fault occurs, the DC fault current quickly increases and the DC voltage rapidly drops, which seriously affects the safe and stable operation of HVDC grids. DC circuit breakers (DCCBs) can soon isolate the fault area and maintain the normal operation of the nonfault area. Traditionally, DCCBs are divided into mechanical, solid-state and hybrid DCCBs (Bucher and Franck, 2016)- (Chen et al., 2021). Several mechanical DCCBs use semiconductors such as thyristors to improve the interruption performance, obscuring the boundary between mechanical and hybrid DCCBs (Wen et al., 2018)- (Wu et al., 2020a). In this paper, DCCBs that interrupt the fault current by semiconductors with turn-off ability are called semiconductor-based DCCBs (S-DCCBs); DCCBs that interrupt the fault current by charging the internal capacitor to a voltage higher than the system voltage are called capacitor-based DCCBs (C-DCCBs).

In S-DCCBs, the main breaker (MB), which is composed of insulated-gate bipolar transistors (IGBTs) or integrated gate commutated thyristors (IGCTs), can interrupt the fault current. In (Hafner and Jacobson, 2011; Hassanpoor et al., 2015; Wen et al., 2016; Jovcic et al., 2019), S-DCCBs conduct the system current with small conduction losses during a normal state. During interruptions, the system current is commutated into the MB and then interrupted by the MB. S-DCCBs have attracted considerable attention because of good interruption performances. In China, S-DCCBs with different topologies have been applied to the Zhoushan DC project and Zhangbei DC grid project, respectively (Jovcic et al., 2019). However, the interruption capacity of S-DCCBs is limited by the turn-off capacity of IGBT and IGCT, and IGBT and IGCT bring high construction costs.

For C-DCCBs, the system current is commutated into the internal capacitor during the interruption. It gradually decreases to 0 after the capacitor is charged to a voltage higher than the system voltage. C-DCCBs usually use semiconductors without turn-off ability to save the construction cost, such as thyristors and diodes. C-DCCBs with different topologies in China have been applied to the Zhangbei DC grid project and the Nan'ao DC grid project, respectively (Liu, 2019)- (Chen et al., 2018). Many topologies have been proposed to improve the C-DCCB performances regarding bidirectional interruption, interruption speed, pre-activation ability, etc. The C-DCCB in (Wu et al., 2020b) achieves bidirectional current commutation using bridge-type branches. In (Jamshidifar and Jovcic, 2018), the C-DCCB uses fast thyristors to quickly interrupt large fault currents. In (Sima et al., 2019), the capacitor is inserted into a bridge composed of spark gap switches, and this topology guarantees that the C-DCCB can consecutively interrupt the fault current. The pre-activation of DCCB achieves that the DCCB operation time overlaps with the protection time, which effectively reduces the fault interruption time (Hafner and Jacobson, 2011). However, the C-DCCBs in (Chen et al., 2018; Jamshidifar and Jovcic, 2018; Liu, 2019; Sima et al., 2019; Wu et al., 2020b) do not have the pre-activation ability. For C-DCCBs in (Wu et al., 2019) and (Guo et al., 2020), the thyristors in the MB can temporarily conduct the load current, thus achieving the pre-activation ability. In (Augustin et al., 2021), a C-DCCB family consisting of one unidirectional and six bidirectional concepts is presented, and all concepts have the pre-activation ability. Nevertheless, the reclosing of C-DCCBs is not considered in (Liu, 2019)- (Augustin et al., 2021).

Considering that most overhead line faults are transient, the DCCB should reclose in time to restore the power transmission after isolating (Wang et al., 2203). However, in case of a permanent fault, the direct reclosing will bring a second fault shock, which is harmful to the HVDC grid. To solve this problem, the permanent and transient faults should be discriminated, and the DCCB only reconnects the HVDC grid to the isolated line when the fault is transient, which is called adaptive reclosing.

The fault property identification is key to the adaptive reclosing strategy. Because the permanent and transient faults result in different boundary conditions, the fault property can be identified according to the traveling wave characteristics (Wang et al., 2203)- (Mei et al., 2021). In (Wang et al., 2203), the voltage pulse is produced by the hybrid MMC on the healthy pole. However, considering the construction and conduction cost, the half-bridge MMC is more attractive than the hybrid MMC for HVDC grids. In (Song et al., 2019)- (Zhang et al., 2020), the voltage pulse is injected into the fault line by controlling the MB of S-DCCBs. The MMC and S-DCCB are simultaneously controlled to produce the voltage pulse in (Yang et al., 1123). In (Mei et al., 2021), the voltage pulse comes from the energy absorption module of S-DCCB. In (Li et al., 2020), the HVDC grid charges the fault line through the arrester of S-DCCB, and the fault property is identified using the fault line voltage. In (Pei et al., 2019), the fault property can be identified using the fault current, and the fault current is limited because the MB modules are sequentially turned on. However, the methods in (Wang et al., 2203)- (Pei et al., 2019) do not consider the C-DCCBs.

For C-DCCBs, most previous papers consider the direct reclosing and the consecutive interruption ability rather than the fault property identification is focused on. For example (Sima et al., 2019),- (Augustin et al., 2021) use different methods to quickly restore the interruption ability of C-DCCBs before the direct reclosing. Nevertheless, the fault property identification and adaptive reclosing of C-DCCBs are worth studying to improve the reclosing performance. In (Wen et al., 2021), for HVDC grids adopting C-DCCBs, the fault property is identified by comparing the residual voltages at two ends of the isolated fault line. However, this method only applies to symmetrical monopole DC systems and requires long-distance communication. In (Torwelle et al., 2021), a grounded branch is added to the C-DCCB, which enables the internal capacitor charges the fault line, and the fault property is identified using the line voltage. However, the capacitor may need to charge the fault line multiple times, which obviously increases the reclosing time.

Although several C-DCCBs with good interruption performances have been proposed, the C-DCCB with adaptive reclosing ability needs further research. In this paper, a novel C-DCCB is proposed to serve HVDC grids. On the one hand, the proposed C-DCCB achieves good interruption performances; on the other hand, it has the ability of adaptive reclosing, which is the main contribution of this paper. The adaptive reclosing ability avoids the second fault shock in case of permanent faults and the voltage oscillations in case of transient faults. The paper is structured as follows. Section 2 describes the

topology and operation of the proposed C-DCCB. Section 3 analyzes the parameter design and fault property identification. Section 4 shows the simulation results, which validate the performance of the proposed C-DCCB. Finally, Section 5 concludes this paper.

2 Proposed DC circuit breaker

2.1 Topology of the proposed C-DCCB

As shown in Figure 1, the proposed C-DCCB contains the main conductor (MC), MB, energy absorber (EA) and precharge branch. The MC is composed of a fast disconnector (FD) and a load commutation switch (LCS), and the LCS only endures the commutation voltage. The MB is composed of an inductor L, capacitor C, diodes D_1–D_2, and thyristors T_1–T_4. The EA is composed of an arrester and diode D_3. The precharge branch is composed of a resistor R_1 and thyristor T_5. Both sides of the C-DCCB are equipped with residual current breakers (RCBs). The RCB can interrupt residual DC currents of up to 10 A, and the interruption time is 30 ms. After a current zero occurs, the FD can restore its dielectric strength within a few milliseconds to withstand the peak transient interruption voltage (TIV). In practical engineering, the FD can be composed of several vacuum circuit breakers to achieve operation performance (Shi et al., 2015).

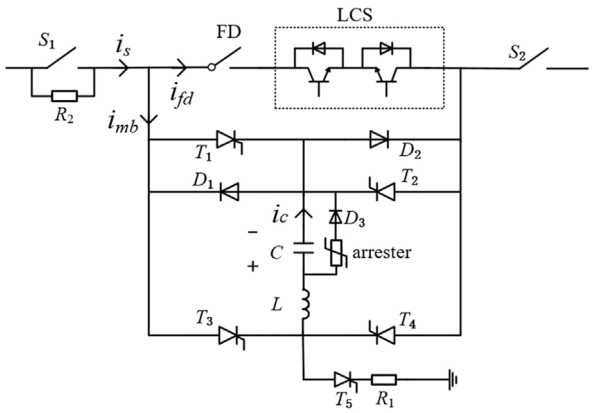

FIGURE 1
Topology of the capacitor-based DC circuit breaker.

To clarify the operation processes, the current curves in C-DCCB during interrupting fault currents and reclosing with transient faults are shown in Figure 2, where i_s, i_{mb}, i_{fd}, i_c and i_{ar} are the currents of the DC system, MB, FD, capacitor C and arrester, respectively. The reference directions of currents and capacitor voltage u_c are marked in Figure 1. During operations, the main switching events and time labels are given in Figure 2.

2.2 Operation processes of the C-DCCB

2.2.1 Capacitor precharge

Initially, the HVDC grid precharges the capacitor C by turning on T_1, T_2 and T_5, and the current path is shown in Figure 3A. After the capacitor voltage u_c is charged to the system voltage, T_1, T_2 and T_5 naturally turn off. Because of the

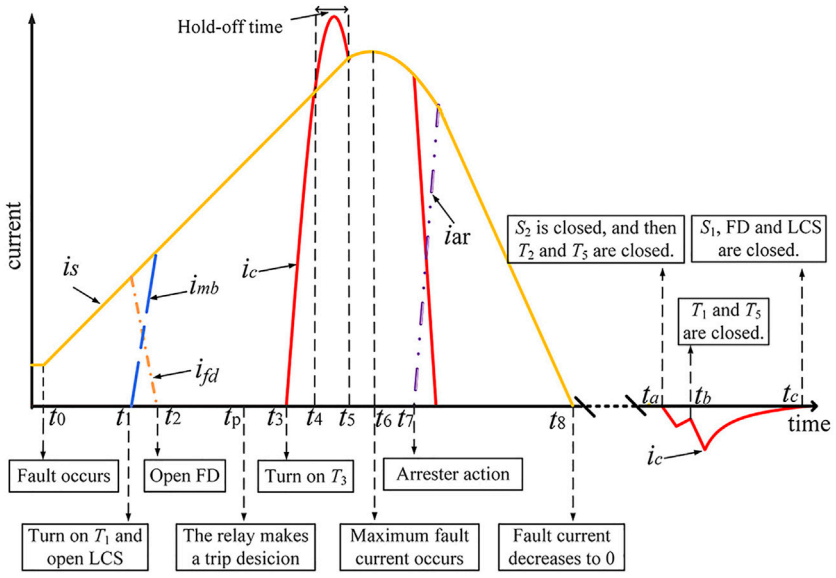

FIGURE 2
Current curves during interrupting fault currents and reclosing with a transient fault.

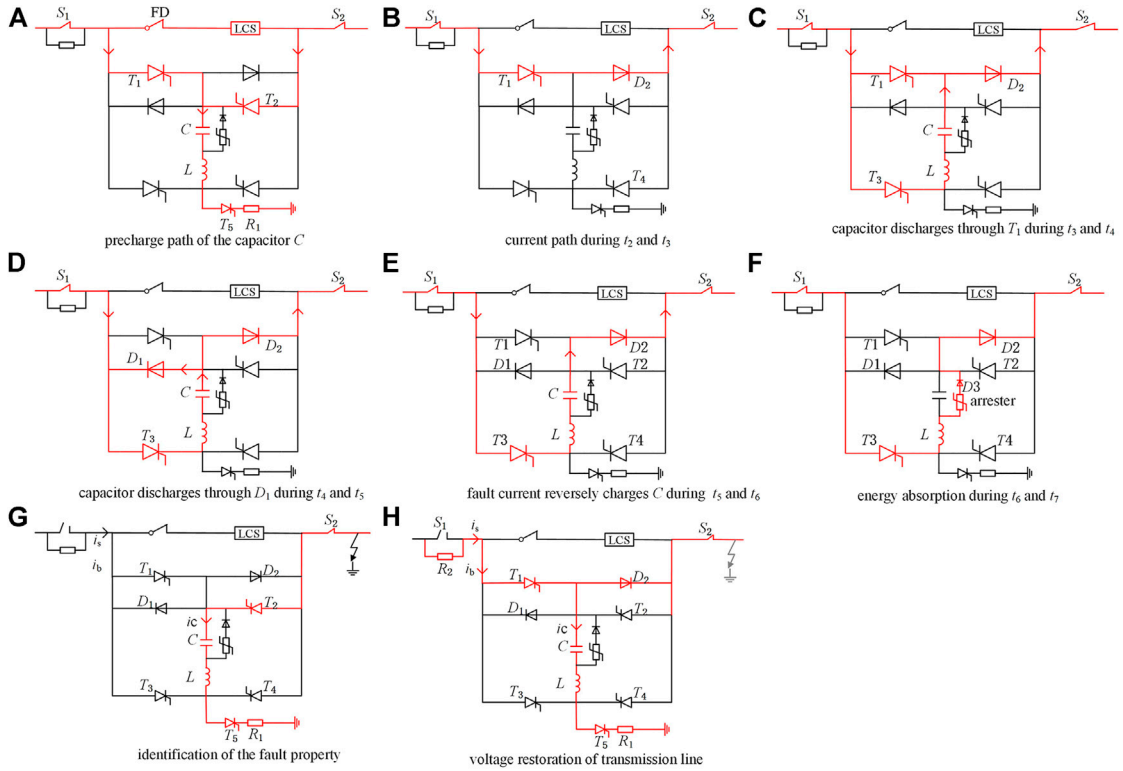

FIGURE 3
Operation procedures of the C-DCCB.

leakage discharge, u_c slowly decreases during the normal state. Once u_c decreases to a preset value, T_1, T_2 and T_5 are turned on to precharge the capacitor. Thus, u_c is always no less than the preset value during the normal state.

2.2.2 Current commutation

During the normal state, the MC conducts the load current with small conduction losses. Considering the pre-activation strategy, once the protection detects a potential fault at $t = t_1$, the C-DCCB commutates the current into the MB by turning on T_1 and turning off the LCS. At $t = t_2$, i_{fd} decreases to 0, and the FD begins to open. After that, the current path in the C-DCCB is shown in Figure 3B. If the protection decides not to interrupt the current at $t = t_p$, the C-DCCB successively closes the FD and LCS; thus, the current naturally commutates into the MC, and the thyristor T_1 turns off naturally after the current of T_1 is smaller than the holding current; Otherwise, the C-DCCB performs the following interruption operations.

During t_1–t_p, the voltage drop in the C-DCCB is equal to the on-state voltages of T_1 and D_2; thus, the disturbance caused by the pre-activation is insignificant. By pre-commutating the system current from the MC into the MB, the C-DCCB operation time overlaps with the protection time. Thus, the pre-activation effectively reduces the fault clearing time.

2.2.3 Capacitor discharge

As shown in Figure 3C, during t_3 and t_4 the system provides the fault current to the fault point through S_1, T_1, D_2 and S_2. At the same time, the capacitor discharges through the following loop: C—T_1—T_3—L. As shown in Figure 3D, after i_c exceeds the fault current at $t = t_4$, T_1 is reversely blocked, and the discharging loop is changed as: C—D_1—T_3—L. After i_c decreases to the fault current at $t = t_5$, D_1 is reversely blocked, and T_1 begins to endure the forward voltage stress, as shown in Figure 3E. To reliably turn off T_1, the time interval between t_4 and t_5, which is the reverse-bias time of T_1 and marked as t_R, should be greater than the turn-off time t_q. The turn-off time t_q, which can be found in the datasheet, is the minimum reverse-bias time to ensure the turn-off of the thyristor (Technical Information, 2012).

During t_2 and t_5, the voltage drop in the C-DCCB is rather small compared with the system voltage. After $t = t_5$, the voltage drop in the C-DCCB is approximately equal to the capacitor voltage and quickly charged to the system voltage. We mark the FD operation time as t_{FD}. The value

of t_3 should meet the following two constraints: 1) t_3 should not be earlier than t_p, and 2) the FD recovers its dielectric strength at $t = t_2 + t_{FD}$, which time instant should be earlier than t_5 to avoid the interruption failure. Considering that the interval between t_3 and t_5 is greater than t_q, these two constraints can be satisfied when t_3 is selected as:

$$t_3 = \max\left(t_p, t_2 + t_{FD} - t_q\right) \tag{1}$$

2.2.4 Energy absorption

After the capacitor is charged to the arrester reference voltage, the fault current commutates into the EA and gradually decreases, as shown in Figure 3F. The arrester releases the residual energies stored in the system, and the peak TIV usually is limited to 1.5 times the system voltage. After the fault current decreases to 10 A, S_1, and S_2 are opened to isolate the fault totally. After the isolation, the capacitor voltage u_c is opposite to its initial state.

2.2.5 Adaptive reclosing

To guarantee that the DC line recovers its insulation characteristic, the reclosing is usually hundreds of milliseconds later than the isolation (Yang et al., 1123).

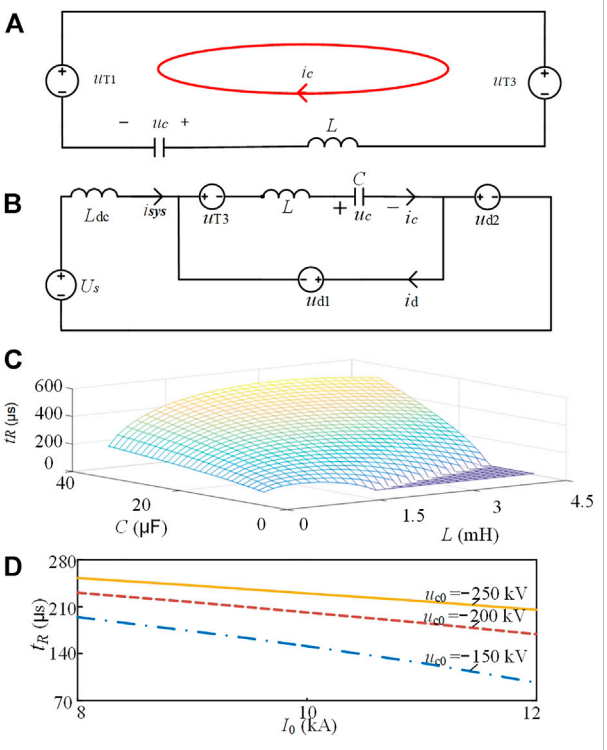

FIGURE 4
(A) Equivalent circuit of the capacitor discharging during t3 and t4. **(B)** equivalent discharge circuit of the capacitor during t4 and t5; **(C)** relations of tR, L, and C **(D)** relations of IR. Io. and uc0.

After receiving the adaptive reclosing command, the C-DCCB closes S_2 and turns on T_2 and T_5. If the fault is permanent, the capacitor C significantly discharges through the following loop: C—L—T_5—R_1—fault point—S_2—T_2, as shown in Figure 3G. If the fault is transient, the capacitor slightly discharges through the equivalent grounded capacitance of the DC line.

After identifying the permanent fault, S_2 is opened to isolate the fault when the discharging current is smaller than 10 A. After identifying the transient fault, the C-DCCB turns on T_1 and T_5; thus, the capacitor C and the DC line are charged to the system voltage, as shown in Figure 3H; after that, the C-DCCB successively closes S_1, FD and LCS, and the reclosing is completed.

After reclosing the C-DCCB located on one side of the DC line, if the fault is transient, the line voltage is close to the system voltage; otherwise, the line voltage is much less than the system voltage. Thus, the C-DCCB located on the other side of the DC line directly identifies the fault property using the line voltage.

3 Parameter design and fault property identification of the C-DCCB

3.1 Turning T_1 off

During t_3 and t_4, the capacitor discharging loop is equivalent to the circuit shown in Figure 4A, where u_{Ti} is the voltage drop in T_i, $i = 1, 2, 3, 4$. Assume that thyristors have the same voltage drops of u_T, then we can obtain:

$$\begin{bmatrix} \bullet u_c \\ \bullet i_c \end{bmatrix} = \begin{bmatrix} 0 & -1/C \\ -1/L & 0 \end{bmatrix} \begin{bmatrix} u_c \\ i_c \end{bmatrix} \tag{2}$$

where the initial values of i_c and u_c are 0 and u_{c0}, respectively, and u_{c0} is negative under the reference direction in Figure 1.

After a metallic fault occurs at the load side of the C-DCCB, the system side of the C-DCCB is equivalent to a voltage source connected in series with an inductor L_{dc}. The equivalent capacitor discharge circuit during t_4 and t_5 is shown in Figure 4B, where i_{sys} is the system current, i_d is the current flowing through D_1, u_{di} is the voltage drop in D_i, $i = 1, 2$. Assume that the diodes have the same voltage drop of u_d, then we can obtain:

$$\begin{bmatrix} 0 & 0 & 0 & -L \\ L_{dc} & 0 & 0 & L \\ 1 & 1 & 0 & -1 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} \bullet i_{sys} \\ \bullet i_d \\ \bullet u_c \\ \bullet i_c \end{bmatrix} = \begin{bmatrix} u_c + u_T + u_d \\ U_s - u_c - u_T - u_d \\ 0 \\ i_c/C \end{bmatrix} \tag{3}$$

In Eq. 3, the initial values of u_c and i_c can be obtained from those final values in Eq. 2; i_{sys} and i_c have the same initial value, and i_d has an initial value of 0.

In this analysis, U_s = 200 kV, L_{dc} = 0.04 H, u_{c0} = −200 kV, and the fault current at t_3 has a value of I_0 = 10 kA. Substituting these parameters into (2) and (3), the relations of the reverse-bias time t_R, L and C can be obtained. As shown in Figure 4C, t_R increases with C, because the larger capacitor stores more energy to maintain the reverse-bias of T_1. When L is small, t_R increases with L. However, when L exceeds a critical value L_C, t_R decreases with L. When C is too small and L is too large, t_R is 0. When C = 9 μF and L = 1.2 mH, the relations of t_R, I_0 and u_{c0} are shown in Figure 4D. The value of t_R decreases with I_0 and increases with the absolute value of u_{c0}.

According to the relations of t_R and system parameters, the parameter design principles of the C-DCCB are as follows: 1) the values of L and C should guarantee that t_R is greater than the turn-off time t_q under the worst interruption condition, i.e., the C-DCCB interrupts the maximum fault current when the initial capacitor voltage u_{c0} has a minimum absolute value; 2) the value of L should be close to the critical value L_c to improve the utilization efficiency of L and C.

3.2 Fault property identification

3.2.1 Analysis model:

This section takes the reclosing after a positive pole fault as an example. As shown in Figure 5A, the systems on both sides of the negative pole are represented by the Thevenin equivalent circuits; U_{eq1} and U_{eq2} are Thevenin voltages; Z_{eq1} and Z_{eq2} are Thevenin impedances; u_r is the capacitor voltage at the beginning of reclosing. Taking the fault point as a boundary, the DC line is divided into two parts. If the fault is permanent, the switch k_1 is closed; otherwise, k_1 is opened. The turn-on commands of thyristors T_L and T_R represent the reclosing commands of C-DCCBs on the left and right sides, respectively.

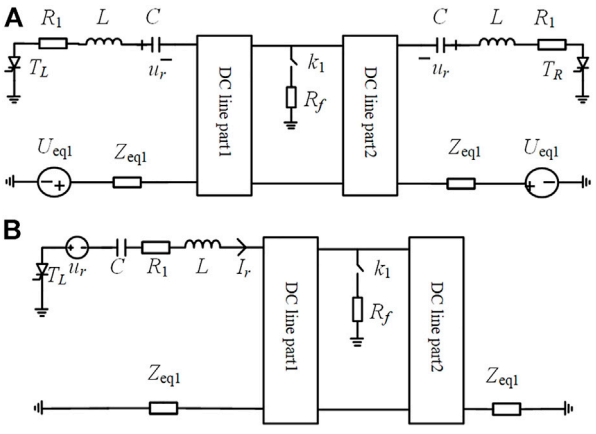

FIGURE 5
(A) Schematic of the system circuit after isolating the fault pole; **(B)**equivalent system circuit during the reclosing.

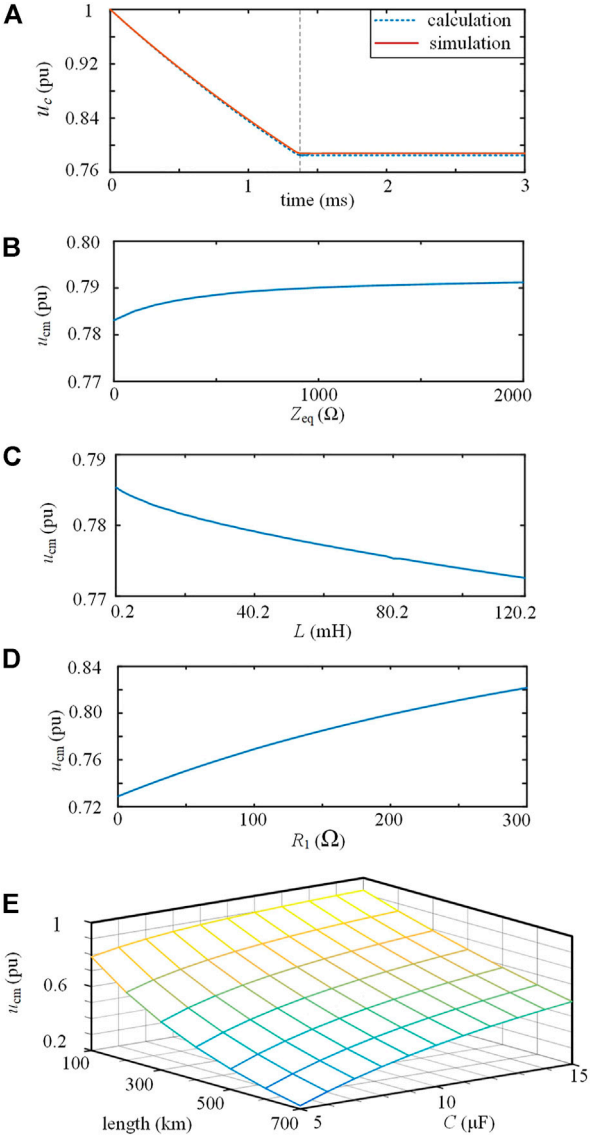

FIGURE 6
(A) Simulation and calculation values of Δu during reclosing without fault; **(B)** relation between ucm and Zeq **(C)** relation between ucm and L **(D)** relation between ucm and R1 **(E)** relations of ucm, C and line length.

We assume that the C-DCCB on the left side closes S_2, T_2 and T_5, which is equivalent to that T_L is turned on in Figure 5A. According to the superposition theorem, during the reclosing, the system response change is caused by the excitation of the voltage source u_r. Considering only the excitation of u_r, the equivalent system circuit is shown in Figure 5B.

Using the DC line's frequency-dependent parameter, the nodal admittance matrix of the DC line can be obtained, and

then the bus admittance matrix of the circuit in Figure 5B can be established. The self-impedance of the node connecting the voltage source u_r and the capacitor C is marked as Z_{self}, then the current injected into the DC line, marked as I_r, is:

$$I_r = u_r / \left(sZ_{self} \right) \tag{4}$$

where s is the Laplace operator.

During reclosing, the capacitor voltage u_c is:

$$u_c = u_r + I_r / (sC) \tag{5}$$

The value of u_c in the frequency domain can be calculated by combining (4) and (5). The value of u_c in the time domain can be obtained using the numerical inversion of the Laplace transform (Gómez and Uribe, 2009). The detailed calculation process can refer to the method in (Guo et al., 2021) and is not repeated in this paper.

3.2.2 Transient fault:

At the beginning of reclosing, the voltage source u_r generates a current traveling wave on the DC line. When the fault is transient, because the DC line end is an open circuit, the current traveling wave is totally reflected at the DC line end, and the reflection wave is in the opposite direction of the original traveling wave. When the reflection current wave transmits to the DC line head, I_r decreases to 0, and the thyristor T_L is reversely biased, causing the capacitor voltage u_c keeps unchanged.

According to the system parameters in Section 4, we take u_r = 1 pu, C = 9 μF, L = 1.2 mH, R_1 = 150 Ω, $Z_{eq1} = Z_{eq2}$ = 100 Ω. As shown in Figure 6A, the capacitor discharges through the DC line during reclosing without fault, and u_c gradually decreases. Because of the current reflection wave, the thyristor T_L is turned off and u_c keeps unchanged after 1.36 ms. The deviation between the calculation and simulation values of u_c is relatively small, which validates the accuracy of the analysis model.

During reclosing, the minimum value of u_c is marked as u_{cm}. The relations of u_{cm} and the system parameters are discussed using the above analysis model. The values of Z_{eq1} and Z_{eq2} are related to the non-fault area of the DC grid. When $Z_{eq1} = Z_{eq2} = Z_{eq}$, the relation between u_{cm} and Z_{eq} is shown in Figure 6B. When Z_{eq} increases from 0 to 2 kΩ, u_{cm} only increases by 1.0%, indicating that the non-fault area of the DC grid has little influence on u_{cm}.

As shown in Figure 6C, when L increases from 0.2 to 120.2 mH, u_{cm} only decreases by 1.6%, indicating that the influence of L on u_{cm} is not significant. As shown in Figure 6D, u_{cm} increases with increasing R_1, because R_1 limits the amplitude of the current traveling wave, thus limiting the discharge of capacitor C. As shown in Figure 6E, u_{cm} increases with the increasing C. With the DC line length increase, the arrival time of the current reflection wave increases, causing the increase in capacitor discharge time and the decrease of u_{cm}.

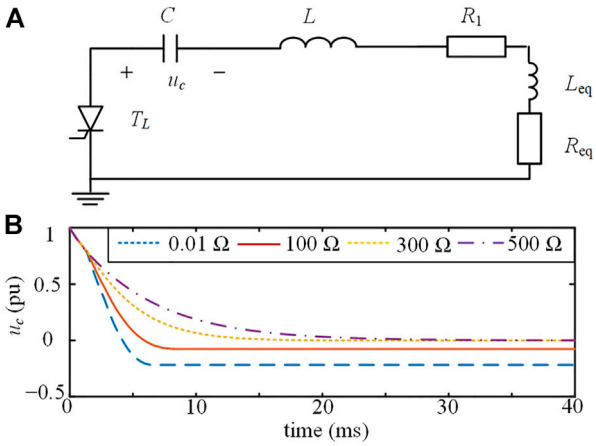

FIGURE 7
(A) Equivalent discharge circuit during reclosing with a permanent fault; **(B)** waveforms of uc, when the permanent fault has different fault resistances.

3.2.3 Permanent fault:

After reclosing the C-DCCB with a permanent fault, the current traveling wave will be reflected at the fault point. If the fault resistance is less than the line wave impedance, the current reflection wave has the same polarity as the original current traveling wave; otherwise, compared to the original current traveling wave, the current reflection wave has an opposite polarity and smaller amplitude. Therefore, the traveling wave effect will not cause the capacitor current to cross zero during reclosing with a permanent fault.

As shown in Figure 3G, the capacitor significantly discharges through R_1, L and the fault line during reclosing with a permanent fault. The equivalent parallel admittance of the DC line has little effect on the discharge. Using the lumped parameter model of the DC line, the equivalent capacitor discharge circuit is shown in Figure 7A, where R_{eq} and L_{eq} are the equivalent resistance and inductance of the DC line, respectively. For this second-order circuit, when $(R_1 + R_{eq}) > 2\sqrt{(L + L_{eq})/C}$, the discharge process is overdamped, and u_c gradually decreases to 0. When $(R_1 + R_{eq}) < 2\sqrt{(L + L_{eq})/C}$, the discharge process is underdamped, and u_c decreases to a negative value when the discharge current crosses zero. After the discharge current crosses zero, the thyristor T_L is turned off, and u_c maintains the negative value.

As shown in Figure 7B, for a permanent fault located at the DC line end, when the fault resistance is 0 and 100 Ω, the discharge is underdamped, and the minimum value of u_c is less than 0. When the fault resistance is 300 and 500 Ω, the discharge process is overdamped, and u_c decreases to 0. These results are consistent with the above analysis.

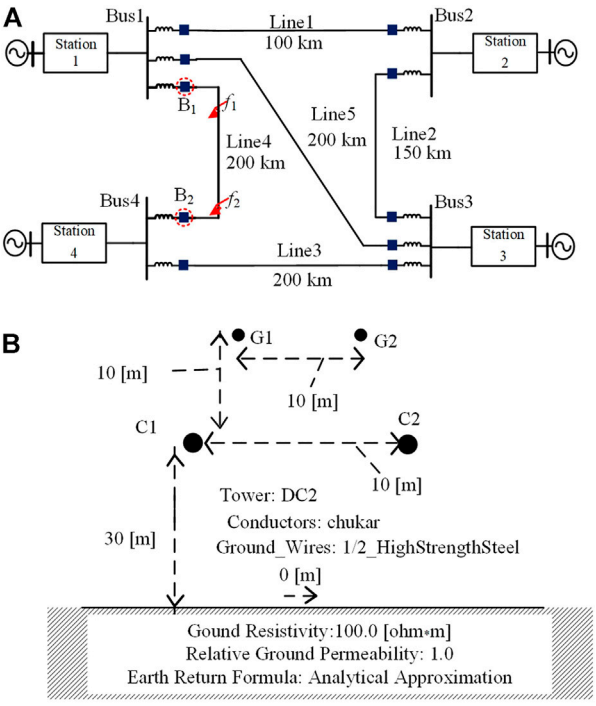

FIGURE 8
(A) Topology of the DC grid; **(B)** configuration of transmission line.

3.2.4 Criteria for identifying the fault property:

According to the above analysis, during reclosing with transient faults, u_c decreases to a positive value u_{cm}, which can be calculated using Eq. 4 and Eq. 5. During reclosing with permanent faults, u_c decreases to be no more than 0. A permanent fault is identified using the following criterion:

$$u_c(t) \le u_{th} = u_{cm} - u_{mar1} \tag{6}$$

where u_{th} is the voltage threshold, and u_{mar1} is a positive safety margin.

A transient fault is identified using the following criterion:

$$u_c(t) > u_{th} \;\; \& \;\; |u_c(t-\Delta t) - u_c(t)| < u_{error} \tag{7}$$

A slighter fault causes a slower capacitor discharge rate during reclosing with a permanent fault. The values of u_{error} and Δt should satisfy the following conditions: 1) the criterion in Eq. 7 is not true in the case of the slightest permanent fault, which occurs at the end of DC line and has the largest fault resistance; and 2) u_{error} is greater than the maximum measurement error.

In addition, to correctly identify the transient fault that lasts longer than hundreds of milliseconds, the following method is adopted: after identifying a permanent fault, the C-DCCB will perform another reclosing attempt to identify the fault property again unless the number of reclosing attempts reaches the maximum value allowed by the system.

TABLE 1 Parameters of the C-DCCB.

Parameter	Value
Interruption capacity	12 kA
Peak TIV	300 kV
FD operation time t_{FD}	2 ms
Capacitance C	9 μF
Inductance L	1.2 mH
Resistances R_1, R_2	100 Ω, 800 Ω
Preset recharge value of u_c	−180 kV
Turn-off time of T_1 and T_2	60 μs (5STF28H2060)
Voltage threshold u_{th}	140.7 kV

4 Simulation results

4.1 Simulation parameters

As shown in Figure 8A, a four-terminal bipolar DC grid is established in PSCAD/EMTDC, and the rated voltage is ±200 kV. In the DC grid, each station contains 2 MMCs, and its neutral point is directly earthed. For the equivalent model, all sub-modules in each MMC arm are equivalent to a Thevenin equivalent circuit; thus, the simulation efficiency is greatly improved. The DC grid is bipolar and has a rated voltage of ±200 kV, and the detailed equivalent model of MMC in (Cigré, 2014) is used. Both ends of the DC line are equipped with C-DCCBs and current-limiting inductors of 0.04 H. The C-DCCB located on the Bus1 side of Line 4 is marked as B_1 and taken as an example. For simplicity, only simulation results of the positive pole are shown in this paper. The parameters of the C-DCCB and simulation model

TABLE 2 Main parameters of the HVDC Grid.

Parameters	Values
Rated power of station (MW)	Station 1: −600 Station 2: 600 Station 3: −600 Station 4: 600
Length of the Overhead Lines (km)	line l_1: 100 line l_2: 150 line l_3: 200 line l_4: 200 line l_5: 200
Arm inductance L_{arm} (mH)	Station 1: 19 Station 2: 58 Station 3: 29 Station 4: 19
Capacitance of sub-module C_0 (μF)	Station 1: 450 Station 2: 150 Station 3: 300 Station 4: 450
Arm resistance r_0 (Ω)	Station 1: 0.18 Station 2: 0.55 Station 3: 0.27 Station 4: 0.18
L_{dc} (mH)	40
Number of arm sub-modules n_0	200

are shown in Table 1 and Table 2, and the design of reclosing parameters is presented as follows.

During the interruption, the internal capacitor voltage u_c is charged to the peak TIV of 300 kV. After the interruption, the capacitor C slowly discharges through the arrester and D_3. After a time delay of 300 ms, the capacitor voltage is discharged to u_r = 192 kV at the beginning of reclosing. The transmission line is based on the frequency-dependent model, and the line configuration is shown in Figure 8B. Substituting the C-DCCB and line parameters into (4) and (5), we can obtain that u_{cm} = 0.785 u_r. In this paper, the safety margin u_{mar1} is taken as 10 kV. Then, the voltage threshold u_{th} in (6) and (7) has a value of 0.785 × 192–10 = 140.7 kV.

For DC grid protections, the maximum value of fault resistance is usually hundreds of ohm. In simulations, even if the permanent fault located on the B_2 side of Line 4 has a fault resistance of up to 1 kΩ, u_c decreases to u_{th} within 3 ms during the reclosing process. Thus, as long as Δt is greater than 3 ms and u_{error} is less than (u_r–u_{th}), the permanent fault will not cause malfunctions of criterion in Eq. 7. We assume that the capacitor voltmeter has a voltage range of 350 kV and an accuracy ratio of 0.1%; thus, the maximum measurement error of the voltmeter is 0.35 kV. Considering these above conditions, we select u_{error} and Δt as 0.5 kV and 5 ms, respectively.

4.2 Interruption of fault current

As shown in Figure 8A, considering the most serious fault condition, a metallic fault occurs at the line side of B_1 at t = 0 ms, and the initial capacitor voltage is −180 kV. After the fault is detected at t = 1 ms, the interruption results are shown in Figure 9, where i_{dc}, i_{T1}, i_c and i_{ar} are the currents flowing through Line 4, T_1, C and arrester, respectively.

We assume that the protection detects the fault at t = 1 ms. As shown in Figure 9, after t = 1 ms, T_1 is turned on and then the LCS is turned off. At t = 1.16 ms, i_{dc} is commutated into the MB, and the FD is opened without arc. Substituting system parameters into (1), T_3 is turned on at t = 3.1 ms. After that, i_c rapidly exceeds the fault current; thus, T_1 is reversely biased. The reverse-bias of T_1 continues until i_{dc} exceeds i_c. The reverse-bias time is 120 μs and two times t_q, which is sufficient to turn off T_1. With the charging of the capacitor, i_{dc} reaches the maximum value of 11.7 kA at t = 3.29 ms and then gradually decreases. At t = 3.42 ms, i_{dc} is commutated into the arrester. At t = 10.3 ms, i_{dc} falls to below 10 A.

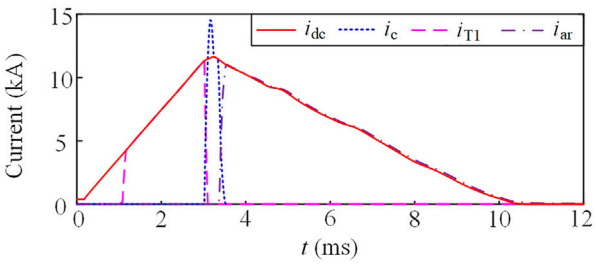

FIGURE 9
Current waveforms during the interruption.

For the typical hybrid DCCB in (Hafner and Jacobson, 2011), the fault current decreases almost immediately after the FD recovers the dielectric strength. For the C-DCCB, the fault current begins to fall at t = 3.29 ms, which is only 0.13 ms later than the instant that the FD recovers the dielectric strength at t = 3.16 ms. The time interval from the fault inception to the moment that the fault current begins to decrease is defined as the fault neutralization time. The fault neutralization time of C-DCCB is only a few hundred microseconds longer than that of typical hybrid DCCB, indicating a quick interruption speed.

4.3 Reclosing with a permanent fault

4.3.1 Permanent metallic fault

We set a permanent fault at the midpoint of Line 4 at t = 0 ms, and the fault resistance is 0.01 Ω. At t = 300 ms, B_1 begins to reclose, i.e., T_2 and T_5 are turned on. As shown in Figure 10A, u_c gradually decreases during reclosing and is smaller than u_{th} = 140.7 kV after t = 301.08 ms. Thus, B_1 identifies the permanent fault. During reclosing, the capacitor discharges through R_1, L and the fault line, and this second-order discharge circuit is underdamped because the fault resistance is small. As shown in Figure 10A, when i_c crosses 0 at t = 305.08 ms, u_c decreases to a negative value, and T_2 and T_5 are turned off. After that, S_2 is opened to isolate the permanent fault.

At the initial stage of reclosing, i_c undergoes multiple abrupt changes because of the traveling wave effect. The traveling impact

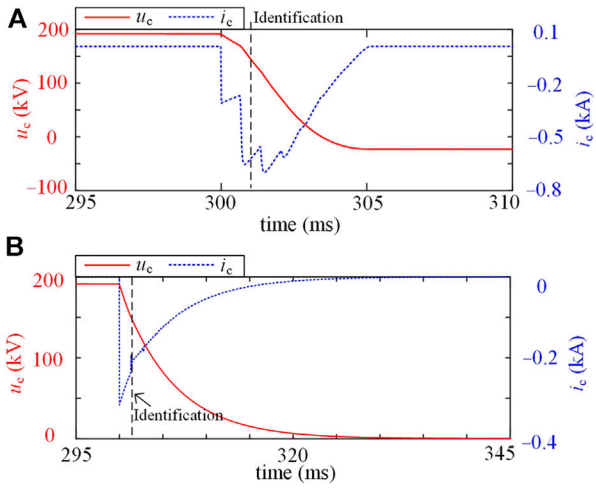

FIGURE 10
Simulation results during reclosing: **(A)** permanent metallic fault: **(B)** permanent high resistance fault.

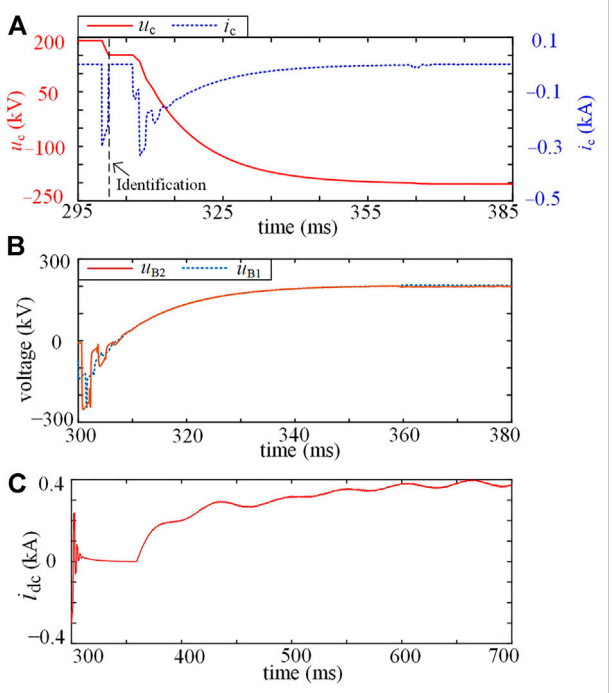

FIGURE 11
Simulation results during reclosing with a transient fault: **(A)** the value of uc and ic; **(B)** line voltages uB1 and uB2; **(C)** line current idc.

decreases over time and is not significant after 302.5 ms. At t = 305.08 ms, the zero crossing of i_c is caused by the underdamped discharge process rather than the traveling effect, which is consistent with the analysis in Section 3.2.

4.3.2 Permanent high-resistance fault

We set a permanent fault at the B_2 side of Line 4, and the fault resistance is 500 Ω. After the interruption, B_1 begins to reclose at t = 300 ms. As shown in Figure 10B, u_c decreases to u_{th} = 140.7 kV at t = 301.76 ms; thus, the permanent fault is identified. Because the fault resistance is large, the capacitor discharge process is overdamped. At t = 320 ms, u_c decreases to 6.7 kV and i_c is smaller than 10 A. Then, S_2 begins to be opened, and the fault is totally isolated at t = 340 ms.

4.4 Reclosing with a transient fault

After isolating a transient fault on Line 4, B_1 begins to reclose at t = 300 ms; thus, a current traveling wave is injected into Line 4. The current traveling wave transmits along Line 4 and is totally reflected at the end of Line 4. As shown in Figure 11A, at t = 301.40 ms, the current reflection wave arrives at the head of Line 4 and causes i_c to cross 0, because the reflected wave is in the opposite polarity of the original traveling wave. After that, u_c maintains at 151 kV. At t = 306.36 ms, the criterion in Eq. 7 is activated, indicating that the fault on Line 4 has disappeared. After that, B_1 turns on T_1 and T_5; thus, the DC grid charges the capacitor C and Line 4 through the resistor R_2. Finally, the capacitor C is charged to the system voltage.

As shown in Figure 11B, the voltage of Line 4 on B_1 side, marked as u_{B1}, increases to 190 kV at t = 339.20 ms, and B_1 begins to close S_1. At t = 339.24 ms, the voltage of Line 4 on B_2 side, marked as u_{B2}, increases to 190 kV; thus, B_2 directly identifies that the line fault has disappeared, and S_1, S_2, FD and LCS in B_2 are successively closed. After that, u_{B1} and u_{B2} gradually recover to close to 200 kV.

During the reclosing process, the discharging of the capacitor and charging of Line 4 cause negative and positive abrupt changes in i_{dc}, respectively, as shown in Figure 11C. After t = 360 ms, MCs of B_1 and B_2 have been closed; thus, i_{dc} begins to restore to the normal value. Line 4 begins to restore the power transmission. This restoration process takes hundreds of milliseconds. A special control strategy can be used to improve the restoration speed, which will be considered in future work.

4.5 Comparisons

In this section, the C-DCCBs in (Liu, 2019), (Wu et al., 2019) and (Guo et al., 2020) are compared with the proposed C-DCCB.

4.5.1 Interruption performance

In these C-DCCBs, only the C-DCCB in (Liu, 2019) opens the FD with arcing, which increases the FD operation time. Thus, when the same FD is used, the C-DCCB in (Liu, 2019) has a longer interruption time than the other three C-DCCBs. For the other three C-DCCBs, the fault current decreases within a few hundred microseconds after the FD recovers the dielectric strength, indicating a quick interruption speed.

Except for the MC, the C-DCCB in (Liu, 2019) cannot provide another current path to conduct the load current, whereas the other three C-DCCBs can conduct the load current using the thyristors in the MB. Therefore, the C-DCCB in (Liu, 2019) does not have the pre-activation ability, whereas the other three C-DCCBs have the pre-activation ability. Combining the protection and pre-activation, these three C-DCCBs can further reduce the interruption time.

During the interruption of backward direction currents, the C-DCCB in (Liu, 2019) cannot decrease the FD current to 0 until the capacitor discharge current is reversed, causing a larger interruption time. In (Wu et al., 2019), the C-DCCB interrupts only the forward direction currents and cannot interrupt the backward direction fault currents. Because of the symmetry of topology, the proposed C-DCCB can interrupt bidirectional currents with the same performance, and the C-DCCB in (Guo et al., 2020) also has this interruption characteristic.

4.5.2 Semiconductor cost

The peak TIV of these C-DCCBs, marked as U_p, is selected as 300 kV to compare the semiconductor cost. For the proposed C-DCCB, T_1 and T_2 are turned off during the interruption of the

TABLE 3 Semiconductor costs of C-DCCBs.

C-DCCB	N2825 TE400	5STF 28H2060 (¥)	W3082MC450(¥)	Total cost (¥)
In (Liu, 2019)	558,450 (¥)	0 (¥)	215,740 (¥)	774,190 (¥)
In (Wu et al., 2019)	558,450 (¥)	2,479,500 (¥)	0 (¥)	3,037,950 (¥)
In (Guo et al., 2020)	2,792,250 (¥)	826,500 (¥)	1,078,700 (¥)	4,697,450 (¥)
Our	1,675,350 (¥)	1,653,000 (¥)	647,220 (¥)	3,975,570 (¥)

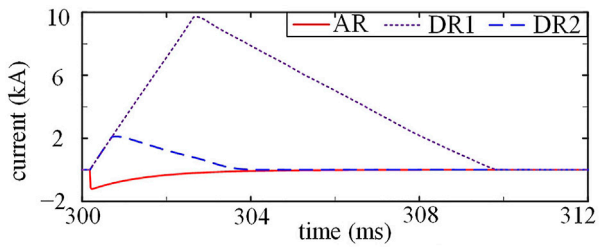

FIGURE 12
Waveforms of idc when the C-DCCB recloses with a permanent fault using different reclosing strategies.

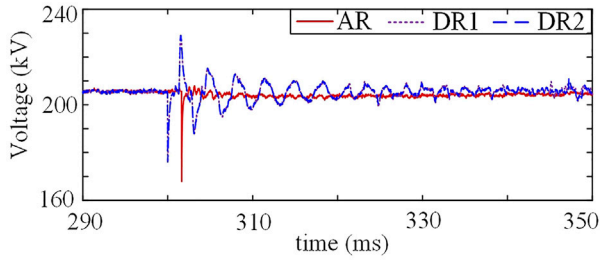

FIGURE 13
Waveforms of ubus1 when the C-DCCB recloses with a transient fault using different reclosing strategies.

forward direction and backward direction currents, respectively. They should be composed of fast thyristor modules to maintain a short interruption time. The thyristors T_3 and T_4 are naturally turned off after the interruption, and the thyristor T_5 is naturally turned off after the precharge process; thus, thyristors T_3, T_4 and T_5 can be composed of phase-control thyristor modules. Then, the proposed C-DCCB contains phase-control thyristor modules with a voltage rating of $3U_p$, fast thyristor modules with a voltage rating of $2U_p$, and diode modules of $3U_p$.

For the C-DCCB in (Liu, 2019), a triggered spark gap or reverse-conducting thyristor can be used to trigger the capacitor discharge during the interruption. The reverse-conducting thyristor comprises phase-control thyristor modules with a voltage rating of U_p and diode modules with a voltage rating of U_p. In (Wu et al., 2019), three thyristors need to be turned off during the interruption process. They should be composed of fast thyristor modules with a voltage rating of $3U_p$; one thyristor is naturally turned off after the interruption and can be composed of phase-control thyristor modules with a voltage rating of U_p. In (Guo et al., 2020), one thyristor is turned off during the interruption process and composed of fast thyristor modules with a voltage rating of U_p. In addition, phase-control thyristor modules with a voltage rating of $5U_p$ and diode modules with a voltage rating of $5U_p$ are also needed in (Guo et al., 2020).

We assume that the thyristor module N2825TE400 (4 kV, ¥ 3,723 (findic and digikey, 2021)), fast thyristor module 5STF 28H2060 (2 kV, ¥ 2,755 (findic and digikey, 2021)) and diode module W3082MC450 (4.5 kV, ¥ 1,610 (findic and digikey, 2021)) are used, and a safety voltage margin of 2 is maintained. Then, the device costs of these C-DCCBs are given in Table 3, and the unit of device costs is RMB. The C-DCCBs in (Liu, 2019) and (Guo et al., 2020) have the smallest and largest semiconductor costs, respectively, and the proposed C-DCCB has a higher semiconductor cost than the C-DCCB in (Wu et al., 2019).

According to the evaluation method in (Evans et al., 2019), the capacitor C of 9 μF in the proposed C-DCCB has a cost of ¥ 2,231,323, which is more than half of the total semiconductor cost of ¥ 3,975,570. Thus, the capacitor cost is vital for evaluating the construction cost of C-DCCBs. For C-DCCBs, the capacitor value is related to the interruption conditions, such as voltage rating and interruption capacity. Comparing capacitor costs of C-DCCBs should be based on the same interruption conditions. Considering that the capacitor values in (Liu, 2019), (Wu et al., 2019), (Guo et al., 2020) and this paper are selected based on different interruption conditions, the capacitor costs are not compared to avoid injustice.

4.5.3 Reclosing performance

For the C-DCCB in (Liu, 2019), the polarities of the capacitor voltage are in the opposite directions before and after the interruption. The C-DCCB in (Liu, 2019) requires additional circuits to restore the normal state of the capacitor before reclosing, which increases the construction cost and is not conducive to fast reclosing. The C-DCCB in (Wu et al., 2019) has the same polarity of capacitor voltage before and after the interruption, and the C-DCCB in (Guo et al., 2020) can quickly restore the initial capacitor voltage using the grounded branch. Thus, these two C-DCCBs have a fast reclosing ability.

However, direct reclosing rather than adaptive reclosing is considered in previous papers. The direct reclosing strategy

directly recloses the C-DCCB to reconnect the HVDC grid to the isolated line, and the C-DCCB interrupts the fault current in case of permanent faults. Considering that these C-DCCBs have similar performances during the direct reclosing, the proposed C-DCCB is used to perform the direct reclosing to validate the advantage of the proposed adaptive reclosing strategy.

For the first direct reclosing method, which is marked as DR1, the proposed C-DCCB successively closes S_1, S_2 and FD. For the second direct reclosing method, which uses the pre-activation ability and is marked as DR2, the proposed C-DCCB successively closes S_1—S_2 and turns on T_1—T_2, and then the system current is commutated into the MC by closing FD and turning on LCS. Compared with the DR1, the DR2 effectively reduces the interruption time during the permanent fault because the process of commutating the fault current from MC into MB is avoided. The proposed adaptive reclosing strategy is marked as AR.

We set a permanent metallic fault at the head of Line 4. For DR1 and DR2, we assume that the fault detection time is only 0.2 ms. As shown in Figure 12, compared with DR1, DR2 reduces the maximum value of i_{dc} from 9.73 to 2.11 kA because DR2 has a much shorter interruption time. For the proposed adaptive reclosing strategy, the maximum absolute value of i_{dc} is only 1.22 kA. Therefore, compared with direct reclosing strategies, the proposed adaptive reclosing strategy effectively limits the fault current during the permanent fault.

We set a transient fault at Line 4, and B_1 recloses using different reclosing strategies. The simulation results are shown in Figure 13. For DR1 and DR2, the HVDC grid directly charges the positive pole of Line 4, causing oscillations in the Bus1 voltage u_{bus1}, and DR1 and DR2 almost have the same waveforms of u_{bus1}. For the adaptive reclosing strategy, the HVDC grid charges the positive pole of Line 4 and the internal capacitor of C-DCCB through the resistor R_2 at 301.6 ms; thus, u_{bus1} drops to 168 kV and then quickly returns to the normal value without significant oscillations. Compared with direct reclosing strategies, the adaptive reclosing strategy effectively reduces the voltage oscillations in HVDC grids.

5 Conclusion

This paper proposes a novel C-DCCB with adaptive reclosing ability. The parameter design is analyzed to ensure the reliable turn-off of the thyristor, which is key to the successful interruption. The transient process during adaptive reclosing is analyzed to identify the fault property. The semiconductor cost, interruption and reclosing performances of the proposed C-DCCB are compared with those of previous C-DCCBs. The main conclusions are summarized as follows.

1) The proposed C-DCCB achieves good interruption performances, such as quick interruption speed and pre-activation ability. During interruptions, the fault current decreases within a few hundred microseconds after the FD restores the dielectric strength. Using the pre-activation, the fault current is commutated into the MB during the protection time, thus effectively reducing the interruption time.
2) During the adaptive reclosing, the internal capacitor has a large initial voltage and discharges through the grounded branch. The capacitor voltage decreases to a positive value when the fault is transient, and the capacitor voltage is no more than 0 when the fault is permanent; thus, the fault property is identified using the capacitor voltage.
3) The adaptive reclosing of C-DCCBs is less considered in previous papers. An adaptive reclosing strategy is designed for the proposed C-DCCB, which is the main contribution of this paper. Using the adaptive reclosing strategy, the proposed C-DCCB avoids the second fault shock in case of permanent faults, and the power transmission is restored without significant voltage oscillations in transient faults.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author.

Author contributions

ZX: Writing-Original Draft, Visualization. JL: Writing–Review and Editing, Supervision. YG: Conceptualization, Methodology, Writing-Original Draft. YW: Supervision.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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