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A Three-Input Central Capacitor Converter for a High-Voltage PV System

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High-voltage photovoltaic (PV) techniques have their own advantages in PV plants for reducing the construction cost and improving the operational efficiency. However, the high input PV voltage increases the mismatch losses of PV arrays, which is also a key factor that influences the energy yield of PV plants. This paper proposes a three-input central capacitor (TICC) dc/dc converter for a high-voltage PV system, where four low-rating cascaded buck-boost converters connect to the series-connected three low-voltage PV arrays and two capacitors and realize the maximum power point tracking independently. Meanwhile, there is a neutral point in the proposed converter, enabling it to be connected with the rear-end three-level inverter directly. It can also help balance the three-level dc-link voltage by properly regulating the transferred energy among three input sources. Compared with other transformer-less dc-dc converters, the proposed converter is able to reduce the semiconductor voltage/current stress and therefore achieve the high efficiency. Simulation and experimental results verified the performance of the proposed TICC converter.

Keywords: PV system, three-level converter, central capacitor converter, photovoltaic (PV), dc-link voltage

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1 INTRODUCTION

Nowadays, the insulation level of PV panels has been developed to reach 1,500 V or even higher to improve the operational efficiency and reduce the construction cost of PV plants. It is claimed that the increment of PV maximum voltage from 1,000 to 1,500 V can lead to 15%–85% saving in conductor mass of cables and 25%–60% saving in the number of combiner boxes (Gkoutioudi et al., 2013). In addition, a high efficiency can be achieved by the reduced current on the dc bus and ac output and the larger operational range of inverters (Serban et al., 2015). However, the increased voltage level also brings some problems. In specific, the high-input PV voltage results in large mismatch power losses among PV panels caused by shadows, manufacturing tolerances, dirtiness, and so on (Kjaer et al., 2005). In addition, the high dc-link voltage leads to high voltage stress on semiconductor devices and a high common mode voltage, especially in the traditional two-level converters.

Currently, there are three widely used grid-tied PV inverters, which are the centralized inverter, the string or multi-string inverter, and the ac module or the module integrated converter (MIC) (Moghadasi et al., 2018). Among these converters, the centralized inverter and string or multi-string inverter are widely used in large-scale PV plants. Centralized inverters are usually connected to several PV arrays, each of which consists of many PV panels connected to the inverter dc-link, which

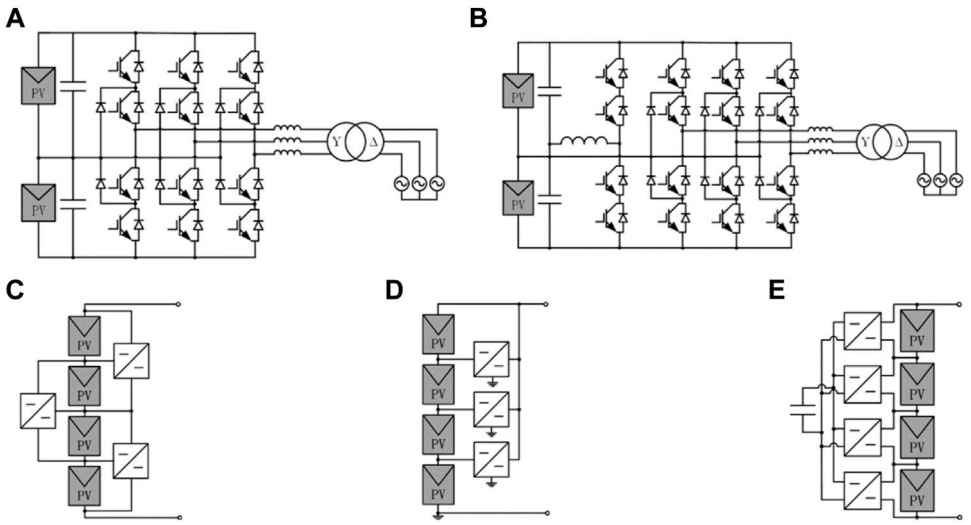

FIGURE 1 | (A) Dual-input three-level inverter. **(B)** Dual-input three-level inverter with an auxiliary power converter. **(C)** PV-to-PV DPP converter. **(D)** PV-to-bus DPP converter. **(E)** PV-to-virtual bus converter.

is simple, reliable, and efficient (Karanayil et al., 2019). However, this configuration can only provide a single MPPT operation, and hence, it will increase the mismatch loss with the increment of PV panels in series. Thus, although the insulation voltage level of PV panels has reached 1,500 V, the voltage of PV strings may not be suitable to reach such a high voltage level. Therefore, there is usually a trade-off between the voltage level and mismatch losses. Some works have been carried out to solve this problem (Park et al., 2013; Choi et al., 2015; Choudhury et al., 2016; Karanayil et al., 2019; Yan et al., 2019). In specific, a general control scheme for the dual-input three-level inverter shown in **Figure 1A** was proposed to track the maximum power points (MPPs) of two PV arrays independently (Yan et al., 2019). Moreover, an auxiliary power converter was proposed to operate under serious partial shading to reduce mismatch losses among PV arrays as shown in **Figure 1B** (Karanayil et al., 2019).

To improve the energy harnessing ability and reduce the switching voltage, several series differential power processing (DPP) architectures have been proposed (Shenoy et al., 2013; Stauth et al., 2013; Olalla et al., 2015), which are able to achieve the high efficiency by reducing the power rating of converters. As shown in **Figures 1C–E**, these series DPP architectures can be mainly classified into three groups: PV-to-PV DPP architectures, PV-to-bus architectures, and PV-to-virtual bus architectures. Regardless of the specific DPP architectures, each PV string can operate at its MPP. However, the total output voltage of the DPP converters is determined by the sum of the MPP voltages of all PV strings, which obviously makes DPP converters lack the voltage boost capability.

Another way to increase the voltage level of PV systems without too much PV panels connected in series is to use the two-stage PV systems with the front-end voltage boost capability. It can provide several advantages, such as a high energy yield and flexibility in plant design (Agamy et al., 2014). Although the distributed converters will lead to the decrease in conversion efficiency as well as an increase in cost per unit power as compared with the centralized converters, an annual energy yield gain of 6%–8% can be achieved to compensate the losses and cost of the additional converters (Elasser et al., 2010). In two-stage PV systems, the boost converter is widely used to step up the input PV voltage. Compared with the two-level inverter, the multi-level inverter can reduce the common mode voltage and improve the operational efficiency. Thus, the three-level boost converter can be assumed in front to reduce the voltage stress on semiconductor devices (Jung-Min Kwon et al., 2008; Tofoli et al., 2015). In Abdullah et al., 2014, a five-level diode-clamped inverter with the three-level boost converter was proposed to output a balanced five-level switching voltage, which further reduces the voltage stress.

Although the boost converter and three-level boost converter can step up the input voltage, they are more efficient when their input voltage is close to their output voltage as indicated in Zientarski et al., 2019. However, a higher input voltage means more PV panels in series and thus more mismatch losses. Therefore, it brings a trade-off between the converter efficiency and mismatch loss as the voltage level of the PV system increases. To overcome such a problem, a dual-input central capacitor (DICC) converter as shown in **Figure 2A** was proposed to simultaneously track two MPPs and then the input voltage of each PV array and semiconductor voltage/current stress of the converter can be reduced (Chen et al., 2017). Moreover, compared with DPP converters, DICC can maintain the dc-link voltage when the PV array voltage varies, which guarantees its energy harnessing ability. However, it is observed that both DPP converters and the DICC converter need an additional dc-link capacitor stage when they are connected to the multi-level rear-end inverters since these topologies have no distinct neutral point.

Being different, this paper proposes a three-input central capacitor (TICC) dc-dc converter, which can track the MPPs

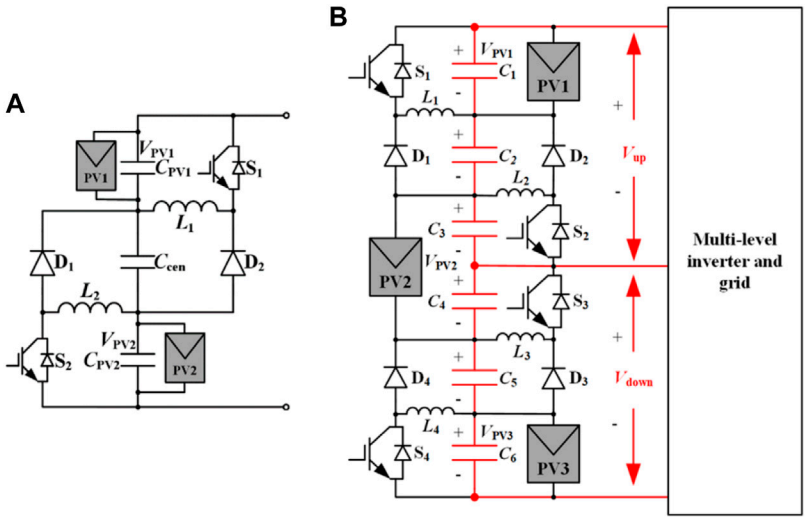

FIGURE 2 | (A) Dual-input central capacitor converter. **(B)** Three-input central capacitor converter.

of three PV sources independently. It combines the merits of DPP converters and traditional boost converters, reducing the mismatch loss and voltage/current stress as DPP converters and keeping a constant dc-link voltage as boost converters. Besides, it has a distinct neutral point, ensuring that it can be connected to the popular three-level inverter directly. Moreover, by regulating the power transfer of three input PV sources, the proposed converter can help balance the three-level dc-link voltage. The configuration principle of the TICC converter can be extended to build the generalized topologies for involving more PV sources. This paper is organized as follows: **Section 2** analyzes the operational principles and scalability of the proposed converter. Then, its control scheme is elaborated in **Section 3**. After that, a comparative study with its counterparts for high-voltage distributed PV architectures is presented in **Section 4**. Finally, Matlab simulations and an experiment prototype verified the performance of the proposed dc-dc converter.

2 OPERATIONAL PRINCIPLES AND SCALABILITY OF THE TICC CONVERTER

2.1 Operational Principles of the Proposed Converter

The proposed three-input central capacitor converter is drawn in **Figure 2B**, where six capacitors are in series to power the inversion stage. As a result, the dc-link voltage is divided by the capacitors in series, which reduces the voltage stress on semiconductor devices and provides the necessary neutral point for connecting the rear-end multi-level inverters. Moreover, the output dc voltage V_{bus} is equal to the voltage sum of six capacitors V_{CX} (X = 1–6), which can be written as

$$\begin{cases} V_{bus} = V_{up} + V_{down} \\ V_{up} = V_{C1} + V_{C2} + V_{C3} \\ V_{down} = V_{C4} + V_{C5} + V_{C6} \end{cases} \tag{1}$$

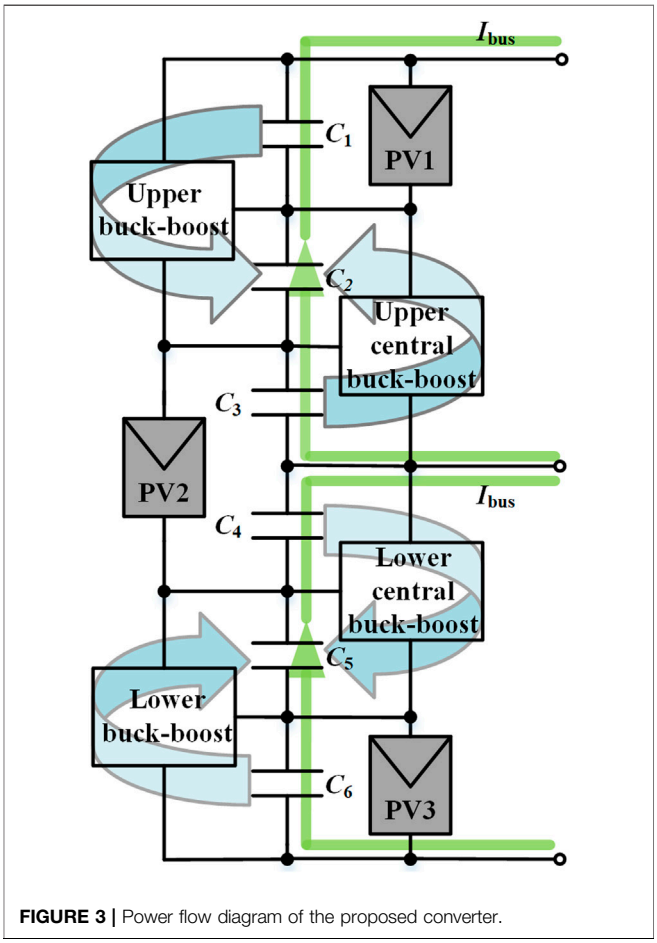

FIGURE 3 | Power flow diagram of the proposed converter.

where V_{up} and V_{down} are the upper and lower half parts of the dc bus voltage, respectively. Then, PV sources PV1 and PV3 are parallel with capacitors C_1 and C_6, respectively, and PV source

PV2 is parallel with capacitors C_3 and C_4, which makes the equivalent input voltage increase 3-fold.

The proposed converter consists of four cascaded buck-boost converters, as illustrated in **Figure 3**. To distinguish the four buck-boost converters, they are defined as an upper converter, an upper central converter, a lower central converter, and a lower converter from top to bottom. The upper converter and lower converter can regulate the output power of PV1 and PV3, respectively. Moreover, the upper central and lower central converters could regulate the output power of PV2 together.

As shown in **Figure 3**, each buck-boost converter transfers part of the output power of PV sources to the central capacitor C_2 and C_5. Moreover, the central capacitor discharges its energy by the dc-bus current I_{bus}. As long as the charging energy and discharging energy of the central capacitors C_2 and C_5 are balanced dynamically, the voltage of central capacitors can be well regulated. Therefore, the voltage of the central capacitor can vary as the output voltage of the PV source changes, and then the proposed converter can keep a constant dc-bus voltage, which distinguishes it from DPP converters. When the converter operates under CCM conditions, the relationship between the inductor currents and bus current can be calculated as

$$\begin{cases} (1-\boldsymbol{d_1})\boldsymbol{i_{L1}} + (1-\boldsymbol{d_2})\boldsymbol{i_{L2}} = \boldsymbol{I_{bus}} \\ (1-\boldsymbol{d_3})\boldsymbol{i_{L3}} + (1-\boldsymbol{d_4})\boldsymbol{i_{L4}} = \boldsymbol{I_{bus}} \end{cases} \tag{2}$$

where d_{x} (x = 1–4) is the duty cycle of switch $\mathrm{S_x}$ (x = 1–4). The voltage gain under CCM can be calculated as

$$\begin{cases} \boldsymbol{V_{C2}}/\boldsymbol{V_{C1}} = \boldsymbol{d_1}/(\boldsymbol{1}-\boldsymbol{d_1}) \\ \boldsymbol{V_{C2}}/\boldsymbol{V_{C3}} = \boldsymbol{d_2}/(\boldsymbol{1}-\boldsymbol{d_2}) \\ \boldsymbol{V_{C5}}/\boldsymbol{V_{C4}} = \boldsymbol{d_3}/(\boldsymbol{1}-\boldsymbol{d_3}) \\ \boldsymbol{V_{C5}}/\boldsymbol{V_{C6}} = \boldsymbol{d_4}/(\boldsymbol{1}-\boldsymbol{d_4}) \end{cases} \tag{3}$$

Therefore, the output dc voltage V_{bus} can be expressed as

$$\boldsymbol{V_{bus}} = \frac{1}{1-\boldsymbol{d_1}}\boldsymbol{V_{PV1}} + \boldsymbol{V_{PV2}} + \frac{1}{1-\boldsymbol{d_4}}\boldsymbol{V_{PV3}} \tag{4}$$

where V_{PV1} and V_{PV3} are the output voltages of PV sources PV1 and PV3, which are equal to V_{C1} and V_{C6}, respectively, and V_{PV2} is the output voltage of PV source PV2, which can be calculated as

$$\boldsymbol{V_{PV2}} = \boldsymbol{V_{C3}} + \boldsymbol{V_{C4}} \tag{5}$$

The DCM of the proposed converter differs from CCM by having an extra interval during each switching cycle when the instantaneous inductor current reaches zero. The boundary condition between CCM and DCM is attained as follows:

$$\boldsymbol{I_L} = \frac{\boldsymbol{V_{in}}\cdot\boldsymbol{d}}{2\boldsymbol{L}\cdot\boldsymbol{f_{sw}}} \tag{6}$$

where V_{in} is the input voltage on the capacitor of each buck-boost converter, and f_{sw} represents the switching frequency of the transistor. Like the buck-boost converter, DCM is likely to happen under low power and low inductance value conditions. The boost ratio under DCM can be expressed as

TABLE 1 | Main operational states of the proposed converter.

Switching combinations				Operational state
S_1	S_2	S_3	S_4	
1	1	1	1	State 1
1	1	1	0	
0	1	1	1	
0	1	1	0	
1	1	0	1	State 2
1	1	0	0	
0	1	0	1	
0	1	0	0	
1	0	1	1	State 3
1	0	1	0	
0	0	1	1	
0	0	1	0	
1	0	0	1	State 4
1	0	0	0	
0	0	0	1	
0	0	0	0	

$$\frac{\boldsymbol{V_{cen}}}{\boldsymbol{V_{PV}}} = \sqrt{1+\frac{3\boldsymbol{R_{eq}}\cdot\boldsymbol{d}^2}{8\boldsymbol{L}\cdot\boldsymbol{f_{sw}}}} - 1 \tag{7}$$

where $R_{\mathrm{eq}} = V_{\mathrm{bus}}/I_{\mathrm{bus}} = {V_{\mathrm{bus}}}^2/(3V_{\mathrm{PV}}I_{\mathrm{PV}})$, representing the equivalent load resistance of the inversion stage.

In addition, the DCM operation announces the merit of lower switching loss. Under DCM conditions, the transistors turn ON under zero current switching (ZCS), and also, the diodes turn OFF under ZCS. The reverse recovery current of the diode is well eliminated because the falling rate of diode current is limited by the inductor.

The three PV sources usually have the same specifications. However, in practice, their output power may be different and time-variant due to the variation of irradiance and some other factors, which can be expressed as

$$0 < \boldsymbol{P_{PVX}} \le \boldsymbol{P_{max}} \tag{8}$$

where P_{max} is the maximum rated output power of PV sources. During operation, the output power of upper and lower half parts of the TICC converter should be balanced dynamically to make V_{up} equal V_{down}, respectively, which can be achieved by properly regulating four independent switches. In specific, there are 16 switching combinations in total as listed in **Table 1**. Because the upper converter and the lower converter can work independently, the switching combinations of the proposed converter are then divided into four states according to the working states of the upper central and lower central converters, which need to coordinate with each other to regulate the output power of PV2 and balance the dc-bus voltage.

State 1: Both S_2 and S_3 are turned ON. PV2 charges inductors L_2 and L_3, as shown in **Figure 4A**.

State 2: Only S_2 is turned ON. The energy from PV2 is stored in L_2, and inductor L_3 discharges its energy to the central capacitor C_5, as shown in **Figure 4B**.

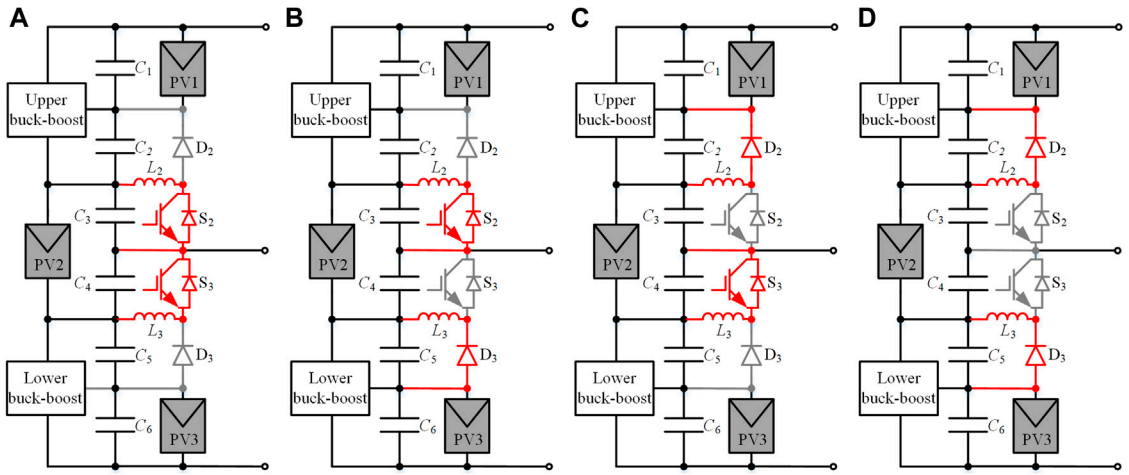

FIGURE 4 | (A) State 1, **(B)** state 2, **(C)** state 3, and **(D)** state 4 of the proposed converter.

State 3: Only S_3 is turned ON. The energy from PV2 is stored in L_3, and inductor L_2 discharges its energy to the central capacitor C_2, as shown in **Figure 4C**.

State 4: Both S_2 and S_3 are turned OFF. Inductors L_2 and L_3 discharge their energy to C_2 and C_5, respectively, as shown in **Figure 4D**.

It can be seen from State 2 and State 3 that the upper central converter and lower central converter can deliver differential power to capacitors C_2 and C_5, respectively. In specific, powers P_{C3} and P_{C4} absorbed by the upper central converter and lower central converter, respectively, from PV source PV2 can be expressed as

$$\begin{cases} \boldsymbol{P_{C3}} = \boldsymbol{V_{C3}} \cdot \boldsymbol{I_{PV2}} \\ \boldsymbol{P_{C4}} = \boldsymbol{V_{C4}} \cdot \boldsymbol{I_{PV2}} \end{cases} \tag{9}$$

Therefore, when the voltages on capacitors C_3 and C_4 are different, the upper central converter and lower central converter can send differential energy to capacitors C_2 and C_5, respectively, to balance the output voltage. In specific, the relationship between P_{C3} and P_{C4} should satisfy the following equation:

$$\boldsymbol{P_{PV1}} + \boldsymbol{P_{C3}} = \boldsymbol{P_{PV3}} + \boldsymbol{P_{C4}} \tag{10}$$

Thus, the dc-link voltage can be balanced by regulating the power difference P_{dif} between P_{C3} and P_{C4}, which can be derived as

$$\boldsymbol{P_{dif}} = \boldsymbol{P_{C3}} - \boldsymbol{P_{C4}} = \boldsymbol{V_{C3}}\boldsymbol{I_{PV2}} - \boldsymbol{V_{C4}}\boldsymbol{I_{PV2}} \tag{11}$$

where V_{C3} and V_{C4} can be expressed as

$$\begin{cases} \boldsymbol{V_{C3}} = (1 - \boldsymbol{d_2})\left(\boldsymbol{V_{up}} - \boldsymbol{V_{PV1}}\right) \\ \boldsymbol{V_{C4}} = (1 - \boldsymbol{d_3})\left(\boldsymbol{V_{down}} - \boldsymbol{V_{PV3}}\right) \end{cases} \tag{12}$$

Then, the power difference P_{dif} can be further calculated as

$$\boldsymbol{P_{dif}} = (1 - \boldsymbol{d_3})\left[\left(\boldsymbol{V_{up}} - \boldsymbol{V_{down}}\right) + \left(\boldsymbol{V_{PV3}} - \boldsymbol{V_{PV1}}\right)\right]\boldsymbol{I_{PV2}} - (\boldsymbol{d_2} - \boldsymbol{d_3}) \cdot \left(\boldsymbol{V_{up}} - \boldsymbol{V_{PV1}}\right)\boldsymbol{I_{PV2}} \tag{13}$$

Because V_{PV1} is approximately equal to V_{PV3} and V_{up} is approximately equal to V_{down}, the **Eq. 13** can be simplified as

$$\boldsymbol{P_{dif}} \approx -(\boldsymbol{d_2} - \boldsymbol{d_3}) \cdot \left(\boldsymbol{V_{up}} - \boldsymbol{V_{PV1}}\right)\boldsymbol{I_{PV2}} \tag{14}$$

Thus, the upper central converter and lower central converter can help balance the power difference between P_{PV1} and P_{PV3} by regulating the difference between d_2 and d_3, and then the proposed converter can output a balanced three-level dc-bus voltage. The input power of PV2 can be derived as

$$\begin{aligned} \boldsymbol{P_{PV2}} = \boldsymbol{P_{C3}} + \boldsymbol{P_{C4}} = \\ (2 - \boldsymbol{d_2} - \boldsymbol{d_3}) \cdot \left(\boldsymbol{V_{up}} - \boldsymbol{V_{PV1}}\right) \cdot \boldsymbol{I_{PV2}} - (1 - \boldsymbol{d_3}) \\ \left[\left(\boldsymbol{V_{down}} - \boldsymbol{V_{up}}\right) + \left(\boldsymbol{V_{PV1}} - \boldsymbol{V_{PV3}}\right)\right] \cdot \boldsymbol{I_{PV2}}\,(1 - \boldsymbol{d_3}) \\ \left[\left(\boldsymbol{V_{down}} - \boldsymbol{V_{up}}\right) + \left(\boldsymbol{V_{PV1}} - \boldsymbol{V_{PV3}}\right)\right] \cdot \boldsymbol{I_{PV2}} \end{aligned} \tag{15}$$

Similarly, the **Eq. 15** can be simplified as

$$\boldsymbol{P_{PV2}} \approx (2 - \boldsymbol{d_2} - \boldsymbol{d_3}) \cdot \left(\boldsymbol{V_{up}} - \boldsymbol{V_{PV1}}\right) \cdot \boldsymbol{I_{PV2}} \tag{16}$$

Then, the sum of d_2 and d_3 can also help regulate the output power of PV2. Thus, the proposed converter can regulate the power of three PV sources and balance the three-level dc-link voltage.

Under normal conditions, where the power difference among three PV sources is small, the upper converter and the lower converter can track the MPPs of PV1 and PV3, respectively. The upper central converter and the lower central converter can track the MPP of PV2 together and compensate the power difference between P_{PV1} and P_{PV3}, as illustrated in **Figure 5A**.

However, under some extreme conditions, where there is a large power mismatch among three PV sources as shown in **Figure 5B**, the unbalance of three-level dc-link voltage may occur. In specific, the proposed converter cannot keep a balanced output voltage when the power difference

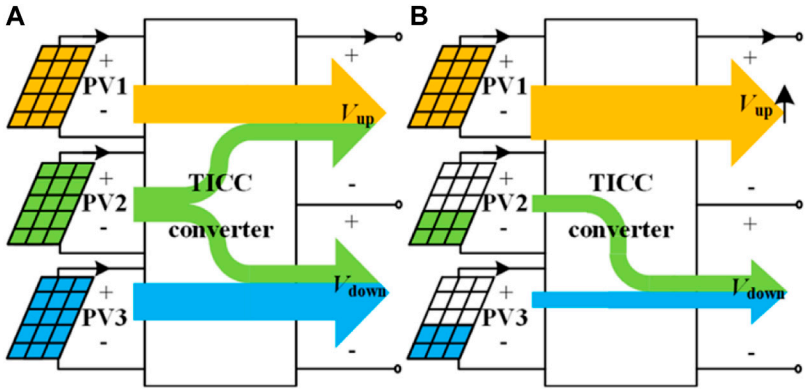

FIGURE 5 | Power flow diagrams of the TICC converter **(A)** when PV2 can compensate the power difference between PV1 and PV3 and **(B)** when PV2 cannot compensate the power difference between PV2 and PV3.

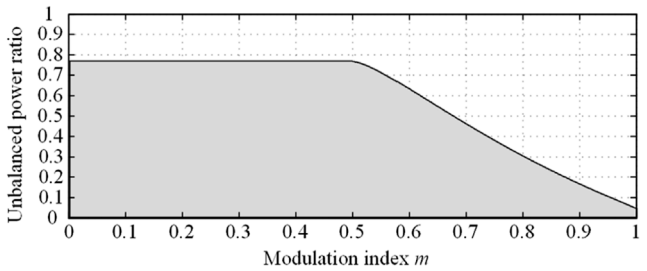

FIGURE 6 | Voltage balance limit of the NPC inverter using SVM.

between P_{PV1} and P_{PV3} is larger than P_{PV2}, which can be expressed as

$$|\boldsymbol{P}_{\mathbf{PV1}} - \boldsymbol{P}_{\mathbf{PV3}}| > \boldsymbol{P}_{\mathbf{PV2}} \tag{17}$$

However, fortunately, the rear-end three-level inverter can help balance the output voltage of the proposed converter by regulating its PWM sequences (Lyu et al., 2015; Rivera et al., 2015; Tan et al., 2016). In such a case, PV2 sends all its power to compensate the power difference between P_{PV1} and P_{PV3}, as shown in **Figure 5B**. The rest power difference is compensated by the rear-end three-level inverter, whose ability to balance the dc bus voltage varies with the different methods. For example, the method presented in Rivera et al., 2015, which used the SVM for the NPC inverter, can achieve the compensation ability as shown in the shaded area of **Figure 6**, which can be expressed as

$$\boldsymbol{\eta}_n = \frac{12\boldsymbol{\alpha}}{2\sqrt{3\pi \boldsymbol{m}}} \tag{18}$$

Here, η_n is the limit of the maximum unbalanced power ratio between the unbalanced power and the output power, α is the maximum voltage drift that can be minimized by redistributing the dwell time allocation for redundant small vectors, and m is the modulation index of the NPC inverter. Thus, the NPC inverter

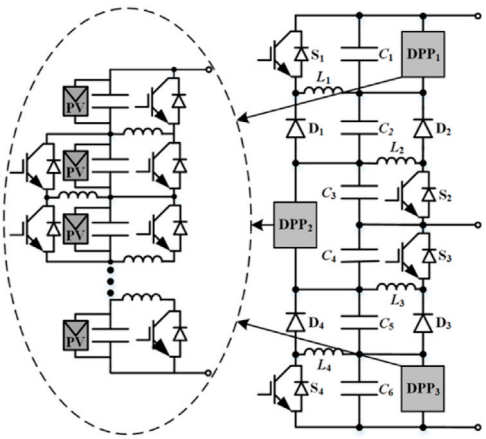

FIGURE 7 | Extended configuration of the TICC converter where each PV source is replaced with the DPP converter.

can balance the dc bus voltage when the unbalanced power ratio is lower than the limit as expressed below:

$$\frac{|\boldsymbol{P}_{PV1} - \boldsymbol{P}_{PV3}| - \boldsymbol{P}_{PV2}}{\boldsymbol{P}_{PV1} + \boldsymbol{P}_{PV2} + \boldsymbol{P}_{PV3}} < \boldsymbol{\eta}_n \tag{19}$$

Therefore, even if any PV source suffers a permanent damage, the other two PV sources can still work well as long as the **Eq. 19** is satisfied. When the three-level inverter is unable to balance the output voltage because the inverter needs more freedom to improve the grid-side current quality (Yaramasu and Wu, 2014) or the unbalanced power ratio is higher than the limit, a non-maximum power point tracking (non-MPPT) algorithm (also known as constant power generation) (Vekic et al., 2017; Liu et al., 2018; Tafti et al., 2018) is enabled to reduce the output power of PV1 or PV3 by forcing it to track the given power references.

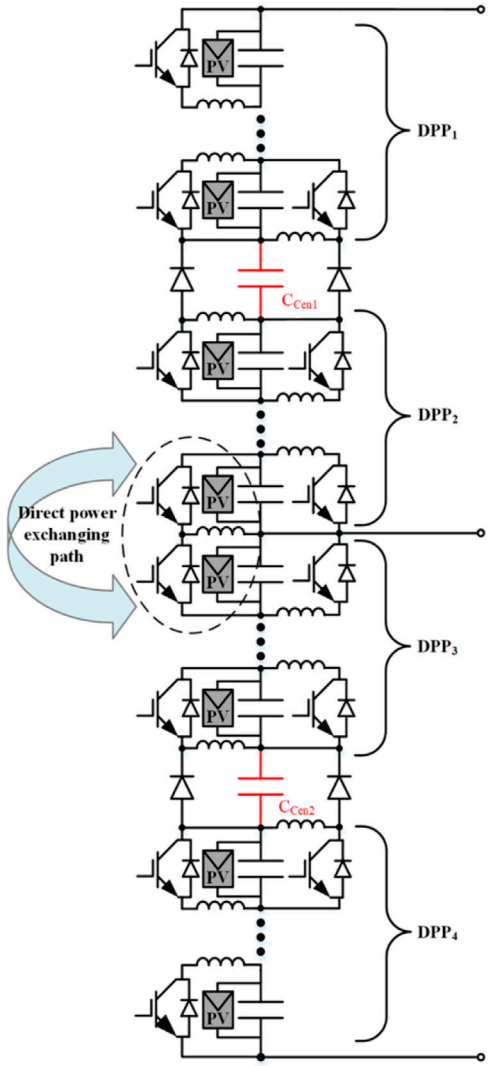

FIGURE 8 | Extended configuration of the TICC converter where four PV-to-PV DPP converters are embedded.

2.2 Scalability of the Proposed Converter

To further extend the generalization of the proposed converter configuration, two methods are presented here to scale up the number of PV sources. The first method is to replace each PV source in the TICC converter with a DPP converter, as shown in **Figure 7**, whose advantage is that it can decouple the control of the TICC converter and each DPP converter, which is beneficial to the modular design. The second method is to embed four PV-to-PV DPP converters to the TICC converter as shown in **Figure 8**, which can also be seen as embedding two central capacitors in a PV-to-PV DPP converter. It is noted that there is a direct power exchanging path between the upper half part and the lower half part in **Figure 8**, which can help balance the dc-link voltage, and then the converter can output the qualified three-level voltages. The detailed operational principle of **Figure 7** and **Figure 8** will not be comprehensively elaborated because they are out of the scope of this paper.

3 CONTROL STRATEGY OF THE PROPOSED CONVERTER

3.2 Operational Principles of the Proposed Converter

In each sampling period, the output power of each PV source and the voltage balance limit η_n are calculated to allocate the balancing task between the proposed converter and the rear-end three-level inverter. The flow chart of their coordinated control scheme is demonstrated in **Figure 9A**.

When the inverter cannot balance the dc-link voltage or P_{PV2} is enough to compensate the power difference between P_{PV1} and P_{PV3}, which can be expressed as an **Eq. 20**

$$|P_{PV1} - P_{PV3}| < P_{PV2} \tag{20}$$

the voltage balance control (VBC) in the dc side is responsible to balance the dc-link voltage. Otherwise, the VBC in the ac side is enabled to help balance the dc-link voltage and all the output power of PV2 is sent to compensate the power difference between P_{PV1} and P_{PV3} in the dc side. Therefore, the power difference P_{dif} between P_{C3} and P_{C4}, which determines the compensated power provided by PV2, can be calculated as

$$|P_{dif}| = P_{PV2} \tag{21}$$

Then, if the unbalanced power ratio is within the maximum voltage balance limit η_n as expressed in the **Eq. 19**, the VBC in the dc side or ac side can keep a balanced dc-link voltage when three PV sources work at their MPPs. Otherwise, PV1 or PV3 is forced to operate at the non-MPPT mode and track the given power reference until the possible maximum unbalanced power ratio is reduced to the voltage balance limit. The flow chart of switching the control mode of each PV source and generating its power reference at non-MPPT control is shown in **Figure 9B**. When the power difference of three PV sources is lower than the limit of the maximum unbalanced power ratio of the NPC inverter η_n as indicated in **Eq. 19**, the three PV sources can all work at the MPPT mode. Otherwise, the non-MPPT mode of PV1 or PV3 is enabled to balance the dc-link voltage. The power reference of the PV source at the non-MPPT mode can be calculated by

$$\begin{cases} P_{ref1} = \dfrac{1+\eta_n}{1-\eta_n}(P_{PV2} + P_{PV3}) \\ \quad or \\ P_{ref3} = \dfrac{1+\eta_n}{1-\eta_n}(P_{PV2} + P_{PV1}) \end{cases} \tag{22}$$

Then, it can return to the MPPT mode until the possible maximum unbalanced power ratio is reduced to the voltage balance limit. The possible maximum unbalanced power ratio is given by

$$\begin{cases} \dfrac{P_{max} - P_{PV2} - P_{PV3}}{P_{max} + P_{PV2} + P_{PV3}} < \eta_n \\ \quad or \\ \dfrac{P_{max} - P_{PV1} - P_{PV2}}{P_{max} + P_{PV1} + P_{PV2}} < \eta_n \end{cases} \tag{23}$$

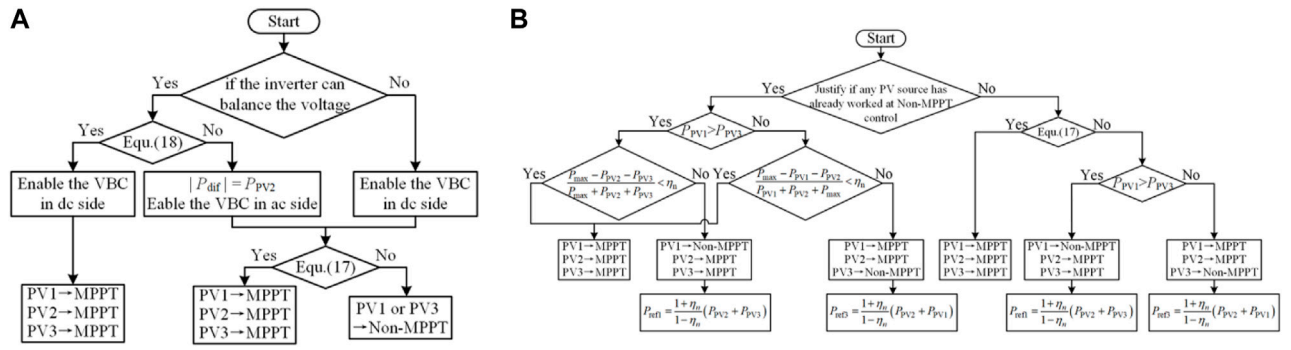

FIGURE 9 | Flow chart of **(A)** coordinated control scheme between the proposed converter and the rear-end inverter. **(B)** Switching the control mode of each PV source and generating its power reference at non-M.

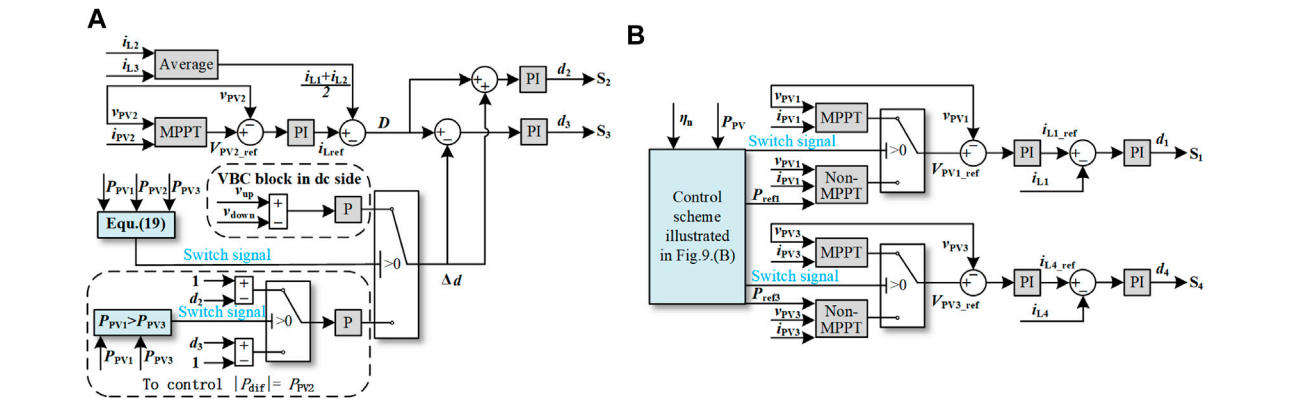

FIGURE 10 | (A) Control scheme of the upper central and lower central converters. **(B)** Control scheme of the upper and lower converters.

where P_{max} is the maximum output power of PV sources.

Figure 10A shows the control scheme of the upper central and lower central converters. The P&Q method is used to track the MPP of PV source PV2 and provides the voltage reference V_{PV2_ref} (Qian Zhang et al., 2014). A double-loop control strategy is applied to control the converters (Tan and Middlebrook, 1995), in which the outer loop regulates the output voltage of PV2 by generating the current reference i_{Lref} and the inner loop regulates the average current of i_{L2} and i_{L3} and balances the dc-link voltage. A voltage balance component Δd is introduced to regulate the power difference between P_{C3} and P_{C4}. When the VBC in the dc side is responsible to balance the dc-link voltage (Kim et al., 2018), Δd is given by the **Eq. 24**

$$\boldsymbol{\Delta d = kp_{balance}\left(V_{up} - V_{down}\right)} \tag{24}$$

where $kp_{balance}$ is the proportional gain of the controller. As demonstrated in **Section 2.1**, the difference between d_2 and d_3 plays an important role in regulating P_{dif}. The relationship between duty ratios d_2 and d_3 can be calculated as

$$\boldsymbol{d_2 - d_3 = 2G_{PI}(s) \cdot \Delta d} \tag{25}$$

Then, Δd can be used to regulate P_{dif} and is proportional to the difference between V_{up} and V_{down}, which therefore can be used to balance the three-level dc-link voltage. The sum of d_2 and d_3 can determine the value of P_{PV2}, which can be calculated as

$$\boldsymbol{d_2 + d_3 = 2G_{PI}(s) \cdot D} \tag{26}$$

where D is the deviation between the current reference i_{Lref} and the average current of i_{L2} and i_{L3}. Therefore, D can be used to control P_{PV2}.

While the VBC in the ac side is enabled to balance the dc-link voltage, the power difference P_{dif} between P_{C3} and P_{C4} need to equal P_{PV2}. Because the sum of P_{C3} and P_{C4} equals P_{PV2}, P_{C3} and P_{C4} can be calculated as

$$\begin{cases} \boldsymbol{P_{C3}} = \begin{cases} 0, & \boldsymbol{P_{PV1} > P_{PV3}} \\ \boldsymbol{P_{PV2}}, & \boldsymbol{P_{PV1} < P_{PV3}} \end{cases} \\ \boldsymbol{P_{C4}} = \begin{cases} \boldsymbol{P_{PV2}}, & \boldsymbol{P_{PV1} > P_{PV3}} \\ 0, & \boldsymbol{P_{PV1} < P_{PV3}} \end{cases} \end{cases} \tag{27}$$

It can be seen from the **Eq. 9** and **Eq. 12** that P_{C3} and P_{C4} decrease to 0 when d_2 and d_3 increase to 1. Thus, to make P_{dif} equal P_{PV2}, P_{C3} or P_{C4} needs to decrease to 0 by controlling d_2 or d_3. Then, the voltage balance component Δd can be calculated as

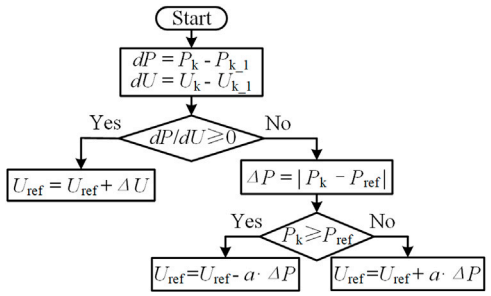

FIGURE 11 | Flowchart of the non-MPPT algorithm.

$$\Delta \boldsymbol{d} = \begin{cases} \boldsymbol{kp} \cdot (1 - \boldsymbol{d}_2), & \boldsymbol{P}_{PV1} > \boldsymbol{P}_{PV3} \\ \boldsymbol{kp} \cdot (\boldsymbol{d}_3 - 1), & \boldsymbol{P}_{PV1} < \boldsymbol{P}_{PV3} \end{cases} \tag{28}$$

where kp is the proportional gain of the controller.

The upper and lower converters also employ the double-loop control strategy, as shown in **Figure 10B**. The control scheme shown in **Figure 9B** is used to switch the control modes of PV1 and PV3 between the MPPT control and non-MPPT control. Then, the outer loop regulates the output power of PV sources by controlling their output voltage, and the inner loop controls the inductor current i_L by providing the duty cycle to the switch.

3.3 Non-Maximum Power Point Tracking Algorithm

There are several methods for PV sources to track the given power references (Vekic et al., 20172017; Liu et al., 2018; Tafti et al., 2018). Among them, the non-MPPT algorithm described in Liu et al., 2018 is used in this paper, whose flowchart is shown in **Figure 11**, where the comparison of dP/dU with zero is performed first to make a distinction between states in the unacceptable zone (left from the MPP) and desired zone (right from the MPP) (Vekic et al., 20172017). Then, a variable step ΔP is employed to reduce both the overshoot of the dc-link voltage and the active power oscillations, which reduces its value when P_k is close to P_{ref}. a is the coefficient of the power point tracking step.

4 PERFORMANCE COMPARISON AND PASSIVE COMPONENT DESIGN

To evaluate the properties of the proposed converter, its performance has been compared with its counterparts including the traditional boost converter, interleaved boost converter, three-level boost converter, and dual-input central capacitor converter.

4.1 Analysis and Comparison of Device Quantity

The device quantity of the proposed converter and its counterparts has been compared from the aspects of total and average device quantity as listed in **Table 2**. The average device quantity is the ratio of total device quantity over the quantity of PV sources. It can be observed that although the total device quantity of the proposed converter increases, the average device quantity of the proposed converter is less than or almost equal to those of its counterparts.

4.2 Analysis and Comparison of Semiconductor Device Stress

When the proposed converter operates under CCM and the output power and voltage of three PV sources are equal, the relationship between the input PV voltage V_{PV} and the output voltage V_{bus} can be derived from **Eq. 29**

$$\begin{cases} \boldsymbol{V}_{\mathbf{PV}} \cdot \boldsymbol{d}_1 = \dfrac{1}{2} (\boldsymbol{V}_{\mathbf{bus}} - 3\boldsymbol{V}_{\mathbf{PV}}) \cdot (1 - \boldsymbol{d}_1) \\ \dfrac{\boldsymbol{V}_{\mathbf{PV}}}{2} \cdot \boldsymbol{d}_2 = \dfrac{1}{2} (\boldsymbol{V}_{\mathbf{bus}} - 3\boldsymbol{V}_{\mathbf{PV}}) \cdot (1 - \boldsymbol{d}_2) \end{cases} \tag{29}$$

Also, when the output power and voltage of three PV sources are equal, the power transferred from PV1 and PV3 to the central capacitors is equal and PV2 transfers equal power to the central capacitor C_2 and C_5. Thus, the power transferred from PV1 to C_2 is twice the power transferred from PV2 to C_2. According to the method of power balance on the central capacitor C_2, the following equation can be derived:

$$\begin{cases} \dfrac{2}{3} \boldsymbol{V}_{C2} \cdot \boldsymbol{I}_{bus} = \boldsymbol{V}_{C1} \cdot \boldsymbol{I}_{avg\_S1} \\ \dfrac{1}{3} \boldsymbol{V}_{C2} \cdot \boldsymbol{I}_{bus} = \boldsymbol{V}_{C3} \cdot \boldsymbol{I}_{avg\_S2} \end{cases} \tag{30}$$

where V_{C2} can be calculated as

$$\boldsymbol{V}_{C2} = \frac{1}{2} (\boldsymbol{V}_{bus} - 3\boldsymbol{V}_{PV}) \tag{31}$$

and V_{C1} and V_{C3} can be calculated as

$$\begin{cases} \boldsymbol{V}_{C1} = \boldsymbol{V}_{PV} \\ \boldsymbol{V}_{C3} = \boldsymbol{V}_{PV}/2 \end{cases} \tag{32}$$

Thus, the average currents through S_1 and S_2 can be calculated as

$$\begin{cases} \boldsymbol{I}_{\mathbf{avg\_S1}} = \dfrac{(\boldsymbol{V}_{\mathbf{bus}} - 3\boldsymbol{V}_{\mathbf{PV}}) \cdot \boldsymbol{I}_{\mathbf{bus}}}{3\boldsymbol{V}_{\mathbf{PV}}} \\ \boldsymbol{I}_{\mathbf{avg\_S2}} = \dfrac{(\boldsymbol{V}_{\mathbf{bus}} - 3\boldsymbol{V}_{\mathbf{PV}}) \cdot \boldsymbol{I}_{\mathbf{bus}}}{3\boldsymbol{V}_{\mathbf{PV}}} \end{cases} \tag{33}$$

Because the switches only conduct during turn-on intervals, their peak current stresses can be calculated as

$$\begin{cases} \boldsymbol{I}_{\mathbf{peak\_S1}} = \dfrac{\boldsymbol{I}_{\mathbf{avg,\ IGBT\_S1}}}{\boldsymbol{d}_1} = \dfrac{(\boldsymbol{V}_{\mathbf{bus}} - \boldsymbol{V}_{\mathbf{PV}})\boldsymbol{I}_{\mathbf{bus}}}{3\boldsymbol{V}_{\mathbf{PV}}} \\ \boldsymbol{I}_{\mathbf{peak\_S2}} = \dfrac{\boldsymbol{I}_{\mathbf{avg,\ IGBT\_S2}}}{\boldsymbol{d}_2} = \dfrac{(\boldsymbol{V}_{\mathbf{bus}} - 2\boldsymbol{V}_{\mathbf{PV}})\boldsymbol{I}_{\mathbf{bus}}}{3\boldsymbol{V}_{\mathbf{PV}}} \end{cases} \tag{34}$$

Here, the inductor current ripple has been neglected for simplicity. Similarly, the average current of diodes D_1 and D_2 can be expressed as

TABLE 2 | Comparison of device quantity.

	Boost	Interleaved boost	Three-level boost	Dual-input central capacitor	TICC
Quantity of PV sources	1	1	1	2	3
Total quantity of transistors	1	2	2	2	4
Total quantity of diodes	1	2	2	2	4
Total quantity of inductors	1	2	1	2	4
Total quantity of capacitors	2	2	3	3	6
Total quantity of voltage sensors	2	2	3	3	5
Total quantity of current sensors	2	3	2	4	7
Average quantity of transistors	1	2	2	1	4/3
Average quantity of diodes	1	2	2	1	4/3
Average quantity of inductors	1	2	1	1	4/3
Average quantity of capacitors	2	2	3	3/2	2
Average quantity of voltage sensors	2	2	3	3/2	5/3
Average quantity of current sensors	2	3	2	2	7/3

TABLE 3 | Comparison of semiconductor device stress.

	Boost	Interleaved boost	Three-level boost	Dual-input central capacitor converter	TICC	
					S1 (4)/D1 (4)	S2 (3)/D2 (3)
Peak voltage stress of transistors/diodes	V_{bus}	V_{bus}	$V_{bus}/2$	$V_{bus} - V_{PV}$	$(V_{bus} - V_{PV})/2$	$V_{bus}/2 - V_{PV}$
Peak current stress of transistors/diodes	$\frac{V_{bus} \cdot I_{bus}}{V_{PV}}$	$\frac{V_{bus} \cdot I_{bus}}{2V_{PV}}$	$\frac{V_{bus} \cdot I_{bus}}{V_{PV}}$	$\frac{(V_{bus}-V_{PV}) \cdot I_{bus}}{2V_{PV}}$	$\frac{(V_{bus}-V_{PV}) \cdot I_{bus}}{3V_{PV}}$	$\frac{(V_{bus}-2V_{PV}) \cdot I_{bus}}{3V_{PV}}$
Average current stress of transistors	$\frac{(V_{bus}-V_{PV}) \cdot I_{bus}}{V_{PV}}$	$\frac{(V_{bus}-V_{PV}) \cdot I_{bus}}{2V_{PV}}$	$\frac{(V_{bus}-V_{PV}) \cdot I_{bus}}{V_{PV}}$	$\frac{(V_{bus}-2V_{PV}) \cdot I_{bus}}{2V_{PV}}$	$\frac{(V_{bus}-3V_{PV}) \cdot I_{bus}}{3V_{PV}}$	
Average current stress of diodes	I_{bus}	$I_{bus}/2$	I_{bus}	$I_{bus}/2$	$2I_{bus}/3$	$I_{bus}/3$
Sum of processed maximum powers of all semiconductor devices	$\frac{2V_{bus}^2 \cdot I_{bus}}{V_{PV}}$	$\frac{2V_{bus}^2 \cdot I_{bus}}{V_{PV}}$	$\frac{2V_{bus}^2 \cdot I_{bus}}{V_{PV}}$	$\frac{2(V_{bus}-V_{PV})^2 \cdot I_{bus}}{V_{PV}}$	$\frac{2[(V_{bus}-V_{PV})^2+(V_{bus}-2V_{PV})^2] \cdot I_{bus}}{3V_{PV}}$	

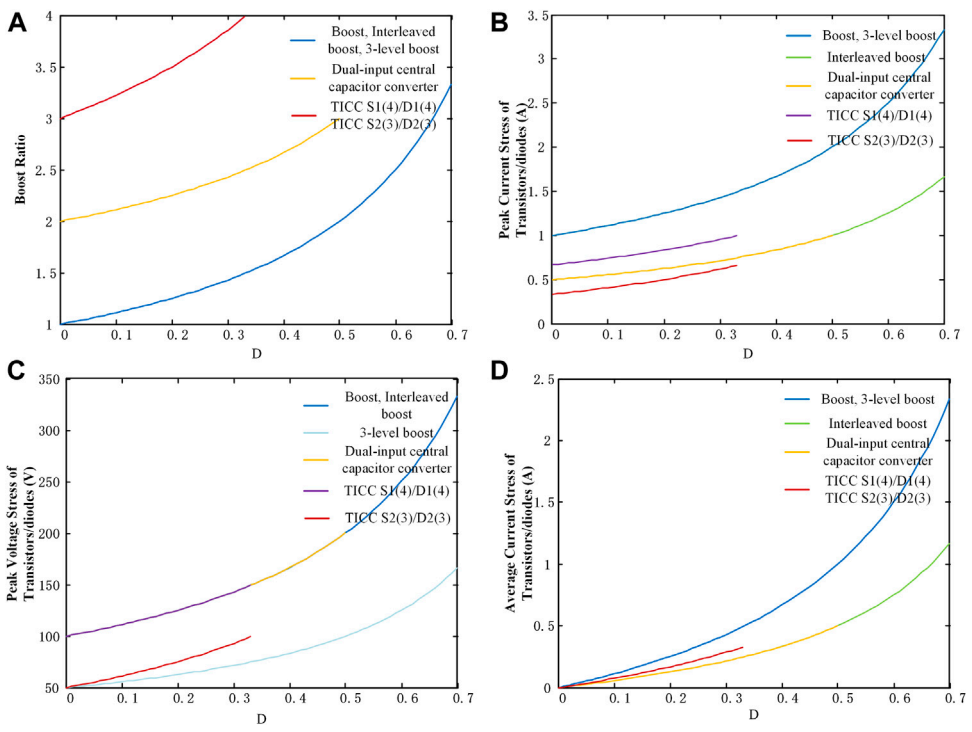

FIGURE 12 | (A) Boost ratio, **(B)** peak current stresses of transistors/diodes, **(C)** peak voltage stresses of transistors/diodes, **(D)** average current stresses of transistors/diodes vs. duty ratio.

TABLE 4 | Comparison of semiconductor device stress.

	Boost	Interleaved boost	Three-level boost	Dual-input central capacitor converter	TICC	
					S1 (4)/D1 (4)	S2 (3)/D2 (3)
Boost ratio	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{2-D}{1-D}$	$\frac{3-D}{1-D}$	
Peak voltage stress of transistors/diodes	$\frac{V_{PV}}{1-D}$	$\frac{V_{PV}}{1-D}$	$\frac{V_{PV}}{2(1-D)}$	$\frac{V_{PV}}{1-D}$	$\frac{V_{PV}}{1-D}$	$\frac{(1+D)V_{PV}}{2(1-D)}$
Peak current stress of transistors/diodes	$\frac{I_{bus}}{1-D}$	$\frac{I_{bus}}{2(1-D)}$	$\frac{I_{bus}}{1-D}$	$\frac{I_{bus}}{2(1-D)}$	$\frac{2I_{bus}}{3(1-D)}$	$\frac{(1+D)I_{bus}}{3(1-D)}$
Average current stress of transistors	$\frac{DI_{bus}}{1-D}$	$\frac{DI_{bus}}{2(1-D)}$	$\frac{DI_{bus}}{1-D}$	$\frac{DI_{bus}}{2(1-D)}$	$\frac{2DI_{bus}}{3(1-D)}$	

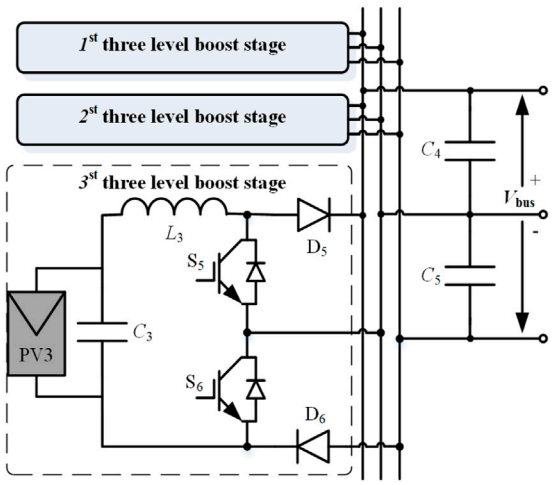

FIGURE 13 | Three three-level boost converters.

$$\begin{cases} \boldsymbol{I}_{\mathbf{avg\_D1}} = 2\boldsymbol{I}_{\mathbf{bus}}/3 \\ \boldsymbol{I}_{\mathbf{avg\_D2}} = \boldsymbol{I}_{\mathbf{bus}}/3 \end{cases} \tag{35}$$

The processed maximum power of each semiconductor device can be derived by multiplying its peak voltage stress by its peak current stress. The comparison of semiconductor device stress is listed in **Table 3**. It can be seen that the voltage and current stresses of transistors and diodes in the proposed converter are mostly lower than those of its counterparts. Although more devices have been used, the sum of the processed maximum power of all switches and diodes for the TICC converter is the smallest.

Figure 12 illustrates the relationship between boost ratio, voltage stress, current stress, and duty ratio when the input voltage V_{PV} equals to 100 V and the current of dc bus I_{bus} equals to 1 A, where their equations are listed in **Table 4**.

It can be seen that the boost ratio has nearly tripled and the peak and average current stresses have been halved, compared with the three-level boost converter. Although the peak voltage stress has nearly doubled when the duty ratio is the same, the voltage stress under the same output voltage is reduced as listed in **Table 3**.

4.3 Analysis and Comparison of Power Loss

As analyzed in Dusmez et al., 2015, the three-level boost converter shows its superior efficiency performance over the traditional boost converter and interleaved boost converter. Therefore, to analyze the efficiency performance of the proposed converter, the proposed TICC converter can be only compared with three-level boost (THB) converters shown in **Figure 13** under the same input and output conditions. The loss calculation is based on the parameters listed in **Table 5**. The calculation process of the semiconductor losses is composed of two steps. First, the loss-calculation model for a single device (IGBT or diode), which satisfies the requirement of the maximum conduction current and withstand voltage, is established by using the method of curve fitting to get the function relationship between the collector current and turn-on losses, the function relationship between the collector current and turn-off losses, and so on. Here, a datasheet of the IGBT module from Infineon is used to establish the loss-calculation model (Infineon, 2017). Then, the switching and conduction losses during each switching period can be obtained from the loss-calculation model in Agamy et al., 2014.

The semiconductor losses are composed of IGBT's switching losses and conduction losses, the diode's reverse-recovery losses, and conduction losses, which can be calculated as

$$\begin{cases} \boldsymbol{P}_{\mathbf{switch\_IGBT}} = \left(\boldsymbol{E}_{\mathbf{on}}\left(\boldsymbol{i}_{\mathbf{peak}}\right) + \boldsymbol{E}_{\mathbf{off}}\left(\boldsymbol{i}_{\mathbf{peak}}\right)\right) \cdot \dfrac{\boldsymbol{V}_{\mathbf{sw}}}{\boldsymbol{V}_{\mathbf{rated}}} \cdot \boldsymbol{f}_{\mathbf{sw}} \\ \boldsymbol{P}_{\mathbf{con\_IGBT}} = \boldsymbol{I}_{\mathbf{avg\_IGBT}} \cdot \boldsymbol{V}_{\mathbf{CE}}\left(\boldsymbol{i}_{\mathbf{peak}}\right) \\ \boldsymbol{P}_{\mathbf{rec\_diode}} = \boldsymbol{E}_{\mathbf{rec}}\left(\boldsymbol{i}_{\mathbf{peak}}\right) \cdot \dfrac{\boldsymbol{V}_{\mathbf{sw}}}{\boldsymbol{V}_{\mathbf{rated}}} \cdot \boldsymbol{f}_{\mathbf{sw}} \\ \boldsymbol{P}_{\mathbf{con\_diode}} = \boldsymbol{I}_{\mathbf{avg\_diode}} \cdot \boldsymbol{V}_{\boldsymbol{F}}\left(\boldsymbol{i}_{\mathbf{peak}}\right) \end{cases} \tag{36}$$

where $P_{\text{switch\_IGBT}}$ and $P_{\text{con\_IGBT}}$ represent the switching and conduction power losses of IGBTs, and E_{on} (i_{peak}) and E_{off} (i_{peak}) refer to the turn-on and turn-off energy losses of IGBT, which are the functions of the collector current i_{peak} that passes through the IGBT. V_{sw} is the practical switching voltage of the switching process, V_{rated} is the rated switching voltage of the switching process, and f_{sw} is the switching frequency. $I_{\text{avg\_IGBT}}$ and $I_{\text{avg\_diode}}$ are the average currents that pass through IGBT and diode, respectively. V_{CE} (i_{peak}) is the collector-emitter voltage of IGBT, which is the function of the collector current i_{peak}. $P_{\text{rec\_diode}}$ and $P_{\text{con\_diode}}$ are the reverse-recovery and conduction power losses of diodes, respectively. E_{rec} (i_{peak}) is the reverse-recovery energy loss of the diode, which is the function of the forward current

TABLE 5 | Parameters for loss calculation.

Parameter	Value
Dc-bus voltage V_{bus}	1200 V
Dc-bus current I_{bus}	9 A
Switching frequency f_{sw}	20 kHz
IGBT module	FP10R12W1T4P, 10 A/1,200 V
Inductor core, DC resistance for 3-THB (V_{PV} = 200 V)	Magnetics 77,166, 0.0977 Ω
Inductor core, DC resistance for 3-THB (V_{PV} = 300 V)	Magnetics 77,166, 0.197 Ω
Inductor core, DC resistance for 3-THB (V_{PV} = 400 V)	Magnetics 77,166, 0.333 Ω
Inductor core, DC resistance for 3-THB (V_{PV} = 500 V)	Magnetics 77,735, 0.4 Ω
Inductor core, DC resistance for 3-THB (V_{PV} = 600 V)	Magnetics 77,735, 0.5696 Ω
Inductor core, DC resistance for 3-THB (V_{PV} = 700 V)	Magnetics 77,735, 0.8 Ω
Inductor core, DC resistance for TICC (V_{PV} = 200 V) L_1 (L_4)	Magnetics 77,735, 0.207 Ω
Inductor core, DC resistance for TICC (V_{PV} = 200 V) L_2 (L_3)	Magnetics 77,735, 0.149 Ω
Inductor core, DC resistance for TICC (V_{PV} = 300 V) L_1 (L_4)	Magnetics 77,869, 0.207 Ω
Inductor core, DC resistance for TICC (V_{PV} = 300 V) L_2 (L_3)	Magnetics 77,617, 0.196 Ω

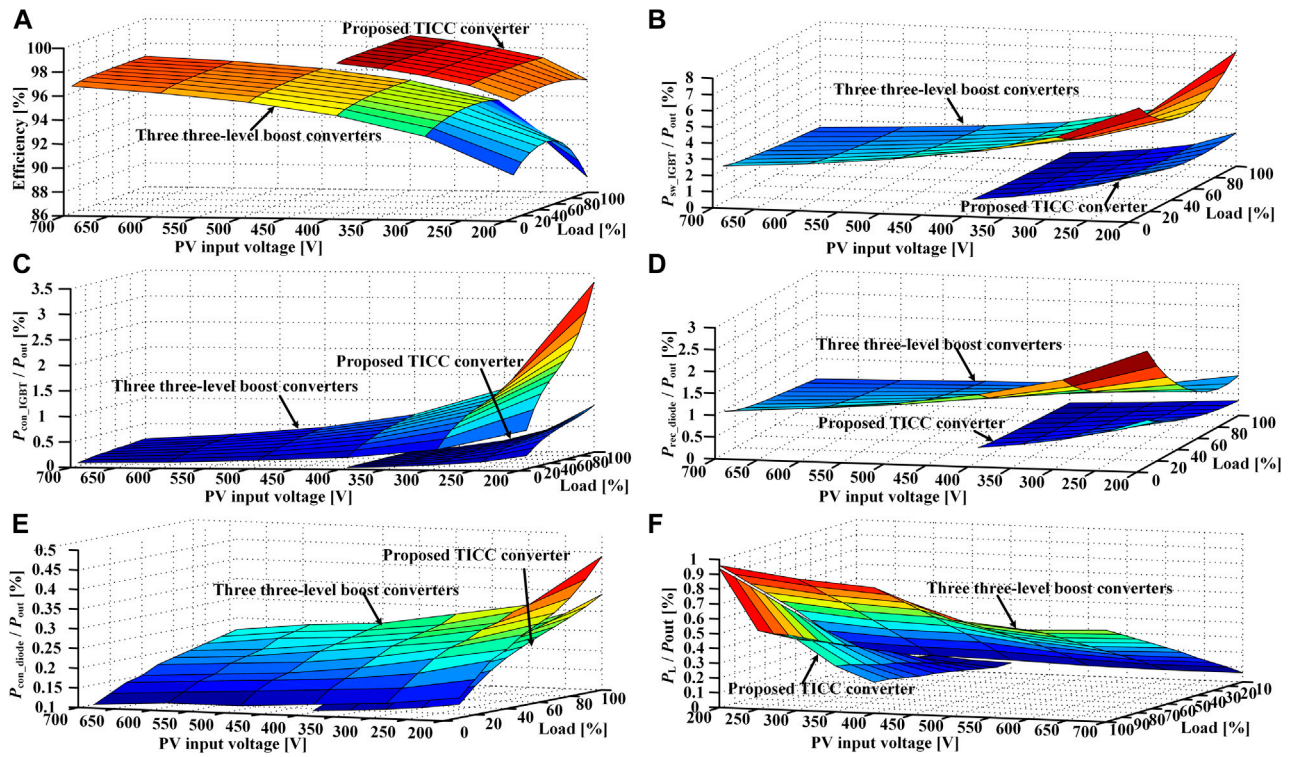

FIGURE 14 | (A) Efficiency of the proposed TICC converter and three three-level boost converters, **(B)** fraction of power dissipated by IGBT's switching among two converters, **(C)** fraction of power dissipated by IGBT's conduction among two converters, **(D)** fraction of power dissipated by the diode's reverse recovery among two converters, **(E)** fraction of power dissipated by the diode's conducting among two converters, and **(F)** fraction of power dissipated on the inductor among two converters.

i_{peak} that passes through the diode. $V_F(i_{peak})$ is the forward voltage of the diode, which is the function of the forward current i_{peak}.

The inductors can be selected by the software from Magnetics (Kjaer, 2004); then the corresponding losses of the inductor can be expressed as

$$P_{L\_loss} = P_{core} + P_{copper} \tag{37}$$

where P_{core} and P_{copper} are the core loss and copper loss of the inductor, respectively, which can be calculated as

$$\begin{cases} P_{core} = f\left(I_{dc}, I_{ripple}, f_{sw}, L\right) \\ P_{copper} = I_{dc}^2 R_{dc} \end{cases} \tag{38}$$

where I_{dc} is the effective dc current flowing through the inductor, which approximately equals i_{peak}. I_{ripple} is the high-frequency

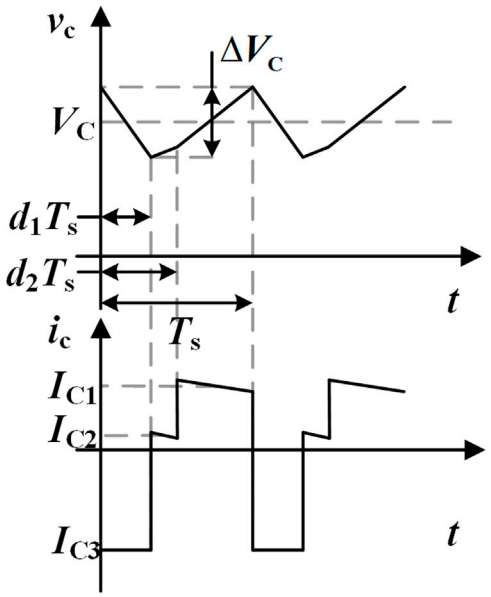

FIGURE 15 | Central capacitor voltage and current in the TICC converter.

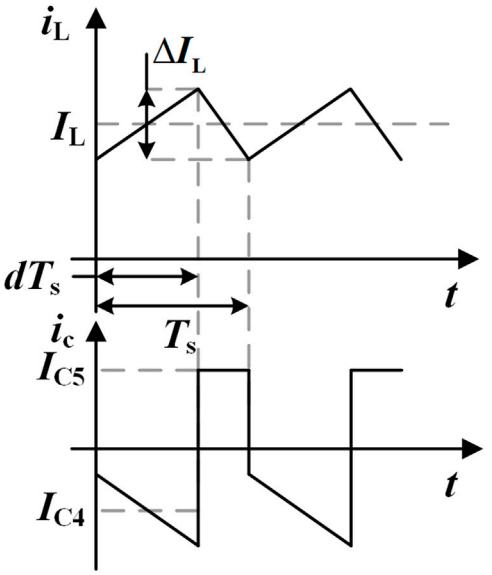

FIGURE 16 | Currents of the inductor and input capacitor in the TICC converter.

ripple current, which is usually 30% of the dc current passing through the inductor. R_{dc} is the dc resistance of the inductor, and L is the inductance that must be maintained by the inductor, which can be calculated as

$$L = \frac{V_{in} \cdot d}{I_{ripple} \cdot f_{sw}} \tag{39}$$

where V_{in} is the input charging voltage of the inductor and d is the duty cycle of the charging state of the inductor.

Figure 14A shows the evaluated efficiency of these two converters under different load conditions (10%–100%) as the input voltage varies, indicating a higher efficiency of the proposed TICC converter over the three-level boost converter when their input PV voltages are equal. Here, the capacitor losses are neglected since the equivalent series resistance of the capacitor is usually quite small, for example, dozens of milliohms. With the increment of input PV voltage, the efficiency of the three-level boost converter can be improved. However, it will bring more mismatch power losses between PV modules. **Figures 14B–E** shows the fractions of power dissipated by the IGBT's switching, the IGBT's conduction, the diode's reverse recovery, and the diode's conduction operations, respectively. It can be seen that the proposed TICC converter reduces the IGBT switching and conduction losses and the diode's reverse-recovery losses effectively, compared with three three-level boost converters. In addition, although one more inductor is used, the proposed converter has lower inductor losses as shown in **Figure 14F** because the currents flowing through the inductors of the TICC converter are low, which reduces its copper loss.

4.4 Passive Component Design

The inductor can be calculated by

$$L = \frac{V_{in} \cdot d}{I_{ripple} \cdot f_{sw}} \tag{40}$$

where V_{in} is the input charging voltage of the inductor and d is the duty cycle of the charging state of the inductor. I_{ripple} is the high-frequency ripple current, which is usually 30% of the dc current I_{dc} passing through the inductor. I_{dc} approximately equals i_{peak}, which is the peak current stress of transistors.

Then the voltage ripple factor K_C, which is important when we select the capacitor, can be calculated as

$$K_C = \frac{\Delta V_C}{V_C} \tag{41}$$

where V_C is the capacitor voltage and ΔV_C is the voltage ripple, which can be calculated as

$$\Delta V_C = \frac{1}{C} \int i_C dt \tag{42}$$

There are three states of the central capacitor C_2 and C_5, as shown in **Figure 15**. In the first state ($0 \sim d_1T_s$), the capacitor current I_{C1} equals the dc bus current I_{bus}, which can be expressed as

$$I_{C1} = -I_{bus} \tag{43}$$

and in the second state ($d_1T_s \sim d_2T_s$), the capacitor current I_{C2} can be calculated as

$$I_{C2} = I_{L1} - I_{bus} \tag{44}$$

where I_{L1} is the current of inductor L_1. In the third state ($d_2T_s \sim T_s$), the capacitor current I_{C3} can be calculated as

TABLE 6 | Parameters of the simulation model.

Parameter	Value
PV MPP voltage (1,000 W/m^2,20°C)	250 V
PV MPP current (1,000 W/m^2,20°C)	6.57 A
Rated dc bus voltage	1,200 V
Grid voltage (line to neutral)	220 V_{RMS}
Switching frequency	20 kHz
Dc inductor/grid side inductor	3 mH/5 mH
PV capacitor/central capacitor	430 uF/550 uF

$$I_{C3} = I_{L1} + I_{L2} - I_{bus} \tag{45}$$

where I_{L2} is the current of inductor L_2. The inductor currents I_{L1} and I_{L2} approximately equal I_{peak}, which can be calculated by **Eq. 34**. Then the voltage ripple on the central capacitor can be calculated as

$$\Delta V_C = \frac{I_{C1} D_1 T_S}{C} \tag{46}$$

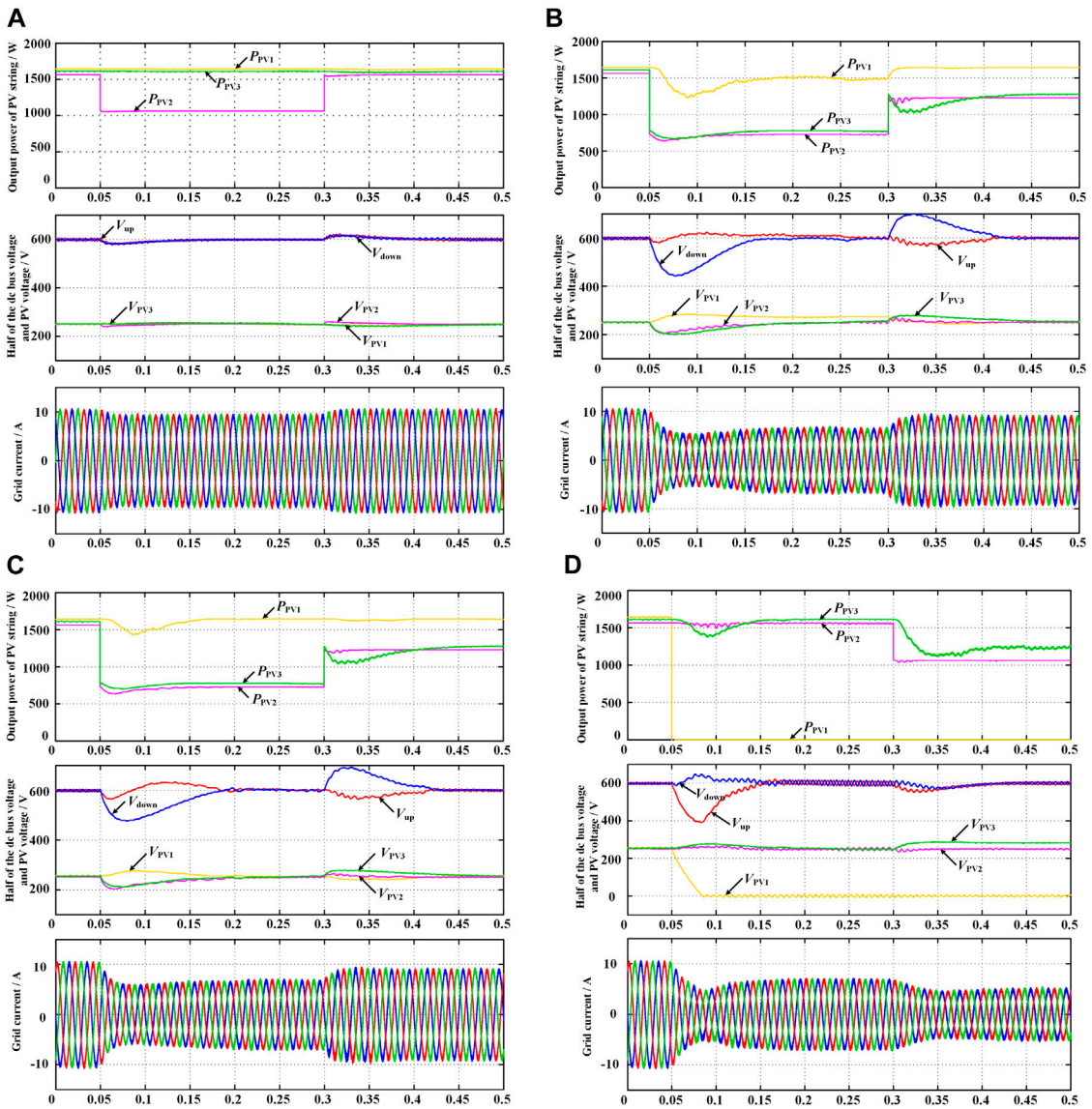

FIGURE 17 | (A) Simulated waveforms when the PV2 irradiance declines from 950 W/m^2 to 650 W/m^2 at 0.05 s and recovers to 950 W/m^2 at 0.3 s, **(B)** simulated waveforms when the irradiation levels of PV2 and PV3 reduce from 950 W/m^2 to 450 W/m^2 and from 980 W/m^2 to 480 W/m^2, respectively, at 0.05 s and recover to 750 W/m^2 and 780 W/m^2, respectively, at 0.3 s, **(C)** simulated waveforms when the variation of the irradiation level of PV2 and PV3 is the same as that in the previous case, but the inverter is involved to balance the dc-link voltage, and **(D)** simulated waveforms when the irradiation level of PV1 reduces to 0 W/m^2 at 0.05 s and the irradiation level of PV2 reduces by 300 W/m^2 at 0.3 s.

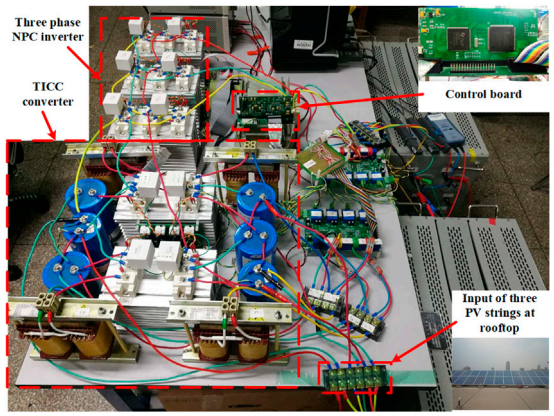

FIGURE 18 | Experimental testbed.

TABLE 7 | Parameters of the experimental prototype.

Parameter	Value
PV MPP voltage (800 V/m^2, 20°C)	180 V
PV MPP current (800 V/m^2, 20°C)	4.6 A
PV capacitor/central capacitor	EACO 430 uF/550 uF, 800 V
TICC/inversion stage switch	FF100R12RT4, 100 A, 1,200 V
DC inductor/grid side inductor	3 mH/5 mH
Rated dc bus voltage	630 V
Grid voltage (line to neutral)	220 V_{RMS}, 50 Hz
Switching frequency	20 kHz
Control chip	DSP + FPGA

where D_1 and D_2 are the conduction duty cycles of switches S_1 and S_2, respectively. Thus, the central capacitor can be calculated as

$$C = \frac{I_{bus} D_1 T_S}{V_C \cdot K_C} \tag{47}$$

and there are two states of the input capacitor, as shown in **Figure 16**. In the first state ($0 \sim dT_s$), the capacitor current can be calculated as

$$I_{C4} = I_{PV} - I_{bus} - I_L \tag{48}$$

In the second state ($dT_s \sim T_s$), the capacitor current can be calculated as

$$I_{C5} = I_{PV} - I_{bus} \tag{49}$$

Then the voltage ripple on the input capacitor can be calculated as

$$\Delta V_C = \frac{I_{C5}(1-D)T_S}{C} \tag{50}$$

Thus, the input capacitor can be calculated as

$$C = \frac{(I_{PV} - I_{bus})(1-D)T_S}{V_C \cdot K_C} \tag{51}$$

5 SIMULATIONS AND EXPERIMENTAL RESULTS

The Matlab simulation model has been built to verify the performance of the proposed three-input central capacitor converter, whose corresponding circuit parameters are listed in **Table 6**. To simulate the irradiation variations on the grid-tied PV system, the irradiation level of PV2 varies from 950 W/m^2 to 650 W/m^2 at the time of 0.05 s and recovers to 950 W/m^2 at the time of 0.3 s, while the irradiation levels of PV1 and PV3 keep unchanged at 1,000 W/m^2 and 980 W/m^2. **Figure 17A** shows the simulation waveforms. When the irradiation level of PV source PV2 suffers a disturbance, its output power varies with the change of the irradiation level. It can be seen that half of the dc-link voltage is regulated steadily to 600 V and the grid currents are not deteriorated.

Another scenario is defined to evaluate the performance of the proposed converter under non-MPPT control by disabling the dc-link voltage regulation capability of the rear-end inverter. The irradiation levels of PV2 and PV3 reduce from 950 W/m^2 to 450 W/m^2 and from 980 W/m^2 to 480 W/m^2, respectively, at the time of 0.05 s and recover to 750 W/m^2 and 780 W/m^2, respectively, at the time of 0.3 s, while the irradiation level of PV1 keeps unchanged at 1,000 W/m^2. At the time of 0.05 s, the output power of PV1 is higher than the sum of the output powers of PV2 and PV3, which enables the non-MPPT control of PV1. As a result, the output voltage of PV1 is controlled to rise up in order to reduce its output power. It can be seen that the output power of PV1 is then kept to a constant value, which equals the sum of the output powers of PV2 and PV3. Therefore, the three-level dc-bus voltage can still keep balanced as shown in **Figure 17B**. Moreover, at the time of 0.3 s, the sum of the output powers of PV2 and PV3 is larger than the maximum output power of PV1 and then PV1 recovers to MPPT control. The output power of PV1 recovers to the initial level. Thus, the proposed converter can balance the dc-link voltage independently.

The next case is to verify the performance of the coordinated control between the proposed converter and the rear-end three-level inverter when the unbalanced power ratio is lower than the power balance limit, where the variation of the irradiation level of three PV sources is the same as that in the previous case, but the inverter is able to balance the dc-link voltage. Although the output power of PV1 is higher than the sum of the output powers of PV2 and PV3 at the time of 0.05 s, the three PV sources can still work at their MPPs because the inverter can help balance the dc-link voltage, as shown in **Figure 17C**. Then at the time of 0.3 s, the output power of PV2 and PV3 increases with the variation of the irradiation level.

Finally, to show the performance of the proposed converter when any PV source suffers a permanent damage, the irradiation level of PV1 reduces to 0 W/m^2 at the time of 0.05 s and the irradiation level of PV2 reduces from 950 W/m^2 to 650 W/m^2 at the time of 0.3 s, while the irradiation level of PV3 keeps

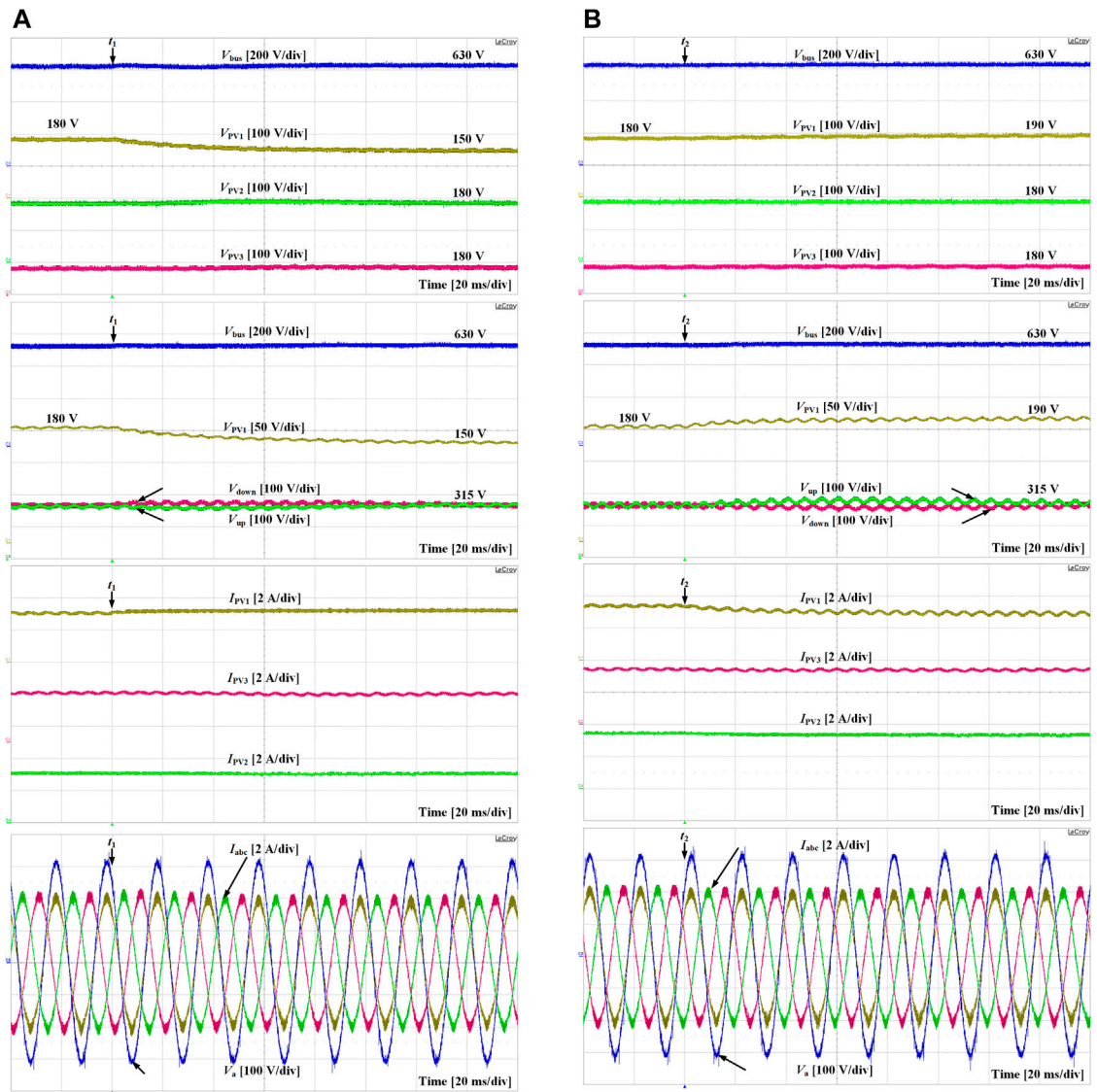

FIGURE 19 | Experimental waveforms when **(A)** PV1 reference declines from 180 V to 150 V at instant t_1 and **(B)** PV1 reference rises up from 180 V to 190 V at instant t_2.

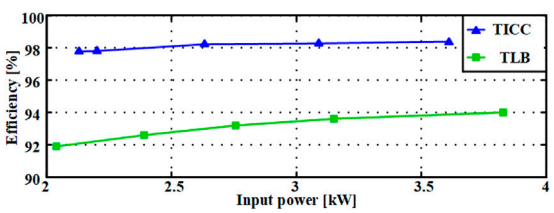

FIGURE 20 | Measured efficiencies of the three-level boost converter and TICC converter under the same input voltage.

unchanged at 980 W/m^2. It can be seen from **Figure 17D** that PV2 and PV3 can still work at their MPPs before the time of 0.3 s, where the unbalanced power ratio is within the power balance limit. Here, the power balance limit is defined as 0.08. At the time of 0.3 s, a further decrease of the irradiation level of PV2 causes that the unbalanced power ratio exceeds the power balance limit. Therefore, the non-MPPT control of PV3 is enabled to track the given power reference and help balance the dc-link voltage. As shown in **Figure 17D**, the non-MPPT control and the VBC in the ac side can coordinate well to balance the dc-link voltage.

To further evaluate the performance of the proposed converter, an experimental prototype was built as shown in **Figure 18**, whose component values and circuit parameters are listed in **Table 7**. All control algorithms are programmed in a DSP TMS320F28335 from TI and an FPGA XC3S500E. Three independent PV strings are connected in front. Since the irradiance level cannot be flexibly controlled for the installed rooftop PV strings, this experimental prototype can only examine

the steady-state operation and the transient operation where PV voltage references suffer sudden changes.

Figure 19A shows the experimental results when the PV voltage reference suffers a sudden decline to examine the PV voltage tracking and dc-link voltage balancing capability of the proposed converter. The voltage reference of PV1 is reduced from 180 V to 150 V at instant t_1. It can be seen that the dc-link voltage can keep balanced automatically, and the grid voltage and grid currents are in phase. **Figure 19B** shows the experimental waveforms when the PV2 voltage reference rises up from 180 V to 190 V at instant t_2. After a transient process, half of the dc-link voltage can be regulated to the steady-state value of 315 V, guaranteeing the normal operation of the rear-end inverter.

To analyze the efficiency performance of the proposed converter, the proposed TICC converter is compared with three-level boost converters shown in **Figure 20**. Because it is difficult to evaluate the mismatch loss at different input voltages, they are compared under the same input and output conditions. The input PV strings are replaced with the dc sources to adjust the output power flexibly. Then, with the input voltage of 250 V and the output dc-link voltage of 1,000 V, the efficiencies of the proposed TICC converter and three-level boost converters under different input power conditions are measured using a power analyzer, which samples V_{PV1}, I_{PV1}, V_{PV2}, I_{PV2}, V_{PV3}, I_{PV3}, V_{up}, I_{dc+},V_{down}, *and* I_{dc-}. Then the efficiency can be calculated by

$$\eta = \frac{\boldsymbol{V_{PV1}I_{PV1}} + \boldsymbol{V_{PV2}I_{PV2}} + \boldsymbol{V_{PV3}I_{PV3}}}{\boldsymbol{V_{up}I_{dc+}} + \boldsymbol{V_{down}I_{dc-}}} \tag{52}$$

where V_{PVX} and I_{PVX} ($X = 1$–3) are the output voltage and current of PV sources, respectively, V_{up} and V_{down} are the upper and lower half parts of the dc bus voltage, respectively, and $I_{\mathrm{dc+}}$ and $I_{\mathrm{dc-}}$ are the dc bus currents. It can be seen from **Figure 20** that the proposed converter can provide a higher efficiency under the same input and output voltage.

6 CONCLUSION

This paper proposes a three-input central capacitor converter for a high-voltage PV system, which can output a balanced three-level dc-link voltage and track the MPPs of three PV sources independently. The three-level structure enables it to be connected to the three-level inverter directly and reduces the voltage stress on semiconductors. Compared with the widely used boost and three-level boost converters, the proposed converter can reduce the mismatch losses and therefore has better energy harnessing ability due to the MPPT control of three split PV sources. Then, its operational principles and scalability are presented in detail. In addition, its corresponding control strategy is proposed to balance the three-level dc-link voltage when there is a large difference among the output power of three PV sources. A comparative study is carried out to demonstrate the advantages of the proposed converter, indicating its low semiconductor voltage/current stress and high efficiency. The performance of the three-input central capacitor converter along with its control strategy was verified by both simulation and experimental results.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/Supplementary Material; further inquiries can be directed to the corresponding author.

AUTHOR CONTRIBUTIONS

XM and JL came up with the idea. XM is responible for carrying out the simulation and experiment verifications. GW and JF help check the simulation and experiment results.

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Conflict of Interest: Author JL was employed by State Grid Weihai Power Supply Company. GW was employed by State Grid Yantai Power Supply Company.

The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.