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An Improved Dual-Loop Feedforward Control Method for the Enhancing Stability of Grid-Connected PV and Energy Storage System Under Weak Grids

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Although the stability of the grid-connected photovoltaics (PV) and energy storage systems under weak grids has been widely researched, the classical improvement methods focus more on suppressing the harmonics introduced by the phase-locked loop (PLL). Furthermore, the current distortion caused by the DC voltage loop is difficult to be eliminated. In this study, based on the hybrid energy storage system of battery-supercapacitor, a dual-loop compensation method is proposed. First, the small-signal model and output impedance matrix are built in d-q axis. Second, for different disturbance loops, a DC voltage loop disturbance compensation method based on power feedforward is proposed to suppress the harmonics caused by the DC voltage controller (DVC). In addition, a voltage feedforward PLL disturbance compensation method is proposed, which can reduce the PLL perturbations and revise the output impedance to improve system stability. Finally, the output impedance frequency characteristic analysis and the hardware-in-the-loop (HIL) simulation results show that the proposed control method can effectively improve the stability of the system under weak grids.

Keywords: PV and energy storage system, weak power grids, grid-connected inverter, phase-locked loop, stability analysis

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1 INTRODUCTION

Renewable energy sources such as PV have the characteristics of intermittency and randomness. In order to ensure the stability of the microgrid system, certain capacity energy storage devices need to be configured in the microgrid system. The battery-supercapacitor (SC)–based hybrid energy storage system (HESS) has been proposed to mitigate the impact of dynamic power exchanges on the battery's lifespan (Jing et al., 2017). Aiming at the control of the PV and energy storage microgrid, (Akram et al., 2018), proposed an iterative search algorithm to improve the optimal size of the PV and energy storage systems in the microgrid. (Tricarico et al., 2020) made improvements on the microgrid topology. In (Xu and Cen, 2021), a coordinated control strategy was used to suppress the power fluctuations of grid-connected PV power generation systems. Due to the interaction between the inverter and grid impedance, will cause a decrease in system stability. Therefore, considering the

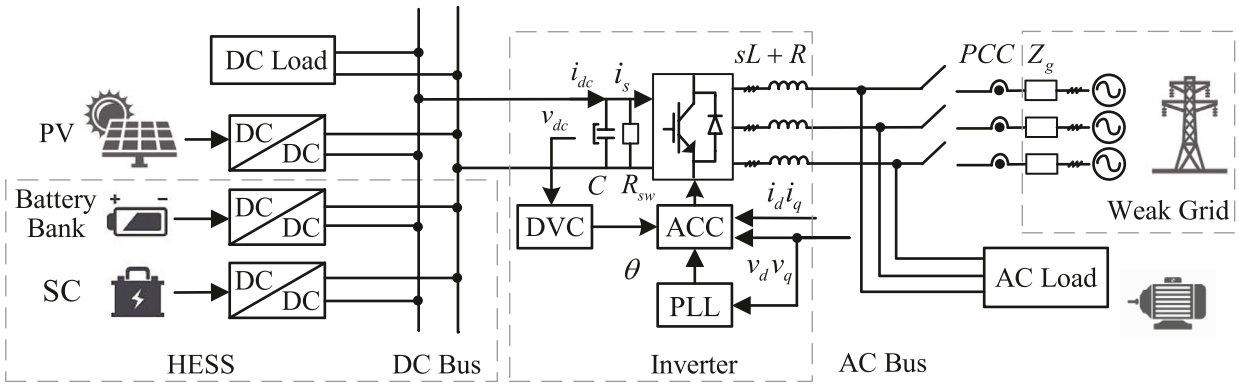

FIGURE 1 | Grid-connected PV and energy storage system.

weak grid conditions, the research on stable control of grid-connected inverters is particularly important.

The impedance analysis is widely used in the stability analysis of grid-connected inverters. (Sun, 2011) pointed out that if the ratio of the grid impedance to the inverter output impedance satisfies the Nyquist stability criterion, the system will remain stable. (Wen et al., 2014) analyzed the control of the voltage controller in the low-frequency range, the output impedance decreases as the voltage loop bandwidth increases, and the wider will be the frequency range of the negative impedance. In this regard, (Xu et al., 2017), proposed an adaptive control method, which adjusts the voltage feedforward signal through an adaptive criterion to improve the stability. (Lu et al., 2018) revealed that the dc-link voltage control may cause high-frequency oscillations in the inverter. (Yuan et al., 2017) pointed out that controller parameters of DVC affect the oscillation. In addition, (Harnefors et al., 2015), suggested not to select the bandwidths of DVC, unnecessarily large, to avoid oscillation. (Dong et al., 2014); (Wen et al., 2015a); (Wen et al., 2015b); (Bakhshizadeh et al., 2016); (Yang et al., 2019); (Nicolini et al., 2020) mainly analyzed the influence of the PLL on the stability of the inverter and pointed out that the PLL is one of the main factors that affect the stability of the system. The method of introducing a feedforward function was used by (Wang et al., 2010); (Xue et al., 2012); (Zhang et al., 2018) to improve stability.

To solve the influence of PLL on system stability, (Cespedes and Sun, 2014); (Yang et al., 2014); (Zhou et al., 2014); (Davari and Mohamed, 2016) made different attempts. In (Zhou et al., 2014), a small-signal model of the control system including the PLL was established. It was discussed that the gain of the PLL has a greater effect on the stability of the inverter, and a method is proposed to reduce the bandwidth of the PLL to solve this problem. (Yang et al., 2014) used virtual impedance to regulate the output impedance instead of adjusting the current loop gain to improve the inverter's harmonic suppression and stability robustness. The current control loop can be independently designed. (Wang et al., 2014) reviewed the control methods of VSCs and CSCs based on virtual impedance. (Cao et al., 2017) proposed an impedance matrix modeling method, which simplifies the stability judgment process. However, the impact of the DC side voltage fluctuation is ignored. For PV grid-connected systems, the DC side voltage will fluctuate under the influence of factors such as intensity of light. Therefore, it is necessary to take DC voltage fluctuations into consideration.

This study aims at the stability of weak grid-connected PV and energy storage systems. To meet the dynamic response requirements, a HESS is adopted. For the grid-connected inverter, the small-signal analysis and impedance method are used to analyze the stability of the system, including the influence of the PLL and the voltage loop controller. The main contributions are as follows:

1) Considering the State of Charge (SoC) of the battery, an adaptive bandwidth frequency low-pass filter (LPF) is proposed, smoothing the low-frequency power from the battery, ensuring DC bus voltage stability.
2) A DC voltage loop disturbance compensation control based on power feedforward is added to the DVC to reduce the perturbation signals caused by the controller parameters.
3) To eliminate the negative effects introduced by PLL, a disturbance compensation method based on voltage feedforward is proposed, which further improves the stability of grid connections.

The rest of this article is organized as follows. Section 3 establishes the impedance model of the grid-connected inverter. Section 4 discusses the proposed control method and analyzes the control effect. Section 5 builds a HIL platform to verify that the proposed method can reduce the frequency range of the negative impedance characteristics. The conclusion is given in Section 6.

2 GRID-CONNECTED PV AND ENERGY STORAGE SYSTEM UNDER WEAK GRIDS

Figure 1 is a weak grid-connected PV and energy system. PV and HESS are connected to the DC bus through DC/DC converters. Therefore, the DC bus voltage becomes a key indicator for stable

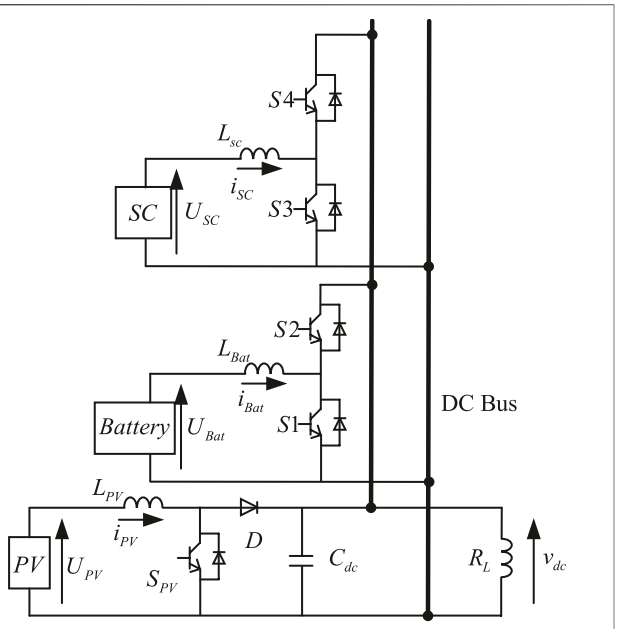

FIGURE 2 | DC microgrid structure.

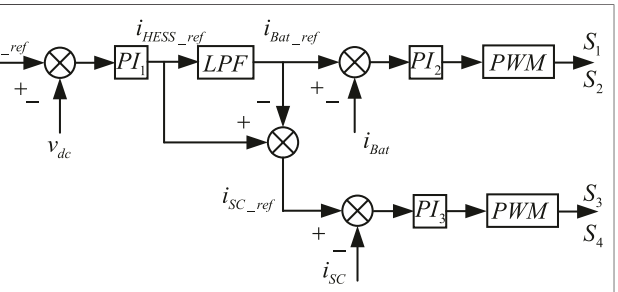

FIGURE 3 | Structure of voltage stabilization control.

operation. L is the filter inductance on the inverter side, and R is the parasitic resistance on the inductance. The grid impedance is represented by Z_g, which comprises an inductance L_g and a resistance R_g, and θ is the phase angle of the PLL. DC bus voltage and current are represented by v_{dc} and i_{dc}, respectively. The control system of the inverter comprises a DVC, an AC current controller (ACC), and PLL.

2.1 Structure Design of HESS

The PV array is connected to the DC microgrid through a boost converter, which adopts the MPPT control algorithm. The HESS uses a bidirectional DC/DC converter to connect to the DC microgrid. Due to the imbalance between power generation and load demand, the HESS is proposed to maintain the DC bus voltage v_{dc} stability.

In **Figure 2**, R_L represents the load of the DC bus, U_{PV}, i_{PV}, U_{Bat}, i_{Bat}, U_{SC}, and i_{SC} represent the voltage and output current of PV array, battery, and SC; L_{PV}, L_{Bat}, and L_{SC} are the filter inductance of the converter; C_{PV} is the filter capacitor; and S_1, S_2, S_3, S_4, and S_{PV} are the control switches.

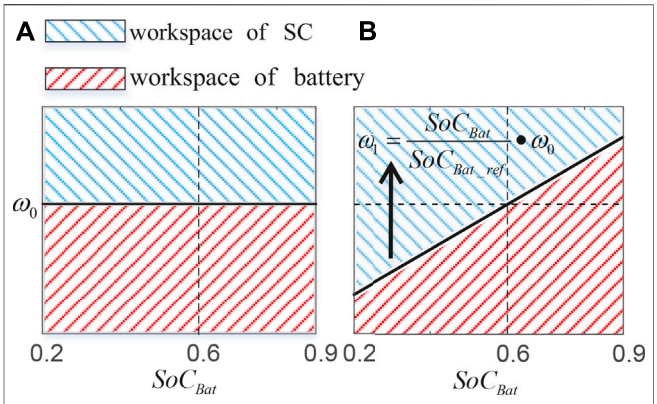

FIGURE 4 | (A) Traditional LPF power distribution diagram, **(B)** self-adaptive LPF power distribution diagram considering SoC_{Bat}.

2.2 Self-Adaptive LPF Considering SoC_{Bat}

The control block diagram of the voltage stabilization control strategy is shown in **Figure 3**. The basic idea of this control strategy is that the battery supports the low-frequency part of power changes and the SC supports the high-frequency part of power changes. Therefore, v_{dc} is compared with its reference value v_{dc_ref}, and the total current i_{HESS_ref} is provided by the PI controller. A low-pass filter (LPF) is used to divide the total current into a steady-state power component and a dynamic power component. The steady-state power component is used as the reference value i_{Bat_ref} for battery current control, and the dynamic power component is used as the reference value i_{SC_ref} for SC current control.

The smaller the bandwidth frequency of the LPF, the smoother the power borne by the battery after P_{HESS} passes through the LPF, and the more the power borne by the SC. Therefore, the power distribution effect of the LPF can be optimized by changing the size of bandwidth frequency.

On the basis of the traditional power distribution method, the SoC of the HESS is considered, and the bandwidth of the LPF is changed in real time according to its SoC value to realize the reasonable distribution of the power in HESS.

We set the improved self-adaptive bandwidth frequency ω_1 as follows:

$$\omega_1 = \frac{SoC_{Bat}}{SoC_{Bat\_ref}} \cdot \omega_0, \tag{1}$$

where $0.2 < SoC_{Bat} < 0.9$, ω_0 is the initial bandwidth frequency of the LPF, and SoC_{Bat_ref} is the optimal SoC of the battery, with a magnitude of 0.6.

In **Figure 4**, the power with a frequency lower than ω_1 is borne by the battery, and the power with a frequency higher than ω_1 is borne by the SC. **Figure 4A** shows the power distribution under the traditional LPF, where $\omega_1 = \omega_0$. **Figure 4B** shows that the larger SoC_{Bat} means larger ω_1, and the battery bears more range of power output. When the battery power is low, ω_1 decreases with SoC_{Bat}. SC takes on more range of power output so as to extend the working time of HESS and protect the battery.

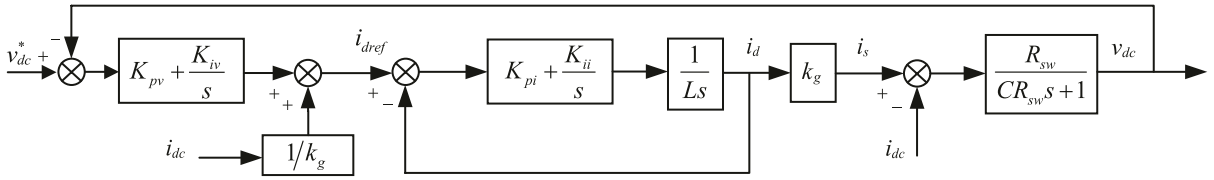

FIGURE 5 | Dual-loop control structure of the inverter.

With the self-adaptive LPF power distribution method, the new reference current i_{Bat_ref} and i_{SC_ref} are obtained. By sending these parameters to the PI controllers, we can get the bidirectional DC/DC control signals.

2.3 System Power Distribution

In the power distribution control strategy, the DC bus voltage is controlled by the PV and the HESS. P_{inv} is the power at the input of the inverter, and P_L is the power of DC load. P_{dc} represents the output power from the DC bus side. P_C is the power of the DC bus capacitor.

$$P_{dc} = P_{inv} + P_L. \tag{2}$$

$$P_C = P_{PV} + P_{HESS} - P_{dc}. \tag{3}$$

$$P_C = v_{dc} \cdot C_{dc}\frac{dv_{dc}}{dt}. \tag{4}$$

In order to stabilize the DC bus voltage, $dv_{dc}/d_t = 0$, which means $P_{HESS} = P_{DC} - P_{PV}$. The HESS is responsible for balancing the power between the DC bus side and the PV. The power of the HESS is allocated to the battery and the SC.

$$P_{HESS} = P_{Bat} + P_{SC}. \tag{5}$$

When the energy emitted by the system can satisfy (5), v_{dc} can remain stable.

3 DESIGN OF THE GRID-CONNECTED INVERTER

3.1 Design of Inverter Controllers

Figure 5 is the dual-loop control block diagram with a power feedforward. The proportional and integral gain of the PI controllers are k_{pv} and k_{pi}; k_{iv} and k_{ii}.

According to **Figure 1**, the mathematical model of the grid-connected inverter under the dq axis is as follows:

$$\begin{cases} C\dfrac{dv_{dc}}{dt} + \dfrac{v_{dc}}{R_{sw}} = i_{dc} - i_s \\ L\dfrac{di_d}{dt} - \omega L i_q + u_d = v_d \\ L\dfrac{di_q}{dt} + \omega L i_d + u_q = v_q \end{cases}, \tag{6}$$

where i_d and i_q are the dq-axis components of the grid-connected current at the PCC point, u_d and u_q are the dq-axis components

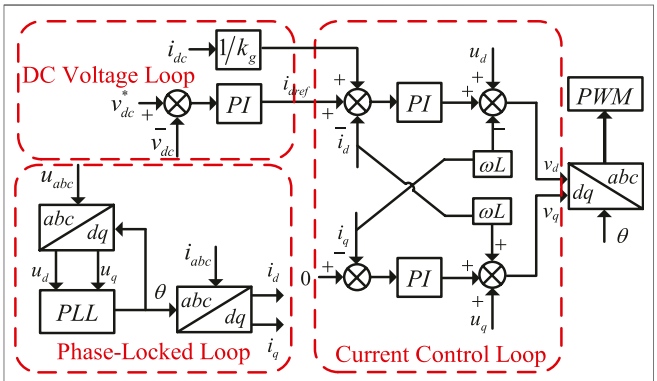

FIGURE 6 | Topology diagram of the control system.

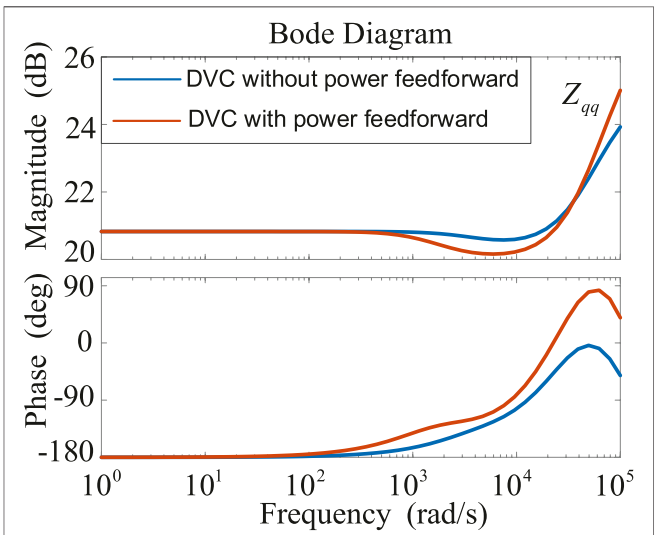

FIGURE 7 | Frequency characteristics of Z_{qq} with and without power feedforward.

of the PCC voltage, v_d and v_q are the inverter output voltage, and ω is the grid angle frequency. We usually set $v_q = 0$, $i_q = 0$. The topology diagram of the control system is shown in **Figure 6**. According to the power conservation at the input and output of the inverter, we can get

$$P_{inv} = i_{dc}v_{dc} = P_{out} = \frac{3v_d i_d}{2}. \tag{7}$$

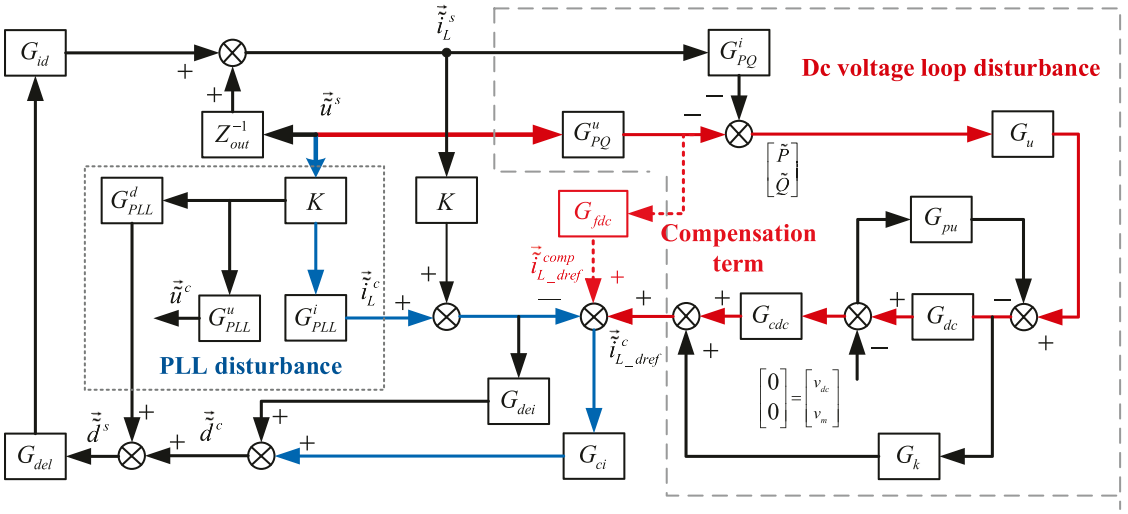

FIGURE 8 | Small signal model of the grid-connected inverter with PLL, ACC, and DVC.

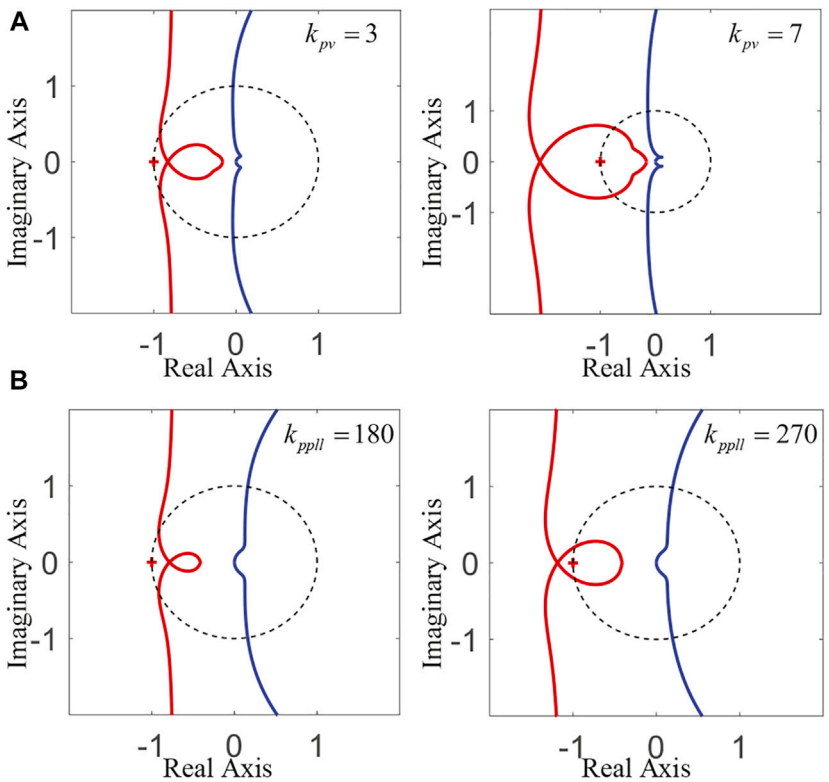

FIGURE 9 | (A) Impedance ratio curves of different k_{pv}; **(B)** impedance ratio curves of different k_{ppll}.

According to (7), i_d can be expressed as follows:

$$i_d = i_{dc} \cdot \frac{2v_{dc}}{3v_d}. \tag{8}$$

According to (8), the power feedforward item $1/k_g = 2v_{dc}/3v_d$ is introduced into the DVC.

The voltage loop control is to maintain the power balance and stabilize the DC side voltage (Harnefors et al., 2007). The

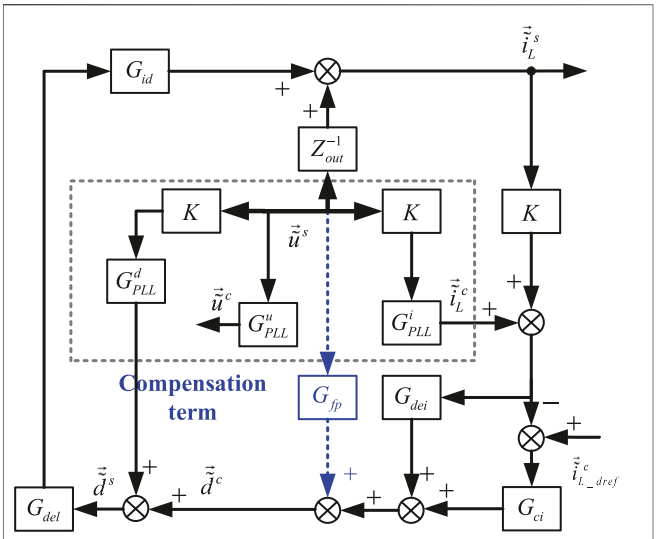

FIGURE 10 | Small-signal model of the grid-connected inverter.

introduction of a power feedforward link will reduce the signal of the outer loop voltage control command, thereby reducing the steady-state error of vdc, improving the response speed. **Figure 7** compares the frequency characteristic curve of Z_{qq} with and without power feedforward. It can be seen that the range of negative impedance characteristics of Z_{qq} is reduced with the addition of power feedforward, which indicates that the feedforward in DVC will improve the stability of the system.

3.2 Modeling of Output Impedance

The model of output impedance is built in d-q axis. In order to distinguish the variables of the system and the control loop, the superscript c represents the control loop variable, and the superscript s represents the system variable.

$$Z_{out} = \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix} = \begin{bmatrix} Ls + R & -\omega L \\ \omega L & Ls + R \end{bmatrix}. \tag{9}$$

K is the transfer function of the filter:

$$K = \begin{bmatrix} \dfrac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} & 0 \\ 0 & \dfrac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \end{bmatrix} \frac{1}{2}. \tag{10}$$

G_{del} is the time delay caused by the control loop and PWM modulation, which can be expressed as follows:

$$G_{del} = \begin{bmatrix} \dfrac{1 - 0.5T_{del}s}{1 + 0.5T_{del}s} & 0 \\ 0 & \dfrac{1 - 0.5T_{del}s}{1 + 0.5T_{del}s} \end{bmatrix}. \tag{11}$$

In the formula, $T_{del} = 1/f_{sw}$, f_{sw} is the switching frequency. G_{id} is the transfer function from duty ratio $\tilde{d}^s$ to inductor current $\tilde{i}_L$, and G_{id} is as (Wen et al., 2015a) follows:

$$G_{id} = \frac{-V_{dc}}{(Ls + R)^2 + (\omega L)^2} \begin{bmatrix} Ls + R & \omega L \\ -\omega L & Ls + R \end{bmatrix}. \tag{12}$$

As mentioned, the inverter uses PLL to obtain the phase information of the grid voltage. The angle output by the PLL will then be used for the d-q axis conversion inside the inverter, so the dynamic characteristics of the PLL will affect the output voltage, current, and duty ratio signals of the inverter, which in turn affects its output impedance (Bakhshizadeh et al., 2016) **Eq. 13** is the transfer function of PLL.

$$G_{PLL} = \frac{k_{ppll} + k_{ipll}/s}{s + U_d^s\left(k_{ppll} + k_{ipll}/s\right)}, \tag{13}$$

where, k_{ppll} and k_{ipll} are the PI controller parameters in the PLL.

When a small signal disturbance is applied to the output voltage, the relationship between the control loop voltage $\vec{u}^c$ and the system voltage $\vec{u}^s$ is as follows:

$$\begin{bmatrix} \tilde{u}_d^c \\ \tilde{u}_q^c \end{bmatrix} \approx \underbrace{\begin{bmatrix} 1 & U_q^s G_{PLL} \\ 0 & 1 - U_d^s G_{PLL} \end{bmatrix}}_{\mathbf{G}_{PLL}^u} \begin{bmatrix} \tilde{u}_d^s \\ \tilde{u}_q^s \end{bmatrix}. \tag{14}$$

In the same way, the duty ratio signal has the following relationship:

$$\begin{bmatrix} \tilde{d}_d^s \\ \tilde{d}_q^s \end{bmatrix} \approx \underbrace{\begin{bmatrix} 0 & -D_q^s G_{PLL} \\ 0 & D_d^s G_{PLL} \end{bmatrix}}_{\mathbf{G}_{PLL}^d} \begin{bmatrix} \tilde{u}_d^s \\ \tilde{u}_q^s \end{bmatrix} + \begin{bmatrix} \tilde{d}_d^c \\ \tilde{d}_q^c \end{bmatrix}. \tag{15}$$

For the control loop inductor current, there is the following relationship:

$$\begin{bmatrix} \tilde{i}_d^c \\ \tilde{i}_q^c \end{bmatrix} \approx \underbrace{\begin{bmatrix} 0 & I_q^s G_{PLL} \\ 0 & -I_d^s G_{PLL} \end{bmatrix}}_{\mathbf{G}_{PLL}^i} \begin{bmatrix} \tilde{u}_d^s \\ \tilde{u}_q^s \end{bmatrix} + \begin{bmatrix} \tilde{i}_d^s \\ \tilde{i}_q^s \end{bmatrix}. \tag{16}$$

G_{PLL}^u, G_{PLL}^d, and G_{PLL}^i respectively, represent the influence of PLL on system voltage, duty ratio, and current.

The ACC control loop in **Figure 8** is realized by converting the system output current $\tilde{i}_L^s$ into the current of the control loop $\tilde{i}_L^c$ under the action of the filter and PLL and then through G_{dei} and G_{ci}. G_{dei} is the feedforward decoupling link:

$$G_{dei} = \begin{bmatrix} 0 & -\dfrac{3\omega L}{V_{dc}} \\ \dfrac{3\omega L}{V_{dc}} & 0 \end{bmatrix}. \tag{17}$$

G_{ci} is the current controller:

$$G_{ci} = \begin{bmatrix} k_{pi} + k_{ii}\dfrac{1}{s} & 0 \\ 0 & k_{pi} + k_{ii}\dfrac{1}{s} \end{bmatrix} \tag{18}$$

Ignoring the power loss of switching devices, the active power balance equation is as follows:

$$v_{dc} i_s = \frac{3}{2}\left(u_d i_d + u_q i_q\right). \tag{19}$$

Add a small signal disturbance the $\vec{u}^s$ helps obtain the power equation:

$$P = P_0 + \tilde{P}. \tag{20}$$

$$Q = Q_0 + \tilde{Q}. \tag{21}$$

In the formula, P_0 and Q_0 and $\tilde{P}$ and $\tilde{Q}$ are

$$\begin{bmatrix} P_0 \\ Q_0 \end{bmatrix} = \frac{3}{2} \cdot \begin{bmatrix} U_d & U_q \\ U_q & -U_d \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix}. \tag{22}$$

$$\begin{bmatrix} \tilde{P} \\ \tilde{Q} \end{bmatrix} = \frac{3}{2} \cdot \begin{bmatrix} U_d & U_q \\ U_q & -U_d \end{bmatrix} \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \end{bmatrix} + \frac{3}{2} \cdot \begin{bmatrix} I_d & I_q \\ -I_q & I_d \end{bmatrix} \begin{bmatrix} \tilde{u}_d \\ \tilde{u}_q \end{bmatrix}. \tag{23}$$

The input current i_s of the inverter is

$$i_s = \frac{P}{v_{dc}}. \tag{24}$$

$$\tilde{i}_s = \frac{\tilde{P}}{V_{dc}} - \frac{P_0}{V_{dc}^2} \tilde{v}_{dc}. \tag{25}$$

Set $G_u = 1/V_{dc}$ and $G_{pu} = P_0/V_{dc}^2$. G_{dc} represents the loss of DC side capacitance and switching device:

$$G_{dc} = \begin{bmatrix} R_{sw}/\left(CR_{sw}s + 1\right) & 0 \\ 0 & R_{sw}/\left(CR_{sw}s + 1\right) \end{bmatrix}. \tag{26}$$

The transfer function matrix G_{PQ}^i and G_{PQ}^u is defined and used for power calculation as

$$G_{PQ}^i = \frac{3}{2} \cdot \begin{bmatrix} U_d & U_q \\ U_q & -U_d \end{bmatrix}. \tag{27}$$

$$G_{PQ}^u = \frac{3}{2} \cdot \begin{bmatrix} I_d & I_q \\ -I_q & I_d \end{bmatrix}. \tag{28}$$

To obtain the impedance model of the inverter, supposing that on the DC side of the inverter, besides the DC voltage v_{dc}, there is also a voltage corresponding to it, which is defined as v_m. G_{cdc} is the voltage controller:

$$G_{cdc} = \begin{bmatrix} k_{pv} + k_{iv}\dfrac{1}{s} & 0 \\ 0 & k_{pv} + k_{iv}\dfrac{1}{s} \end{bmatrix}. \tag{29}$$

Let the power feedforward term $G_k = \begin{bmatrix} 1/k_g \\ 0 \end{bmatrix}$.

Therefore, according to **Figure 8**, the output impedance matrix of the grid-connected inverter small-signal model can be derived as follows:

$$Z_{out\_dc} = (I + G_1 + G_3)\left(G_2 + G_4 + Z_{out}^{-1}\right)^{-1}. \tag{30}$$

$$G_1 = KG_{del}G_{id}\left(G_{ci} - G_{dei}\right). \tag{31}$$

$$G_2 = KG_{PLL}^i G_{del}G_{id}\left(G_{ci} - G_{dei}\right) + KG_{PLL}^d G_{del}G_{id}. \tag{32}$$

$$G_3 = G_{PQ}^i G_u G_{ci} G_{del} G_{id}\left(G_{dc}G_{cdc} + G_k\right) + G_{dc}G_{pu}. \tag{33}$$

$$G_4 = -G_{PQ}^u G_u G_{ci} G_{del} G_{id}\left(G_{dc}G_{cdc} + G_k\right). \tag{34}$$

4 DUAL-LOOP COMPENSATION CONTROL

4.1 The Influence of the Proportional Gain of DVC on the Stability of the System

Under weak grid conditions, the increase of k_{pv} will easily cause DC bus voltage fluctuations and grid-side current distortions.

In **Figure 9A**, the Nyquist curves of the impedance ratio are shown. As k_{pv} increases, the impedance ratio curve gradually includes the (−1, j0) point. It shows that k_{pv} will affect the stability of the system.

4.2 The Influence of the Proportional Gain of PLL on the Stability of the System

In a weak grid, the PLL and the grid impedance are coupled with each other, and the voltage at the PCC point is distorted. The increase in k_{ppll} also increases the output error and reduces the system stability.

In **Figure 9B**, it can be seen that as k_{ppll} increases, the impedance ratio curve gradually includes the (−1, j0) point. It shows that the increase in k_{ppll} will make the grid-connected system unstable.

Aiming at the problem that the grid impedance, the PLL, and the DC voltage loop are coupled with each other, corresponding control methods need to be adopted to suppress unstable factors.

4.3 Disturbance Compensation Method of DVC

The disturbance path of the DC voltage loop in **Figure 8** shows that $\vec{\tilde{u}}^s$ affects $\vec{\tilde{i}}_{L\_dref}$ through the DC voltage loop and then affects the system output current through the current loop. Adding a compensation matrix G_{fdc} at the output of the DVC can offset the disturbance signal. Based on the small-signal model, the compensation matrix can be obtained as follows:

Compensation signal:

$$G_{fdc} = G_u \cdot G_{dc} \cdot G_{cdc}. \tag{35}$$

$$\vec{\tilde{i}}_{L\_dref}^{comp} = -\left(\vec{\tilde{u}}^s \cdot G_{PQ}^u\right) G_{fdc}. \tag{36}$$

Since G_{PQ}^u only affects the d-axis, the control signal can be obtained as follows:

$$i_{dref}^{comp} = -\frac{3}{2} \cdot u_d \cdot i_d \cdot G_{fdc}. \tag{37}$$

Disturbance Compensation Method of PLL

Figure 10 shows the disturbance path of the PLL, where the voltage at the PCC point passes through the transfer matrix G_{PLL}^i and then affects the output voltage command through the current loop. Therefore, a compensation matrix G_{fp} can be added at the ACC to offset the disturbance signal.

According to **Figure 10**, let the compensation term G_{fp} be

$$G_{fp} = K \cdot G_{PLL}^i \cdot G_{ci}. \tag{38}$$

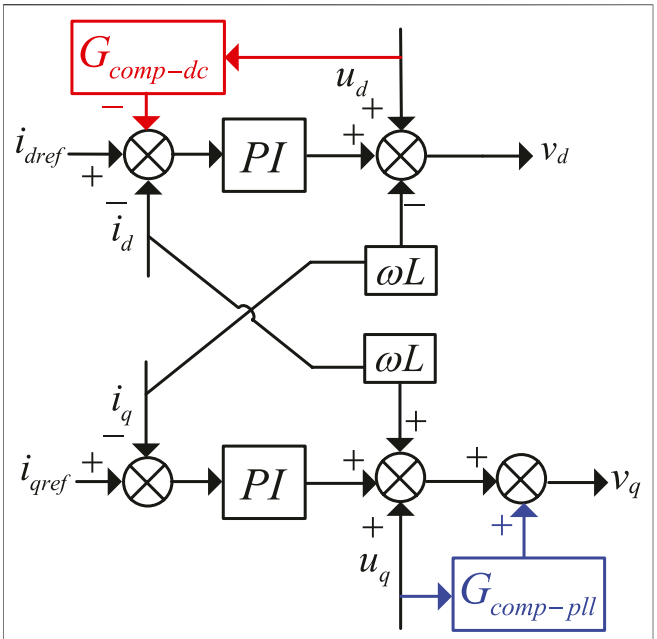

FIGURE 11 | Diagram of the current loop control system with compensation terms.

Due to the control voltage being $\vec{u}^c$, therefore according to the relationship between the control loop voltage $\vec{u}^c$ and the system voltage $\vec{u}^s$, the actual feedforward term can be obtained:

$$G_{fp}^{*} = K \cdot G_{IREF} \cdot G_P \cdot G_{ci}, \tag{39}$$

where

$$G_{IREF} = \begin{bmatrix} 0 & i_{qref} \\ 0 & -i_{dref} \end{bmatrix}. \tag{40}$$

$$G_P = \frac{\left(k_{ppll} + k_{ipll}/s\right)}{s}. \tag{41}$$

Since G_{PLL}^{i} only affects the q-axis current, the improved current control equation of the inverter can be expressed as follows:

$$\begin{cases} v_d = \left(k_p + \dfrac{k_i}{s}\right)\left(i_{dref} + i_{dref}^{comp} - i_d\right) - \omega L i_q + u_d \\ v_q = \left(k_p + \dfrac{k_i}{s}\right)\left(i_{qref} - i_q\right) + \omega L i_d + u_q + u_q \cdot K \cdot G_{fpq} \end{cases}. \tag{42}$$

The adjustment gain ξ is used to adjust the magnitude of the compensation signal, and G_{fpq} can be expressed as follows:

$$G_{fpq} = \frac{-i_{dref} \cdot \left(k_{ppll} + k_{ipll}/s\right) \cdot G_{ci} \cdot \xi}{s}. \tag{43}$$

Figure 11 of the current loop control system with compensation terms is shown in, where $G_{comp-dc} = 3/2 \cdot i_d \cdot G_{fdc}$, $G_{comp-pll} = K \cdot G_{fpq}$.

TABLE 1 | Grid-Connected system parameters.

Parameter	Symbol	Value
Filter inductance	L	19mH
Filter capacitance	C	0V
Filter impedance	R_{sw}	100Ω
DC voltage	v_{dc}	600V
D-axis grid voltage	v_d	200V
Q-axis grid voltage	v_q	0V
D-axis I current reference	i_{dref}	−20A
Q-axis current reference	i_{qref}	0A

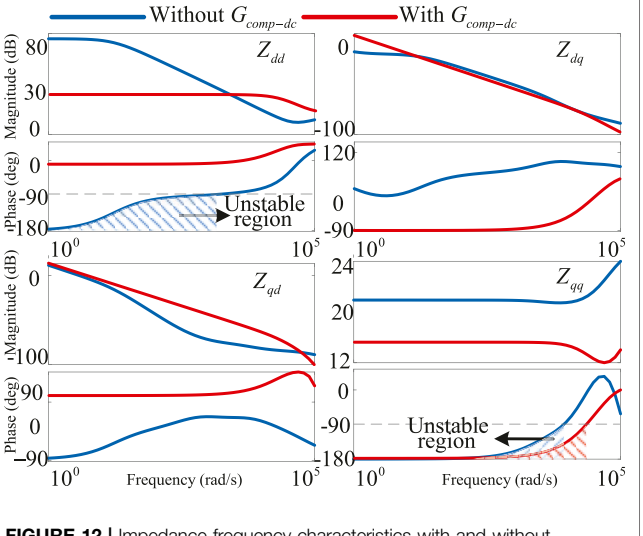

FIGURE 12 | Impedance frequency characteristics with and without $G_{comp-dc}$.

4.5 Analysis of Output Impedance

This section uses the data in **Table 1** to analyze the frequency characteristics of the inverter output impedance based on the previous deduction.

Comparison of simulation results of impedance frequency characteristics with and without $G_{comp-dc}$ is shown in **Figure 12**.

It can be seen from the figure that when the PLL is acting, the output angle of the PLL is affected by the q-axis voltage, and Z_{qq} characteristic is negative. The DVC and ACC use the angle to transform the coordinates and then introduce the negative influence of PLL to the d-axis. Z_{dd} presents a negative characteristic, and its amplitude is related to the output power of the inverter.

After adding $G_{comp-dc}$, Z_{dd} presents the frequency characteristic of positive impedance, which shows that the voltage loop compensation strategy proposed in this study effectively eliminates DVC's negative effects on the d-axis. Z_{qq} still presents negative impedance characteristics.

Figure 13 shows the impedance frequency characteristics with and without $G_{comp-pll}$, and after adding the PLL disturbance compensation, Z_{qq} presents the positive characteristic, and the

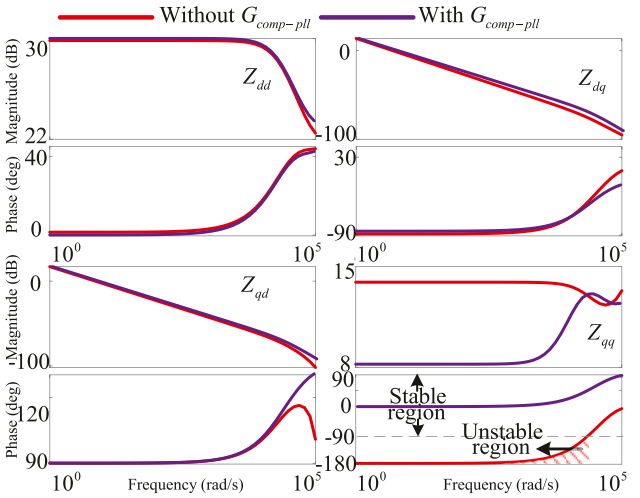

FIGURE 13 | Impedance frequency characteristics with and without $G_{comp-pll}$.

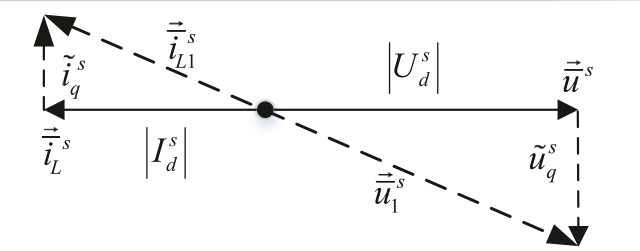

FIGURE 14 | Phasor diagram of the inverter when perturbation happens in q channel.

control method effectively eliminates the negative influence of PLL on the q-axis and improves the stability of the system.

The negative influence of PLL on the q-axis makes Z_{qq} exhibit negative characteristics. As the bandwidth of PLL increases, the range of frequency characteristics of negative impedance on Z_{qq} becomes larger, while the bandwidth of PLL has little effect on the amplitude of Z_{qq}. Its amplitude is related to the output power of the inverter.

As shown in **Figure 14**, the inverter current vector is synchronized with the grid voltage vector. Assuming that the inverter only delivers active power to the grid, when the disturbance occurs on the q-axis, the voltage vector will transition from the original equilibrium state $\vec{u}^{\,s}$ to the new equilibrium state $\vec{u}^{\,s}_{1}$. Similarly, the inverter current vector will be synchronized with the grid voltage vector and transition from the original equilibrium state $\vec{i}^{\,s}_{L}$ to the new equilibrium state $\vec{i}^{\,s}_{L1}$. In the low-frequency band, the calculation formula of Z_{qq} is as follows:

$$Z_{qq} = -\frac{\left|\tilde{v}^{s}_{q}\right|}{\left|\tilde{i}^{s}_{q}\right|} = -\frac{\left|V^{s}_{d}\right|}{\left|I^{s}_{d}\right|}. \tag{44}$$

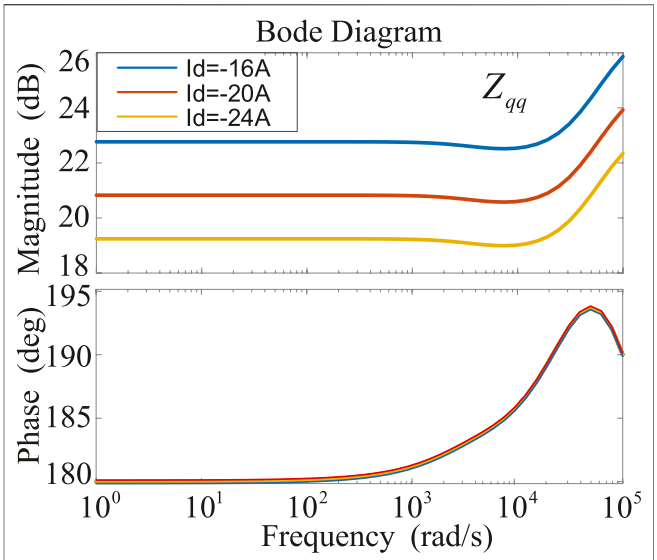

FIGURE 15 | Frequency characteristics of Z_{qq} under different grid-connected power.

The amplitude of grid voltage remains unchanged, and as the grid-connected power becomes larger, the amplitude of Z_{qq} becomes smaller. When the grid-connected power changes, the frequency characteristic curve of Z_{qq} is shown in **Figure 15**.

In **Figure 15**, different grid-connected power has no effect on the phase angle of Z_{qq}, and as the grid-connected power becomes larger, the amplitude of Z_{qq} becomes smaller.

In **Figure 13**, the addition of the compensation term not only eliminates the negative impedance characteristic of Z_{qq} but also reduces the amplitude of Z_{qq} in the low-frequency band and increases the output power of the inverter.

5 EXPERIMENTS

In order to verify the validity of the proposed control strategy, a HIL simulation platform was built in the OPAL-RT real-time simulation system which comprises an external controller and simulation computer. **Figure 16** is the OPAL-RT HIL system structure diagram. The host computer (Host PC) is used to build the system model and download it to the target computer (OP5600) through the TPC/IP channel; the target computer uploads information to the Host PC to monitor the operation of the model in real time. The grid-connected inverter controller adopts the TMS320F28335 digital signal processor (DSP). The DSP controller is responsible for collecting model output signals, performing real-time calculations, and generating PWM signals to send to the I/O board of the target machine to control the inverter.

When the output power of the PV array fluctuates:

Figure 17 shows the control experiment results of the PV and energy storage system under case 1. P_{dc} = 4 kW. By changing light intensity, in the first 2s, $P_{PV} > P_{dc}$, the battery is charged

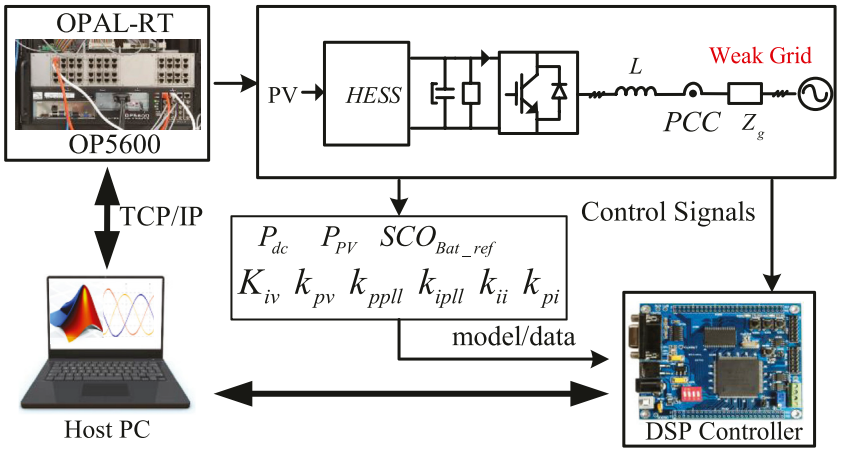

FIGURE 16 | HIL experiment topology.

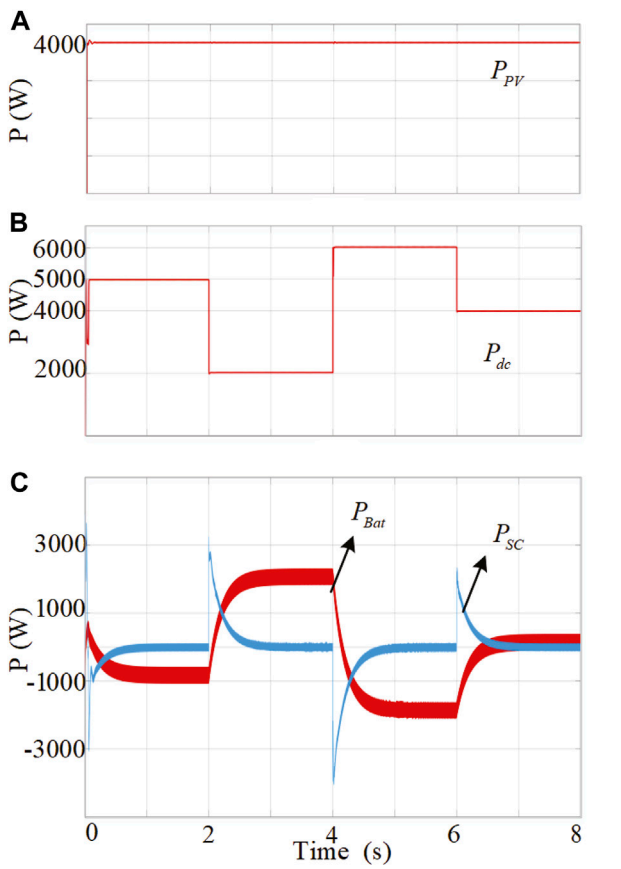

FIGURE 17 | (A) DC bus output power P_{dc}; **(B)** PV array output power P_{PV}; **(C)** HESS output power.

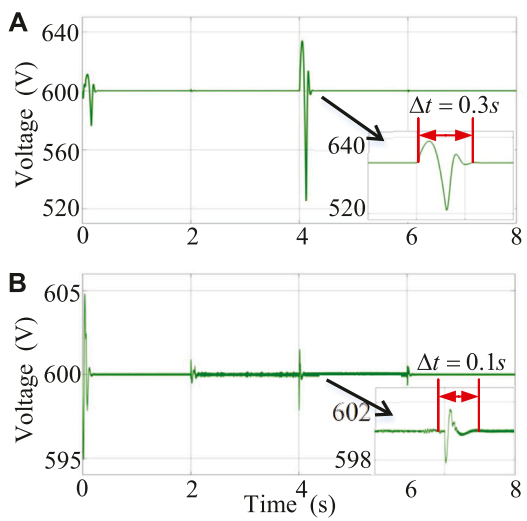

FIGURE 18 | (A) v_{dc} of the system without SC in case 1; **(B)** v_{dc} of HESS in case 1.

smoothly. At 2s, P_{dc} reduces to 2kW, $P_{PV} < P_{dc}$, SC discharges quickly to compensate for the power fluctuation of the system, and the battery discharges smoothly. At 4s, P_{PV} increases to 6kW, SC absorbs the power impact, and the battery is charged smoothly. During 6–8s, $P_{PV} = P_{dc}$, HESS works steadily.

Figure 18 compares the waveforms of the vdc in different energy storage systems versus P_{PV} in case 1. It can be seen that v_{dc} has different degrees of fluctuation and is finally stabilized at 600 V. At 4 s, the fluctuation is the most obvious. The system without SC is stable after 0.3 s with larger fluctuation amplitude; HESS is stable after 0.1 s, and the fluctuation amplitude is smaller. It proves that when P_{PV} fluctuates, the HESS has faster dynamic response performance and higher stability than battery energy storage systems due to introduction of supercapacitors with higher power density.

When the output power of the DC bus fluctuates:

Figure 19 shows the control experiment results of the PV and energy storage system in case 2. At first $P_{PV} < P_{dc}$, the

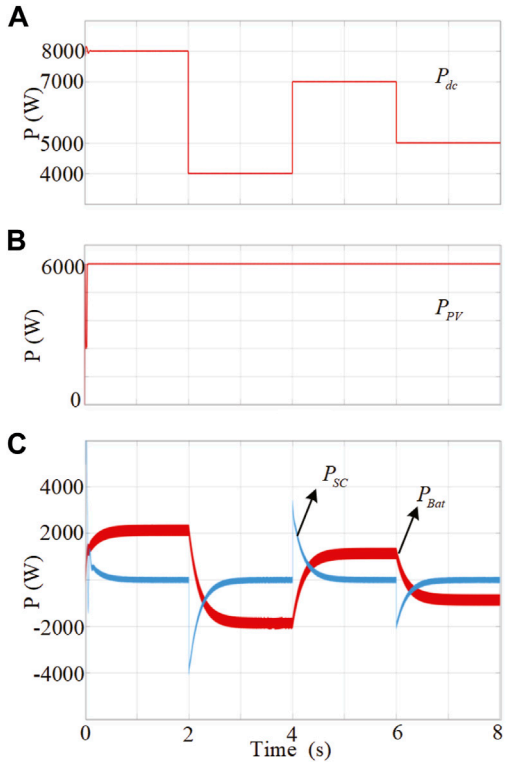

FIGURE 19 | (A) DC bus output power P_{dc}; **(B)** PV array output power P_{PV}; **(C)** HESS output power.

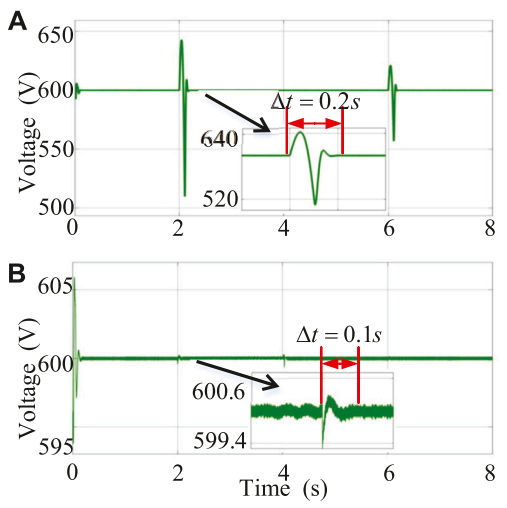

FIGURE 20 | (A) v_{dc} of the system without SC in case 2; **(B)** v_{dc} of HESS in case 2.

battery is in a stable discharge state. Due to load reduction, P_{dc} decreases, SC is charged quickly to compensate for the power fluctuation, and the battery absorbs the remaining power smoothly. When P_{dc} suddenly increases, the SC provides

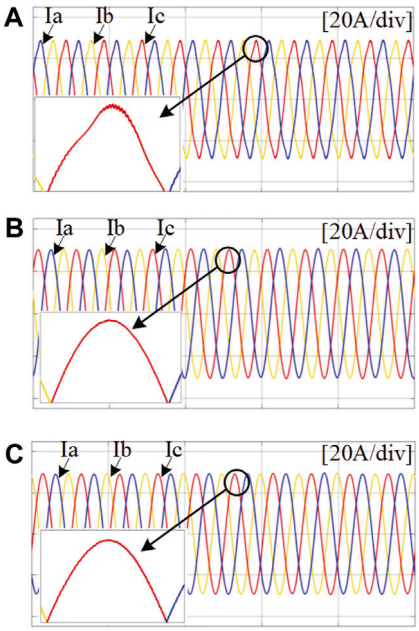

FIGURE 21 | Grid-connected current waveform; **(A)** without compensation; **(B)** with DVC compensation; **(C)** with PLL compensation.

sudden power to offset the impact, during which the battery discharges smoothly.

Figure 20 compares the waveforms of the v_{dc} in case 2. The most obvious fluctuation happens at 2s, the battery energy storage system takes 0.2 s to get stable, and the fluctuation amplitude is larger. The HESS takes 0.1 s to get stable with a smaller fluctuation. The HESS can overcome the shortcoming of the slow response of the battery system to the sudden change of load demand and effectively and quickly reduce the influence of system power fluctuation v_{dc}.

In order to suppress the negative impact of DVC and PLL, the experimental results of the improved method for the traditional inverter control strategy are as follows. **Figures 21**, **22** show the simulation results of the grid-connected current before and after the compensation control is added to the inverter. The addition of the DVC compensation proposed in this article effectively eliminates the negative impact of the DC voltage loop, and the harmonic distortion rate of the grid-connected current is reduced from 4.18% to 1.02%. The system becomes stable and meets the grid-connected standards. The harmonic distortion rate of the grid-connected current is reduced from 1.02% to 0.68% when the negative influence of the PLL is compensated on the q-axis, which proves the validity of the control method proposed in this study.

In **Figure 23**, the experimental results show that in the very weak-grid condition, after compensation is added at 0.5 s, the distortion of the grid current is suppressed. The grid-connected system is restored to a stable state.

The common fault in the grid-connected operation of the PV system is simulated. The single-phase grounding fault current is measured at the PCC point. When a single-phase ground fault

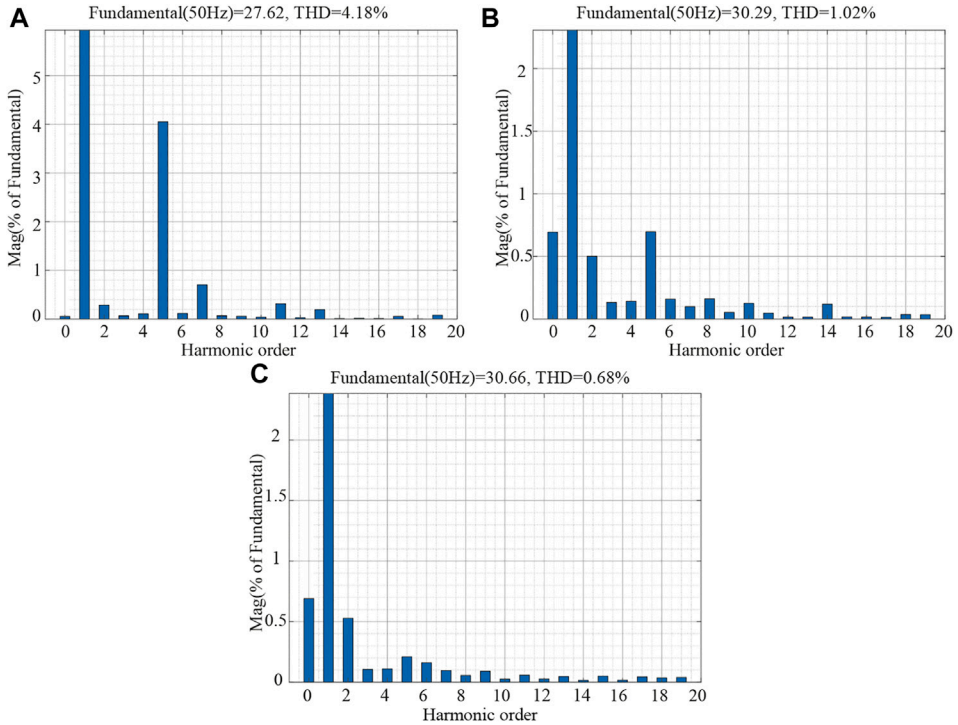

FIGURE 22 | Grid-connected current THD; **(A)** traditional control without compensation; **(B)** with DVC compensation; **(C)** with PLL compensation.

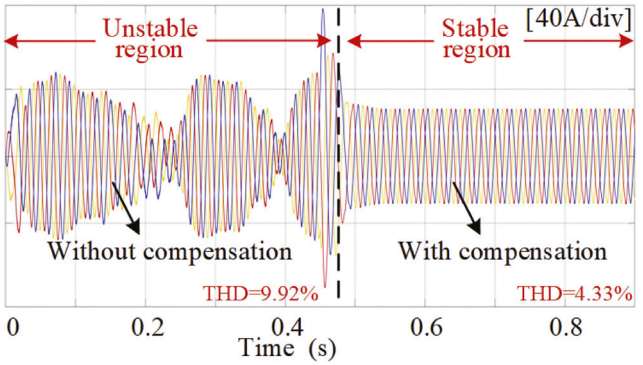

FIGURE 23 | Grid-connected current under very weak-grid.

occurs at the PCC point, the grid-connected current will change rapidly. A-phase ground fault occurs at 0.9 s. At 1.2 s, the A-phase ground fault is eliminated. The experimental results are shown in **Figure 24**. When phase A is grounded, it increases rapidly and distorts. After the fault is eliminated, the current can quickly recover to the current waveform before the A phase is grounded in about 0.01 s. After adding compensation, due to the negative feedback signal in the DVC compensation, the output current is greatly reduced when the fault occurs, and the current waveform is almost stable. The experimental results show that the proposed control method has a certain anti-interference ability to single-phase ground fault.

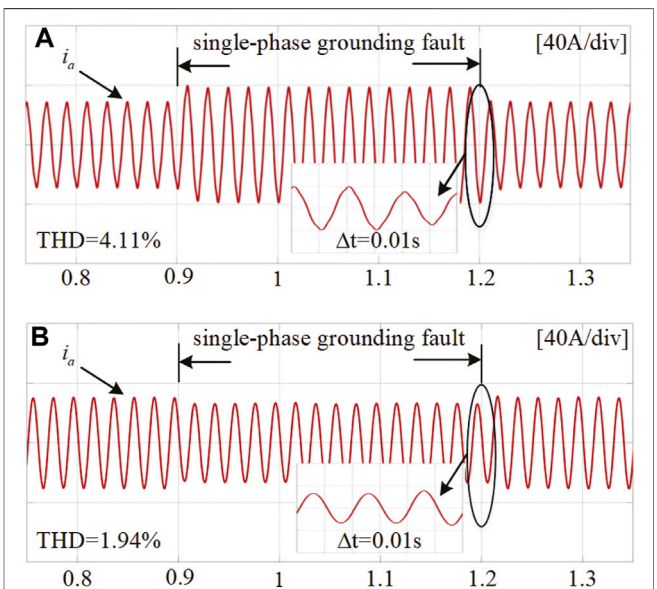

FIGURE 24 | Phase-A grounding fault current; **(A)** without compensation; **(B)** with compensation.

6 CONCLUSION

Aiming at the DC side voltage disturbance of the PV and energy storage system, this study adopts a HESS with a self-adaptive LPF

to quickly and effectively stabilize the DC bus voltage. A small-signal model of the grid-connected inverter is established in the dq coordinate system, and the influence of the DC voltage loop and PLL on the output impedance of the inverter is discussed. The DC voltage loop disturbance compensation method based on power feedforward and the PLL disturbance compensation method based on voltage feedforward are proposed. The analysis results of the impedance frequency characteristics and HIL experiment show that the proposed method can reduce the range that the output impedance appears as a negative characteristic, thereby improving the stability of the system.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/Supplementary Material; further inquiries can be directed to the corresponding author.

AUTHOR CONTRIBUTIONS

XL: Investigation, Conceptualization, Methodology, Validation, and Writing—review and editing. CL: Investigation, Conceptualization, Methodology, Software, Writing—original draft, and Writing—review and editing. RW: Supervision and Validation. YZ: Validation and Writing. LZ: Validation and review and editing.

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Conflict of Interest: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.