# An improved switched diode multilevel inverter topology with fewer on state switches

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A double capacitor double diode double switch (DCDDDS) multilevel inverter is proposed in this paper to generate positive voltage and connect a polarity changing circuit of H-bridge inverter that generates negative voltage. The desired level is achieved by connecting the $j$th number of basic units in series. To generate more stepped levels with fewer switches, various algorithms, such as Natural, Binary, Trinary, and Quasi-Linear sequences, and two new proposed algorithms are discussed to determine the magnitude of DC voltage sources. The proposed multilevel inverter eliminates the need to turn on more power switches for different levels, which is the highlight of this topology. The proposed multilevel inverter is compared in terms of the switch count, number of ON state switches per level, driver circuits, and total standing voltage with the conventional switched diode multilevel inverters. Real-time results from the test bench of OPAL-RT and simulation have been used to validate the proposed inverter.

## 1 Introduction

Multilevel Inverters offer several advantages over traditional two-level inverters, such as having less total harmonic distortion because the output voltage and current are almost similar to a sinusoidal wave, high efficiency, reduced switching losses, and less peak inverse voltage depending on properly designed topologies. Initially, (Nabae et al., 1981; Meynard and Foch, 1992; Rodriguez et al., 2009) three MLI topologies, namely Neutral Point Clamped MLI (NPC MLI), Flying Capacitor MLI (FC-MLI) and Cascaded H-Bridge MLI (CHB MLI), were developed in the literature; consequently, the inverter output power is improved and the total harmonic distortion is reduced, however, the number of power switches and clamping diodes will increase when the stepped level increases in NPC MLI. Similarly, increasing the single positive and negative stepped level in CHB MLI requires an additional four switches and one dc source, which is the main issue of this topology. Because of high modularity, many researchers have focused on improving conventional cascaded multilevel inverters based on the number of switches with the driver circuit, maximum blocking voltage of each switch including the total standing voltage of the inverter, the number of sources, power losses, and Total Harmonic Distortion. In (Babaei and Hosseini, 2009), Ebrahim Babaei et al. conferred a

semi-bridge type sub-multilevel. The author provides three methods for determining unequal dc magnitudes of sub-multilevel to increase the steps in the output wave without increasing switch count and dc sources. Though this structure has less blocking voltage than others, it needs to turn on more switches to obtain a higher level (Wang et al., 2017). Lei Wang modified the structure proposed by Ebrahim Babaei where one additional switch is connected to remove the spike at the time of reverse current. As the level increases, the number of turn-on switches increases despite providing fewer blocking voltages than other structures and reducing voltage spikes. Ebrahim Babaei et al. developed a basic unit in (Babaei et al., 2014) that generates three positive output staircase levels; to increase the voltage output stepped levels, the basic unit is connected by cascade, thus resulting in a more expensive and bulkier inverter design. In addition, this structure needs auxiliary structures to create first positive stepped levels. In this article, the author explains four different algorithms for choosing DC sources for higher-level generation. Rasoul Shalchi Alishah et al. (Alishah et al., 2014a; Alishah et al., 2014b; Alishah et al., 2014c) have suggested a new switched diode multilevel inverter structure. In this topology, sub cell or sub multilevel consists of a single switch, a single diode, and a single dc source. The number of positive stepped levels depends on the number of cells connected in series. As the number of cells in series increases, the number of activated switches or conducting switches increases linearly, which will cause a significant increase in conduction losses. Consequently, power losses can occur. To generate a negative stepped output voltage level from this topology, H-bridge circuit is needed. Mohammad Ali Hosseinzadeh et al. (2020) developed a switched-diode MLI that consists of three switches, three diodes, and three sources to generate seven levels during equal dc source value. The author has discussed two different methods to select the dc source value for generating high-stepped output level with a lower number of switch count. Although this topology uses fewer power switches and driver circuits, it does not work for a power factor less than 0.99 because, during RL load, the voltage spikes are generated at positive and negative zero levels. This is due to the reverse current. Babak Hosseini Montazer et al. solved this problem in (Hosseini Montazer et al., 2021) through the creation of a new structure for bidirectional current flow. Nevertheless, this requires more switches and driver circuits. Furthermore, the number of conducting power switches increases as the number of levels increases, which results in greater conduction losses. A novel Cascaded H-bridge multilevel inverter is propounded (Seifi et al., 2020) by Ali Seif. The basic structure of this topology is three positive output stepped levels with five switches, three sources, and a single diode. Despite this structure having fewer switches and driver circuits, the total blocking voltage is quite high. Dhafer Almakhles et al. suggested (Sathik et al., 2021a) Symmetrical Diode based Half-Bridge MLI; the basic module this topology produces is a positive stair cases of two levels with two switches, two diodes, two sources, and two dc link capacitors, however a balancing circuit is required, so when two capacitors are connected in series, the voltage across

each capacitor is not equal. Voltage divider circuits are used to equalize the capacitor voltage, which will increase the inverter component and size. Trinary sequence algorithms have been discussed as a way to create higher levels with fewer switches and diodes from this topology. Kaibalya Prasad Panda et al. (Panda and Panda, 2018; Panda et al., 2020) discussed double-source switched diode with unequal DC sources to generate a positive stair-level output. This circuit requires fewer driver circuits with fewer switches, but the source requirements for this structure increases as the level increases, i.e. the main issue with this structure is that it requires four dc sources to produce three positive levels. A novel Switched Diode Multilevel Inverter with fewer switches was created by Ahamed Ibrahim et al. (Panda et al., 2019). The blocking voltage and ON state switches are the topology's advantages, but the problem with it is that every single basic unit needs one bidirectional switch. Kaibalya Prasad Panda (Hosseinpour et al., 2020) created a switched-diode dual source single switch based multilevel inverter. The problem with this design is that when the number of levels is increased, more switches need to be turned on. The bidirectional diode-based multilevel inverter topology with decreased switch was created by Hosseinpour et al. (Ahamed Ibrahim et al., 2019). Although this architecture has fewer switches overall, it has more bidirectional switches, which is its greatest issue. The T-Type inverter is a modified design by Bidyut Mahato et al. (Mahato et al., 2021). Upward sequential cells produce positive levels, and downward sequential cells produce negative levels. There are no bidirectional switches required, and there is less total standing voltage, but when the level increases, the number of cells (single dc source, switch, and diode) required increases as well. The same number of cells should be connected on both sides of the inverter so that an equal level is produced on each half-cycle. The main weakness of this converter is that the number of cells increases on both sides as the number of levels increases. This leads to increased number of turn on switches. According to the literature survey, to increase the level of a switched-diode multilevel inverter, more switches will need to be active; this will increase the conduction losses and energy losses. Conduction losses can be reduced by reducing the conduction duration of the switches. The proposed DCDDDS topology uses fewer on-state switches to produce more levels.

The following are the most important aspects of this work:

- More levels can be achieved with fewer switches in generalized Double dc link capacitor Double Diode Double Switch-based multilevel inverters.
- In relation to the level, the quantity of on-state switches is minimized.
- The proposed multilevel inverter with fewer ON-sate switches can handle both symmetrical and asymmetrical sources. During unequal dc source selection, two algorithms are proposed: proposed algorithm 1 and proposed algorithm 2 (Combination of trinary and quadruple sequences).

- This paper provides the number of levels pertaining to the fundamental units that can generate the desired level using an appropriate algorithm. It is necessary to know the cumulative standing voltage of the topology as well as the blocking voltage at each switch to select the best algorithm.
- Modified multicarrier PWM modulation for reducing THD and improving voltage RMS values is described.

# 2 Proposed multilevel inverter

The basic unit of Double dc link capacitor ($C_1$, $C_2$) Double Diode Double Switch (DCDDDS)-based multilevel inverter are designed to generate a positive sequence of two levels, shown in Figure 1A, and the auxiliary unit consists of one switch and two switches, which is illustrated in Figure 1B. Figure 1C shows the typical waveform of output voltage. The first positive level of $V_{C2}$ is generated when switch $S_2$ is turned on; similarly, the second positive level of $V_{C2} + V_{C1}$ is generated when switch $S_1$ is turned ON. The switching pattern for the basic unit is depicted in Figure 1D. The switch $S_1$ blocks the voltage of $V_{C2} + V_{C1}$ and switch $S_2$ blocks the voltage of $V_{C2}$. With the help of polarity-changing circuit, the negative cycle of $V_{C2}$ and $V_{C2} + V_{C1}$ are generated. The main issue with the polarity-changing circuit is that each switch blocks the voltage of $V_o$. In Figure 1A, the $V_o$ represents the maximum voltage across the terminal and the number of levels can be increased by connecting the basic units in series. Figure 1E shows the generalized structure of basic units with an auxiliary circuit used in symmetrical and asymmetrical multilevel inverters. In this, a dc-link capacitor is balanced using a balancing circuit of Multilevel-Boost Converter. Each unit generates output voltages $V_{01}$, $V_{02}$, $V_{03}$ ... $V_{0j}$ respectively. The output voltage of the first unit is computed as $V_{C2} + V_{C1}$, similarly for all basic units. Accordingly, the proposed generalized configuration requires the following number of components.

$$\text{Number of IGBT: } 2j + 6 \quad (1)$$
$$\text{Number of DC source: } 2j + 1 \quad (2)$$
$$\text{No of diode: } 2j \quad (3)$$
$$\text{Number of gate drive: } 2j + 6 \quad (4)$$

In this configuration, "j" is the number of basic units that are connected in series. The proposed DCDDDS multilevel inverter can handle both equal and unequal magnitude dc sources. The selection of a dc source during unequal magnitude is described in section 2.2.

## 2.1 Symmetrical multilevel inverter

The voltage across each dc-link capacitor in all of the basic units is the same, because the dc-link capacitors are balanced by a balancing circuit. As a result, the voltage across the terminal of each basic unit is equal to the sum of the voltages across its dc-link capacitors $V_{oj} = V_{Cj1} + V_{Cj2}$. Taking the $j$th unit as an example, the Total Standing Voltage is 11j+4 and the number of levels is 4j+3. In this method, the auxiliary unit switches $T_a$ and $T_{a'}$ are redundant so $V_1$ is directly connected to the basic unit 1. The auxiliary dc source magnitude is considered to be half of $V_{o1}$.

### 2.1.1 Determination of blocking voltage of switches

$$V_{Sj1} = V_{Cj1} + V_{Cj2} \quad (5)$$
$$V_{Sj2} = V_{Cj2} \quad (6)$$
$$V_{ST1} - V_{ST4} = V_o \quad (7)$$
$$V_o = V_{o1} + V_{o2} + V_{o3} + \ldots\ldots\ldots + V_{oj} + V_1 \quad (8)$$
$$TSV = 11j + 4 \quad (9)$$

## 2.2 Asymmetrical multilevel inverter

There are two ways to raise the stepped level: First, extend the basic unit into a series arrangement. This will increase the number of switches, drivers, and DC sources. Second, when the right voltage magnitude is determined by a different algorithm, which is known as an asymmetrical multilevel inverter, the number of levels is increased with fewer units which will reduce the switch count, sources, and driver circuits. Several methods are available to detect dc sources such as natural sequence, quasi linear, binary, trinary, and proposed algorithm 1 and 2. The generalized expression for the above selected sequence of numbers of level and TSV with respect to the number of units are discussed below. It is assumed that the dc source value for the auxiliary unit is voltage across $V_{C11}$ or 0.5 $V_{o1}$ throughout the sequence.

### 2.2.1 Natural sequence method

As the input DC voltages increase, the algorithm progresses from $1V_{dc}$ to $2V_{dc}$, $3V_{dc}$, $4V_{dc}$... $jV_{dc}$. According to Eq. 10, the dc-link capacitor voltage must be maintained. Eq. 11 can be used to calculate the algorithm's stepped output level. Because the magnitude of the dc-link capacitor varies by basic unit, the IGBT rating is determined by the maximum blocking voltage of each switch in each unit. The total standing voltage is calculated by adding all of the switch blocking voltages in the generalized topology.

$$V_{cj1} = V_{cj2} = jV_{dc}, j = 1, 2, 3, \ldots \quad (10)$$
$$N_{stepped\ Level} = 2\left(j^2 + j + 1\right) + 1 \quad (11)$$

The Total Standing Voltage of Natural Sequence is
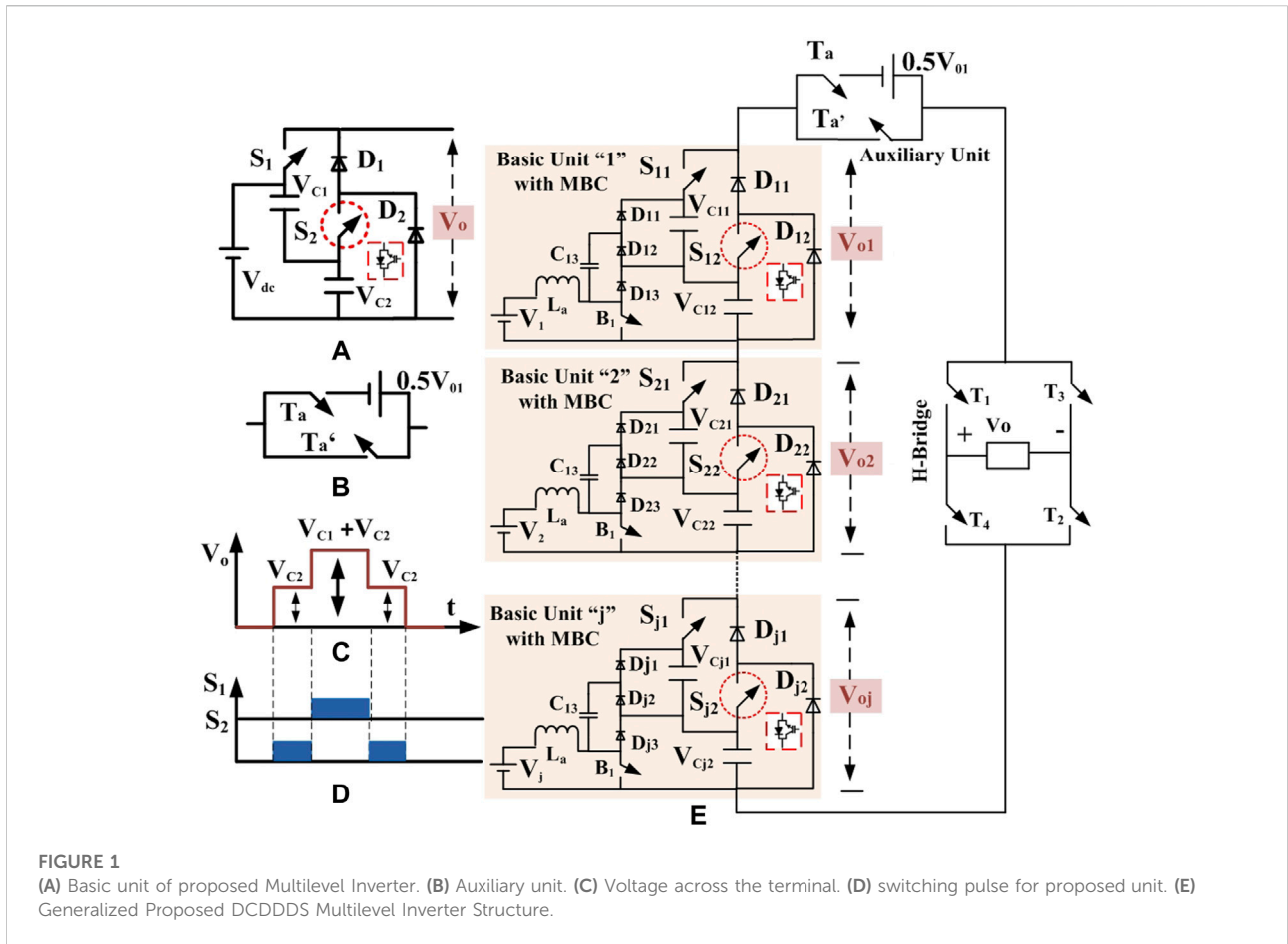
**FIGURE 1**
**(A)** Basic unit of proposed Multilevel Inverter. **(B)** Auxiliary unit. **(C)** Voltage across the terminal. **(D)** switching pulse for proposed unit. **(E)** Generalized Proposed DCDDDS Multilevel Inverter Structure.

$$= \left\{ \left[ \sum_{j=1,2...}^{j} 3j \right] + 2 \right\} + 4 \left\{ \left[ \sum_{j=1,2,3..}^{j} 2j \right] + 1 \right\} \quad (12)$$

### 2.2.2 Binary sequence method

A binary method is used to determine the magnitudes of dc voltage sources, which results in an exponential increase in the levels of the overall outputs with dc voltages. With the binary algorithm the value of dc source is $V_{Cj1} = V_{Cj2} = 2^i V_{dc}$, i = j-1, j = 1, 2, 3. . . ... Hence, the general expression for the number of levels is $2^{(j+2)}$ -1. The switch $S_{j1}$ blocks the voltage of $V_{Cj1}$ plus $V_{Cj2}$; similarly, the switch $S_{j2}$ blocks the voltage of $V_{Cj2}$. The total standing voltage of the binary algorithm is expressed as

$$= \left[ \sum_{i=0}^{j-1} 3 \left( 2^i \right) \right] + 4 \left( 2^{j+1} - 1 \right) V_{dc} \quad (13)$$

### 2.2.3 Trinary sequence algorithm

The dc source value in the trinary sequence is calculated using the power of three, which is $V_{Cj1} = V_{Cj2} = 3^i V_{dc}$. This can

generate levels of 2 $(3^i)$ +1. The expression of total standing voltage for this algorithm is given below.

$$= \left[ \sum_{i=0}^{j-1} 3 \left( 3^i \right) \right] + 4 \left( 3^j \right) V_{dc} \quad (14)$$

### 2.2.4 Quasi-linear sequence algorithm

The voltage magnitude of each basic unit is determined by Eq. 15. The number of levels generated from this algorithm is 4 $(3^{j-1}+3)$. Based on Eq. 16, the TSV is determined for Quasi-Linear algorithm.

$$V_{cj1} = V_{cj2} = \begin{cases} V_{dc}; \text{for } j = 1 \\ 2*3^{(j-2)} V_{dc}; \text{for } j = 2, 3 \dots \end{cases} \quad (15)$$

$$TSV = \left\{ 4 \left[ 3 + \sum_{j=2,3,4}^{j} 4*(3^{j-2}) \right] \right\} + \left\{ \left[ \sum_{j=2,3,4}^{j} 6*(3^{j-2}) \right] + 5 \right\} \quad (16)$$

### 2.2.5 Proposed algorithm 1

$$V_{cj1} = V_{cj2} = \begin{cases} V_{dc}; \text{for } j = 1 \\ 4^{(j-i)} V_{dc}; \text{for } j = 2, 3 \dots \end{cases} \quad (17)$$

According to Eq. 17 above, the dc source value for the first unit is $V_{dc}$, while the remaining units have a voltage of $4V_{dc}$ to generate 2 (8i) +7 number of levels. In a similar fashion, the total standing voltage for *j*th unit of proposed algorithm is

$$= \left\{ 4\left[ 3 + 2\sum_{j=2,3,4..}^{j} 4^{(j-i)} \right] \right\} + \left\{ \left[ \sum_{j=2,3,4..}^{j} 12^{j-i} \right] + 5 \right\} \quad (18)$$

### 2.2.6 Proposed algorithm 2: Trinary and quadruple combined algorithm

The generalized structures shown in Figure 1E are divided into odd and even numbers of units using this algorithm. The trinary sequence, which means power of three, determines the odd unit dc source values, while the quadruple sequence, which means power of four, determines the even unit dc source values, as shown in Eq. 18. The total standing voltage and number of stepped levels are investigated using Eqs 19, 20.

$$V_{Cj1} = V_{Cj2} = \begin{cases} 3^{\frac{(j-1)}{2}}; \text{for } j = 1,3,5\ldots \\ 4^{\left(\frac{j}{2}\right)}; \text{for } j = 2,4,6\ldots \end{cases} \quad (19)$$

$$= 5\left\{ \sum_{j=1,3,5..}^{j} 2*3^{\frac{j-1}{2}} + \sum_{j=2,4..}^{j} 2*4^{\frac{j}{2}} \right\} + \left\{ \sum_{j=1,3,5..}^{j} 3^{\frac{j-1}{2}} + \sum_{j=2,4..}^{j} 4^{\frac{j}{2}} \right\} + 6 \quad (20)$$

$$= 4\left\{ \sum_{j=1,3,5}^{j} 3^{\frac{(j-1)}{2}} + \sum_{j=2,4,6}^{j} 4^{\frac{j}{2}} \right\} + 3 \quad (21)$$

# 3 Calculation and comparison of symmetrical DCDDDS MLI topology with conventional topologies

In terms of component count factor, cost function, number of stepped levels, diode requirement, and total standing voltage, the proposed DCDDDS switched diode multilevel inverter is compared with conventional topologies of the switched diode.

## 3.1 Determination of component count level factor (FCL)

The primary goal of researchers today is to reduce the component count factor of the inverter. In general, higher factor values indicate a need for more components at a given output voltage level. The reduction of factor values has thus become increasingly important in multilevel inverter topologies. From graph 2. D, the similar topology (switched-diode) presented in R2, R7, and R8 (Proposed DCDDDS MLI) has the same number of component counts per level. Though the presented topology in R3 has lower component counts per level

than the proposed topology, but turn on switch count with respect to level little more which is tabulated in Table 1. The Proposed DCDDDS MLI has a lower component count when compared to conventional topologies ($R_1$, $R_5$, $R_6$, and $R_4$).

## 3.2 Calculation of cost function

In order to calculate the total cost of the multilevel inverter, a cost function (CF) is used to calculate all the components of the inverter module, including power semiconductor switches ($N_{sw}$), capacitors ($N_C$), driver circuit ($N_{DRI}$), number of Sources ($N_{DCS}$), number of Diode ($N_{DI}$) and weight coefficient multiplied with per unit of Total standing Voltage. Eq. 22 (Prasad et al., 2021) represents the formula used to calculate the cost factor. In the equation, "α" represents the weight coefficient, and the value is chosen to be greater or lower than one. The cost function of DCDDDS and conventional switched-diode structures are given in Table 1.

$$\text{C.F} = (N_{sw} + N_{DRI} + N_{DI} + N_c + N_x + \alpha\text{TSV}_{,P.U})\,N_{DCS} \quad (22)$$

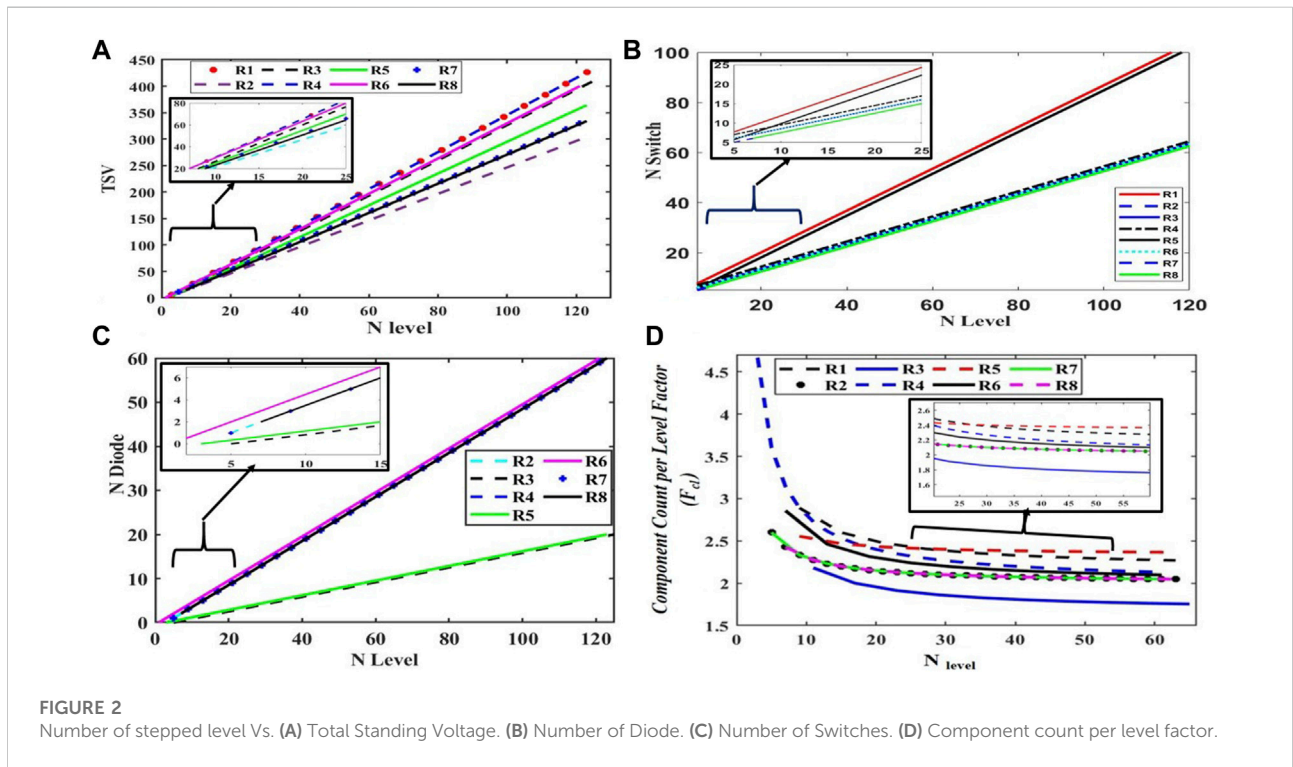$$\text{Total Standing Voltage}_{(PU)} = \frac{V_{TSV}}{V_{0,max}} \quad (23)$$

## 3.3 Comparison with other topologies

Table 1 shows the proposed DCDDDS structure with a similar switched diode conventional structure and provides the switch count, the number of drivers required, and the blocking voltage of the topology. The dc sources in all basic units from proposed DCDDDS inverter are assumed to be symmetrical. Figure 2A clearly shows that the DCDDDS structure requires less total standing voltage than any other switched-diode structure, except R2. Despite the lower standing voltage of the R2 structure, the turn-on switches are proportional to the stepped level, so the conduction losses will increase. In Figure 2C, there is a comparison between number of stepped levels and switch count. The topology presented in R1 and R5 needed more switches. Similarly, the topology presented in R2, R3, R4, R6, and R7 is close to the proposed DCDDDS structure. This clearly shows that the proposed structure requires fewer switches than the other switched-diode MLI structure. Figure 2B depicts the number of diodes used in both the conventional and DCDDDS proposed structures. Therefore, an equal number of diodes must be used to develop the topology presented in R2, R4, R7, and the proposed DCDDDS structure. However, the required number of diodes is lower for R3 and R5, which has a greater need for switches and gate drivers.

Figure 3A compares the same configuration of a conventional structure with proposed DCDDDS MLI in

TABLE 1 Comparison of different Switched-Diodes with Proposed DSDDDS.

| References | Notation in graph | $V_{o,max}$*$(V_{dc})$ | $N_{Level}$ | $N_{Switches}$ | $N_{IGBT}$ | $N_{Driver}$ | $N_{Diode}$ | TBV | C.F$_{pu}$/N$_L$ | | FCL |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | 0.5 | 1.5 | |
| Babaei et al. (2014) | R1 | 3j+1 | 6j+3 | 5j+6 | 5j+6 | 5j+6 | NIL | 21j+6 | 11.28 | 14.27 | 2.8889 |
| Alishah et al. (2014a) | R2 | 2j | 2j+3 | j+4 | j+4 | j+4 | j | 5j+4 | 8.61 | 10.72 | 2.3333 |
| Alishah et al. (2014b) | R2 | 2j | 2j+3 | j+4 | j+4 | j+4 | j | 5j+4 | 8.61 | 10.72 | 2.3333 |
| Karasani et al. (2016) | R3 | 3j+2 | 6j+5 | 3j+6 | 3j+6 | 3j+6 | j | 20j+10 | 10.00 | 12.72 | 2.1818 |
| Wang et al. (2017) | R4 | j | 2j+1 | j+5 | j+5 | j+5 | j | 7j-1 | 11.33 | 14.44 | 2.8889 |
| Sedaghati and Majareh, (2019) | R2 | 2j | 2j+3 | (2j+8)/2 | (2j+8)/2 | (2j+8)/2 | j | 5j+4 | 8.61 | 10.72 | 2.3333 |
| Seifi et al. (2020) | R5 | 3j+1 | 6j+3 | 5j+4 | 5j+4 | 5j+4 | j | 18j+4 | 9.67 | 12.11 | 2.5556 |
| Hosseinzadeh et al. (2020) | R6 | 3j | 6j+1 | 3j+4 | 3j+4 | 3j+4 | 3j | 20j | 8.71 | 11.57 | 2.8571 |
| Sathik et al. (2021a) | R7 | 2j | 4j+1 | 2j+3 | 2j+3 | 2j+3 | 2j-1 | 11j | 8.78 | 11.22 | 2.3333 |
| **[proposed DSDDDS]** | **R8** | **2j+1** | **4j+3** | **2j+4** | **2j+4** | **2j+4** | **2j** | **11j+4** | **10.27** | **12.63** | **2.4286** |



**FIGURE 2**
Number of stepped level Vs. **(A)** Total Standing Voltage. **(B)** Number of Diode. **(C)** Number of Switches. **(D)** Component count per level factor.

order to identify the number of switches that need to be turned on to generate the same level; it considers the symmetrical value of dc source for a conventional as well as proposed MLI. Two and three switches, respectively, are required to be turned on to generate positive stepped first level and second level presented in R2, R3, R5, R7 and proposed DCDDS MLI, whereas conventional structures presented in R1, R4 and R6 require

slightly more switches to be turned on to generate the same levels. Generating stepped third, fourth, fifth, and sixth level from DCDDDS MLI needs fewer switches to turn on compared to a conventional structure. As a result, by decreasing the number of on state switches with respect to levels, conduction losses can be minimized and efficiency can be improved by reducing the conduction losses.

FIGURE 3
(A) The number of turn-on switches for various topologies. (B) Modified Carrier Signal.
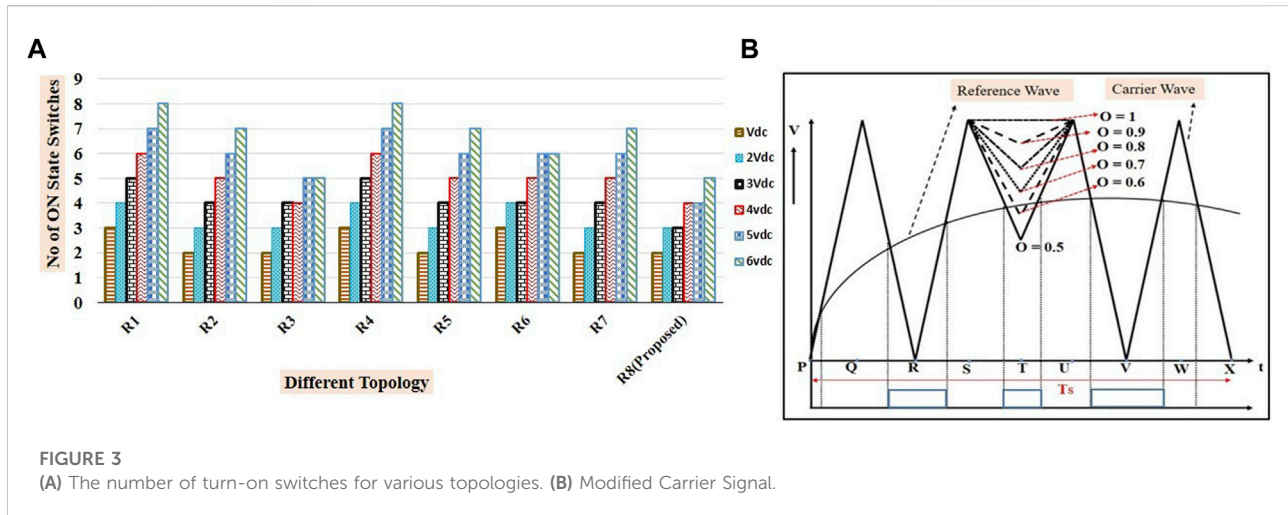
## 3.4 Determination of power losses

Both their conduction and switching transitions are responsible for these losses. Switching losses are the costs associated with turning switches ON and OFF, or transitioning between switches. Conduction losses, on the other hand, result from the switches' conduction. The power loss analysis should be taken into account while calculating these losses. As a result, various losses have been collected and PLECS software has been used to estimate the proposed converter's thermal performance. Figure 5 depicts the heat loss profile for the Infineon IKW30N60DTP. Figures 2A–C, respectively, illustrate the thermal description of the turn-on loss, turn-off loss, and conduction loss. With the aid of a heat sink and thermal resistance of 0.75 K/W at an ambient temperature of 25℃, this is obtained in a PLECS environment. The switching losses and conduction losses are illustrated in Figure 4 and the efficiency of the proposed inverter is 97.55%.

## 4 Modified modulation technique

In conventional carrier waveforms, the amplitude of the voltage varies from 0 to 1 in the time interval of Ts/2 and from 1 to 0 in the time interval of Ts, respectively, under level-shifted multilevel pulse width modulation. The author of (Sathik et al., 2021b) has modified the traditional carrier wave to improve power quality, i.e., to reduce total harmonic distortion and to increase RMS voltage. Additionally, the modified carrier wave is once again modified in order to reduce the total harmonic distortion. A novel switching scheme based on Level-Shifted multilevel pulse width modulation, under which the carrier wave amplitude is decided by dividing the sampling time period of Ts equally into nine intervals marked in Figure 3B, is

proposed to reduce THD. The nine intervals (P-X) are 0 to Ts/8, Ts/8 to 2Ts/8, 2Ts/8 to 3Ts/8, 3Ts/8 to 4Ts/8, 4Ts/8 to 5Ts/8, 5Ts/8 to 6Ts/8, 6Ts/8 to 7Ts/8, and 7Ts/8 to Ts. The amplitude for the corresponding point of carrier wave form changes from 0 to 1, 1 to 0, 0 to 1, 1 to 0.5, 0.5 to 1, 1 to 0, 0 to 1, and 1 to 0 respectively. The proposed pulse width modulation becomes a conventional triangular carrier waveform when the point T amplitude is 0. Similarly, when the amplitude of T is 1, the point between R to V changes to trapezoidal to generate two pulses.

## 5 Result discussion

### 5.1 Simulation results

In order to examine whether the proposed MLI is capable of generating a desired stepped output voltage waveform according to the proposed algorithm and conventional algorithm, it has been simulated using MATLAB/SIMULINK. As shown in Figure 1E, two basic circuits with auxiliary circuits are used to analyze the performance of the suggested inverter. In this, the self-balancing circuit of a multilevel boost converter is interfaced between an unregulated source/regulated source and a multilevel inverter circuit in order to balance a dc link capacitor. In a multilevel boost converter, when the source is photovoltaic, the dc-link capacitor voltage is balanced by varying the duty cycle of switches $B_1$ and $B_2$. Initially, the proposed inverter is validated using the trinary sequence algorithm. From a trinary sequence, the voltage magnitudes of the first basic units ($V_{11}$) are assumed to be 10 V, and the voltage magnitudes of the second basic unit are assumed to be three times the magnitude of the first basic unit. The voltage magnitude of the auxiliary unit is equal to the voltage across the dc-link capacitor of $C_{11}$.

**FIGURE 4**
Thermal description of IKW30N60DTP **(A)** ton losses. **(B)** toff losses. **(C)** Conduction losses. **(D)** IGBT power losses calculated using PLECS software. **(E)** Calculated Diode losses.
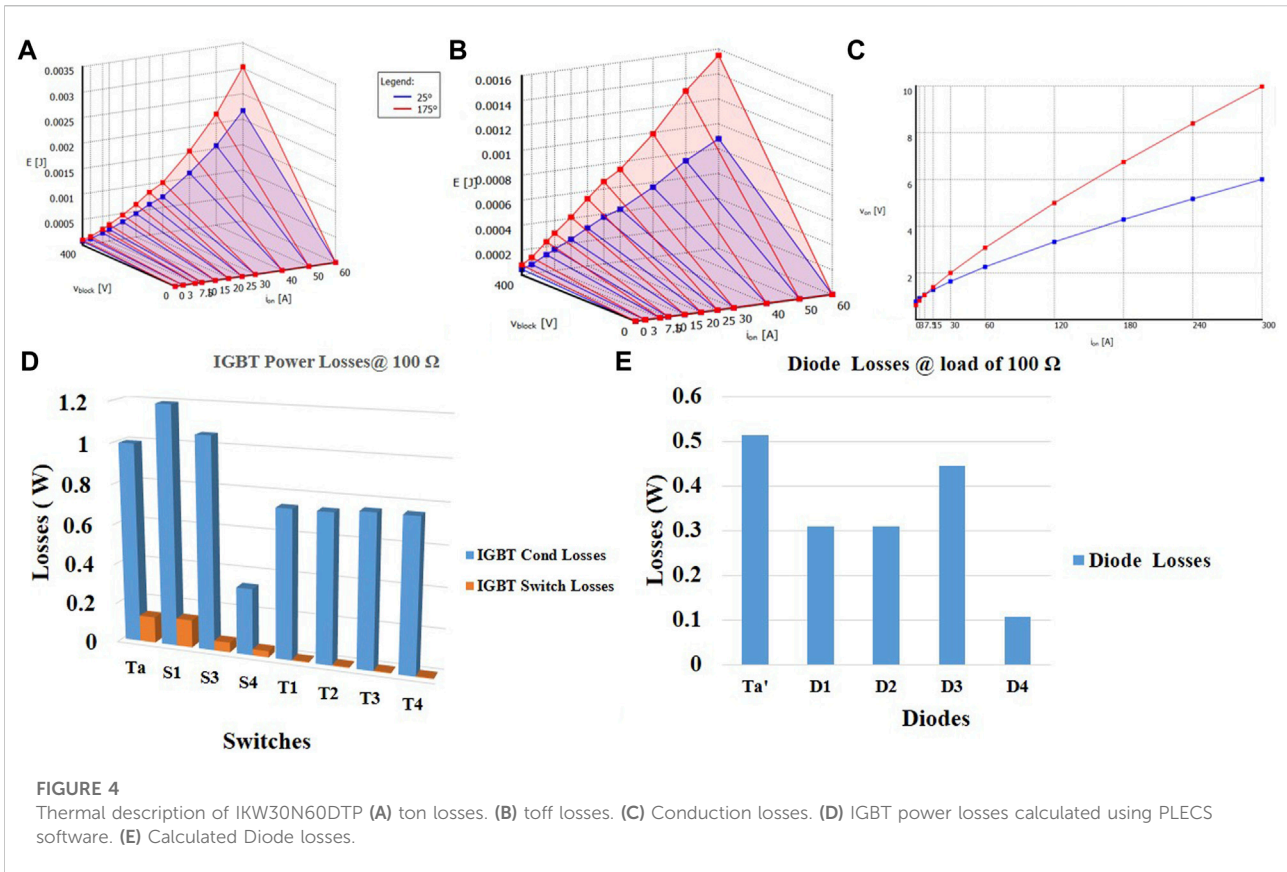
Figure 5A, illustrates the load voltage and current for a trinary sequence and Figure 5B proves that the dc-link capacitor voltage is balanced with the help of a multilevel boost converter. The proposed DCDDDS multilevel inverter with trinary sequence is examined with modulation indices of 1, 0.6, 0.4, and 0.2. As modulation indices decrease, the number of levels decreases. According to the modulation index, 19 levels are created if it is in unity, while thirteen, nine level, and five level are created if it is 0.6, 0.4, and 0.2, respectively. Even after varying modulation indices, the dc-link capacitor voltage remains balanced. Furthermore, the two proposed algorithms are evaluated on the same circuit depicted in Figure 1E. The auxiliary unit and first basic unit values remain the same. The second basic unit's dc source value is four times that of the first unit. Figure 5C shows the results of using dynamic load changes to study load voltages and currents.

## 5.2 Real time test result

To obtain test results, a test bench called the OPAL-RT is used. RT-LAB is used to build Simulink models, which are loaded to the OPAL-RT 4510 real-time interface. A digital storage oscilloscope records real-time analog voltage and

current outputs of the proposed DCDDDS MLI. OPAL-RT 4510 can output 15V to -15V as its maximum output voltage. Figure 6A depicts the experimental setup of the proposed DCDDDS MLI for real-time simulations of OPAL-RT. The resistive load of 100 $\Omega$ is connected to the proposed topology for analysis trinary and proposed sequence-based dc source. First, the trinary sequence has been tested by setting the dc sources $V_{j1}$ and $V_{j2}$ to 10 and 30V, respectively, and the auxiliary source's value is half that of $V_{o1}$. In order for the real-time tech bench to give accurate results, the load voltage and balanced dc-link capacitor voltage must be lowered and kept between +15 and -15. The test result of the proposed DCDDDS with the ratio of 1:3 (trinary sequence) load voltage, load current, and balanced dc-link capacitor voltage from a real-time test bench is depicted in Figure 6B. The dc source values of basic units 1 and 2 are the same for the proposed algorithm 1 and 2, but the dc source values differ from the third to the jth unit basic unit. The proposed topology with the proposed algorithm 2 sequence was tested with various loads, and Figure 6C shows the variation in load voltage and current under dynamic load changes. In the first second, the resistive load of 100 $\Omega$ is connected, in the next second the RL load of 350 $\Omega$ + 50 mH is connected, and in the last second the resistive load of 150 $\Omega$ is connected for the validation of inverter performance.
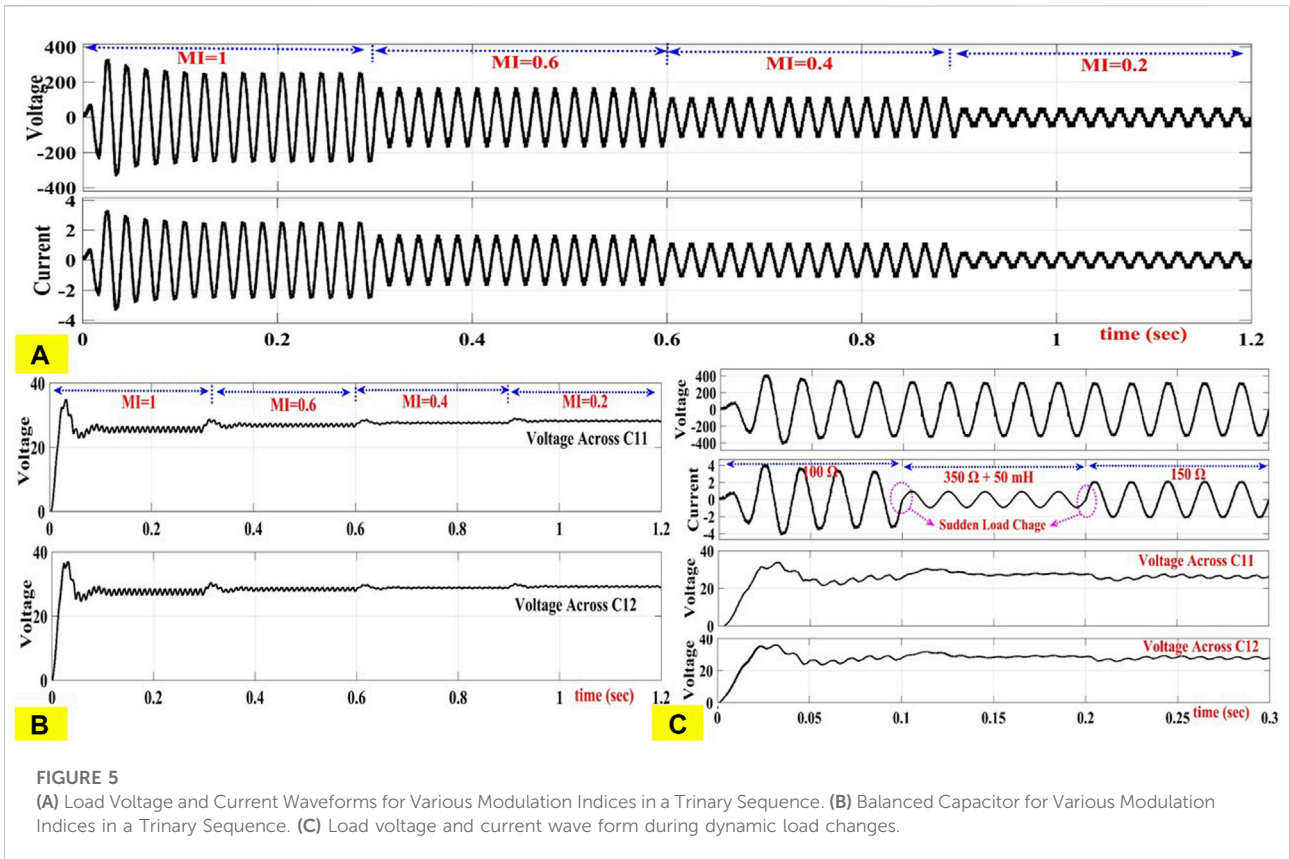
**FIGURE 5**
**(A)** Load Voltage and Current Waveforms for Various Modulation Indices in a Trinary Sequence. **(B)** Balanced Capacitor for Various Modulation Indices in a Trinary Sequence. **(C)** Load voltage and current wave form during dynamic load changes.
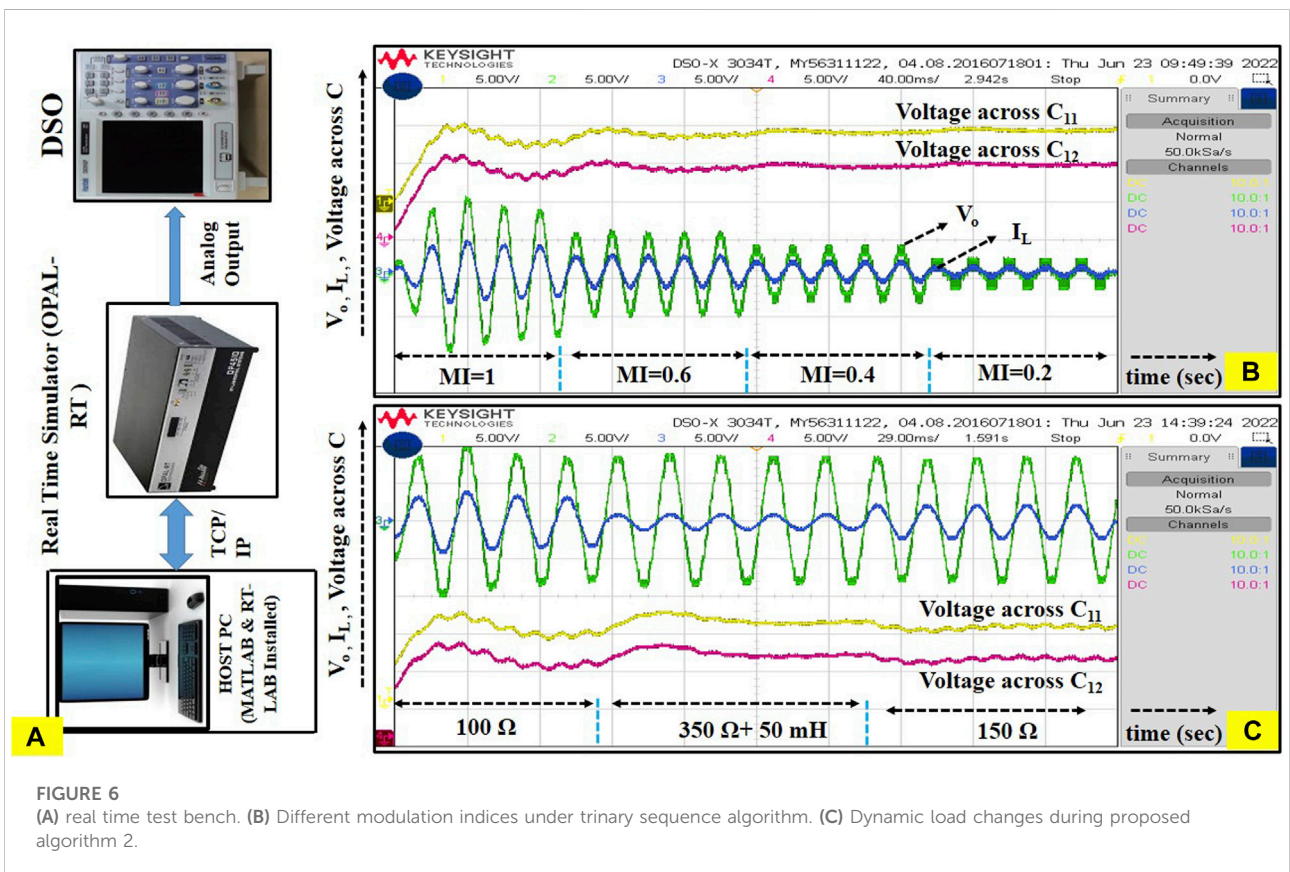


**FIGURE 6**
**(A)** real time test bench. **(B)** Different modulation indices under trinary sequence algorithm. **(C)** Dynamic load changes during proposed algorithm 2.

# 6 Conclusion

The generalized Double Source Double Diode Double Switch with reduced switch count multilevel inverter has been presented and it has been verified that fewer switches are needed to turn on to generate the desired level for symmetrical and asymmetrical values of dc source. The proposed multilevel inverter was verified against different algorithms for generating desired levels and for the same algorithm total standing voltage is also calculated. Compared with symmetric, natural, binary, natural sequence, and quasi-linear algorithms described in the literature, the proposed algorithms deliver a larger number of output levels with lower switch count for lesser basic units. The trinary and proposed algorithm has been tested and the results are verified using simulation and a real-time test bench.

## Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

## Author contributions

VK: Conceptualization, original draft, and Writing, VK and YS: examined the simulation and obtained real-time simulator results.

## Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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