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A strategy for improving the SHEPWM commutation speed of CSI through hybrid switches

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High-power current source inverters (CSI) usually operate at a low switching frequency to reduce switching loss. To suppress low-order harmonics and simplify filter design, the selective harmonic elimination pulse width modulation (SHEPWM) technique is a feasible common modulation strategy in industrial applications. This paper proposes an operational strategy that uses an H7 current source inverter (H7-CSI) with hybrid switches to perform the SHEPWM technique. On the basis of retaining the conventional H6 inverter bridge, the commutation speed of the CSI is improved by an additional shunt-connected high-performance power switch. The proposed scheme solves the problem that the CSIs built with low-speed switches (such as GTOs) may have difficulty for implementing the setting pulse widths of null states, while further reducing the switching losses at an acceptable cost. In addition, mitigating the influence of overlap-time by optimizing the driving signal of the H6 converter bridge. Finally, simulation and experiments have verified the effectiveness of the proposed CSI scheme.

KEYWORDS

selective harmonic elimination pulse width modulation (SHEPWM), current source inverter, minimum pulse width, commutation speed, hybrid switch

1 Introduction

With the emergence of the worldwide energy shortage crisis, more and more attention has been paid to renewable energy (Shahbaz et al., 2020). Under the future trend of the energy revolution, power inverters are playing a vitally important role in the future grid (Sahan et al., 2011). From the form of power supply on the DC side, inverters can be classified as voltage source inverter (VSI) and current source inverter (CSI). Compared to VSI, CSI has the advantages of boosting voltage capability and high reliability (Zmood and Holmes, 2001; Azmi et al., 2011), and it is considered to have potential application value in renewable energy conversion, e.g., photovoltaic (Sahan et al., 2008; Lorenzani et al., 2017), wind energy, and ocean energy systems.

At present, the primary problem of CSI is the high power loss of switching devices, which mainly owing to the fact that CSI has to hold the circuit with a constant current (Trzynadlowski et al., 2001). There are two main technical routes to solve the efficiency problem: One is to replace all the switches with advanced semiconductor devices (e.g., Silicon Carbide (SiC) and Gallium Nitride (GaN) power switches but leaving great burden on the hardware cost of the equipment (Abu-Khaizaran and Palmer, 2007; Mudholkar et al., 2014; Hazra et al., 2016; Guacci

et al., 2019). Another one is to try to make CSI work at a much lower switching frequency (Espinoza and Joos, 1997). However, it carries the risk of reducing power quality. With the introduced large amount of low-order harmonics, the filters are more difficult to design.

The selective harmonic elimination pulse width modulation (SHEPWM) technique is one of the effective solutions to address the above challenges. It is characterized by low switching frequency and excellent harmonic performance, particularly suitable for high-power applications that mitigate switching loss by reducing switching frequency (Pontt et al., 2004; Dahidah et al., 2015). During the implementation of SHEPWM, there are two key issues that need to be considered: one is the establishment of the switching sequence model which determines the harmonic performance, and another is the solution of non-linear transcendental equations which determines the difficulty and accuracy of realization. Karshenas, H. and Kojori, H. investigated the unique characteristics of CSI commutation, and carried out the general CSI switching sequence models (Karshenas et al., 1995). Over the past few decades, scholars have proposed many fruitful methods to find the optimal solutions. Siddique, M.D. using a particle swarm optimization (PSO) algorithm to calculate switching angles. (Siddique et al., 2021). The Newton-Raphson iterative algorithm is the most commonly used method to solve the equations, which needs to find the initial value to fast convergence. Maswood, A.I. proposed using Genetic Algorithm to find the initial switching angels (Maswood et al., 2001). In addition, optimized switching angles are calculated using APSO-GA for seven-level and nine-level inverter (Memon et al., 2022).

Operated with SHEPWM, CSI can effectively eliminate low-order harmonics in theory. However, due to the low switching speed of CSI power switches in practical application, the actual output performance is usually inconsistent with the expectation, some low-order harmonics still occupy a large proportion. This paper analyzes this phenomenon and proposes a new SHEPWM implementation scheme to improve the commutation speed through H7-CSI with hybrid semiconductor switches. Compared to the conventional low-speed switch-based CSIs, the proposed scheme can promote the commutation speed without excessive hardware cost to obtain a better output performance.

This rest of paper is organized as follows. In Section 2, it describes the general SHEPWM implementation process of conventional H6-CSI, and analyzes the limitation of switching speed on modulation. In Section 3, the operational principles of SHEPWM with H7-CSI as well as the hardware configurations are presented in detail. In Section 4, simulation and experimental tests are carried out to validate the theoretical findings.

2 SHEPWM of conventional current source inverters

2.1 Conventional current source inverters topology and its switching combinations

The conventional three-phase CSI is also named as H6-CSI, the topology is shown in Figure 1. It usually uses a voltage power supply and a DC-link inductor to achieve the approximately constant current source I_{dc}. H6 inverter bridge can realize the current commutation and output the three-phase switched currents i_a, i_b, i_c. After the AC filter capacitor C_a, C_b, C_c, the output currents are i_{ao}, i_{bo}, i_{co}. For high-power CSI, H6 inverter bridge is mainly composed of six low-speed power switches (e.g., GTOs, IGCTs) (Xu et al., 2023). When IGBTs are selected, it requires series connected power diodes to increase the reverse-blocking (RB) capability.

At any moment during modulation, there are two switches conducting ON, one on the upper arms (S_1 or S_3 or S_5), and another on the lower arms (S_4 or S_6 or S_2). And CSI adopts lateral commutation mode among the bridge arms. There are nine switching states in total, six of which are active states ({S_1, S_2}, {S_1, S_6}, {S_2, S_3}, {S_3, S_4}, {S_4, S_5}, {S_5, S_6}), the rest three are null states ({S_1, S_4}, {S_2, S_5}, {S_3, S_6}). It is worth noting that the null states actually behave as short-circuit status of the circuit, which is also denoted as the short-circuit pulses in this paper.

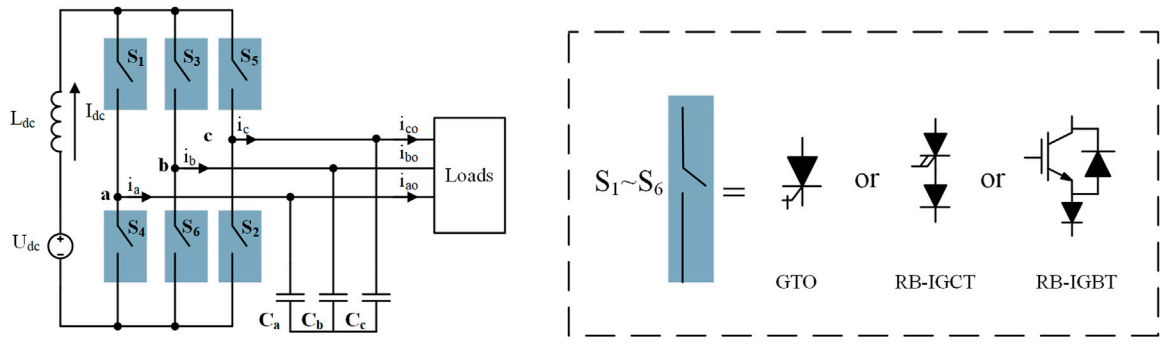

FIGURE 1
Conventional H6-CSI topology and hardware configurations.

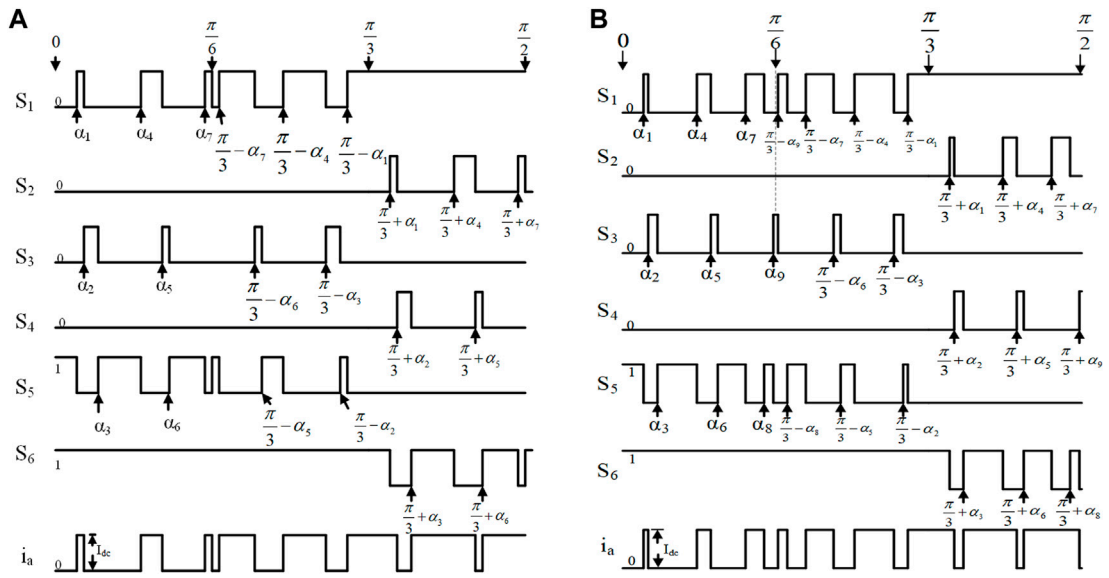

FIGURE 2
(A) SHEPWM scheme of H6-CSI (N = 7), **(B)** SHEPWM scheme of H6-CSI (N = 9).

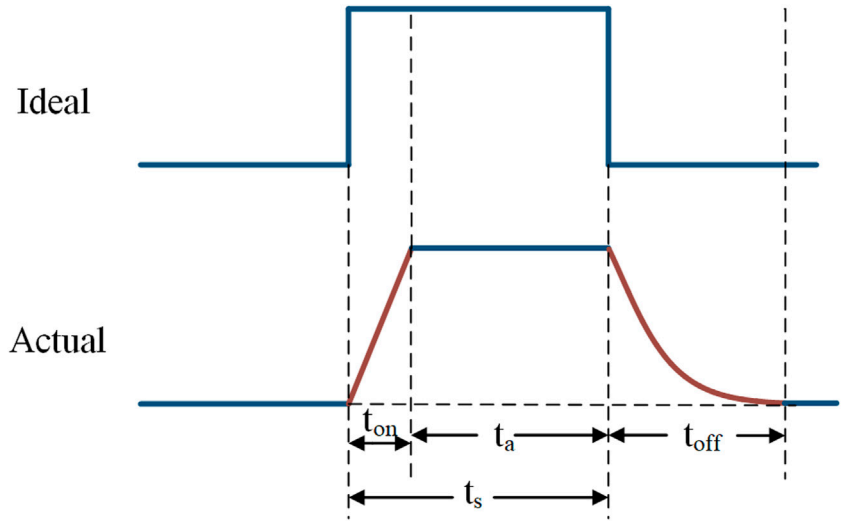

FIGURE 3
The comparison between ideal and actual current waveforms.

2.2 SHEPWM implementation method and the limitations

The SHEPWM method can remove low-order harmonics from the inverter's output by setting the appropriate angles of switching operation. The conventional CSI SHEPWM method is implemented by introducing short-circuit pulses and setting transitions, which is completely different from VSI SHEPWM. Literature (Karshenas et al., 1995) have investigated and listed these differences in the SHEPWM between VSI and CSI in detail.

The operational steps of SHEPWM of conventional CSI are as follows. Step 1: select the low-order harmonics to be eliminated, and set the number of switching angles. N is the number of switching angles and also represents that (N-1) harmonics can be eliminated (e.g., setting N = 5 means to eliminate the harmonics of 5^{th}, 7^{th}, 11^{th}, 13^{th}). It is worth noting that, to maintain the continuity of the current, the switching angles should be set within (0, π/6). Step 2: build the pulse sequences. The characteristic of this scheme is that the driving signals of switches (S_1 ~ S_6) lags π/3 in turn and the output waveform of three-phase current i_a, i_b and i_c lags 2π/3 in turn.

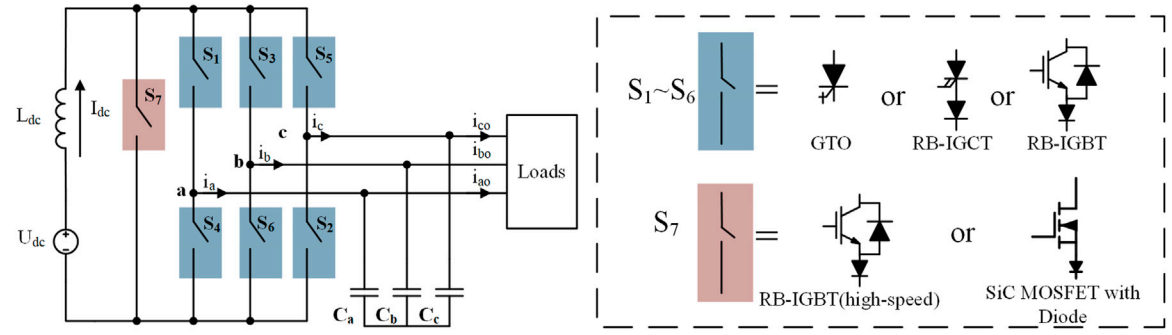

FIGURE 4
H7-CSI topology and hardware configurations.

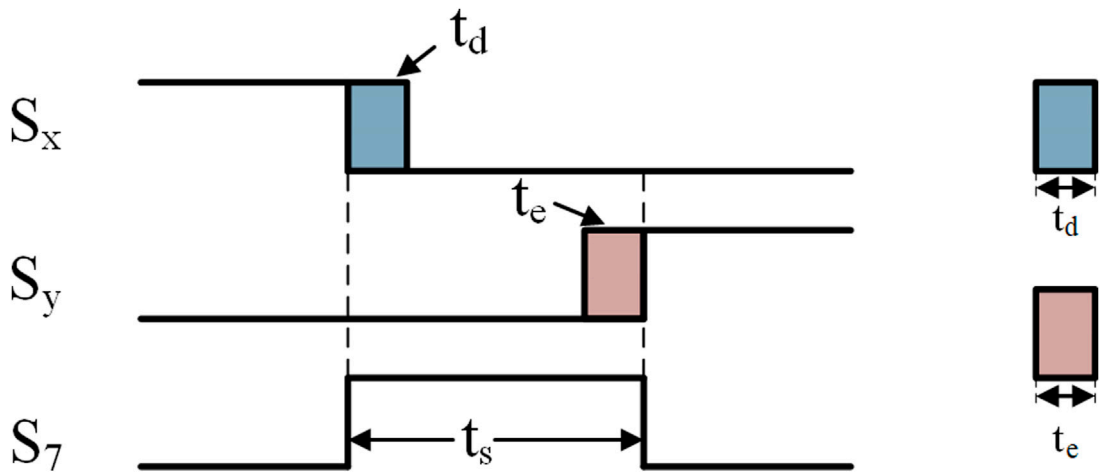

FIGURE 5
Overlap-time optimization scheme.

Step 3: formulate the output current $i(\omega t)$ expression, which owns the features of half-wave symmetry and quarter-wave symmetry. Fourier decomposition is performed on the output current $i(\omega t)$. The decomposition formula is shown as Eq. 1, where $I_{a,n}$ is the amplitude of nth order harmonic of the output phase current i_a, and $I_{a,n}$ can be calculated by Eq. 2.

$$i(\omega t)_{=}\sum_{n=1}^{\infty} I_{a,n}\sin(n\omega t) \tag{1}$$

$$I_{a,n} = \frac{4}{\pi}\int_{0}^{\frac{\pi}{2}} i(\omega t)\sin(n\omega t)d(\omega t) \tag{2}$$

Denote the amplitude of the fundamental current as $I_{a,1}$. Then, the modulation index m can be expressed by Eq. 3. Thus, the switching angles under different modulation index can be solved.

$$m = \frac{I_{a,1}}{I_{dc}} \tag{3}$$

The following takes N = 7 and N = 9 as examples to explain the specific implementation method. When N = 7, the harmonic orders to be eliminated are 5th, 7th, 11th, 13th, 17th, 19th. Therefore, seven switch angles are set (α_1, α_2, α_3, α_4, α_5, α_6, α_7). The specific pulse sequence in a quarter of one period is shown in Figure 2A. The driving sequence of each power switch has four short-circuit pulses in one period. $I_{a,n}$ can be formulated as Eq.4. Using Eq. 3 and Eq. 4, and set $I_{a,n} = 0$ (n = 5, 7, 11, 13, 17, 19), the switching angles can be solved out.

$$I_{a,n} = \frac{4I_{dc}}{n\pi}\begin{bmatrix} cosn\alpha_1 - cosn\alpha_2 + cosn\alpha_4 - cosn\alpha_5 + cosn\alpha_7 - cos\left(\frac{n\pi}{6}\right) \\ +cosn\left(\frac{\pi}{3}-\alpha_7\right) - cosn\left(\frac{\pi}{3}-\alpha_6\right) + cosn\left(\frac{\pi}{3}-\alpha_4\right) - cosn\left(\frac{\pi}{3}-\alpha_3\right) \\ +cosn\left(\frac{\pi}{3}-\alpha_1\right) - cosn\left(\frac{\pi}{3}+\alpha_2\right) + cosn\left(\frac{\pi}{3}+\alpha_3\right) - cosn\left(\frac{\pi}{3}+\alpha_5\right) \\ +cosn\left(\frac{\pi}{3}+\alpha_6\right) - cos\left(\frac{n\pi}{2}\right) \end{bmatrix} \tag{4}$$

Similarly, when N = 9, to eliminate harmonic of 5th, 7th, 11th, 13th, 17th, 19th, 23rd, 25th, the nth harmonic expression of the output current can be formulated as Eq.5. The specific pulse sequence in a quarter of one period is shown in Figure 2B. Compared to the previous sequence (N = 7), the driving

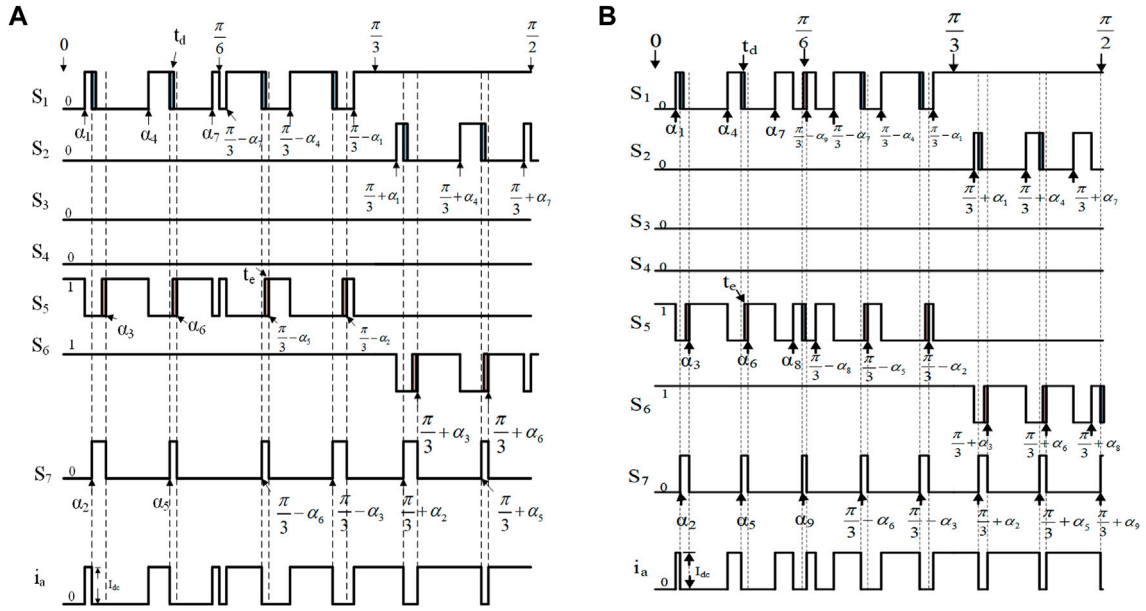

FIGURE 6
(A) SHEPWM sequences of H7-CSI (N = 7), **(B)** SHEPWM sequences of H7-CSI (N = 9).

TABLE 1 Comparison of switching characteristics in one period.

Topology	Commutation speed		Switching loss	
	Active state	Null state	N = 7	N = 9
H6-CSI	Depend on S_1~S_6	Depend on S_1~S_6	180 hard switching	216 hard switching
H7-CSI	Depend on S_1~S_6	Depend on S_7	48 zero current switching	60 zero current switching
			132 hard switching	156 hard switching

pulses (N = 9) of switch S_1 ~ S_6 become denser and have introduced more short-circuit pulses in one period.

$$I_{a,n} = \frac{4I_{dc}}{n\pi}\begin{bmatrix} cosn\alpha_1 - cosn\alpha_2 + cosn\alpha_4 - cosn\alpha_5 + cosn\alpha_7 - cosn\alpha_8 \\ +cosn\left(\frac{\pi}{3}-\alpha_9\right) - cosn\left(\frac{\pi}{3}-\alpha_8\right) + cosn\left(\frac{\pi}{3}-\alpha_7\right) - cosn\left(\frac{\pi}{3}-\alpha_6\right) \\ +cosn\left(\frac{\pi}{3}-\alpha_4\right) - cosn\left(\frac{\pi}{3}-\alpha_3\right) + cosn\left(\frac{\pi}{3}-\alpha_1\right) - \text{cosn}\left(\frac{\pi}{3}+\alpha_2\right) \\ +cosn\left(\frac{\pi}{3}+\alpha_3\right) - \text{cosn}\left(\frac{\pi}{3}+\alpha_5\right) + \text{cosn}\left(\frac{\pi}{3}+\alpha_6\right) - \text{cosn}\left(\frac{\pi}{3}+\alpha_9\right) \end{bmatrix} \quad (5)$$

The above is the modulation scheme under theoretical analysis and ideal conditions. In practical applications, the current of the switch can reflect the commutation process (Bernet et al., 1999). Since the power switch has turn-on time and turn-off time in actual operation, the current of the switch has a rising time (t_{on}) and a falling time (t_{off}), which are different from the ideal waveforms. The comparison between ideal and actual current waveforms are shown in Figure 3. The dwell time of an ideal driving pulse is recorded as t_s, and the dwell time of the actual switching pulse is recorded as t_a. Apparently, the effective pulse width of actual switching is shorter than the ideal setting dwell time. Therefore, the actual current rising and falling process can make the switching angles inconsistent with expectations.

Since high-power CSIs are employed with low-speed switches, the turn-on and turn-off process can last up to a few microseconds. Furthermore, with the increase of the modulation index as well as the number of switching angles, the drive pulses become denser. In particular, the shortest pulse width comes from the null state, so that

TABLE 2 Simulation parameters.

Parameter	Value
DC source voltage (U_{dc})	100 V
DC-link inductor (L_{dc})	5 mH
AC filter capacitor (C)	20 uF
Output resistive loads (R)	20 Ω
Modulation index (m)	0.9
Modulation frequency (f)	50 Hz

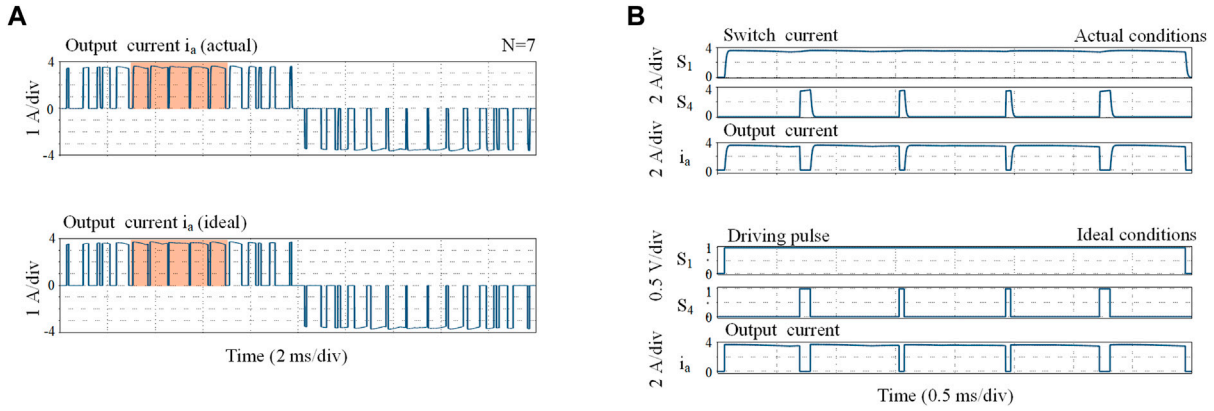

FIGURE 7
(A) Simulated output switched current i_a of H6-CSI (N = 7), **(B)** Corresponding zoomed view within (π/3, 2π/3).

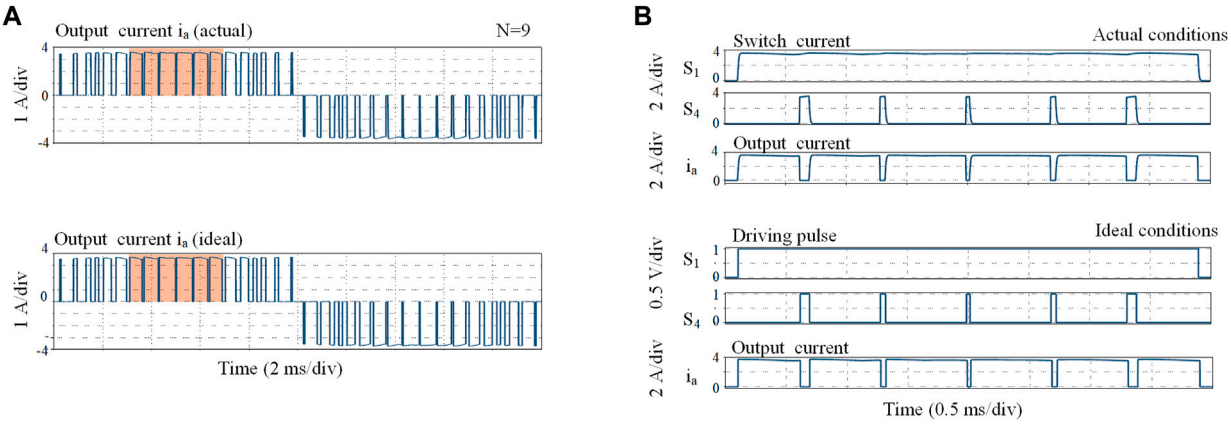

FIGURE 8
(A) Simulated output switched current i_a of H6-CSI (N = 9), **(B)** Corresponding zoomed view within (π/3, 2π/3).

the completion of the short-circuit pulses will be significantly affected by the commutation speed of switches. For example, when m = 0.96 and N = 9, the shortest pulse width occurs at the short-circuit states, which has a width of only about 29 μs. Therefore, conventional CSI who built with low-speed switches (e.g., GTOs, IGCTs) may have difficulty in the switching speed to keep up with the setting short-circuit pulses width, so that the output current cannot reach the expected performance.

In addition, to maintain the continuity of the DC link current, the overlap-time has to be introduced between two switching signals during commutation (Suroso and Noguchi, 2020; Liu et al., 2021). To guarantee the commutation of the low-speed switches is completed, the delay of switching pulses caused by the overlap-time cannot be ignored as well. If not properly set, this phenomenon at short-circuit states will greatly worsen the total harmonic distortion (THD) performance. Therefore, the configuration of overlap-time also need to be carefully considered in conventional CSI.

3 Proposed SHEPWM operational principle with H7-CSI

3.1 Topology and hardware configurations

To improve the commutation speed of low-speed switches of SHEPWM-CSI, this paper proposes a new SHEPWM operational scheme based on the H7-CSI. The topology of the H7-CSI is shown in Figure 4. Compared to conventional CSI, the basic feature of the H7-CSI topology is the added shunt-connected seventh switch, which is the key to improve the inverter's performance (Wang et al., 2018). The seventh switch is connected in parallel with the DC bus, which can be used to replace all the null states. Within 30° power factor angle range, when S_7 is turned on, the current will be quickly switched to this branch, and the remaining six switches can turn on/off with zero current switching (ZCS) capability.

In terms of hardware configuration, the six power switches in the H6 converter bridge retains the same (low-speed switches)

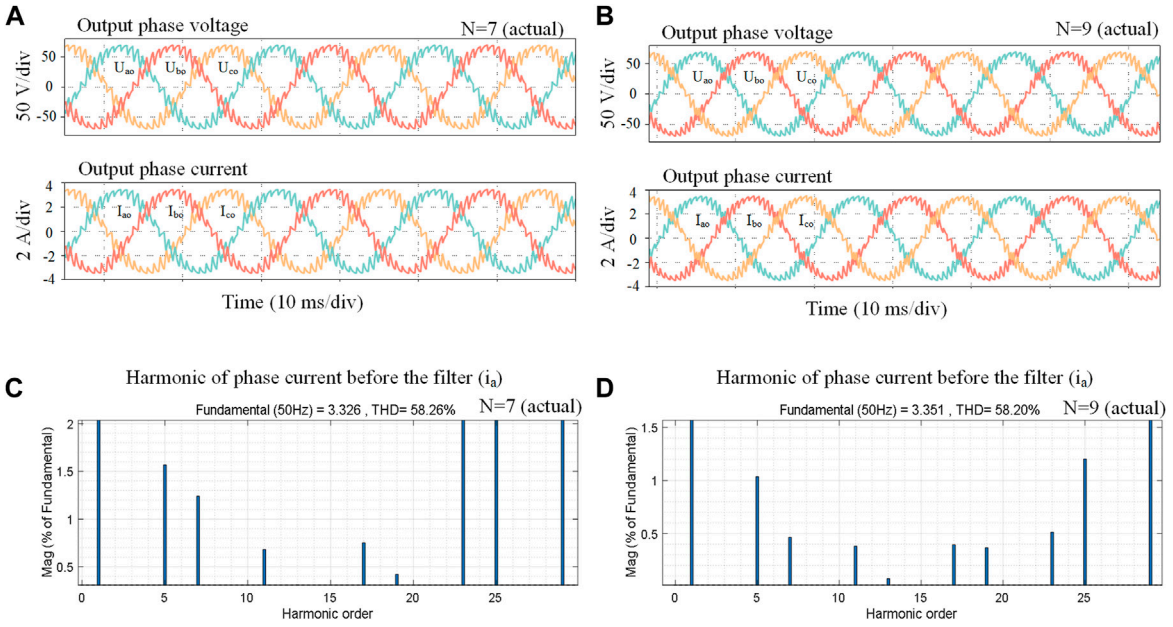

FIGURE 9
Simulated outputs **(A)** Filtered waveforms of conventional SHEPWM-H6-CSI with N = 7, **(B)** Filtered waveforms of conventional SHEPWM-H6-CSI with N = 9, **(C)** Harmonic performance of i_a with N = 7, **(D)** Harmonic performance of i_a with N = 9.

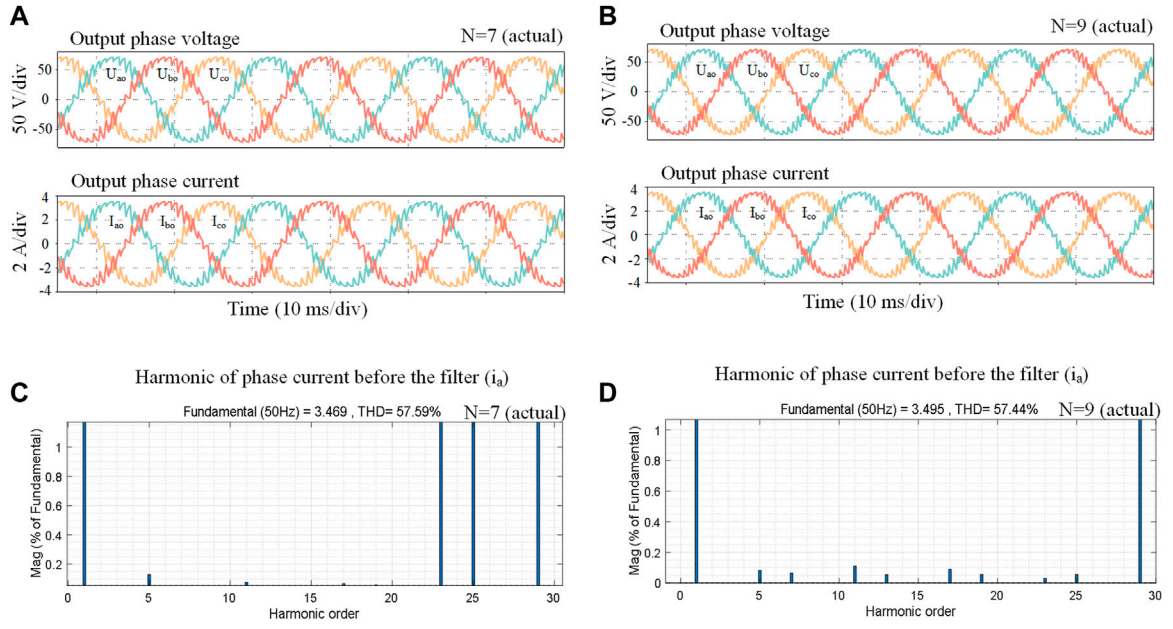

FIGURE 10
Simulated outputs **(A)** Filtered waveforms of proposed SHEPWM-H7-CSI with N = 7, **(B)** Filtered waveforms of proposed SHEPWM-H7-CSI with *N* = 9, **(C)** Harmonic performance of i_a with N = 7, **(D)** Harmonic performance of i_a with *N* = 9.

configuration scheme as the conventional CSI. The key difference is that the seventh switch uses a high-performance power switch. This seventh switch should be characterized by high switching frequency and low loss, which can increase the inverter commutation speed while reducing switching loss. Available choices are high-speed RB-IGBT, or SiC MOSFET with Diode, *etc.* The reverse-blocking capability can be realized *via* series connected power diodes. Compared with the conventional all-hardware-update routine of

TABLE 3 Harmonic performance (% of fundamental).

m = 0.9	5th	7th	11th	13th	17th	19th	23rd	25th	THD (%)
N = 7 (H6-CSI)	1.58	1.25	0.68	0.00	0.75	0.42	—	—	58.26
N = 7 (H7-CSI)	0.14	0.00	0.07	0.00	0.06	0.05	—	—	57.59
N = 9 (H6-CSI)	1.05	0.48	0.39	0.08	0.40	0.38	0.52	1.21	58.20
N = 9 (H7-CSI)	0.09	0.07	0.11	0.06	0.09	0.06	0.03	0.07	57.44

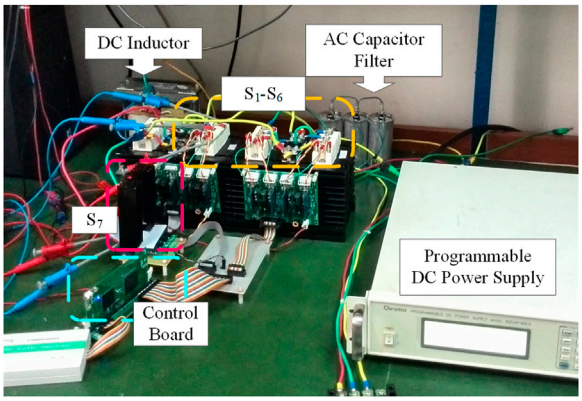

FIGURE 11
Experimental prototype of the H7-CSI.

TABLE 4 Experimental parameters.

Parameter	Value
IGBT-Module (S_1-S_6)	FF100R12RT4 from Infineon
SiC-MOSFET (S_7)	C2M0040120D from Cree
DC source voltage (U_{dc})	120 V
DC-link inductor (L_{dc})	5 mH
AC filter capacitor (C)	20 μF
Output resistive loads (R)	20 Ω
Modulation index (m)	0.9

CSI, the H7-CSI topological solution adopted in this paper can clearly reduce the hardware cost.

3.2 SHEPWM operational principle

The basic idea of proposed SHEPWM solution is to use the seventh switch to help the commutation of other low-speed switches. The specific operating principles are as follows.

1) Select the low-order harmonics to be eliminated, set the number of switching angles, then build the pulse execution scheme of switch S_1~S_6 and formulate the expression of the output current i (ωt), which is basically the same as the conventional SHEPWM-H6-CSI method.
2) Pick out the short-circuit states among the calculated angles, and manage to use switch S_7 to implement these null state pulses.
3) Optimize the driving signal of switch S_1~S_6, regarding the overlap-time issue.

The overlap-time optimization process is pictured as Figure 5. Because the null-state pulses of S_7 are inserted between two different active states (implemented by S_1-S_6), the adjacent turn-off and turn-on operation of S_1-S_6 can be extended with no impact to the output of the circuit. As shown in Figure 5, the original driving sequence is {S_x turn-off, S_7 turn-on} to {S_7 turn-off, S_y turn-on}. To optimize the driving signal, S_x should be delayed for shutdown, the delay time is denoted as t_d, while S_y should be turned on in advance, which is denoted as t_e. Both t_d and t_e should be set within (0, t_s). And the pulse width of S_7 itself remains unchanged. Doing so, on the one hand, it solves the overlap-time issue with no interference to the power quality, and on the other hand, the switching speed challenge of S_1-S_6 can get relieved.

Normally, the delay time and advance time are set as 1–3 μs. Under the premise of meeting the requirements of the rules, the delay time and advance time can be optimized according to the switching speed of the switch.

According to the operating principles described above, pulse sequences of N = 7 and N = 9 can be rebuild, as shown in Figure 6A and Figure 6B. The optimized overlap-time is represented by the shaded area in Figure 6.

The switching characteristics of the proposed SHEPWM scheme with H7-CSI and the conventional SHEPWM-H6-CSI are compared, as shown in Table 1. The proposed SHEPWM scheme basically uses S_7 to improve the commutation speed around the null states, which would be affected by the switching speed most. Since S_7 is characterized by fast switching speed and low switching loss, it is obvious that its actual performance is determined by the hardware selection of S_7.

As for the switching operation, compared to the conventional SHEPWM-H6-CSI, the total number of hard-switching counts of the proposed SHEPWM-H7-CSI is reduced by almost one-third. Moreover, most of the hard-switching transitions are implemented by S_7, which can further reduce the switching loss. In addition, because the implementation of null states uses less power devices, the conduction loss can also decrease. Therefore, it indicates that the proposed SHEPWM-H7-CSI solution can even perform better efficiency.

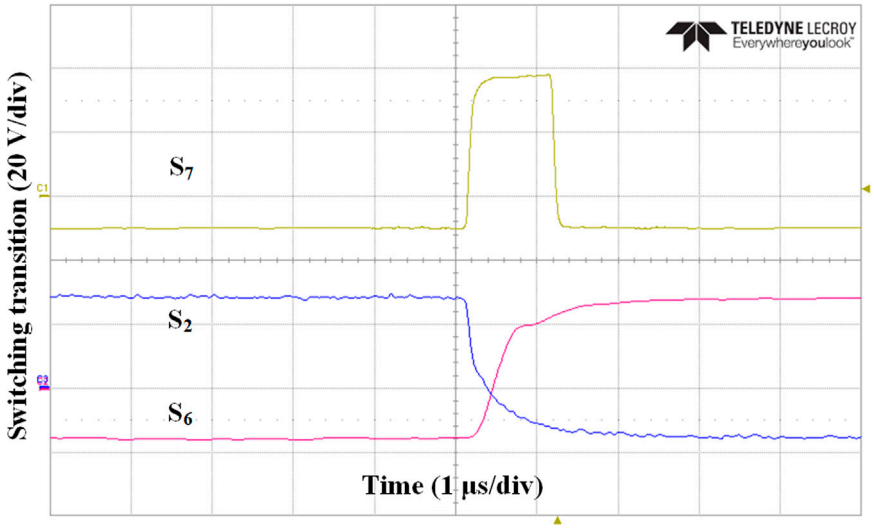

FIGURE 12
Experimental waveforms of switching transition.

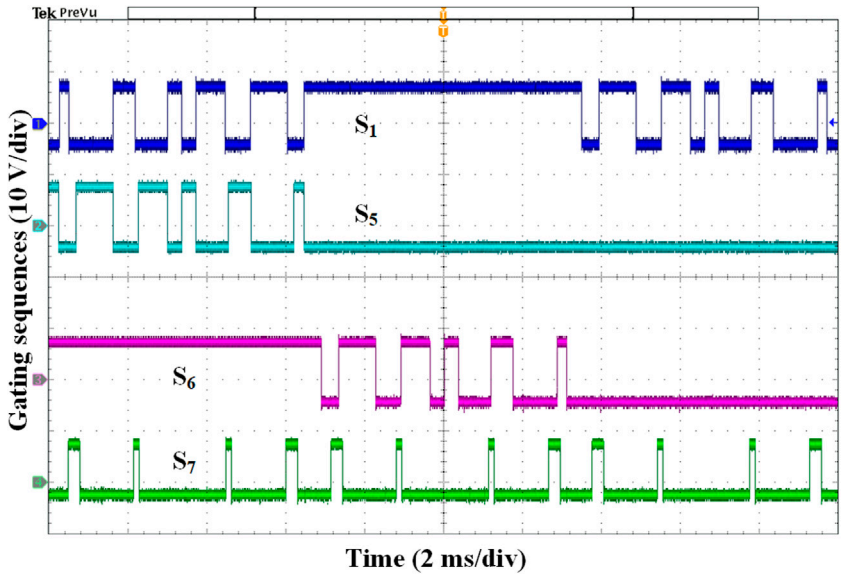

FIGURE 13
Experimental gating pulses sequences.

4 Performance evaluation

4.1 Simulation results

To compare the performance between conventional SHEPWM-H6-CSI and the proposed SHEPWM operational method with H7-CSI, simulation models have been set up using MATLAB with PLECS Blockset, where H6-CSI and H7-CSI are built with the same parameters. The simulation parameters are listed in Table 2.

The conventional H6-CSI using the SHEPWM method is first simulated. The power circuitry is established by PLECS Blockset, which can simulate the turn-on and turn-off process of the power switches. To simulate the behavior of the self-controlled low-speed switches while taking the actual capabilities of the simulation environment into account, the power switch S_1~S_6 are built with the "IGBT with Limited di/dt model", where the "rise time" and "fall time" are configured with 10 s of microsecond. Other parasitic parameters (such as the blocking voltage, stray inductance, on-resistance, *etc.*) are modeled after

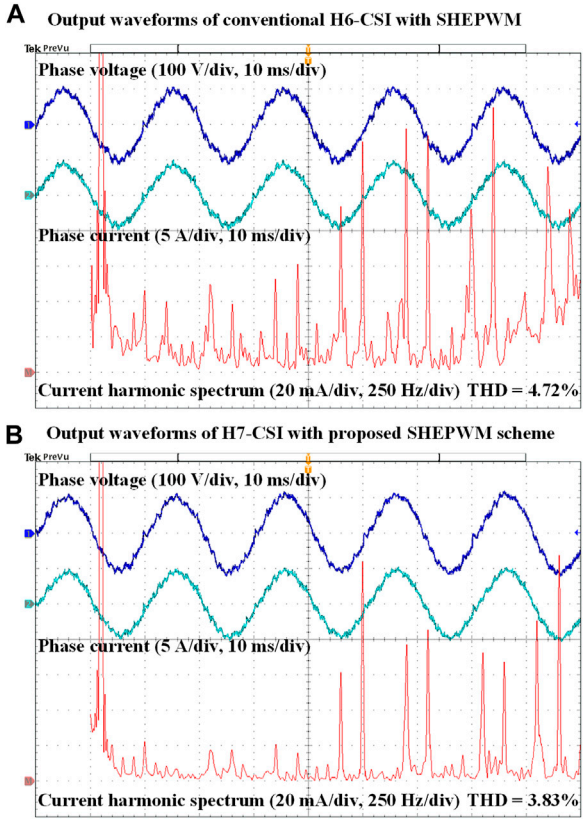

FIGURE 14
(A) Experimental output waveforms of conventional H6-CSI with SHEPWM, **(B)** Experimental output waveforms of conventional H7-CSI with SHEPWM.

the datasheet of typical low-speed switches. MATLAB is used to implement the driving-pulse sequences and analyze the output waveform.

Figure 7A shows the comparison of the output switched current i_a (before the filters) at N = 7. The upper and lower waveforms represent the actual and ideal switched currents, respectively. A zoomed view of the two waveforms during ($\pi/3$, $2\pi/3$) is demonstrated in Figure 7B. During this period, S_1 remains on state, and S_4 performs short-circuit pulses. As can been seen from the comparison, there exists a slight difference in the operating angles as well as the width of switching pulse. The same trend can also be found in Figure 8, which is the waveform comparison of the output switched current with N = 9. Therefore, the phenomenon of actual commutation difference caused by switching speed is reproduced.

Figures 9A,B shows the actual filtered output three phase currents and voltages of H6-CSI using the SHEPWM methods at N = 7 and N = 9, respectively. Figures 9C,D are the corresponding FFT analysis results. These simulation results show that with the increase of switching angles, the pulse sequences become denser. If the low switching speed is taken into account, the low-order harmonics will not be eliminated entirely, which has the high contents of 5^{th} and 7^{th} harmonics.

The following simulation are the verification of the proposed SHEPWM scheme based on H7-CSI method. The power circuitry of H7-CSI is also built in PLECS Blockset. Switch S_7 is set with a shorter turn-on and turn-off time than that of S_1~S_6. Taking N = 7 as an example, the output three-phase voltage and current after the capacitor filters are shown in Figure 10A. And the harmonics of the output current i_a are analyzed by FFT which is shown in Figure 10B. When N = 9, the filtered output waveforms and harmonic analysis of H7-CSI are shown in Figures 10C,D, respectively. The contents of low-order harmonics to be eliminated have been compared and listed in Table 3, which can give a clear view of the harmonic differences. Observing from Figure 10, it can be found that the low-order harmonic contents are almost zero. Compared with the THD value of 58.26% for conventional SHEPWM-H6-CSI with low-speed switches in Figure 9C and Figure 10C, the THD value of proposed SHEPWM based on H7-CSI is 57.59% with the proposed modulation method. These THD values are 58.20% and 57.44% in Figure 9D and Figure 10D, respectively. It is worth noting that low-order harmonics content of 5^{th} and 7^{th} decreased significantly. To sum up, the low-order harmonics that to be eliminated are significantly reduced with the proposed solution. Therefore, the output power quality has been improved.

4.2 Experimental verifications

To verify the performance of the proposed SHEPWM strategy with H7-CSI, an experimental prototype is established displayed in Figure 11. The parameter experimental settings are shown in Table 4. On the controller board, the gating sequences are programmed and implemented by an FPGA of xc3s500e from the family of XILINX Spartan3E. In the power circuitry, the DC inductor, the output capacitor filter and the output resistive loads are consistent with the simulation model. To perform the low switching speed of power switches, S_1-S_6 are selected with modular IGBTs (FF100R12RT4 from Infineon), and the driving resistance is set with 40 Ω S_7 is employed by a silicon carbide power MOSFET (C2M0040120D from Cree).

Figure 12 shows the experimental driving pulses of switches S_7, S_2, S_6 respectively. In Figure 12, the modulation state sequence is from {S_1, S_2}, *via* {S_7}, to {S_1, S_6}. As expected, S_2 and S_6 switch much slower than S_7. To be specific, the turn-on and turn-off time of S_2 and S_6 are nearly 3 μs, while the switching speed of S_7 is less than 200 ns.

Set N = 7 for experimental verification, the gating pulses of switches S_1, S_5, S_6 and S_7 for one period are captured as Figure 13. It is easy to find that the experimental sequences are consistent with the theoretical settings, which have been presented in Figure 6. And the commutation features conform to the description in Table 1.

To go a step further, an additional experimental prototype of conventional H6-CSI with the same hardware has also been carried out to test and compare the harmonic performance. The experimental phase voltage, phase current and the current harmonic spectrum of conventional SHEPWM-H6-CSI with low-speed switches are shown in Figure 14A. The filtered voltage and current waveforms are basically complete sinusoidal waves. The burrs are due to the characteristics of low-speed switching operation. From the spectrum analysis, it can be clearly seen that the output current contains many harmonic components, and the harmonics of 5^{th}, 7^{th}, 11^{th}, 13^{th} still remains a certain content.

By contrast, Figure 14B shows the experimental output waveforms of the proposed H7-CSI with SHEPWM. The inverter also outputs 50 Hz sinusoidal voltage and current. Although the waveforms are not significantly different from that of H6-CSI, spectral analysis shows that

the proposed SHEPWM strategy has less harmonic contents. The THD value of output current has decreased from 4.72% to 3.83%. And the low order harmonics (5^{th}, 7^{th}, 11^{th}, 13^{th}) have almost been eliminated successfully. Thus, the harmonic performance of CSI can be improved with the proposed method.

5 Conclusion

This paper reviews the SHEPWM technique of conventional H6-CSI and investigates the practical effect of low switching speed on the harmonic elimination. In order to enhance the performance of SHEPWM, an operation strategy based on H7-CSI with hybrid switches has been proposed. It utilizes one high-speed switch and six conventional low-speed switches, so that offers an easy and cost-efficient solution to improve the commutation speed of CSI, which can own better harmonic performance with even lower power loss. MATLAB with PLECS Blockset simulations and experimental prototype verify the effectiveness of the proposed method.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

WW and XX substantially contributed to the conception of the study, XM helped perform the analysis with constructive discussions, SR and YZ conducted supervision. All authors have read and agreed to the published version of the manuscript.

Conflict of interest

Author SR was employed by State Grid Shandong Electric Power Company.

The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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