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EDITED BY
Xin Ning,
Chinese Academy of Sciences, China

REVIEWED BY
Gabriel Gomes,
State University of Campinas, Brazil
Yao Liang,
City University of Hong Kong, Hong Kong, SAR China
Yassine Himeur,
Qatar University, Qatar

*CORRESPONDENCE
Shanshan Wang,
ryh513121837@outlook.com

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Study on the characteristic of the grounding fault on the cascaded midpoint side of the hybrid cascaded HVDC system

Yonghao Ren[1], Huadong Sun[2], Shanshan Wang[1]*, Bing Zhao[1], Shiyun Xu[1], Min Liu[1] and Panjie Lian[1]

[1]China Electric Power Research Institute Co. Ltd, Beijing, China, [2]State Key Laboratory of Power Grid Safety and Energy Conservation, Beijing, China

The hybrid cascaded high-voltage direct current (HVDC) system combines the system support capabilities of the modular multilevel converter (MMC) with the capacity of the line-mutated converter's (LCC's) advantage of high-power transmission. The HVDC system is among the key elements of a smart grid where artificial intelligence is applied extensively. However, the characteristics of a grounding fault on the cascaded midpoint side of a hybrid cascaded HVDC system remain unclear. This study analyzes fault characteristics and the impact of faults using analytical methods. First, the topology and basic control strategy are presented. The fault response process is then analyzed by dividing systems into the MMC and LCC parts at the inverter side. A separate theoretical analysis is also conducted. In addition, the impacts of faults on HVDC and alternating current (AC) networks are analyzed. Therefore, even after the HVDC system is disabled, the AC network can supply fault currents using an antiparallel diode. The simulation results show that the proposed analysis method is feasible, and the theoretical analysis is correct. The proposed method can provide a theoretical basis for the selection of equipment for HVDC systems and smart grid construction.

KEYWORDS

smart grid, artificial intelligence, hybrid cascaded HVDC system, cascaded midpoint fault, fault characteristics, Ac low voltage, fault response

1 Introduction

By examining and interpreting power grid data, artificial intelligence (AI) technology can enhance the intelligent management of power grids, thus reducing energy consumption and environmental pollution (Cai et al., 2022; Tang et al., 2022; Wu et al., 2023). The hybrid-cascaded high-voltage direct current (HVDC) transmission technique can effectively reduce power transmission losses, and a combination of the two can boost further the energy utilization efficiency and intelligence of the power grid (Tang et al., 2021; Dong et al., 2023; Liang et al., 2023). In China, the energy distribution is opposite with respect to the center, with bounteous renewable energy sources in the west and developed economies and high-energy demand in the east, and HVDC has numerous potential applications as an important means of large-scale energy transfer. Using the Yangtze Delta area in eastern China as an example, 12-circuit line-mutated converter-based HVDC (LCC-HVDC) landings are located in this area (Zhang et al., 2007). With the commissioning of multiple new LCC-HVDCs, the power grid strength in the Yangtze Delta area of China will be reduced further,

thus leading to an increased risk of commutation failure in LCC-HVDC and a gradual reduction in grid voltage stability, which in turn limits the scale of LCC-HVDC development (Shao and Tang, 2017). Following the rapid development of modular multilevel converter-based HVDC (MMC-HVDC) in recent years, the requirements for the recipient grid strength are low, and they have a certain fault ride-through capability; however, its rated voltage and transmission power are not as good as LCC-HVDC, and MMC-HVDC construction costs are higher compared with LCC-HVDC, thus limiting its application scale (Zhu et al., 2021; Saeedifard and Iravani, 2010; Swedesford et al., 2010). Therefore, hybrid HVDC technology, which considers the scale of the AC network as well as the system characteristics and combines the respective benefits of LCC-HVDC and MMC-HVDC, has become a novel technology used to solve the aforementioned problems and a major research focus in the field of HVDC.

The hybrid cascaded HVDC system forms a hybrid transport unit by the series–parallel connection of the LCC and MMCs. The various series–parallel connections of LCCs and MMCs and the location of the hybrid transport unit constitute different topologies of hybrid cascaded HVDC systems, which can be adapted for different applications (Zhao and Iravani, 1994; Torres-Olguin et al., 2012; Haleem et al., 2018). An HVDC system (with an LCC at the rectifier side) and multiple MMCs in parallel (with the LCC in series topology at the inverter side, which has superior DC fault ride-through capability), has been proposed, while the MMCs at the inverter side can provide a certain voltage support capability (Liu et al., 2018; Meng et al., 2021; Qahraman and Gole, 2005). The topology proposed above was used in the ±800 kV Baihetan–Jiangsu HVDC project in China, and the hybrid cascaded HVDC system based on this topology was also evaluated in this study. Related scholars have studied hybrid cascaded HVDC systems using this topology. A coordinated control strategy based on the dynamic limiter, diodes and LCC-MMC active orders is proposed was suggested to improve the AC side voltage stability (Zhao and Tao, 2021). A supplementary coupling mitigation control strategy was suggested to enhance the stability of a hybrid cascaded HVDC system connected to a weak grid (He et al., 2021). A suppression strategy based on fuzzy clustering and an identification method were proposed to repress the DC overcurrent caused by LCC commutation failure at the inverter side (Guo et al., 2021). When an alternating current (AC) short-line fault occurs in the MMC of the hybrid cascaded HVDC system, the imbalanced power between the AC and DC sides of the MMCs will cause capacitor charging of the submodule, which may lead to the blocking of the MMCs. To address the above problems, (Niu et al., 2020), analyzed the mechanism of the MMC submodule's overvoltage caused by an AC fault and proposed a fault-ride-through strategy based on the fast response of the DC current on the rectifier side. In addition, (Kang et al., 2022), presented a novel method to control the decrease of the adaptive DC voltage that can fully absorb imbalanced power. In the Baihetan–Jiangsu HVDC project in China, a controllable and adaptive energy absorption device was used to absorb surplus power from the DC side to increase the system transient stability (Liu et al., 2021). In addition, considering the MMC overcurrent in DC fault conditions, (Yang et al., 2019), proposed a recovery control strategy for the power regulation of a fixed-active-power MMC. Related studies that have been conducted for hybrid cascaded HVDC systems focused on the solution of the operational characteristics and fault ride-through problems when AC short-line faults occur.

Most previous studies on internal HVDC system faults were conducted on MMC-HVDC: when a short-circuit fault occurs in its DC line, the submodule capacitor discharge and other circumstances will cause a rapid fault-surge current; thus, a reasonable solution for the fault current is needed to provide a basis for the electric design of submodule components in MMC-HVDC (Wang et al., 2011; Wang et al., 2011). When a fault occurs in the DC line of a hybrid cascaded HVDC system, the inverter-side LCC uses its back-blocking characteristics to isolate the fault current fed from the inverter side to the fault point, thus greatly reducing the impact on the HVDC system (Li et al., 2022; Xu et al., 2022). The Comparison of existing contributions and this paper is shown in Table 1. Related studies that have been conducted for hybrid cascaded HVDC systems focused on the solution of the operational characteristics and fault ride-through problems when AC and DC line faults occur.

The topology of the hybrid cascaded HVDC system shows that the high- and low-end connection line parts of the cascaded side include an area with a negative outlet for the DC filter, a negative outlet for the bypass switch of the high-voltage valve, and a positive outlet for the parallel bus and bypass switch of the low-voltage valve. This area is unique to hybrid cascaded HVDC system by its topology and does not exist in LCC-HVDC and MMC-HVDC. Although the length of the line in this area is shorter than that of the DC line, there are numerous connection parts and the structure is more complex. The lines in this area are mostly arranged in the valve hall, and a general fault occurs, which is a permanent grounding fault. Therefore, it is necessary to carry out a detailed theoretical analysis of fault in this area. Based on the fault section and mode mentioned above, this study proposes a detailed theoretical analysis of the fault responses of the cascaded-side MMC and LCC, divides the fault current evolution process into two steps before and after blocking, and proposes a mathematical calculation method for the fault current. Using an advanced digital power system simulator (ADPSS) as a base, an electromechanical–electromagnetic transient hybrid simulation with a hybrid cascaded HVDC system model was constructed (Tian et al., 2016), and the precision of the theoretical calculation was confirmed based on simulation experiments. Based on the simulation results, the dynamic characteristics of the receiving-end system in fault conditions were analyzed to provide a theoretical basis for equipment selection and power system planning of the hybrid cascaded HVDC system. The conclusions of this study provide important support for the construction of smart grids.

2 Hybrid cascaded HVDC system topology and steady-state control strategy

2.1 System topology

The hybrid cascaded HVDC system adopts a symmetrical wiring form for the positive and negative poles with symmetrical positive and negative structures and consistent parameters; the monopole topology is shown in Figure 1. In Figure 1, U_{dr} and U_{di} are the rectifier- and inverter-side DC voltages, U_{diL} and U_{diM} are the high- and low-end DC voltages of the high- and low-end voltages at the inverter side,

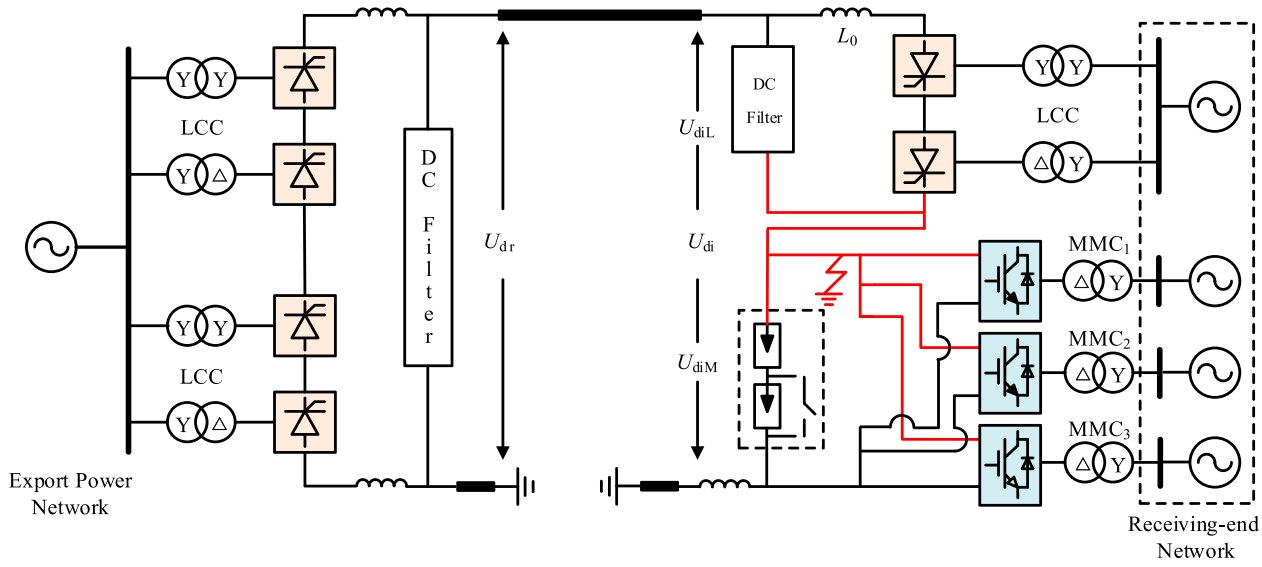

FIGURE 1
Single-pole structure of the hybrid-cascaded high-voltage direct current (HVDC) system.

TABLE 1 Comparison of existing contributions.

Object	AC fault	DC line fault	Cascaded side fault
Guo et al. (2021)	√		
Zhao and Tao (2021)	√		
Kang et al. (2022)	√		
Yang et al. (2019)	√		
Xu et al. (2022)		√	
Li et al. (2021)		√	
This paper			√

respectively; and L_0 is the smoothing reactor. The rectifier side is composed of two groups of 12-pulse LCCs in series, and the inverter side is composed of LCC and MMCs in series, where the high-voltage valve comprises one group of 12-pulse LCC and the low-voltage valve three parallel MMCs; these three parallel MMCs all adopt half-bridge structures, and the inverter side LCC and each parallel MMCs are associated with different buses of the equal AC network.

Meanwhile, to reduce the discharge current induced by a DC line short-circuit defect and to reduce the system's harmonic current, the HVDC system adopts the symmetrical arrangement principle of the pole and neutral lines and sets L_0 on the rectifier and inverter sides, respectively. Table 2 lists the primary parameters of the HVDC system.

2.2 System control strategy

The methods for both the positive and negative controls were the same in the hybrid cascaded HVDC system. A voltage-dependent current-order limiter (VDCOL), minimum trigger angle control, and constant DC current control were configured on the LCC at the rectifier side (Mao et al., 2021). Based on constant DC voltage control, the LCC on the inverter side is configured with a VDCOL, and it uses constant extinction angle and constant current control as standby controls. The corresponding control structure and switching principle are illustrated in Figure 2A. In Figure 2A, UdiLref and UdiL are the reference and instruction values of the DC voltage at the inverter side, respectively, Idcref and Idcf are the reference and instruction values of the DC current of the HVDC system, respectively, and γmin and γ are the reference and instruction values of the extinction angle at the inverter side, respectively.

The parallel MMCs on the inverter side use a DQ axis-based DC vector control approach, which has two control dimensions: one for active control, similar to controlling the active power or DC voltage, and the other for reactive control, similar to controlling the AC bus voltage or reactive power (Saeedifard and Iravani, 2010; Debnath et al., 2014). To guarantee the system's voltage stability, one of the three parallel MMCs which cooperates with the MMC at the inverter side is selected to adopt constant DC voltage control mode, the other MMCs adopt the control mode of constant active power, and Figure 2B displays the equivalent control block diagram. After determining the control strategies for the rectifier and inverter sides of the hybrid cascaded HVDC system, the static I–V characteristic curve can be obtained, as illustrated in Figure 3. The characteristics of the rectifier side consist of 1, 2, and 3 segments; among these, segment 1 is the minimum trigger angle control characteristic; usually, the minimum value of trigger angle α is taken as 5°; segment 2 is the constant DC current control characteristic, which is also the normal operational characteristic; and segment 3 is the control characteristic of the VDCOL because the low end of the inverter side is the MMC converter, its DC voltage retention

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TABLE 2 Main parameters of the hybrid-cascaded high-voltage direct current (HVDC) system.

Object	Parameters	Values
HVDC system	DC voltage	800 kV
	DC Current	5 kA
	DC power (bipolar)	8000 MW
	Flat wave reactor	150 mH
	Grounding pole line resistance	2.17 Ω
	Grounding pole line inductance	68.5 mH
Line-mutated converter (LCC) converter transformer at rectifier side	Variable ratio	525 kV/172.3 kV
	Rated capacity	1218 MVA
	Short circuit voltage percentage	23%
LCC converter transformer at the inverter side	Variable ratio	510 kV/161.4 kV
	Rated capacity	1141 MVA
	Short circuit voltage percentage	18%
Modular multilevel converter (MMCs) at the inverter side	Rated DC power	1000 MW
	Number of sub-modules	200 + 24
	Bridge Arm Inductors	50 mH
	Sub-module capacitance	18 mF
MMCs converter transformer at the inverter side	Variable ratio	510 kV/182.6 kV
	Rated capacity	1125 MVA
	Short circuit voltage percentage	15%

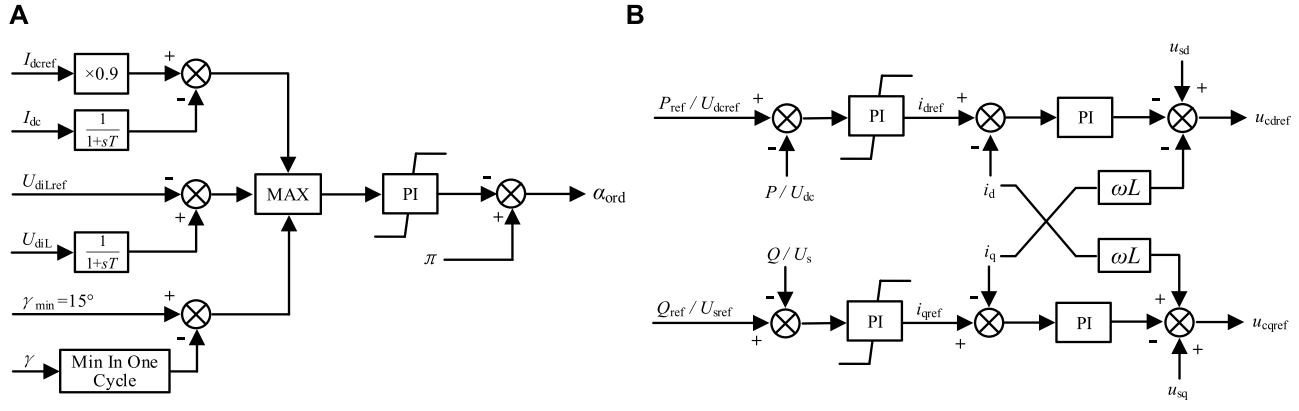

FIGURE 2
Control block diagram. **(A)** Line-mutated converter (LCC) at the inverter side; **(B)** modular multilevel converter (MMC) at the inverter side.

characteristics are better, which limits the reduction of the rectifier side voltage. The characteristics of the inverter side are composed of four, five, six, and seven segments; among these, four segments are constant extinction angle control characteristics, with γ set to 15°; five segments are constant DC voltage control characteristics, which are also normal operating characteristics; and six segments are constant DC current control characteristics. To ensure that the DC current control on the inverter side is inoperative during steady-state operation, its current setting value should be lower than the rectifier-side control setting value. Segment 7 is the control characteristic of the VDCOL. In normal conditions, the HVDC system operates at the black point as shown in Figure 3.

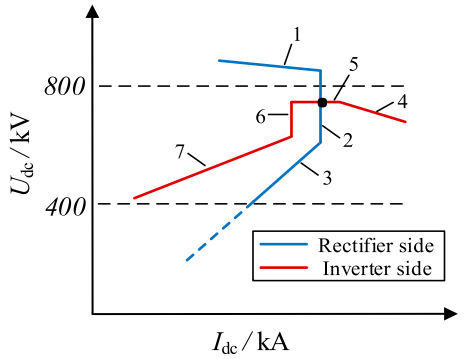

FIGURE 3
Static I–V characteristic of HVDC system.

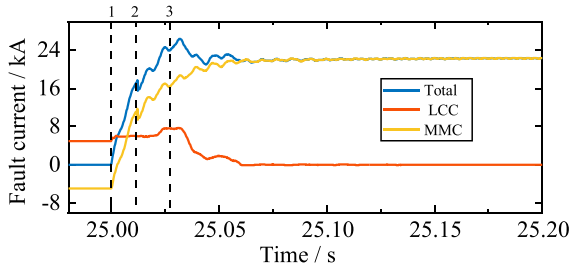

FIGURE 4
Fault current of HVDC system.

3 Failure mechanism

The fault area in the fault conditions described above is shown in Figure 1, and is mostly arranged in the valve hall; therefore, the general occurrence tends to be a permanent ground fault.

In this study, we built a hybrid simulation model containing a hybrid cascaded HVDC system, including an actual control protection program of the HVDC system. The fault current was obtained, as illustrated in Figure 4, and was based on the model used to simulate the fault in this area.

Among them, the actions that play a major role in the transformation of the fault current evolution process include the following.

- Occurrence of failure
- Approximately 10 ms after the failure occurs, MMCs at the inverter side are blocked
- Approximately 40 ms after the failure occurs, the LCC at the rectifier side is forced to undergo a phase shift

From the topology of the hybrid cascaded HVDC system, it is known that after a permanent ground fault occurs in this area, the fault currents originate from the LCC and each parallel MMCs on the inverter side, and are defined as I_{dcL} and I_{dcM}, respectively. When the system operates in the steady state, I_{dcL} and I_{dcM} are equal. Owing to the manufacturing level, the insulated-gate bipolar transistor (IGBT) and capacitor, which are important components of the MMC submodule, have high costs and weak overcurrent capabilities. Before the MMC is blocked, the IGBT and capacitor have to withstand overcurrents at specific levels; once the IGBT or capacitor are damaged by the overcurrent problem, it will affect the equipment's life and may endanger the system's ability to run securely and consistently (Ni et al., 2020). Meanwhile, although the thyristor used in LCC has enhanced overvoltage and overcurrent capabilities, the contact between the HVDC system and the receiving-end system changes significantly during the transient process after a failure occurs (Aik and Andersson, 2018). A theoretical examination of the fault current and system impact in this fault situation is necessary because the power flow of the receiving-end system after a failure differs significantly from that before the failure.

4 Fault current theory analysis of MMCs side

Each parallel MMCs on the inverter side is in normal operation, and there are 2N submodules in the upper and lower bridge arms among which a total of N submodules are in the bypass state, whereas N more submodules are in the input state. It is essentially a time-varying circuit, but during the transient process after a failure occurs, the DC voltage of the MMCs does not increase suddenly; therefore, it can be assumed that each phase's input of the submodules will always have the same number, that is, the equivalent capacitance of any phase is constant. MMCs can be considered linear circuits during this time and can be analyzed using the superposition theorem.

4.1 State before MMCs are blocked

During fault response analysis, the fault current is the sum of three parallel MMC fault currents. The MMCs have the same primary parameters on both sides and are connected to different nodes in the same AC network. The voltage amplitude and phase angle of each MMC are approximately the same. To facilitate the calculations, we assumed that the voltage amplitudes and phase angles of the three parallel MMCs were identical. Taking MMC1 as an example to begin the analysis, the time-domain model is shown in Figure 5.

The complicated frequency-domain model of MMC1, shown in Figure 5, transforms the time-domain model into an arithmetic circuit model, as shown in Figure 6A, where the impedances of the grounding electrode line and smoothing reactor L0 were unified and combined as Rg + jwLg. The excitation sources are shown in Figure 6A were separated as follows.

- DC side excitation source
- AC side excitation source

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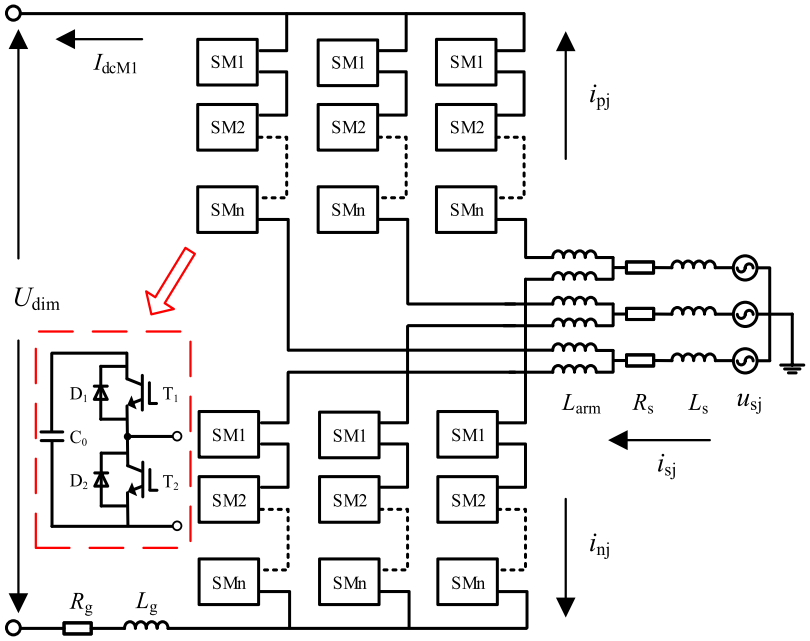

FIGURE 5
Time domain model of MMC1.

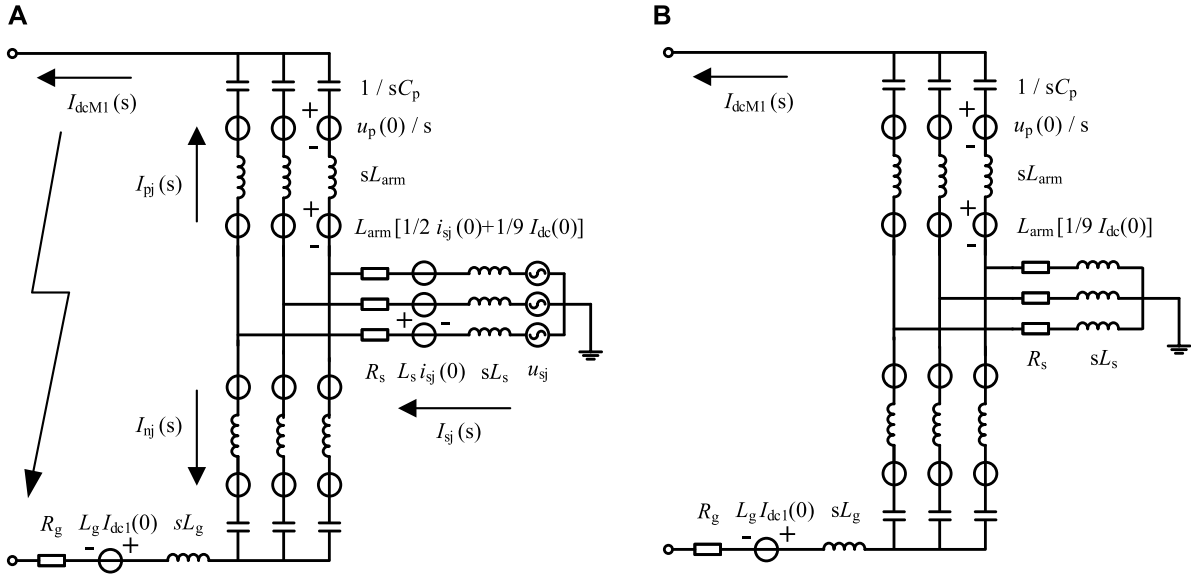

FIGURE 6
(A) Complex frequency domain model of MMC1; **(B)** response circuit of DC excitation source.

The fault current on the MMC_1 side is the outcome of the synergistic work of the two types of excitation sources described above. Therefore, the two types of excitation sources above were decomposed, the response of each group of excitation sources (acting separately) was calculated according to the principle of the superposition theorem, and the total response of the MMC_1 circuit was obtained by summing them.

4.1.1 Response of DC side excitation source

The excitation source for this part of the response circuit consists of three parts: all-submodule capacitors, the excitation source matching the initial value of I_{dc} in the bridge arm reactor, and the source of excitation for the starting value of the current in the smoothing reactor. The DC-side excitation-source response circuit is shown in Figure 6B.

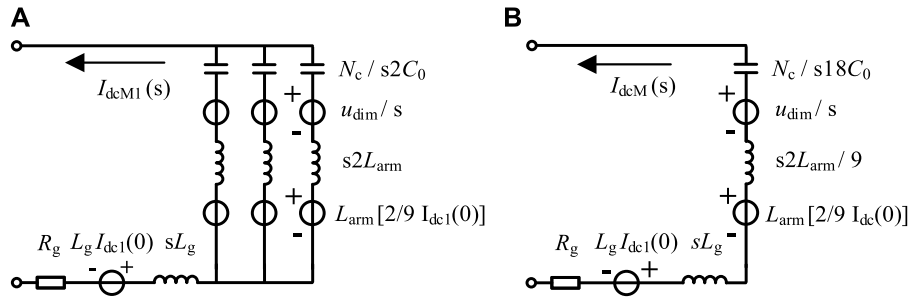

FIGURE 7
Simplified circuit of the DC side excitation source. **(A)** MMC1; **(B)** three parallel MMCs.

To solve this part of the excitation source response, the following simplifications were made.

- In this part of the response, there is no excitation source in the three-phase symmetric AC network. Therefore, the role of the AC network can be disregarded when analyzing the DC line's current
- Each submodule can be considered to have the same capacitance voltage Uc based on the principle of constant-capacitance storage in each submodule. The equivalent capacitance of each phase bridge arm Ceq is expressed as follows,

$$\frac{1}{2}C_{eq}U_{dim}^2 = 2N_c\frac{1}{2}C_0U_c^2 \tag{1}$$

Additionally, considering that $U_{diM} = N_cU_c$, it is obtained that

$$C_{eq} = \frac{2}{N_c}C_0 \tag{2}$$

Based on the simplification principle above, the DC-side excitation source circuit of MMC_1 can be simplified as follows,

As the major part of the circuit is a parallel connection of nine phase units and the lower end of the inverter side is linked in parallel with three groups of MMCs, the circuit of this part may be simplified, as shown in Figure 7B. By solving this simplified circuit, the fault current of the MMCs subject to the response of the excitation source in the complex frequency domain is obtained as follows,

$$I_{dcM}(s) = \frac{s\left(L_g + 2L_{arm}/9\right)I_{dc}(0) + U_{dim}}{s^2\left(L_g + 2L_{arm}/9\right) + sR_g + N_c/18C_0} \tag{3}$$

The fault current I_{dcm}(t) is obtained by substituting the specific parameters of the HVDC system and the system state quantities into the $I_{dcM}(s)$ expression and performing the inverse Laplace transform. In addition, because of the symmetry of each phase unit, $I_{dcm}(t)$ is spread equally throughout the phase units, and the current flowing in each bridge arm is $I_{dcm}(t)/9$.

$$I_{dcM}(t) = -\frac{1}{\sin\theta_1}i_{dc}(0)e^{-\frac{t}{\tau_1}}\sin(\omega_1 t - \theta_1) + \frac{U_{dc}}{R_1}e^{-\frac{t}{\tau_1}}\sin(\omega_1 t) \tag{4}$$

where τ_1 is the time constant of the current decay, ω_1 is the resonant frequency, and θ_1 is the initial phase angle. These parameters are determined by the system parameters.

$$\tau_1 = \frac{4L_{arm} + 18L_g}{9R_g}, \omega_1 = \sqrt{\frac{2N\left(2L_{arm} + 9L_g\right) - 81C_0R_g^2}{C_0\left(4L_{arm} + 18L_g\right)^2}} \tag{5}$$

$$R_1 = \sqrt{\frac{2N\left(2L_{arm} + 9L_g\right) - 81C_0R_g^2}{324C_0}}, \theta_1 = \arctan(\tau_1\omega_1) \tag{6}$$

4.1.2 Response of AC side excitation source

The excitation source for this section of the response circuit consisted of an AC network equivalent power supply, an excitation source allied with the initial value of the inductor current, and an excitation source allied with the initial value of the AC current in the bridge arm reactor. The response circuit is shown in Figure 8A.

Because the equivalent power supply of the AC network and the entire circuit configuration are three-phase symmetric, no current enters the DC line from the AC side. The response circuit was simplified according to this principle, as shown in Figure 8B.

Each bridge arm in each phase carries half of the current on the AC side. When phase A of the upper bridge arm of MMC_1 is used for analysis, the expression of the equivalent source of phase A is assumed to be $u_{sa}(t) = E \sin(\omega_0 t)$. The upper bridge arm's response expression is,

$$i_{pa2}(t) = \frac{1}{2}I_{m2}\sin(\omega_0 t - \varphi_2) + \frac{1}{2}i_{sa}(0)e^{-\frac{t}{\tau_2}} \tag{7}$$

Among them

$$I_{m2} = \frac{E}{\sqrt{R_s^2 + \omega^2\left(L_s + L_{arm}/2\right)^2}}, \varphi_2 = \arctan\frac{\omega\left(L_s + L_{arm}/2\right)}{R_s}, \quad \tau_2 = \frac{L_s + L_{arm}/2}{R_s} \tag{8}$$

In summary, the total response process of the MMCs before blockage can be obtained. It is evident from the above study that the fault current on the MMCs side is related only to the DC-side excitation source response. The response process is described in (4), (5), (6). From the calculation of ω_1, it is evident that the fault current

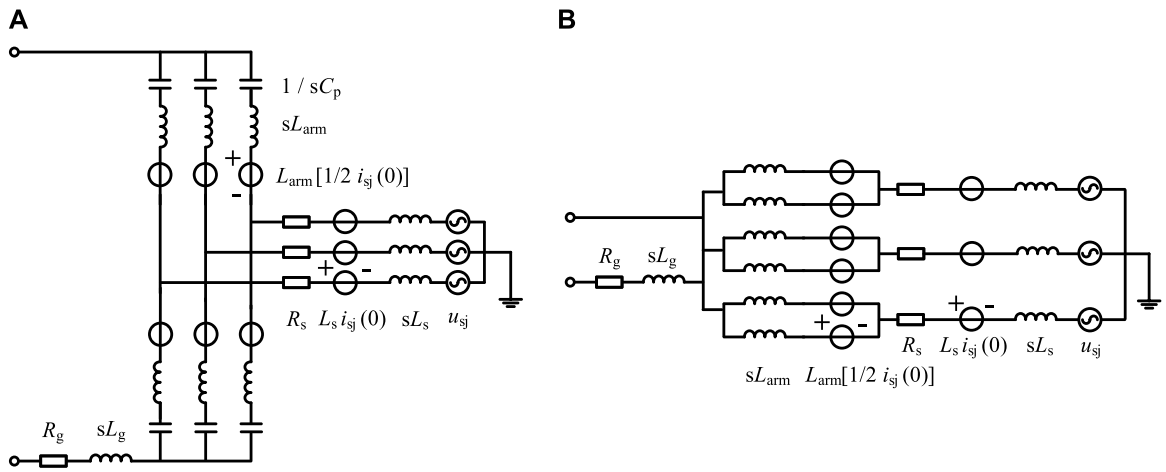

FIGURE 8
Circuit of the AC excitation source. **(A)** Response circuit and **(B)** simplified circuit.

reaches a peak approximately 17 ms after a failure occurs. However, the MMCs were prompted to block approximately 10 ms after failure; therefore, the fault current before blocking increased monotonically. The fault current calculated by (4) was 11.7 kA at 10 ms after failure occurred and matches the simulation results in Figure 4.

4.2 State after MMCs are blocked

In a hybrid cascaded HVDC system, three parallel MMCs transmit power to the DC side. Using the present direction of Figure 5 as an illustration, there exists a DC bias with a value of 1/9 I_{dcM} for each phase of the upper bridge arm current i_{pj} and a DC bias with a value of −1/9 I_{dcM} for each phase of the lower bridge arm current i_{nj}. Before the MMC is triggered to block, the fault current at the MMCs and the bridge arm current of each phase mainly originate from the DC-side excitation source response. The rate of change of this current is extremely fast, which makes the I_{dcM} change from negative to positive within milliseconds, while the reversal process of I_{dcM} also delays the time for the fault current to reach its peak to a certain extent. After the MMCs were blocked, the flow path and pattern of the fault current changed. It is also an important part of the complete response of the HVDC system after the failure occurs. The following is an example of MMC_1 for fault current change characteristic analysis after blocking.

As shown from the topology, each submodule of MMC_1 uses the half-bridge topology. After the blocking command is issued, each submodule is in a blocking state, and there are two operation modes in this state due to the renewal of the antiparallel diodes D_1 and D_2 in each submodule. In the first operation mode, D_1 is on and current passes through D_1 to charge the capacitor. In the second mode of operation, D_2 is turned on, and the current passes through D_2 to bypass the capacitor.

Because the sum voltage of the capacitors on each bridge arm in MMC_1 is greater than the AC voltage amplitude, each submodule operates as illustrated in Figure 9B. Before the bridge-arm current reaches zero, the antiparallel diodes of the upper and lower bridge arms operate in the conducting state, and the single-phase conductivity of the antiparallel diodes is not considered.

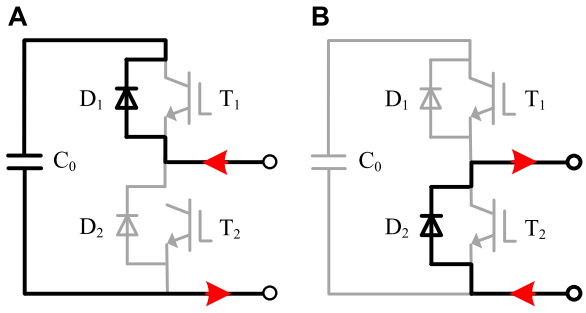

FIGURE 9
Operation mode of MMCs in the blocking state. **(A)** Charging and **(B)** bypassing the capacitor.

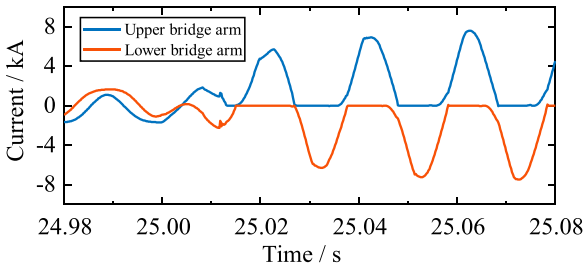

FIGURE 10
Bridge arm current of MMC1.

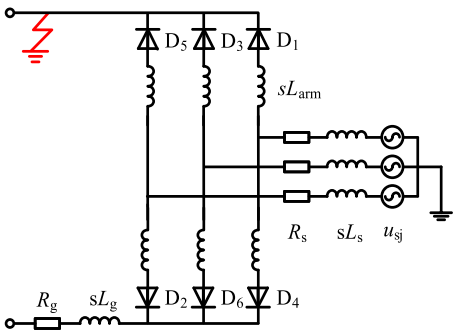

FIGURE 11
Response circuit after MMC1 is blocked.

Compared with MMC_1 before blocking, the DC-side excitation source response changed into a persistent current circuit in the bridge arm reactor. The remaining two excitation source circuits remained unchanged, and the three excitation source responses were superimposed to produce the bridge arm current. Figure 10.

After this part of the current decays to zero for the first time, the antiparallel diode cannot operate. The upper and lower bridge arm currents are switched from a two-way flow to a one-way flow limited by the antiparallel diode; at this time, the three-phase uncontrolled rectifier circuit begins its steady-state operation phase.

In a three-phase uncontrolled rectifier circuit, the conduction instant of the antiparallel diode on each phase bridge arm is the intersection of the phase voltage of that phase with that of the adjacent phase (i.e., the natural phase-change point). In the steady-state operation phase after MMC_1 is blocked, any phase bridge arm midpoint voltage is greater than zero because of the MMC_1 fault ground at the high-tension side, and the phase on the bridge arm's antiparallel diode meets the conduction conditions; thus, the upper bridge arm conducts. In addition, if the midway voltage of the bridge arm of the phase changes from positive to negative, the antiparallel diode will not immediately arc out owing to the current-continuing bridge arm reactor but will continue to conduct for a while and then turn off.

Define θ_{arm} as the angle of continuous conduction of each bridge arm. Based on the above analysis, $\theta_{arm} > \pi$; additionally, define the sum of the inductance of each phase bridge arm in the uncontrolled rectifier as L_{sum}. It is known from Figure 11 that $L_{sum} = L_{arm} + L_s$. Owing to the different ratios of R_g to L_{arm}, the θ_{arm} values are different (Li et al., 2016); this leads to different operating response characteristics. When $R_g/L_{sum} > 100$, $\pi \le \theta_{arm} < 4\pi/3$, and the operating response is alternating between three and four bridge arm conduction. When $R_g/L_{sum} \le 100$, $\theta_{arm} \ge 4\pi/3$, and the operating response is alternating between four and five bridge arms conduction. According to the calculation of the parameters of the HVDC system, R_g/L_{sum} is much less than 100; therefore, the steady-state operating response characteristics of MMC_1 after blocking are based on alternate switch-on operations of four and five bridge arms, and the angle of continuous conduction of each bridge arm can be found as follows,

$$\theta_{arm} = \arcsin\left[\frac{3\omega_0 L_{sum}}{\sqrt{\left(5.2\omega_0 L_{sum} + 27.3R_g\right)^2 + 3\omega_0 L_{sum} + 28.2R_g}}\right] - \arctan\left(\frac{3\omega_0 L_{sum} + 28.2R_g}{5.2\omega_0 L_{sum} + 27.3R_g}\right) + \frac{5\pi}{3} \tag{9}$$

Utilizing the antiparallel diode D_1's conduction as the starting point, the analytic expression for the current in one power frequency period was analyzed. The steady-state circuit after the MMC is blocked, as shown in the figure, and always conducts and opens according to the conduction sequence D_1-D_2-D_3-D_4-D_5-D_6-D_1. Before D_1 was set, D_3, D_4, D_5 and D_6 were tested. According to the circuit analysis, this period satisfies the following expression,

$$u_{dc}(t) = u_{sa} - L_{sum}\frac{di_{pa}}{dt} - u_{sb} + L_{sum}\frac{di_{nb}}{dt} = L_{sum}\frac{di_{pa}}{dt} + L_{sum}\frac{di_{na}}{dt} = u_{sb} - L_{sum}\frac{di_{pb}}{dt} - u_{sa} + L_{sum}\frac{di_{na}}{dt} = L_{sum}\frac{di_{pb}}{dt} + L_{sum}\frac{di_{nb}}{dt} = u_{sc} - L_0\frac{di_{pc}}{dt} - u_{sa} + L_0\frac{di_{na}}{dt} = u_{sc} - L_0\frac{di_{pc}}{dt} - u_{sb} + L_0\frac{di_{nb}}{dt} \tag{10}$$

Meanwhile, according to Kirchhoff's current law, it is obtained that

$$\frac{d(i_{pa} + i_{pb} + i_{pc})}{dt} = -\frac{d(i_{na} + i_{nb})}{dt} = \frac{di_{dc}}{dt} = 0 \tag{11}$$

Substitution of (11) into (10) yields,

$$\begin{cases} L_{sum}\dfrac{di_{pa}}{dt} = u_{sb} - u_{sc} \\ L_{sum}\dfrac{di_{pb}}{dt} = u_{sc} - u_{sa} \\ L_{sum}\dfrac{di_{pc}}{dt} = u_{sa} - u_{sb} \end{cases} \tag{12}$$

LLet the phase A equivalent source expression be $u_{sa}(t) = E\sin(\omega_0 t)$. Then, when $\omega_0 t = 0$, it satisfies $i_{pa} = 0$. By substituting this initial condition, the phase-A upper bridge arm current under this conduction condition can be obtained as follows,

$$i_{pa}(t) = \frac{E}{\omega_0 L_{sum}} - \frac{E}{\omega_0 L_{sum}}\cos(\omega_0 t) \tag{13}$$

Thereafter, the operating response of the bridge arm current is defined by the alternative operation of the four- and five-bridge arm conductions; thus, the above analysis method can be used to solve all conduction conditions to obtain an analytical expression for the current in one power frequency period as follows,

$$i_{pa}(t) = \begin{cases} -\dfrac{E}{\omega_0 L_{sum}}\cos(\omega_0 t) + \dfrac{E}{\omega_0 L_{sum}} & 0 \le \omega_0 t \le \theta - \dfrac{4\pi}{3} \\ -\dfrac{0.866E}{\omega_0 L_{sum}}\cos\left(\omega_0 t - \dfrac{\pi}{6}\right) + \dfrac{E}{\omega_0 L_{sum}} - \dfrac{E}{2\omega_0 L_{sum}}\sin\left(\theta - \dfrac{\pi}{2}\right) & \theta - \dfrac{4\pi}{3} \le \omega_0 t \le \theta - \pi \\ -\dfrac{1.732E}{2\omega_0 L_{sum}}\sin(\omega_0 t) + \dfrac{E}{\omega_0 L_{sum}} + \dfrac{\sqrt{7}E}{2\omega_0 L_{sum}}\sin\left(\theta - \dfrac{25\pi}{18}\right) & \theta - \pi \le \omega_0 t \le \dfrac{2\pi}{3} \\ -\dfrac{E}{\omega_0 L_{sum}}\cos(\omega_0 t) - \dfrac{E}{4\omega_0 L_{sum}} + \dfrac{\sqrt{7}E}{2\omega_0 L_{sum}}\sin\left(\theta - \dfrac{25\pi}{18}\right) & \dfrac{2\pi}{3} \le \omega_0 t \le \theta - \dfrac{2\pi}{3} \\ -\dfrac{\sqrt{3}E}{2\omega_0 L_{sum}}\cos\left(\omega_0 t + \dfrac{\pi}{6}\right) - \dfrac{E}{4\omega_0 L_{sum}} + \dfrac{1.803E}{\omega_0 L_{sum}}\sin(\theta - 4.468) & \theta - \dfrac{2\pi}{3} \le \omega_0 t \le \dfrac{4\pi}{3} \\ -\dfrac{E}{\omega_0 L_{sum}}\cos(\omega_0 t) - \dfrac{3E}{4\omega_0 L_{sum}} + \dfrac{1.803E}{\omega_0 L_{sum}}\sin(\theta - 4.468) & \dfrac{4\pi}{3} \le \omega_0 t \le \theta \\ 0 & \theta \le \omega_0 t \le 2\pi \end{cases} \tag{14}$$

Based on the operating response characteristics of the different stages after MMC_1 is blocked and the conduction of each bridge arm, the fault current of MMC_1 can be determined as follows,

$$I_{\mathrm{dcMMC1}} = \frac{3.12E}{\omega_0 L_{\mathrm{sum}}} \sin(\theta - 4.64) \tag{15}$$

In conclusion, it was possible to determine MMC_1's steady-state operational response properties. The angle of continuous conduction of each bridge arm was calculated to be equal to 280° by (9), MMC_1 fault current was calculated to be 7.87 kA using (15), and the fault current I_{dcM} provided by each parallel MMCs was 23.6 kA, which coincides with the simulation results in Figure 5.

5 Fault current theory analysis of LCC side

From the topology of the HVDC system, the LCC fault current I_{dcL} is equal to I_{dc} and is expressed as

$$R_{\mathrm{line}} I_{\mathrm{dc}} + L_{\mathrm{line}} \frac{\mathrm{d}I_{\mathrm{dc}}}{\mathrm{d}t} = U_{\mathrm{dr}} - U_{\mathrm{di}} = \Delta U_{\mathrm{d}}(t) \tag{16}$$

where U_{dr} and U_{di} are the DC voltages within L_0 on the rectifier and inverter sides, and R_{line} and L_{line} are the DC line impedances, respectively. The differential term in (16) is zero during the steady-state operation; therefore, I_{dc} is related only to the difference between U_{dr} and U_{di}. The differential term is not zero after a failure occurs, and its solution is obtained as follows,

$$I_{\mathrm{dc}} = \mathrm{e}^{-\frac{t}{\tau_{\mathrm{L}}}} \left[\int \frac{\Delta U_{\mathrm{d}}(t)}{L} \mathrm{e}^{\frac{t}{\tau_{\mathrm{L}}}} \mathrm{d}t + C \right] \tag{17}$$

where $\tau_{\mathrm{L}} = L_{\mathrm{dc}}/R_{\mathrm{dc}}$. Expanding for U_{di}, we obtain

$$\begin{aligned} U_{\mathrm{di}} &= L_0 \frac{\mathrm{d}I_{\mathrm{dc}}}{\mathrm{d}t} + U_{\mathrm{diL}} + U_{\mathrm{diM}} \\ &= L_0 \frac{\mathrm{d}I_{\mathrm{dc}}}{\mathrm{d}t} + N_{\mathrm{i}} \left(1.35 \frac{U_{\mathrm{sL}}}{k_{\mathrm{L}}} \cos\beta + \frac{3}{\pi} X_{\mathrm{sL}} I_{\mathrm{dc}} \right) + U_{\mathrm{diM}} \end{aligned} \tag{18}$$

where N_{i} is the number of 6-pulse LCC converters in each pole, U_{sL} is the LCC bus line voltage at the inverter side, k_{rL} and X_{sL} are the LCC converter transformer ratio and leakage resistance at the inverter side, respectively, and β is the advanced LCC trigger angle of the inverter side.

After a failure occurs, the system's triggers a blocking fault-pole strategy. Meanwhile, the pole control system sends a blocking command to each valve control system running the LCC after receiving the pole-blocking command from the station or the opposite station. During this process, the LCC on the rectifier side is forced to shift the phase to accelerate the fault current decay. Therefore, the LCC-side fault response is also discussed in two phases: before and after the forced phase shift of the LCC on the rectifier side.

5.1 State before forced phase shift

When the AC voltage at the inverter side is lowered, a constant extinction angle control is utilized to lower the possibility of commutation failure. Constant current control is employed to keep the I_{dc} flowing when the rectifier side experiences a defect and to speed up power recovery after a failure has occurred. During steady-state operation, U_{diL} and U_{diM} were both 400 kV, U_{di} was approximately 800 kV, and γ_{iL} was greater than 15°. The output signal of the constant extinction angle control was negative, and the output signal of the constant DC voltage control was zero; therefore, the constant extinction angle control did not operate.

After the fault occurred, U_{di} decreased to ~400 kV. Eq. 17 shows that a significant decrease in U_{di} after a failure leads to an increase in I_{dc}. From the commutation principle of the LCC, it is known that there is a relationship between μ_{iL}, γ_{iL}, and β_{iL},

$$\begin{aligned} \mu_{\mathrm{iL}} &= \arccos\left[\cos\gamma_{\mathrm{iL}} - \frac{6X_{\mathrm{sL}} I_{\mathrm{dc}}}{1.35\pi U_{\mathrm{sL}}/k_{\mathrm{L}}} \right] - \gamma_{\mathrm{iL}}, \gamma_{\mathrm{iL}} \\ &= \arccos\left[\frac{U_{\mathrm{diL}} + 3X_{\mathrm{sL}} I_{\mathrm{dc}}/\pi}{1.35 U_{\mathrm{sL}}} \right], \beta_{\mathrm{iL}} = \gamma_{\mathrm{iL}} + \mu_{\mathrm{iL}} \end{aligned} \tag{19}$$

The increase in I_{dc} causes μ_{iL} to increase and γ_{iL} to decrease, thus resulting in a) the output <0 in the constant DC voltage control side, b) an output signal of the constant extinction angle control side <0, and c) the LCC at the inverter side moving to constant extinction angle control. Simultaneously, when $\gamma_{\mathrm{iL}} < \gamma_{\mathrm{min}}$, the LCC on the inverter side induces a commutation failure. The LCC extinction angle on the inverter side during a fault is shown in Figure 12A.

Unlike general AC system faults at the inverter side, which cause commutation failure induced by voltage dips at the commutation bus, the same problem of commutation failure is induced at the internal fault conditions of the HVDC system. However, the essence is that the increase of I_{dc} causes the increase of the μ_{iL} and the decrease of t γ_{iL}, thus resulting in γ_{iL} values < γ_{min}.

5.2 State after the forced phase shift

After receiving the pole blocking command, the LCC system adopts the forced phase shift strategy to reduce U_{dr} to a negative value so that the HVDC system's energy can be promptly transferred back to the AC system. This helps I_{dcL} decay to zero quickly. During the initial stage, after the forced phase shift of the LCC at the rectifier side, the trigger angle increased to 120° instead of 165° to avoid commutation failure induced by small phase-change angles after entering the inverted state. When I_{dc} was detected to be lower than 0.05 p. u., after a time delay, the LCC triggered phase-shift locking.

6 Characterization of the AC network at the receiving end

After failure occurs, it is clear from the above analysis that U_{dr} reduces to a negative value during the blocking process through a forced phase-shift strategy, which helps I_{dcL} decay to zero quickly, thus ensuring that the LCCs on the rectifier and inverter sides are reliably blocked and have no power interaction with the AC side after blocking. Figure 13.

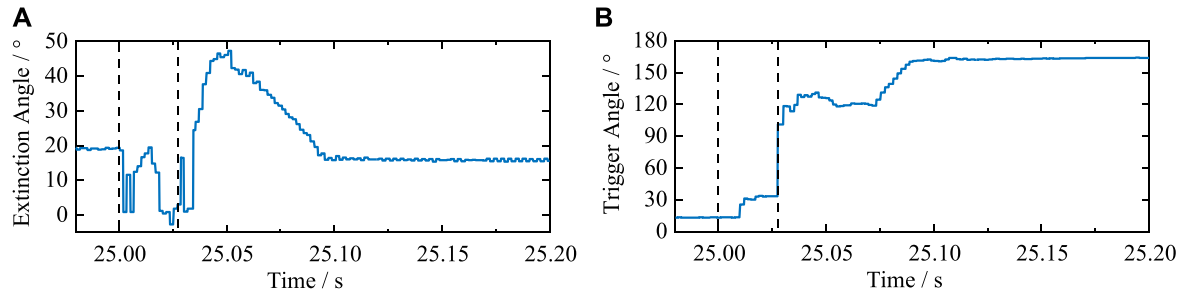

FIGURE 12
(A) LCC extinction angle at the inverter side; **(B)** LCC trigger angle at the rectifier side.

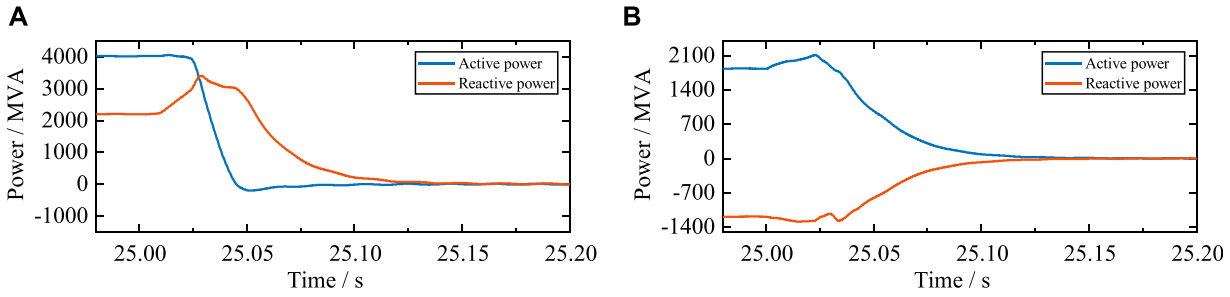

FIGURE 13
(A) Total power and **(B)** LCC power responses.

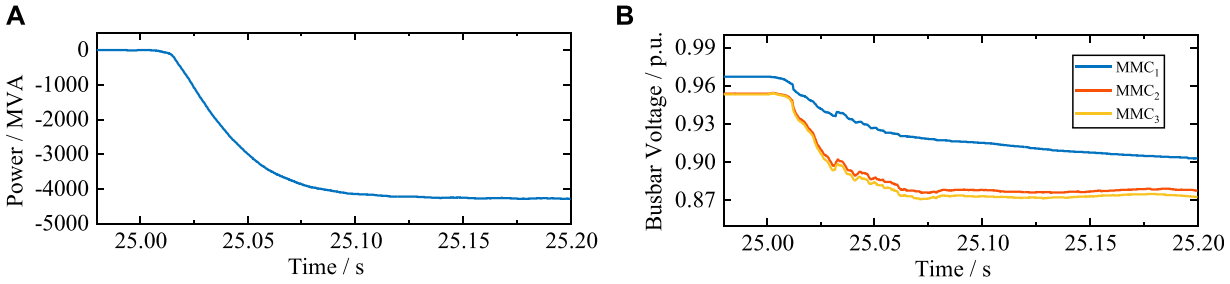

FIGURE 14
(A) Reactive power response of MMCs; **(B)** busbar voltage responses of MMCs.

On the inverter side, each parallel MMC uses a constant reactive power regulation method, and the reactive power interaction between the MMCs and the AC network is nearly zero before failure occurs. After the MMCs are blocked, the submodule capacitor no longer provides fault currents to the fault point. However, the AC network can still provide fault currents, and the converter leakage resistance and bridge arm reactance of the MMC consume a significant amount of reactive power.

From the receiving-end grid VQ curve of the reactive power supply and load, the load reactive power suddenly increases significantly, and the load VQ curve shifts upward (Liu et al., 2016). If the reactive power supply capacity is insufficient, the voltage at the new intersection of the VQ curves of the reactive power supply and the load decreases, thus forcing the reactive power supplier to increase the output of Q and the load side to decrease consumption. Thus, the receiving-end grid reaches a new stable balance state at a low-voltage level, and the AC bus voltage of each parallel MMC side is shown in Figure 14B.

Therefore, because of the slow opening and shutting times of the AC switch, the MMC approximates a three-phase uncontrolled rectifier, and its converter leakage resistance and bridge arm reactance must consume a large amount of Q. If the reactive power capacity is insufficient, the voltage at each node is reduced. The simulation results show that if the responses of the

long-term dynamic components and parts are not considered, the AC network does not meet the relevant long-term voltage stability evaluation criteria.

7 Conclusion

This study used a hybrid cascaded HVDC system as the research object and simulated a permanent ground fault in high- and low-end connecting lines on the cascaded side. It then conducted a thorough theoretical analysis of the fault responses of MMCs and LCCs as well as the impact of the AC network. The relevant conclusions are as follows:

The fault current on the MMC_1 side was the result of the combined action of the aforementioned two types of excitation sources. Therefore, the two types of excitation sources were decomposed, the response of each group of excitation sources acting separately was calculated according to the principle of the superposition theorem, and the total response of the MMC_1 circuit was obtained by adding them together.

- Because of the reliable blocking of the MMCs and the reverse process of I_{dcm}, there was no need to consider the IGBT overcurrent of each submodule before the MMCs were blocked
- The LCC on the inverter side may lead to commutation failure owing to the increase in I_{dc} in the fault conditions described above
- During the steady-state process, after the MMCs were blocked, the HVDC system consumed a significant amount of reactive power; this resulted in a reduction in the AC voltage at the receiving grid. This does not satisfy the relevant long-term voltage stability evaluation criteria.

From the calculation and simulation results, the theoretical analysis presented above yielded results that were consistent with the actual response, thus providing a theoretical basis and calculation method for the design, testing, and performance evaluation of HVDC systems. In addition, the HVDC system is a significant part of smart grids in the broad range of applications of AI and there is a close connection between the two. The theoretical analysis presented above can also realize intelligent management and control of power systems, improve the energy utilization efficiency and stability of the power grid, and provide strong support for energy transformation. In the future, further research will be conducted in terms of reducing the overcurrent peak of the bridge arm after the failure occurs.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

YR, HS, SW, BZ, and SX was responsible for contributing conception and design of the study and writing sections of the manuscript. YR wrote the first draft of the manuscript. ML and PL was responsible for model building, simulation. All authors participated in the reading and approved the submitted version.

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Conflict of interest

YB, SW, BZ, SX, ML, and PL were employed by China Electric Power Research Institute Co. Ltd.

The remaining author declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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