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*CORRESPONDENCE Junliang Liu, ⊠ ljl@cqu.edu.cn

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Stability analysis of two-terminal HVDC transmission systems using SISO open-loop gains

Shangning Tan, Junliang Liu*, Xiong Du, Hongjun Yang and Yuelong Cao

State Key Laboratory of Power Transmission Equipment and System Security and New Technology, Chongqing University, Chongqing, China

The ports of a three-phase voltage source converter have multiple frequency electrical parameters, which makes HVDC systems with these converters present multiple input multiple output (MIMO) characteristics. The generalized Nyquist criterion of the MIMO model is often used to analyze the system stability. However, this model is more difficult to obtain than the single-input single-output (SISO) model, and the stability margin and the oscillation frequency band are difficult to capture. To solve these problems, this paper took the two-terminal HVDC transmission system as the research object to derive a SISO model that can be measured by a port. Moreover, this study also proposed a method for analyzing the system stability through envelope SISO open-loop gains. Finally, the key port and parameters affecting the system stability were analyzed according to the stability margin, which provided theoretical support for the design of the system parameters. The established model and the proposed analysis method were verified in a MATLAB/Simulink simulation model.

KEYWORDS

phase margin, stability analysis, port model, parameter design, partition point

1 Introduction

With the increase in transmission capacity, HVDC systems have become an ideal transmission solution (Flourentzou et al., 2009). However, this has brought about concerns related to the stability of the interconnected systems (Sun et al., 2017). The small-signal stability of HVDC systems can be studied using state space model-based eigenvalue analysis (Du et al., 2018; Dewangan and Bahirat, 2020) and impedance models (Chang et al., 2021)-(Cao et al., 2017). However, as the establishment of a state space model requires detailed parameters, this model cannot be used when model parameters are unknown or user privacy is protected. Because the impedance model can be obtained by port measurement, stability analysis based on the impedance model has been widely studied and applied in recent years.

System stability is analyzed based on DC single-input single-output (SISO) impedance models (Chang et al., 2021) or AC SISO impedance models of two-terminal DC transmission systems (Sun, 2011). To facilitate the analysis of the system stability, the sending end converter of the system is equivalent to a constant voltage source (Shah and Parsa, 2017) or constant power (Zou et al., 2018), and the simplified model is used to analyze the system stability. Bo et al. (2017) established the second-order impedance matrix of the converter in the rotating coordinate system and demonstrated that when the converter operates at a specific high-power factor, the coupling of the dq axis can be ignored and the MIMO model is reduced to the SISO model. Chou et al. (2020) also analyzed the system stability based on

two SISO port models. However, multiple frequency interactions occur between the AC and DC ports of voltage source converters. If a single-frequency small signal voltage disturbance appears on the AC side of the converter, dual-frequency AC currents can be generated. These dual-frequency currents generate the disturbance voltage response of the corresponding frequency so that the two frequencies on the AC side are coupled to each other. At the same time, another frequency of current response also is produced at the DC port (Zhang et al., 2019a). Multi-frequency AC-DC interactions exist in two-terminal HVDC transmission systems (Tan et al., 2020). The AC-DC interactions are ignored in these models, which may cause errors in stability determination (Huang and Wang, 2018).

Zou et al. (2018) analyzed system stability according to the positive and negative sequence SISO impedances of a single partition point. Sun 2021) used the DC port impedance ratio considering the interactions to determine the system stability based on the Nyquist criterion. These systems must determine the number of zeros and poles in the right half-plane of the subsystems. Zhang et al. (2020) and Fan and Miao (2020) pointed out that system models of a single partition point may not accurately determine the global stability of the system but did not report on partition point selection. Cao et al. (2017) and Eto et al. (2023) used iterative analyses to ensure that there were no zeros in the right half-plane of the subsystem impedance at a single partition point, and then determined the system stability. Liu et al. (2014) determined the system stability by the system equivalent impedance sum. However, in practical applications, it is difficult to determine the number of zeros and poles in the right half-plane; moreover, it is also difficult to obtain the stability margin. Sun (2022) and Zhang et al. (2019b) determined the system stability by analyzing the SISO transfer function of multiple control loops in a single grid-connected inverter. However, this method was not used in the two-terminal HVDC transmission system. Zhu et al. (2023) used the 6-order MIMO admittance parameter matrix to describe the AC-DC port interactions of the system and analyzed the system stability using the generalized Nyquist eigenvalue. Zhang et al. (2021) used the determinant phases between the system MIMO admittance matrix and the grid impedance in the full frequency band to judge the system stability. However, in analysis methods based on the MIMO system model, it is difficult to capture the oscillation frequency band of the system and obtain the stability margin. The stability margin is a key indicator of the system's robustness. A stability margin is necessary for parameter design in practical engineering (Healey, 1976; Yang et al., 2021).

To accurately analyze the system stability and obtain the stability margin of the system, this paper used the two-terminal HVDC transmission system as the research object and determined the ports for analyzing the system stability by introducing the envelope division system. Based on the port parameter matrix representing the AC-DC interactions of the system sub-module, the SISO openloop gains of the system were obtained. Based on the SISO openloop gains of the ports, the oscillation frequency band of the system was analyzed to avoid screening of the zero and pole points in the right half-plane. Finally, the key modules and parameters affecting the system stability were identified. The research results provide a theoretical basis for accurate parameter design. The rest of this report is arranged as follows. Section 2 establishes the port parameter matrix model of each module of the system. Section 3 takes the two-terminal HVDC system as the research object. Based on the envelope division system, the SISO port equivalent impedance/admittance model of the system is derived and the accuracy of the model is verified. Section 4 analyzes the system stability based on the SISO model established by the envelope. The key parameters affecting the system stability are identified in Section 5. Section 6 summarizes this work.

2 Port models of the system submodules

The two-terminal HVDC transmission system consists of two converters and a DC network. The port parameter matrixes of the HVDC system sub-modules and AC grids are established in this section.

The main circuit diagram of the two-terminal HVDC transmission system is shown in Figure 1. The VSC1 is a rectifier with current control. The VSC2 controls the DC voltage. v_{pa} , v_{pb} , v_{pc} , i_{pa} , i_{pb} , and i_{pc} are the three-phase AC voltage and the AC current of the converter, respectively. $H_i(s)$ is the current control loop. $H_i(s) = K_{pi} + K_{ii}/s$, K_{pi} and K_{ii} are the proportional and integral coefficients of the current PI control, respectively. θ_{pll} is the output phase angle of the PLL. $H_{pll}(s)$ is an open-loop small-signal model of the phase-locked loop (PLL). I_{dref} and I_{qref} are the dq axis reference current of the converter. L is the converter AC filter inductance. v_{dcj} and i_{dcj} are DC voltage and current, respectively. Z_{line} and Z_f are the equivalent impedances of transmission lines and DC filters, respectively.

2.1 Admittance parameter models of the converter modules

Based on the AC-DC interactions at the ports of the three-phase converter, the admittance parameter matrix of the three-phase converter in the stationary coordinate system can be expressed as

$$\begin{bmatrix} I_{dcj}(s-j\omega_1)\\ I_{pj}(s)\\ I_{pj}(s-j2\omega_1) \end{bmatrix} = \begin{bmatrix} Y_{ssj}(s) & Y_{spj}(s) & Y_{snj}(s)\\ Y_{psj}(s) & Y_{ppj}(s) & Y_{pnj}(s)\\ Y_{nsj}(s) & Y_{npj}(s) & Y_{nnj}(s) \end{bmatrix} \begin{bmatrix} V_{dcj}(s-j\omega_1)\\ V_{pj}(s)\\ V_{pj}(s-j2\omega_1) \end{bmatrix},$$
(1)

where $\omega_1 = 2\pi f_1$, f_1 is the fundamental frequency; $I_{pj}(s)$, $I_{pj}(s - j2\omega_1)$, $V_{pj}(s)$, and $V_{pj}(s - j2\omega_1)$ are the three-phase AC current and voltage small signal models at different frequencies of the *j*th converter; and $I_{dcj}(s - j\omega_1)$ and $V_{dcj}(s - j\omega_1)$ are the DC current and voltage of the *j*th converter, respectively.

The parameters in the matrix model represent the interactions between the voltage disturbances of the converter at different frequencies and the corresponding current responses. The main diagonal element is the admittance of the converter port voltage interference and the current response at the same frequency. The remaining admittance elements characterize the relationship between the converter port voltage disturebances and the current responses at different frequencies. Each admittance parameter is derived when the other voltage disturbances except the



corresponding voltage disturbances are short-circuited. The specific derivation is as follows.

A perturbation $V_{pj}(s)$ on the AC side of the system inverter results in a small perturbation at the output phase by the PLL. Based on the structure of the PLL in Zou et al. (2018), the relationship between the variables in the stationary reference frame and the rotating coordinate system can be obtained as

$$X_{dai}(s - j\omega_1) = X_{pi}(s) - 0.5X_{dai}T_{bll}(s - j\omega_1)V_{pi}(s),$$
(2)

$$X_{dqj}(j\omega_1 - s) = X_{pj}(2j\omega_1 - s) + 0.5X_{dqj}T_{pll}(j\omega_1 - s)V_p^*(s), \quad (3)$$

where X represents the AC current, voltage, or duty cycle D of the converter; X_{dqj} and $X_{dqj} (s - j\omega_1)$ are the steady-state complex coefficient and small signal model, respectively; $X_{dqj} = X_{dj} + X_{qj}$. $X_{pj}(s)$ is a small-signal model of AC current, voltage, or duty cycle in the stationary coordinate system; $V_{pj}^*(s)$ is the conjugate quantity of $V_{pj}(s)$; and $T_{pll}(s - j\omega_1)$ is the closed loop transfer function of the PLL, $T_{pll}(s) = H_{pll}(s)/[1 + V_1H_{pll}(s)]$.

The small signal model of the main circuit and the current loop in the Appendix can be derived as

$$sLI_{pj}(s) = D_{pj}(s)V_{dcj} - V_{pj}(s),$$
(4)

$$(2j\omega_1 - s)LI_{pj}(2j\omega_1 - s) = D_{pj}(j2\omega_1 - s)V_{dcj},$$
(5)

$$D_{dqj}(s) = \frac{1}{2V_{cr}} \left[-H_i(s) + j\omega_1 L \right] I_{dqj}(s),$$
(6)

where L is the converter AC filter inductor.

According to the small signal relationship between the main circuit and the control circuit (6), the relationship between the voltage disturbance $V_{pj}(s)$ and the current response can be derived as

$$Y_{ppj}(s) = \frac{I_{pj}(s)}{V_{pj}(s)} = \frac{1 - 0.5V_{dcj} D_{dqj} T_{pll}(s - j\omega_1) + [j\omega_1 L - H_i(s - j\omega_1)] 0.5I_{dqj} T_{PLL}(s - j\omega_1)}{(s - j\omega_1)L + H_i(s - j\omega_1)},$$
(7)

where $H_i(s)$ is the current control loop; $T_{pll}(s - j\omega_1)$ is the closed loop transfer function of the PLL, $T_{pll}(s) = H_{pll}(s)/[1 + V_1H_{pll}(s)]$; $H_{pll}(s)$ is an open-loop small-signal model of the PLL; V_{dcj} is the steady-state DC voltage of the *j*th converter; and I_{dqj} and D_{dqj} are the steady-state values of AC current and duty cycle, respectively.

Similarly, the relationship between the small disturbance and response of the converter at different frequencies in the main circuit and the control circuit can be deduced. The specific formula is shown in the Appendix.

2.2 Parameter models for AC and DC networks

The DC network of the system is composed of DC transmission lines and DC filters. The transmission parameter matrix of the DC network port is described as

$$\begin{bmatrix} V_{dc2}(s-j\omega_1)\\ I_{dc2}(s-j\omega_1) \end{bmatrix} = T_{dcn}(s) \begin{bmatrix} V_{dc1}(s-j\omega_1)\\ I_{dc1}(s-j\omega_1) \end{bmatrix},$$
(8)

where $T_{dcn}(s) = T_{c1}(s)^* T_{dcl}(s)^* T_{c2}(s)$; $T_{c1}(s)$ and $T_{c2}(s)$ are the transmission parameter matrix of the rectifier and inverter DC filter; and $T_{dcl}(s)$ is the transmission parameter matrix of the DC transmission line.

$$T_{cj}(s) = \begin{bmatrix} 1 & 0 \\ -Y_f(s - j\omega_1) & 1 \end{bmatrix},$$
(9)

$$T_{dcl}(s) = \begin{bmatrix} 1 & -2Z_{line}(s - j\omega_1) \\ 0 & 1 \end{bmatrix},$$
 (10)

where $Y_f(s - j\omega_1)$ and $Z_{line}(s - j\omega_1)$ are the equivalent admittance of the DC filter and the equivalent impedance of the DC transmission line, respectively.

The impedance parameter matrix $Z_{dcn}(s)$ of the DC network can be obtained by the transmission parameter matrix conversion.

$$\begin{bmatrix} V_{dc1}(s - j\omega_1) \\ V_{dc2}(s - j\omega_1) \end{bmatrix} = \mathbf{Z}_{dcn}(s) \begin{bmatrix} I_{dc1}(s - j\omega_1) \\ I_{dc2}(s - j\omega_1) \end{bmatrix}$$
$$= \begin{bmatrix} Z_{n11}(s) \ Z_{n12}(s) \\ Z_{n21}(s) \ Z_{n22}(s) \end{bmatrix} \begin{bmatrix} I_{dc1}(s - j\omega_1) \\ I_{dc2}(s - j\omega_1) \end{bmatrix}.$$
(11)

The elements in the matrix are the impedance parameters of the DC network. $Z_{n11}(s)$ and $Z_{n22}(s)$ are the input impedances of DC ports B and D, respectively, and $Z_{n12}(s)$ and $Z_{n21}(s)$ are the transfer impedances between DC ports B and D, respectively.

The port impedance parameter model $Z_{gz}(s)$ of the AC grids is expressed as

$$\begin{bmatrix} V_{p1}(s) \\ V_{p2}(s-j2\omega_{1}) \\ V_{p2}(s) \\ V_{p2}(s-j2\omega_{1}) \end{bmatrix} = \mathbf{Z}_{gz}(s) \begin{bmatrix} I_{p1}(s) \\ I_{p1}(s-j2\omega_{1}) \\ -I_{p2}(s) \\ -I_{p2}(s-j2\omega_{1}) \end{bmatrix}$$
$$= \begin{bmatrix} \mathbf{Z}_{g1} & \mathbf{0} \\ \mathbf{0} & \mathbf{Z}_{g2} \end{bmatrix} \begin{bmatrix} I_{p1}(s) \\ I_{p1}(s-j2\omega_{1}) \\ -I_{p2}(s) \\ -I_{p2}(s) \\ -I_{p2}(s-j2\omega_{1}) \end{bmatrix}, \quad (12)$$

where Z_{gj} is the equivalent impedance model of the AC grid *j*.



$$\mathbf{Z}_{gj} = \begin{bmatrix} Z_{gj}(s) & 0\\ 0 & Z_{gj}(s - j2\omega_1) \end{bmatrix}.$$
 (13)

3 Stability analysis of HVDC transmission systems

We propose a method for the stability analysis of the HVDC transmission system based on an envelope line and port SISO models. The stability analysis based on the SISO open loop gains can be used to obtain the oscillation frequency band and the stability margin, which provide a theoretical basis for the subsequent parameter design.

3.1 Loop gains of HVDC transmission systems

Different from the system divided by a single partition point, this work proposes to use the envelope line to divide the interconnected system. A closed envelope is formed by cutting the ports of the interconnected system. The purpose of dividing the envelope system is to ensure the stability of the divided subsystem. If the stability of the HVDC transmission system cannot be guaranteed when operating alone, the envelope divides the system into converter and grid subsystems by cutting the AC and DC ports of the system. The converter subsystem consists of two converters, which are designed to operate stably, while the grid subsystem is composed of an AC power grid and a DC transmission network. All components of the grid subsystem are passive, so the subsystem can operate stably. When the envelope is divided into two ends of the HVDC transmission system, as shown in Figure 2, it intersects with the four ports of the system; namely which are AC (ports A and C), and DC (ports B and D), respectively. The system stability of the interconnection between the HVDC transmission system and the weak grid is analyzed based on the impedance ratios of the intersection ports of the envelope line.

Therefore, the port models of the system rectifier and inverter can be obtained based on (1). The port admittance parameter model of the HVDC system's converter module is obtained by port expansion.

$$\begin{bmatrix} I_{dc1}(s - j\omega_{1}) \\ I_{dc2}(s - j\omega_{1}) \\ I_{p1}(s) \\ I_{p1}(s - j2\omega_{1}) \\ I_{p2}(s) \\ I_{p2}(s - j2\omega_{1}) \end{bmatrix} = \begin{bmatrix} \mathbf{Y}_{dd}(s) \ \mathbf{Y}_{da}(s) \\ \mathbf{Y}_{ad}(s) \ \mathbf{Y}_{aa}(s) \end{bmatrix} \begin{bmatrix} V_{dc1}(s - j\omega_{1}) \\ V_{dc2}(s - j\omega_{1}) \\ V_{p1}(s) \\ V_{p1}(s - j2\omega_{1}) \\ V_{p2}(s) \\ V_{p2}(s - j2\omega_{1}) \end{bmatrix},$$
(14)

where $Y_{dd}(s)$ and $Y_{aa}(s)$ represent the characteristics of the DC and AC ports of the converters and $Y_{da}(s)$ and $Y_{ad}(s)$ represent the interactions between the AC and DC ports of the converters, respectively. Because the converter module is stable, the admittance parameter matrix in (14)has no right half-plane pole (RHP).

3.1.1 SISO open-loop gains of AC ports

To obtain the SISO open-loop gains of AC ports A and C, the DC ports of the converter are interconnected with the DC transmission network, and the DC ports are eliminated. The admittance parameter models of two converter AC ports A and C are expressed as

$$\begin{bmatrix} I_{p1}(s) \\ I_{p1}(s - j2\omega_1) \\ -I_{p2}(s) \\ -I_{p2}(s - j2\omega_1) \end{bmatrix} = \begin{bmatrix} \mathbf{Y}_{RR} & \mathbf{Y}_{RI} \\ \mathbf{Y}_{IR} & \mathbf{Y}_{II} \end{bmatrix} \begin{bmatrix} V_{p1}(s) \\ V_{p1}(s - j2\omega_1) \\ V_{p2}(s) \\ V_{p2}(s - j2\omega_1) \end{bmatrix}, \quad (15)$$
$$\begin{bmatrix} \mathbf{Y}_{RR} & \mathbf{Y}_{RI} \\ \mathbf{Y}_{IR} & \mathbf{Y}_{II} \end{bmatrix} = \mathbf{Y}_{aa}(s) - \mathbf{Y}_{ad}(s) [\mathbf{Y}_{dcn}(s) - \mathbf{Y}_{dd}(s)]^{-1} \mathbf{Y}_{da}(s), \quad (16)$$

where Y_{RR} , Y_{RI} , YM_{IR} , and YM_{II} are 2-order square matrices and Y_{RR} and Y_{II} represent the characteristics of the AC port of a single rectifier and a single inverter, respectively. YM_{RI} and YM_{IR} represent the interactions of AC port voltage disturbance and current response between two converters in a two-terminal HVDC system, respectively. Because the converter module of the system is stable, there is no RHP in Y_{RR} , Y_{RI} , YM_{IR} , and YM_{II} .

The DC port of the HVDC system forms a feedback loop with the DC network. The stability of the feedback loop can be analyzed by the loop transfer function $[Y_{dcn}(s) - Y_{dd}(s)]^{-1}$. If the feedback loop is unstable, the admittance in (Eq. 16) has right half-plane poles.

When the AC port of the system is connected to the AC grid, the AC port is eliminated to form a feedback loop. The system can be reduced to obtain a second-order matrix of a single AC port.





Therefore, the admittance models of port A and port C can be expressed as

$$\begin{bmatrix} I_{p1}(s) \\ I_{p1}(s-j2\omega_{1}) \end{bmatrix} = \left(Y_{RR} + Y_{RI}Z_{g2} \left(I - Z_{g2}Y_{II} \right)^{-1} Y_{IR} \right) \\ \times \begin{bmatrix} V_{p1}(s) \\ V_{p1}(s-j2\omega_{1}) \end{bmatrix} \\ = \begin{bmatrix} YR_{11}(s) YR_{12}(s) \\ YR_{21}(s) YR_{22}(s) \end{bmatrix} \begin{bmatrix} V_{p1}(s) \\ V_{p1}(s-j2\omega_{1}) \end{bmatrix}, \quad (17) \\ \begin{bmatrix} I_{p2}(s) \\ I_{p2}(s-j2\omega_{1}) \end{bmatrix} = \left(Y_{II} + Y_{IR}Z_{g1} \left(I - Z_{g1}Y_{RR} \right)^{-1} Y_{RI} \right) \\ \times \begin{bmatrix} V_{p2}(s) \\ V_{p2}(s-j2\omega_{1}) \end{bmatrix} \\ = \begin{bmatrix} YI_{11}(s) YI_{12}(s) \\ YI_{21}(s) YI_{22}(s) \end{bmatrix} \begin{bmatrix} V_{p2}(s) \\ V_{p2}(s-j2\omega_{1}) \end{bmatrix}, \quad (18)$$

where $YR_{11}(s)$, $YR_{22}(s)$, $YI_{11}(s)$, and $YI_{22}(s)$ are the selfadmittances of ports A and C, respectively. These admittances represent the relationships between the AC port voltage disturbance and the current response at the same frequency. $YR_{12}(s)$ and $YR_{21}(s)$ are the mutual admittances of port A. $YI_{12}(s)$ and $YI_{21}(s)$ are the mutual admittances of port C. The mutual admittances describe the frequency coupling of ports A or C.

The feedback loops are introduced into the reduceddimensional system port model. The stability of the two admittance models of ports A and C can be determined by $Z_{g2}Y_{II}$ and $Z_{g1}Y_{RR}$.

Due to the port-connected grid impedances, the secondorder admittance parameter matrix in (Eq. 17) can be further reduced to a SISO impedance. The SISO impedance model of port A is

$$Y_{a1}(s) = YR_{11}(s) + Z_{g1}(s - j2\omega_1)YR_{12}(s) \left[1 - Z_{g1}(s - j2\omega_1)YR_{22}(s)\right]^{-1}YR_{21}(s),$$
(19)



where $YR_{11}(s)$ and $YR_{22}(s)$ are the relationship between the same frequency voltage disturbance and the current response of port A, and $YR_{12}(s)$ and $YR_{21}(s)$ describe the frequency coupling of port A.

The transfer function $GL_A(s)$ of port A voltage disturbance and output voltage can be expressed as

$$GL_{A}(s) = \frac{V_{p1}(s)}{V_{g1}(s)} = \frac{1}{1 + H_{A}(s)} = \frac{1}{1 + Z_{g1}(s)Y_{a1}(s)}$$
$$= \frac{1}{\left[1 - Z_{g1}(s - j2\omega_{1})YR_{22}(s)\right]^{-1} \left|I - Z_{g1}Y_{RR}\right| \left|I - (I - Z_{g1}Y_{RR})^{-1}Y_{RI}Z_{g2}(I - Z_{g2}Y_{II})^{-1}Y_{IR}\right|\right]^{2}}$$
(20)

where $H_A(s)$ is the open-loop gain of port A. Eq. 20 shows that if $GL_A(s)$ is stable, whether $H_A(s)$ satisfies the Nyquist criterion must be determined.

The SISO impedance model of port C is expressed as

$$Y_{a2}(s) = YI_{11}(s) +Z_{g2}(s - j2\omega_1)YI_{12}(s) [1 - Z_{g2}(s - j2\omega_1)YI_{22}(s)]^{-1}YI_{21}(s),$$
(21)

where $YI_{11}(s)$ and $YI_{22}(s)$ are the relationship between the same frequency voltage disturbance and the current response of port



C, respectively, and $YI_{12}(s)$ and $YI_{21}(s)$ describe the frequency coupling of port C.

Based on the SISO impedance model of port C, the transfer function $GL_C(s)$ of port A voltage disturbance and output voltage can be expressed as

$$GL_{c}(s) = \frac{V_{p2}(s)}{V_{g2}(s)} = \frac{1}{1 + H_{C}(s)} = \frac{1}{1 + Z_{g2}(s)Y_{a2}(s)}$$
$$= \frac{1}{\left[1 - Z_{g2}(s - j2\omega_{1})YI_{22}(s)\right]^{-1} \left|I - Z_{g2}Y_{II}\right|^{-1} Y_{IR}Z_{g1}(I - Z_{g1}Y_{RR})^{-1}Y_{RI}\right]},$$
(22)

where $H_C(s)$ is the open-loop gain of port C. If $GL_C(s)$ is stable, whether $H_C(s)$ satisfies the Nyquist criterion must be determined.

3.1.2 SISO open-loop gains of DC ports

To obtain the SISO open-loop gains of DC ports B and D, the AC ports are eliminated. The AC ports of the converters are interconnected with the AC grids to form a feedback loop. The DC port admittance model of the system converter module is expressed as

$$\begin{bmatrix} I_{dc1}(s-j\omega_1)\\ I_{dc2}(s-j\omega_1) \end{bmatrix} = \begin{bmatrix} Y_{d11}(s) & 0\\ 0 & Y_{d22}(s) \end{bmatrix} \begin{bmatrix} V_{dc1}(s-j\omega_1)\\ V_{dc2}(s-j\omega_1) \end{bmatrix}, \quad (23)$$

$$\begin{array}{c} Y_{d11}(s) & 0\\ 0 & Y_{d22}(s) \end{array} \end{bmatrix} = Y_{dd}(s) \\ & -Y_{da}(s)Z_{gz}(s) \Big[I - Z_{gz}(s)Y_{aa}(s) \Big]^{-1}Y_{ad}(s),$$

$$(24)$$

where $Y_{d11}(s)$ and $Y_{d22}(s)$ represent the input admittance models of DC ports B and D, respectively.

The stability of the admittance model in Eq. 24 can be analyzed using the loop transfer function $[I - Z_{gz}(s)Y_{aa}(s)]^{-1}$.

To obtain the SISO impedance model of port B, port D is eliminated. According to the port model of the DC network and the admittance model of port B, the SISO impedance model for port B is shown as

$$Z_{dciz}(s) = Z_{n11}(s) + Z_{n12}(s) [Z_{n22}(s) - (Y_{d22}(s))^{-1}]^{-1} Z_{n21}(s).$$
(25)

The transfer function $GL_B(s)$ of port B voltage disturbance and output voltage can be expressed as

$$GL_B(s) = \frac{1}{1 + H_B(s)} = \frac{1}{1 + Z_{dciz}(s)Y_{d11}(s)},$$
(26)



where $H_B(s)$ is the open-loop gain of port B. $Z_{dciz}(s)$ and $Y_{d11}(s)$ are the output impedance and input admittance models of port B, which can be obtained by small signal measurement of port B.

Based on the parametric model of port D, the SISO impedance model of port D is expressed as

$$Z_{dcrz}(s) = Z_{n22}(s) + Z_{n21}(s) [Z_{n11}(s) - (Y_{d11}(s))^{-1}]^{-1} Z_{n12}(s).$$
(27)

The transfer function $GL_D(s)$ of port D voltage disturbance and output voltage can be expressed as

$$GL_{D}(s) = \frac{[Y_{d22}(s)]^{-1}}{1 + H_{D}(s)} = \frac{[Y_{d22}(s)]^{-1}}{1 + [Z_{dcrz}(s)*Y_{d22}(s)]^{-1}},$$
 (28)

where $H_D(s)$ is the open-loop gain of port D. $Z_{dcrz}(s)$ and $Y_{d22}(s)$ are the output impedance and input admittance models of port D, which can be obtained by small signal measurement of port D.

The system stability can be determined by the open-loop gain. The open-loop gain is composed of the SISO input impedance and output admittance of the port. These equivalent impedance/ admittance can be obtained by small-signal measurements of the electrical parameters of the port and Fourier analysis. However, before using the open-loop gain of a single partition point to analyze the system stability, whether the SISO model of the system contains RHPs must be determined. When the open-loop gain of port A is used to analyze the system stability, the stability of the equivalent admittance must be determined. Because the converters divided by the envelope line and the AC/DC network module are stable, the key factor causing the instability of port A in (Eq. 19) is to eliminate the feedback loop introduced from port B to port D. The sub-feedback loops of the equivalent impedance/admittance are all composed of passive power grids and models ignoring partial AC-DC interactions. For example, to establish the admittance parameter matrix of port A in Eq. 17, the feedback loop $(I - Z_{g2}Y_{II})^{-1}$ is introduced. When using the input admittance and output impedance of port C to analyze stability, the transfer function in (Eq. 22) contains the feedback loop $(I - Z_{g2}Y_{II})^{-1}$. Therefore, the SISO model of port C can be used to reflect the stability of the feedback loop. Similarly, it can be deduced that the SISO open-loop gain of the *j*th port contains the feedback loop introduced when the jth port is eliminated. The stability of the feedback loop can be determined by the SISO open-loop gain of the *j*th port, which can avoid analyzing the right half-plane poles of the port model.

The partition points of the system are the ports where the envelope intersects with the system. The system divided by a single partition point has only one equivalent source. The system divided by the envelope has multiple partition points. This indicates that the system is equivalent to source-load models at multiple ports. Based on the superposition theorem, the equivalent perturbation sources of the intersecting ports of the envelope must be considered individually. The system stability is determined by the SISO openloop gains of the ports intersecting the envelope line.

The stability of the HVDC transmission system is analyzed by the open-loop gain of ports A to D, which are $Z_{g1}(s)Y_{a1}(s)$, $Y_{dciz}(s)[Y_{d11}(s)]^{-1}$, $Z_{g2}(s)Y_{a2}(s)$, and $Z_{dcrz}(s)Y_{d22}(s)$. If the SISO open-loop gains of ports A to D intersecting with the envelope line satisfy the Nyquist criterion, the HVDC transmission system is stable. Otherwise, the system is unstable.

3.2 Model verification

To verify the accuracy of the aforementioned models based on the envelope port parameters, the two-terminal HVDC system model shown in Figure 1 is built in MATLAB/Simulink. The parameters of the model are shown in Supplementary Table S1. First, the accuracy of the system model is verified. The equivalent admittance/impedance model of the system can obtain the corresponding current response value by injecting small voltage disturbances of different frequencies into the port. The equivalent impedance measurement model of the system is obtained by Fourier analysis. This paper selected two SISO equivalent impedances of the two-terminal HVDC transmission system to verify the accuracy of the system model, as shown in Figure 3. The results show that the analytical model can accurately reflect the system for system stability analysis. As the model verification of the DC ports is consistent with the AC models, it is no longer described here.



The stability analysis of the ports intersecting the envelope line is shown in Figure 4 when the short circuit ratios of the AC grids are 2.1 and the power reference of the system is set to 7.2 MW. The corresponding simulation current waveforms and the spectrum are shown in Figure 5.

In Figure 4A, the AC input impedance model of the system based on port A with intersecting envelope lines intersects the impedance of the interconnected power grid at a frequency of 202.8 Hz, and the corresponding phase difference is 130.8° . The phase difference is < 180° . The AC input impedance model of the system based on port C with intersecting envelope lines intersects with the impedance of the interconnected power grid at a frequency of 152 Hz, and the corresponding phase difference is 180.6°. The phase difference exceeds 180°, and the system is unstable. In Figure 4B, the equivalent input impedance amplitudes of DC port B are much larger than the output, and there is no amplitude intersection. The equivalent input and output impedance of DC port D intersects at the frequency of 6.3 Hz, and the corresponding phase difference is 74.2°.

The analysis showed that the system is stable only when the impedance ratios of the ports intersecting the envelope line satisfy the Nyquist stability criterion. Therefore, the system is determined to be unstable. Figure 5B shows the spectrum of system simulation waveforms by fast Fourier transform (FFT) in Figure 5A. The spectrum shows that the system has a large amount of harmonics near 152 Hz and 52 Hz, where the system output current oscillates and the system is unstable. This is consistent with the results of the theoretical stability analysis. Therefore, stability analysis based on the ports intersecting the envelope line can reflect the stability of HVDC transmission systems.

4 Key parameter identification and design

Based on the stability analysis of the ports, port C has the smallest stability margin and is the key port that causes instability of the HVDC transmission system. Moreover, the module inverter VSC2 corresponding to AC port C is the key module affecting the system stability. This section discusses the effects of the phase-locked loop and the DC voltage bandwidth on the stability margin of the port.

To intuitively measure the effect of parameters on system stability, the phase margin of the port is defined. In practical engineering, an appropriate phase margin is necessary to ensure the safe and stable operation of the system. The phase margin of the system should be at least 30° in practice (Healey, 1976), (Yang et al., 2021). This paper assumed that the subsystems on both sides of the partition point are stable when running alone. The phase margin φ_k of the *kth* port is defined as

$$\varphi_{k} = 180^{0} - Abs \bigg[\varphi[H_{k}(s_{i})]_{|20 * lg[H_{k}(s_{i})]=0} \bigg],$$
(29)

where $H_k(s)$ is the open-loop gains of the *kth* port.

Based on the relationship between the control loops of the individual converters and the oscillation interval reported by Sun (2021), the DC voltage control and the PLL are the control parameters causing the oscillation of AC port C. Therefore, the variation in the phase margin of port C with the PLL and the bandwidth of the dc-voltage loop is represented in Figure 6. The upper right corner of Figure 6 is a two-dimensional plane. For port C, the AC phase margin decreases as the DC voltage bandwidth of converter VSC2 and the PLL bandwidth increase.

The effect of the PLL bandwidth in converter VSC1 on port C can be neglected.

As the PLL bandwidth increases from 5 Hz to 20 Hz in Figure 6A, the stability margin of port C decreases from 43.3° to 30° . As the dc-voltage loop bandwidth increases from 5 Hz to 20 Hz in Figure 6B, the stability margin of port C decreases from 43.4° to 37.2° . Compared to the dc-voltage bandwidth, AC port C is more sensitive to changes in the PLL. Therefore, system stability can be achieved by adjusting the key control PLL bandwidth that affects the stability margin of the system ports.

The stability margin of converter VSC2 port C is 30°, which corresponds to a converter PLL bandwidth of 20 Hz.

If only the stability of the system is considered qualitatively, the range of the PLL bandwidth to guarantee the stability of the system is <50 Hz, and a PLL bandwidth of 45 Hz is chosen.

As the system power increases from 6 MW to 7.2 MW at 2s, the system grid-connected current waveforms under the two parameters are shown in Figure 7. Figure 7A is the dc voltage waveform with a PLL bandwidth of 45 Hz. When the power increases, the dc voltage waveform changes from stable to divergent, and the system is unstable. Figure 7B shows that the dc voltage based on the envelope SISO open-loop gain analysis and design parameters can be rapidly adjusted and can still recover stability after being subjected to voltage perturbations.

Compared with the qualitative analysis, the parameters designed based on the quantitative analysis of the envelope SISO open-loop gains can guarantee good system robustness.

5 Conclusion

This study proposed an analysis method for determining the system stability by the SISO open-loop gains. The system is divided by the envelope into sub-modules that are stable when operating individually. Based on the port parameter models of the system, the SISO open-loop gains of the ports were derived. The system stability was analyzed according to the SISO open-loop gains of the ports intersecting the envelope line. The key port and parameters affecting the stability of the system were located based on the stability margin.

Compared with the stability analysis of the single partition point division system, the iterative screening of the zeros and poles of the small feedback loop was avoided. Compared with the qualitative stability analysis, the proposed analysis method can obtain the stability margins of the system and the oscillation frequency band, which can be used to locate the key modules affecting the system stability and to design the parameters. The designed parameters can ensure that the system has good robustness. The results of the stability analysis provide a theoretical basis for system

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parameter design and network planning. Future studies will further evaluate the application of this stability analysis method in system planning and parameter design.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material. Further inquiries can be directed to the corresponding author.

Author contributions

ST conceived the article and edited the manuscript. JL and XD edited the framework and logic of the manuscript. HY edited the introduction and abstract. YC edited the grammar. All authors contributed to the article and approved the submitted version.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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Supplementary material

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