Soft switching modulation strategy based on bipolar (PSM) with improved efficiency in high-frequency link inverters

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High Frequency-Link (HFL) Inverters have been employed to integrate renewable energy sources into utility grids and electric vehicles. The soft-switching range of High-Frequency Link Inverters (HFLI) is increased using auxiliary inductors and capacitors. The application of auxiliary components increases the conduction loss and the complexity of the circuit. The literature indicates that the existing soft-switching methods suffer from higher duty cycle loss, voltage spikes, and lower efficiency owing to the resonance between the parasitic capacitance of switches and the leakage inductance of the transformer. Therefore, it is imperative to develop a modulation strategy that can improve the efficiency of HFLI. In this context, the proposed study develops a cycloconverter-type High-Frequency Link Inverter (CHFLI) based on a Bipolar Phase Shift Modulation (BPSM) strategy without the use of auxiliary components. The proposed modulation strategy enables the semiconductor switches to operate under zero voltage switching. The full-bridge inverter and Full Bridge Active Clamper Circuit (FBAC) switches operate at the same gating signals with a constant duty cycle of 50%. The proposed topology uses built-in magnetizing inductance to achieve zero voltage switching and reduce the duty cycle loss. The leakage energy is recycled from the output filter inductor to the load side using the FBAC. The results indicate that the proposed modulation strategy achieves ZVS and simultaneously achieves an efficiency of 95%. The proposed modulation strategy is easy to implement and does not require complex circuitry.

KEYWORDS

soft switching, high-frequency-link (HFL) inverter, bipolar (PSM), full bridge active clamper circuit (FBAC), zero voltage switching (ZVS)

1 Introduction

Growing concerns over environmental issues and diminishing fossil fuels have stimulated the progress of Renewable Energy Resources (RES), such as photovoltaics, wind, and fuel cells. This development has attracted the attention of utilities worldwide, leading to a greater integration of RES into the utility grid. However, this integration necessitates the use of grid-tied inverters (Faranda et al., 2015; Pinto et al., 2016; Iyer et al., 2017; Meng et al., 2017). The most recent developments in inverters lack performance,

FIGURE 1
Conventional inverter with Commercial Line Frequency Transformer.
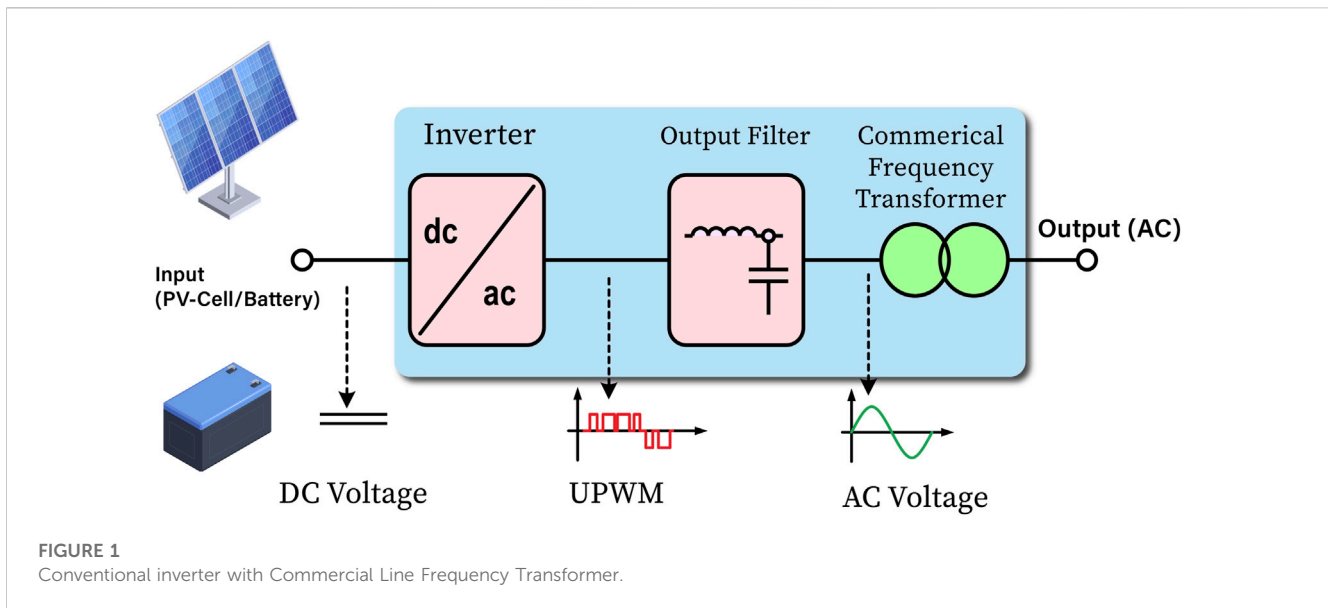
efficiency, and power density (Qinglin et al., 2005). Inverters with line-frequency isolation transformers as depicted in Figure 1, are common in conventional utility grids. Therefore, this approach increases the inverters' size, volume, and cost, which in turn jeopardizes the power density and efficiency.

Inverters that employ HFL are designed to incorporate High-Frequency Transformers (HFT) for isolation. This arrangement offers advantages, such as reduced weight, smaller volume, higher power density, miniaturization, lower cost, excellent reliability, and improved efficiency, as highlighted in (Guo et al., 2018; Nayak et al., 2019; Wu et al., 2023). In addition to RES, HFL inverters have been extensively utilized in compact power conversion-based modules for applications in naval, space, and energy storage systems (Mazumder and Rathore, 2011). HFLI inverters are categorized into three groups based on their power conversion stages and circuit structures. The first structure is the conventional HFL inverter, which comprises three steps that insert an HFT between the DC/AC and AC/DC stages as given in Table 1, the configuration I. Conventional HFL inverters typically have three power conversion stages, resulting in reduced efficiency and increased inverter size owing to a bulky intermediate LC filter with high cost (Kan et al., 2014; Zhu et al., 2014; Zhou et al., 2018). The conventional inverter design has been modified to reduce both the size and cost; this modification involves the removal of the intermediate LC filter, which is typically bulky and costly. The alternative is given in Table 1, with configuration II, and is referred to as a rectifier-type high-frequency link (RHFL) inverter (Guo et al., 2018; Chen et al., 2016a).
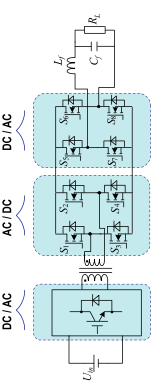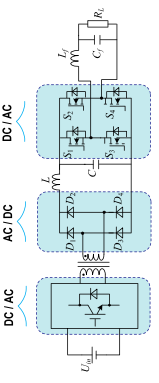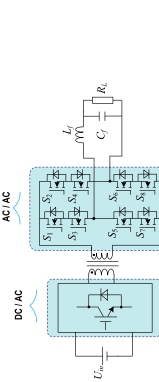
Eliminating the LC filter reduces the inverter size; however, as a result, the DC-pulsating output poses a challenge in devising a modulation approach for the inverter (Zhou et al., 2018). Multiple clamping circuits have been suggested in the existing literature to enhance the effectiveness of pulsating DC voltage removal on the secondary side, as referenced in (Huang and Mazumder, 2008; Wang et al., 1999). The Cycloconverter-type high-frequency link inverter (CHFLI) topology is composed of a primary-side inverter and a secondary-side cycloconverter with a high-frequency transformer (HFT) interposed between them, is given in Table 1,

with configuration III, and is known for its high efficiency, compact size, and lightweight characteristics (Kan et al., 2014; Zhu et al., 2014; Zhou et al., 2018; Yamato et al., 1990).

The CHFL is commonly utilized in standalone photovoltaic systems that require a high level of efficiency to offset the low efficiency of photovoltaic panels (Rocabert et al., 2004). In a previous work (Aganza-Torres and Cárdenas, 2011) a high-frequency link inverter with a multiple carrier modulation scheme for low-power (RES) applications was presented. However, during the commutation period of cycloconverter switches, zero crossing distortion was observed in output voltage. Two types of modulation techniques are utilized in CHFL inverters to enhance the efficiency of switching operations and enable natural commutation for bidirectional switches in cycloconverters (Guo et al., 2018; Zhu et al., 2014; Tao et al., 2021). The primary modulation techniques used by inverters to generate gating signals are Unipolar Pulse Width Modulation (UPWM) and bipolar pulse-width modulation (BPWM) (Zhu et al., 2014; Kan et al., 2014; Mazumder et al., 2010; Yan et al., 2012; Basu and Mohan, 2014).

The three-level output generated by the Unipolar Pulse Width Modulation (UPWM) technique is a frequently applied modulation strategy for a Cascaded H-Bridge Full-bridge (CHFL) inverter. This approach enables bidirectional cyclo-converter switches to achieve natural commutation during the zero level of the modulation signal, thereby facilitating efficient Zero Voltage Switching (ZVS) (Guo et al., 2018; Guo et al., 2016). A Unipolar Pulse Width Modulation (UPWM)-based soft-switching push-pull high-frequency link inverter was proposed in (Chen et al., 2016a). Owing to the rectification of the modulating signal, the output voltage quality was inappropriate (Chen et al., 2016a). A PSM-type UPWM-based inverter was proposed in (Guo et al., 2016), which does not require rectification of the modulating signals, but two auxiliary inductors were used to extend ZVS range at light load conditions. Addition of auxiliary inductor increases the component count for inverter. The inverter proposed in (Guo et al., 2016) has low power level, and cannot be used in renewable energy applications.

TABLE 1 Types of high-frequency link inverters.

	Configuration I	Configuration II	Configuration III
Definition	Conventional HFL inverter	Rectifier-type high-frequency link (RHFL) inverter	Cycloconverter-type high-frequency link (CHFL) inverter
Structure			
Applications	Electrical Vehicles (EV), Utility Grid, Uninterruptable Power Supply (UPS)	Utility Grid, Uninterruptable Power Supply (UPS), Electrical Vehicles (EV)	Energy storage systems, Naval, Space, Utility Grid
Limitations	Reduced efficiency, Bulky intermediate LC filter, Increased inverter size	DC-pulsating output, Complex Modulation Scheme	Hard Switching and Complex Modulation Scheme

The commutation of the load current in the cycloconverter continues to yield voltage spikes on bidirectional switches (Guo et al., 2018; Wang et al., 2018). Overlap commutation switching techniques have been implemented in previous studies (Mazumder and Rathore, 2011; Zhu et al., 2014; Guo et al., 2016) to achieve zero voltage switching (ZVS) of bidirectional switches in cycloconverters. However, a resonance issue arises between the leakage inductance of the transformer and the output capacitance of the bidirectional switches, leading to electromagnetic interference (EMI) (Gandikota and Mohan, 2014; Korkh et al., 2019; Wang et al., 2022).

In (Yamato et al., 1990), switches on both the primary and secondary sides were subjected to hard-switching conditions, resulting in elevated switching losses during high-frequency applications. The authors in (Zhou et al., 2018; Wang et al., 1999) proposed a primary-side phase-shift full-bridge inverter and a secondary-side active clamp circuit (ACC) to achieve soft switching. In (Zhu et al., 2022), primary full bridge inverter switches were operated under hard switching conditions, and the duty cycle of the (ACC) switches is not fixed at 50%, but instead varies from 0 to 1. However, it is challenging for primary-side switches to achieve soft switching under light-load conditions (ul Hassan et al., 2021). In (Guo et al., 2018), a proposal is presented for a high-frequency link inverter of the cycloconverter-type that utilizes wide-range soft-switching high-efficiency (UPWM) technology. The asymmetric phase-shift modulation strategy (APSM) was proposed in (Xiao et al., 2023) to extend the ZVS range; however, it increases the complexity of the modulation circuit. The paper in (Azizipour and Hojabri, 2023) presents a Push Pull type high-frequency link inverter with primary and secondary side switches that undergo hard switching. The resulting output voltage contains a significant amount of harmonics. The proposal of high-frequency link inverter utilizing space vector modulation (SVM) is given in (Jin et al., 2023) aimed to alleviate the current stress on cycloconverter switches, despite the operation of semiconductor switches under hard switching conditions. A de-recoupling based model predictive control scheme for high-frequency link inverters was introduced in (Fu et al., 2022), but it requires complex analytical calculations to determine the optimal vector for generating switching signals.

In (Guo et al., 2018; Sabate et al., 1991), the authors used an auxiliary inductor on the primary side of the full-bridge inverter to achieve the zero voltage switching (ZVS) range of the primary switches. The auxiliary circuit amplifies the complexity and expense of the system (Zhong et al., 2018). Unipolar Pulse Width Modulation (UPWM) creates the problem of zero-crossing distortion and a narrow pulse on the transformer's primary side (Guo et al., 2018; Zhu et al., 2014; Guo et al., 2016). Leakage inductance is another factor contributing to duty cycle loss, resulting in a decreased effective duty cycle on the secondary side. The duty cycle on the primary side of the inverter is indicated by D, where ΔD represents the loss of the duty cycle, as shown in Eq. 1, (Zhao et al., 2015). Furthermore, the effective duty cycle is expressed as d_{eff}. The calculation of duty cycle loss depends upon various factors, including leakage inductance L_{lk}, switching frequency f_s,

primary and secondary current I_{p1}, and input voltage. The duty-cycle loss is calculated using Eq. 2, (Mazumder et al., 2010).

$$D = D_{eff} + \Delta D \qquad (1)$$

$$\Delta D = \frac{2L_{lk}f_s\left(I_{p1} + I_{p2}\right)}{V_{in}} \qquad (2)$$

The voltage ratio of the transformer input to output depends on the effective duty cycle, as determined by Eq. (3), (Guo et al., 2016).

$$\frac{V_{out}}{V_{in}} = \frac{N_p}{N_s}D_{eff} \qquad (3)$$

A comprehensive review of the literature shows that various HFLI topology-based topologies have been employed in the existing literature. However, they suffer from the following limitations.

- Existing studies (Guo et al., 2018; Zhu et al., 2014; Guo et al., 2016) have adopted the Unipolar Pulse Width Modulation (UPWM)-based soft-switching strategy, which suffers from higher duty-cycle losses. During the switched-on state, a voltage drop occurs across the switches, and energy is lost in the form of heat.
- The available literature (Nayak et al., 2019; Wang et al., 2018) indicates that ZVS can be achieved at higher loads; however, to achieve ZVS at lighter loads, the leakage inductance is increased by adding an additional inductor or capacitor. The addition of auxiliary components increases the complexity of the circuit.
- The existing literature (Nayak et al., 2019; Korkh et al., 2019) indicates that losing zero voltage switching (ZVS) significantly increases switching and conduction losses. Voltage spikes are also generated owing to the resonance between the parasitic capacitance and transformer leakage inductance.

Therefore, the proposed study utilizes a Bipolar Phase Shift Modulation (BPSM) strategy with the development of a soft-switched cycloconverter-type high-frequency link inverter (HFLI). The contributions of this study are as follows.

- Development of an efficient cycloconverter-based BPSM to achieve ZVS with minimal duty cycle loss.
- Development of a full-bridge active clamper circuit for minimizing the voltage stress on the cyclo-converter switches and simultaneously recycling the leakage energy of the inductor output filter.
- Design of simplified and practically feasible Bipolar Phase Shift modulation (BPSM) strategy that enables the operation of all switches at a constant duty cycle of 50%.
- The performance of the proposed BPSM modulation strategy is benchmarked against some recent and widely used state-of-the-art modulation strategies.

The bipolar (PSM) modulation has a lower total harmonic distortion (THD) and exhibits better output voltage quality when compared to other modulation techniques. The modulation scheme utilizes only one reference signal and one carrier signal, which facilitates easy implementation. Additionally, the proposed modulation strategy does not exhibit pulse drops around the zero crossing of the output voltage, thereby minimizing duty cycle loss.

As a result of these advantages, bipolar PSM has a higher efficiency and lower distortion in the output voltage.

The remainder of this paper is organized as follows. Section 2 discusses the proposed topology and respective modulation technique. Section 3 presents the operation modes of the proposed topology and modulation strategy. Section 4 examines the soft-switching, steady-state conditions of the switches and efficiency of the proposed topology. Finally, Section 5 presents the conclusions of the study.

2 Methodology

2.1 Proposed modulation strategy

The circuit diagram of the proposed high-frequency link inverter topology is shown in Figure 2. The V_{dc} shows the input DC voltage on the primary side and, T shows the High-frequency transformer for isolation purpose. The topology comprises a full-bridge inverter at the primary side and two bypass capacitors; C_1 and C_2. The bypass capacitance is calculated using Eq. 4, (Guo et al., 2018).

$$C_1 = C_2 = \frac{25T_s^2}{8L_m} \qquad (4)$$

The proposed full bridge inverter configuration comprises of four MOSFET switches, represented as $S_{p1} - S_{p4}$. The high-frequency transformer transfers power from the primary side to the secondary side, and serves the purpose of isolation. The magnetizing inductance is denoted by L_m, while leakage inductance referred to as the secondary, is symbolized as L_{k1} and L_{k2}. To obtain a bipolar phase shift square voltage at the secondary side of the transformer, the maximum flux density is determined using a specific Eq. 5, (Guo et al., 2018).

$$B_{max} = \frac{V_{dcMAX}}{4N_1f_sA_e} \qquad (5)$$

The full wave cyclo-converter type configuration is formed by the switches $M_1 - M_4$ which convert bipolar high-frequency secondary voltage to low frequency. FBAC comprises of four MOSFET switches, C_p represent the clamping capacitor, purpose of C_p is to recycle inductor energy. While L_f and C_f operate the low pass filter at the cyclo-converter side. The value of L_f and C_f is determined using Eqs 6, 7
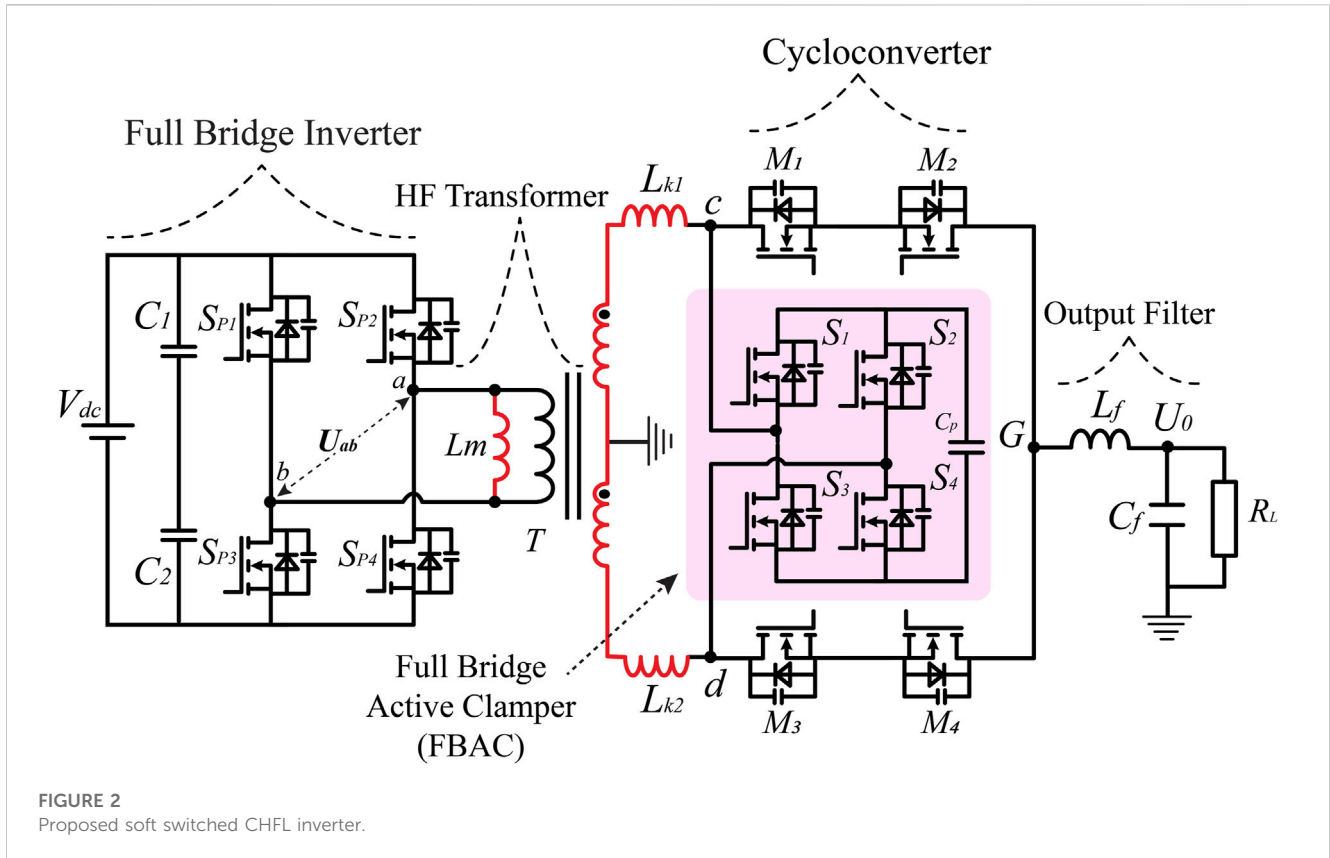
$$L_f = \frac{V_iV_{rms}}{4f_{sw}P_o} \qquad (6)$$

$$C_f = \frac{16}{\pi^2 f_s^2 L_f} \qquad (7)$$

A resistive load, denoted by R_L, is connected to the output of a low-pass filter

2.2 Proposed modulation strategy

The proposed new bipolar phase shift modulation strategy is presented in Figure 3, where V_c represents the carrier sawtooth

FIGURE 2
Proposed soft switched CHFL inverter.

signal of voltage, while V_m denotes the modulating or control signal of voltage. The magnitudes of V_c and V_m is determined using Eq. 8 & Eq. 9

$$v_{ms}(t) = M_a \sin \omega_o \tag{8}$$

$$v_{cs}(t) = \begin{cases} 2\omega_c t/\pi - 1 & 0 \leq \omega_s t \leq \pi \\ \dfrac{2(\omega_c t - \pi)}{\pi} - 1 & \pi \leq \omega_s t \leq 2\pi \end{cases} \tag{9}$$

The primary full bridge inverter switches are driven by comparing the carrier and modulating signals, with the primary switches being operated at a 50% duty cycle ratio. The gating signals for switches S_1/S_4 and S_2/S_3 are complementary, with a small amount of dead time inserted between them. Deadtime enables semiconductor switches to not turn OFF or ON simultaneously, which can damage the circuit. The driving signals for the FBAC are similar to those of the primary full-bridge inverter switches, and it is demonstrated that the switching frequency of all driving signals is twice that of the carrier signal. The gating signals for switches $M_1 - M_4$ in a cycloconverter are generated by comparing the carrier and modulating signals, with a certain degree of phase shift about the primary side inverter switches. The gating signals for switches M_1/M_2 and M_3/M_4 are complementary. The U_{cd} refers to the bipolar high-frequency voltage acquired at the transformer's secondary side, while the U_G symbolizes the bipolar voltage at the end side of the cycloconverter. The I_{lm} parameter represents the magnetizing current of the transformer on the primary side, facilitating the completion of soft switching

for the full bridge inverter switches. The output voltage at the load side, denoted as U_o, is acquired through a low pass filter.

2.3 Switching signal generation strategy

The proposed gating signal generation strategy for creating gating signals for semiconductor switches is illustrated in Figure 4. This process involves the use of two comparators to generate a clock signal for two flip-flops. The upper Comparator-I receives the carrier and modulating signals at its input. C_1 and C_2 are input clock signals for flip flops, C_1 is output of comparator-I, where C_2 is obtained by inverting C_1.The data input for D-flip-flop-I and D-flip-flop-II are derived from the output of Comparator-II. The gating signals for cycloconverter switches $M_1 - M_4$ are obtained from the output of D-flip flop-I, while the gating signals for switches $S_{p1} - S_{p4}$ and $S_1 - S_4$ are obtained from D-flip-flop 1.

3 Operational principle of the proposed inverter

The operational principle of the proposed inverter is presented by assuming that all MOSFET switches are ideal and that their output capacitances are uniform. t_{d1}, t_{d2}, and t_{d3} denote the duration of the dead time between the switching events. The frequency of the modulating signal is much lower than the carrier signal frequency. The proposed inverter's operational modes are partitioned into discrete periods,
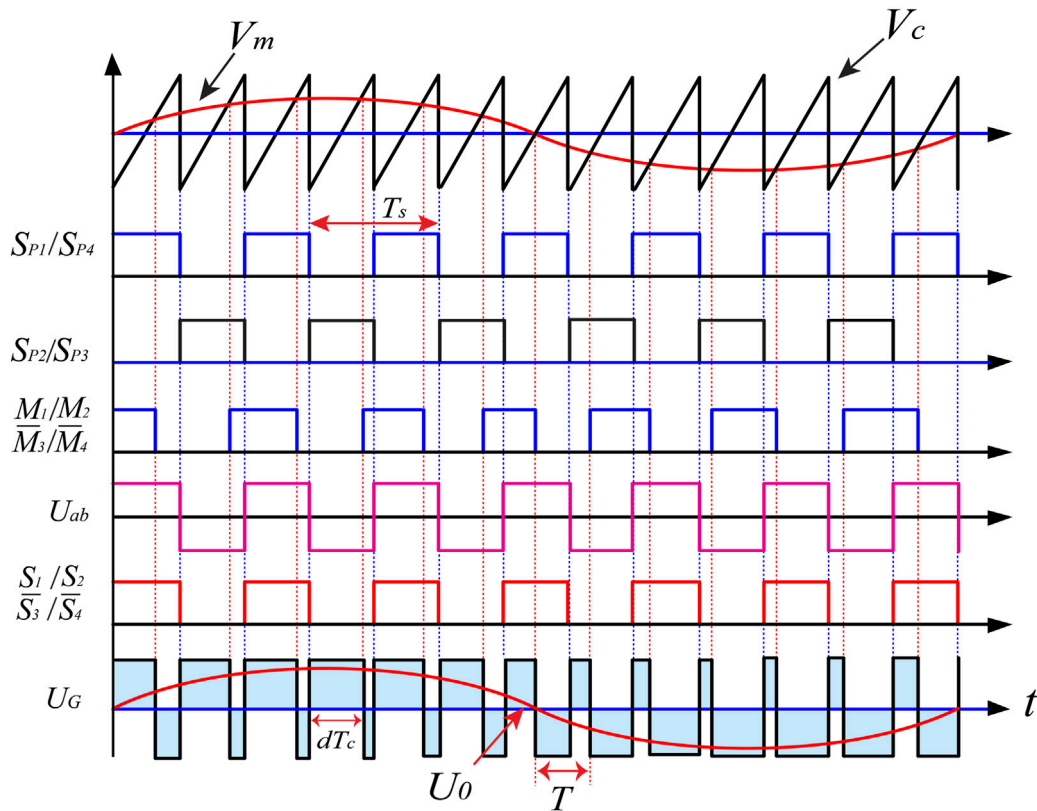
FIGURE 3
Modulation waveforms of Proposed BPSM.
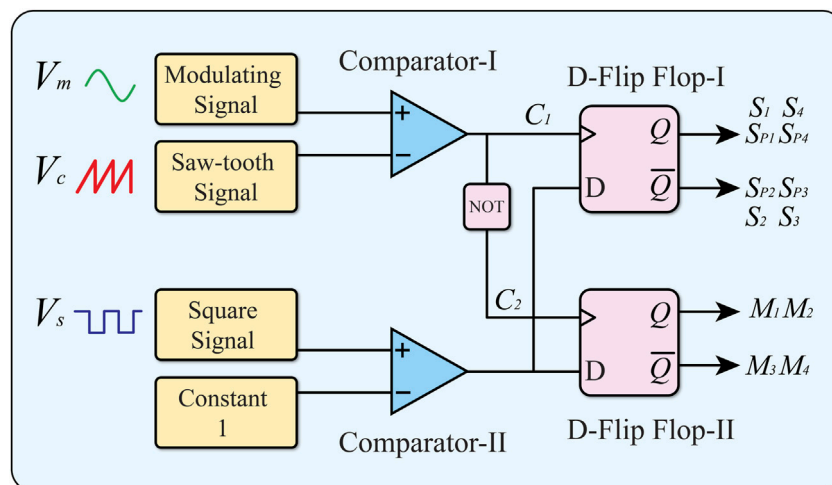
FIGURE 4
Gating signal diagram for proposed BPSM.

precisely ten in number, characterized as t_0 through t_{10}. The former five modes are discussed in detail, whereas the latter five modes are symmetrical with the former five modes. Schematic waveforms during the operation of (CHFLI) employing the proposed modulation strategy are shown in Figure 5.

Equivalent circuits for the corresponding five modes are given in Figure 6

Interval 1 $[t_0 - t_1]$: In the first interval, denoted as $t_0 - t_1$, the transformer operates in a mode where both the primary and secondary voltages, U_{ab} and U_{cd}, exhibit negative polarity. The output voltage

FIGURE 5
Operation modes of proposed inverter.

(U_G), is positive, and specific switches, namely, S_{p1}/S_{p4}, S_1/S_4, and M_3/M_4, are conducting, while all other switches remain inactive. During this mode, power is transferred from the primary to the secondary side, and the clamping capacitor (C_p) discharges energy. In this operational mode, the prim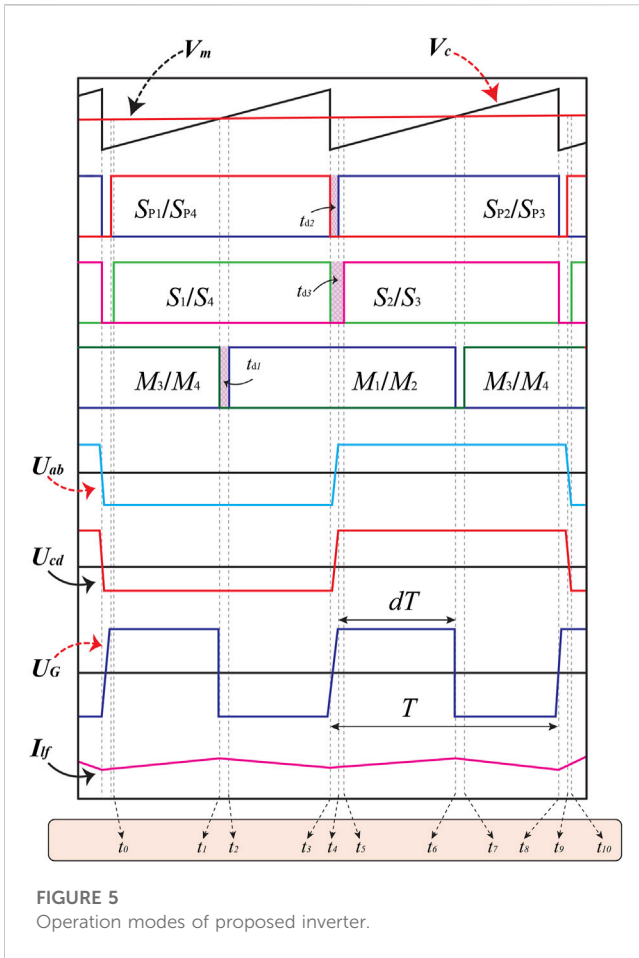ary current and magnetizing current of the transformer exhibit periodic alternations between positive and negative magnitudes. The output capacitor is charged during this time frame, through the leakage inductance current i_{lk1}, and the voltage across it is presented by Eq. 10. The equivalent circuit for mode $[t_0 - t_1]$ is given in Figure 6A

$$V_P(t) = l_{k1}\frac{di}{dt}l_{ki}(t) + Ri_{lk1}(t) \qquad (10)$$

The expression for the current i_{cp} flowing through the clamping capacitor is presented in Eq. 11

$$i_{cp}(t) = -i_{Lk1}(t) = i_{Lk2}(t) - i_{Lf}(t) \qquad (11)$$

The voltage V_{cp}, present across the clamping capacitor can be determined using Kirchhoff's voltage law, where ω_r represents the angular frequency

$$v_{CP}(t) = \left(\frac{V_{dc}}{n} - k\right)\cos\omega_r(t - t_0) + \frac{I_{cp}}{\omega C_P}\sin\omega_r(t - t_0) \qquad (12)$$

Interval 2 $[t_1 - t_2]$: In this operational state, the M_3/M_4 switches are turned OFF as shown in Figure 6B. Cycloconverter lower switch

M_3 is in OFF state during this interval, so the voltage across clamping capacitor (C_p) is presented in Eq. 13

$$V_{CP}(t) = V_{DC} - L_f\frac{d_{iLf}}{dt} \qquad (13)$$

Where V_{DC} is the input DC voltage, i_{Lf} is the current through inductor L_f. M_4 switch is also turned OFF, and amount of voltage through clamping capacitor C_p is calculated by the equation Eq. 14

$$V_{CP}(t) = -L_f\frac{d_{iLf}}{dt} \qquad (14)$$

This results in the discharge of the output capacitance (switch S_2) through the inductor current; there by facilitating a soft switching condition for S_2. Meanwhile, the inductor current charges the output capacitance of switch S_3. The remaining switches maintain their previous state, whereas the output voltage of the cycloconverter reverses from positive to negative.

Interval 3 $[t_2 - t_3]$: In this time frame, the activation of switches M_1/M_2 results in the achieving (ZVS), since the voltage across the output capacitances (from drain to source) is zero, and the output voltage is oriented in a negative direction. While switches S_{p1}/S_{p4} and S_1/S_4 are in a conduction state. The corresponding equivalent circuit for interval 3 is shown in Figure 6C.

Interval 4 $[t_3 - t_4]$: During this mode, it is observed that the switches S_{p1}/S_{p4} and S_1/S_4 are in the off state as given in Figure 6D. Additionally, t_{d2} is identified as the deadtime duration between the lagging and leading legs of the primary side full bridge converter. The output capacitances of switches S_{p1} and S_{p4} have been charged, while the output capacitances of switches S_{p2}/S_{p3} have been discharged, which ensures that the next conducting switch can achieve zero voltage switching. In this mode, the direction of the voltage on the primary side of the transformer and the output of the cycloconverter change from negative to positive. Additionally, the magnetizing current value on the transformer's primary side decreases.

Interval 5 $[t_4 - t_5]$: S_{p2}/S_{p3} are activated in this operational state, given that the output capacitance of S_{p2}/S_{p3} has been completely discharged in the previous state. As a result, both switches are activated with zero voltage switching. Additionally, the output capacitance of S_2/S_3 is discharged in this mode to enable zero voltage switching in the following state. The voltages of both the primary and secondary transformers increased positively. Intervals between $t_6 - t_{10}$ are identical to that of modes $t_5 - t_{10}$. The equivalent circuit for mode $[t_4 - t_5]$ is given in Figure 6E.

4 Results and discussion

A Simulink model is designed in MATLAB 2021b to demonstrate the effectiveness of the proposed topology; the values and parameters of the various components utilized in the model are listed in Table 2.

4.1 ZVS of full bridge inverter switches

The amount of power lost during hard switching of the MOSFET switches is given by Eq. (15).

FIGURE 6
Equivalent Circuits of Operational Modes in one switching cycle **(A)** Interval 1 $[t_0 - t_1]$ **(B)** Interval 2 $[t_1 - t_2]$ **(C)** Interval 3 $[t_2 - t_3]$ **(D)** Interval 4 $[t_3 - t_4]$ **(E)** Interval 5 $[t_4 - t_5]$.
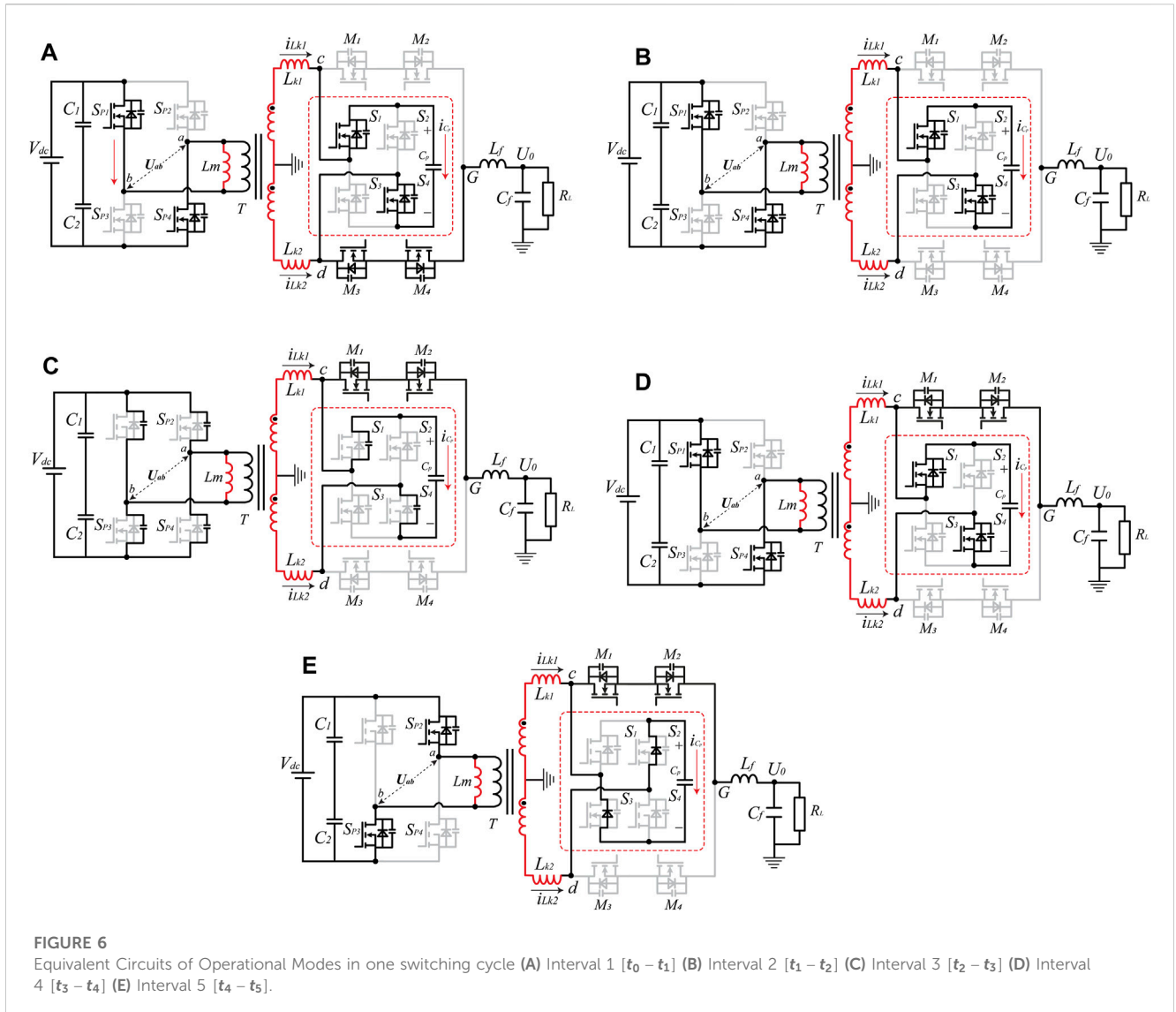
$$P_{loss} = \frac{1}{2} V_{ds} I_{ds} t_{on} f_{sw} \qquad (15)$$

ZVS of Full bridge inverter switches depends mainly on magnetizing inductance current I_{Lm}. Zero voltage switching is achieved by driving the voltage to zero during the turn-on time to reduce switching loss. The overlap between the drain-to-source and gate-to-source voltage is reduced by using the proposed topology magnetizing inductance. The voltage is zero during the ON transition, as shown in Figure 7A. Switches S_{p1} & S_{p3} attains ZVS throughout the whole duty cycle, and the inverter losses are minimized. The magnetizing current provides soft switching of switches and is presented in Eq. 16. The magnetizing inductance value can be obtained using Eq. 17. Figure 7A shows the ZVS of primary side full bridge inverter switch S_{p1}, S_{p3}

$$I_{Lm} = \frac{U_{in}}{4 L_m f_s} \qquad (16)$$

$$L_m = \frac{V_{in}(1-D)N_P}{N_S I_{lfout} 0.5 F_s} \qquad (17)$$

TABLE 2 Circuit parameters for simulation.

Components	Parameters
Input DC Voltage V_{dc}	320 V
Magnetizing Inductance L_m	40 μH
Load Resistance R_L	20 Ω
Filter Inductor L_f	33 mH
Filter Capacitor C_f	280 μF
Switching Frequency f_s	50 kHz
Output Voltage V_{ac}	170 V rms
Clamp Capacitor C_P	1 μF

The equivalent energy must be present to discharge the switches' output capacitance, as given in Eq. (18)

$$\frac{1}{2} L_k (i_{Lk})^2 \geq C_{oss}(V_{in})^2 \qquad (18)$$

FIGURE 7
Zero Voltage switching **(A)** (ZVS) waveforms of Full Bridge Inverter S_{p1}, S_{p3} **(B)** (ZVS) waveforms of Clamper switches S_2, S_3 **(C)** (ZVS) waveforms of Cycloconverter Switches M_1, M_4.
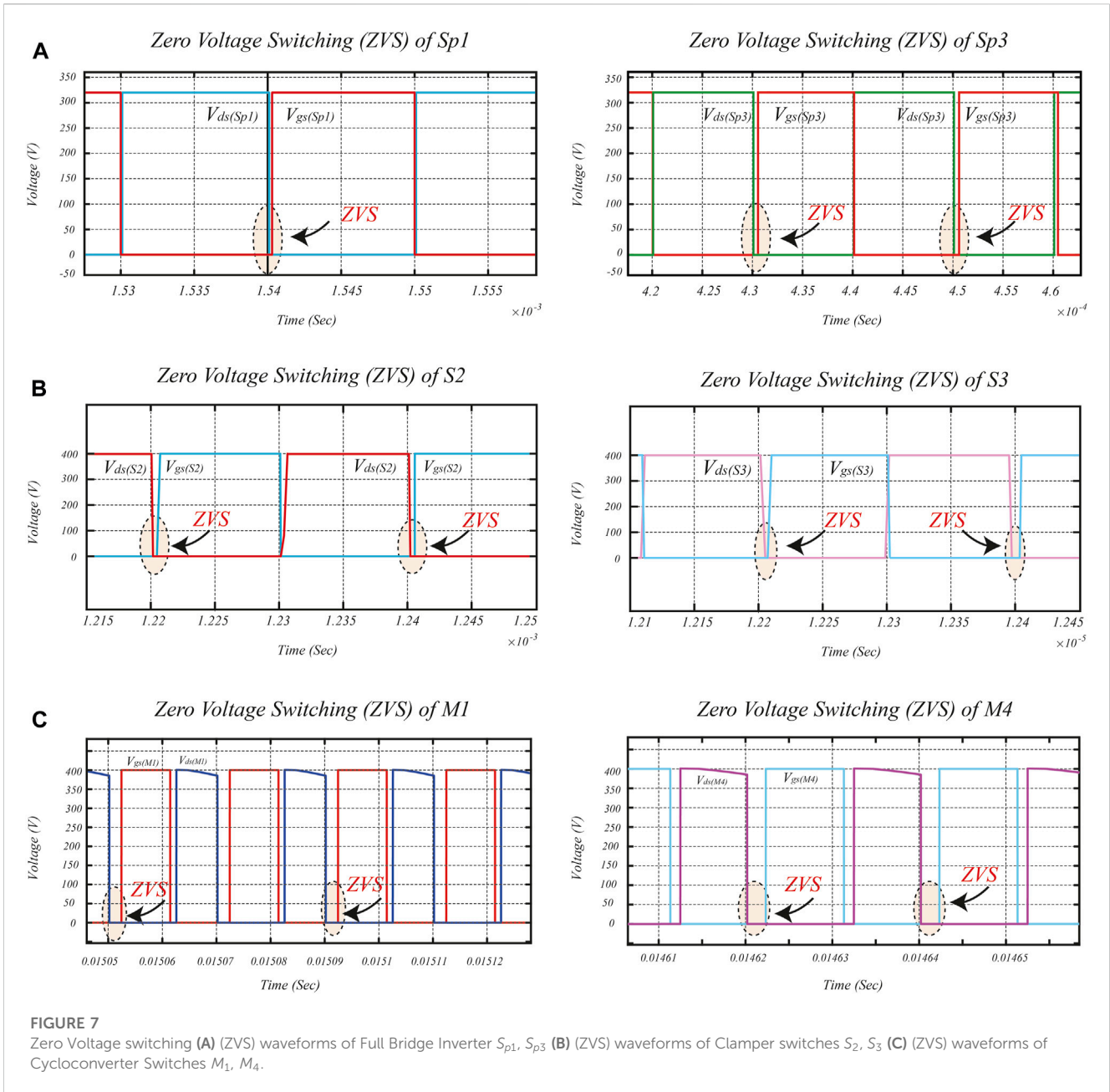
4.2 ZVS of full bridge active Clamper Switches

The zero voltage switching (ZVS) waveform of the Full Bridge Active Clamper (FBAC) switches S_2 and S_3 across the complete spectrum of the output voltage is illustrated in Figure 7B. The zero voltage switching (ZVS) characteristic of switches is contingent upon the accurate computation of leakage inductance L_k value, which can be determined using Eq. 19
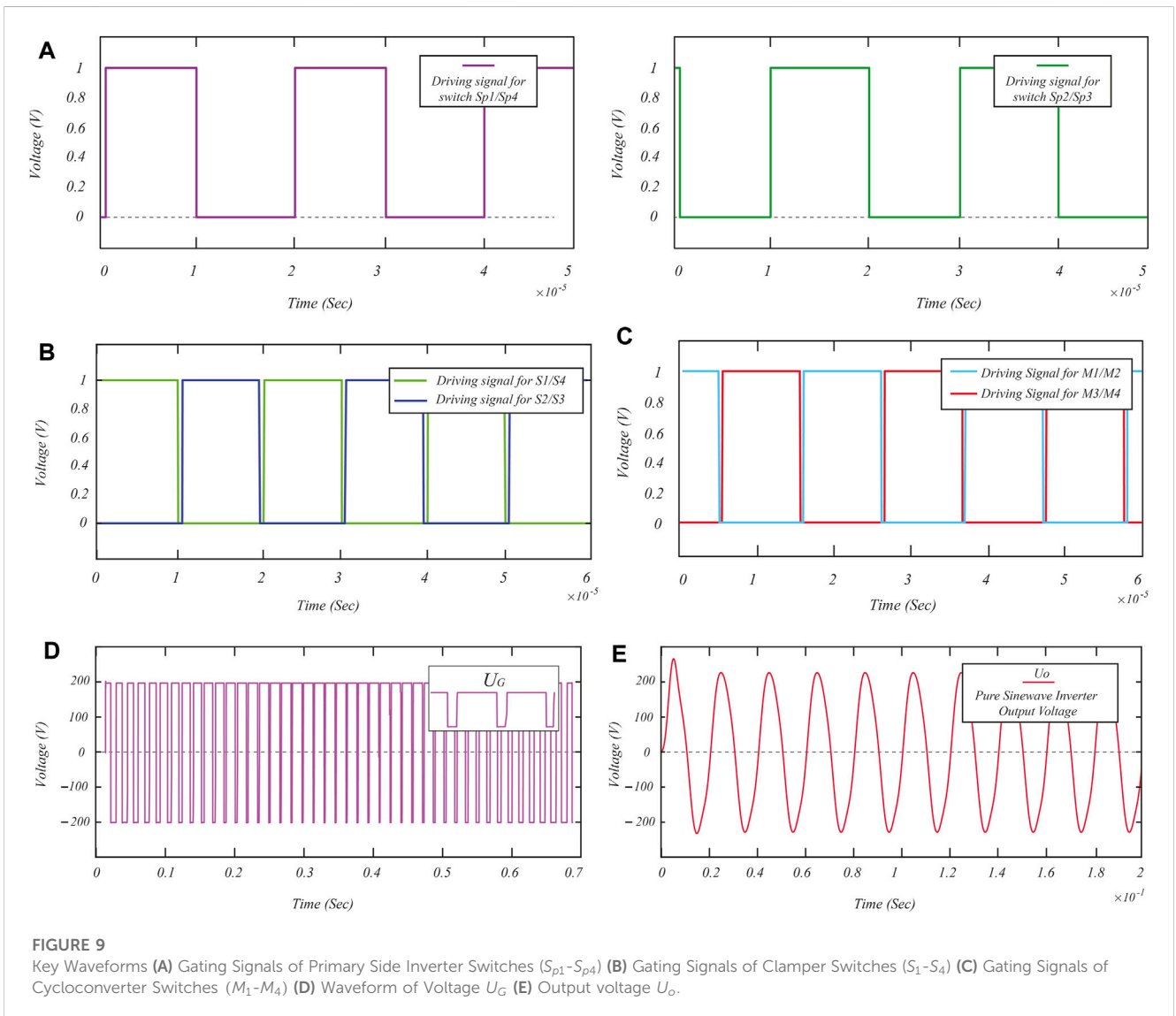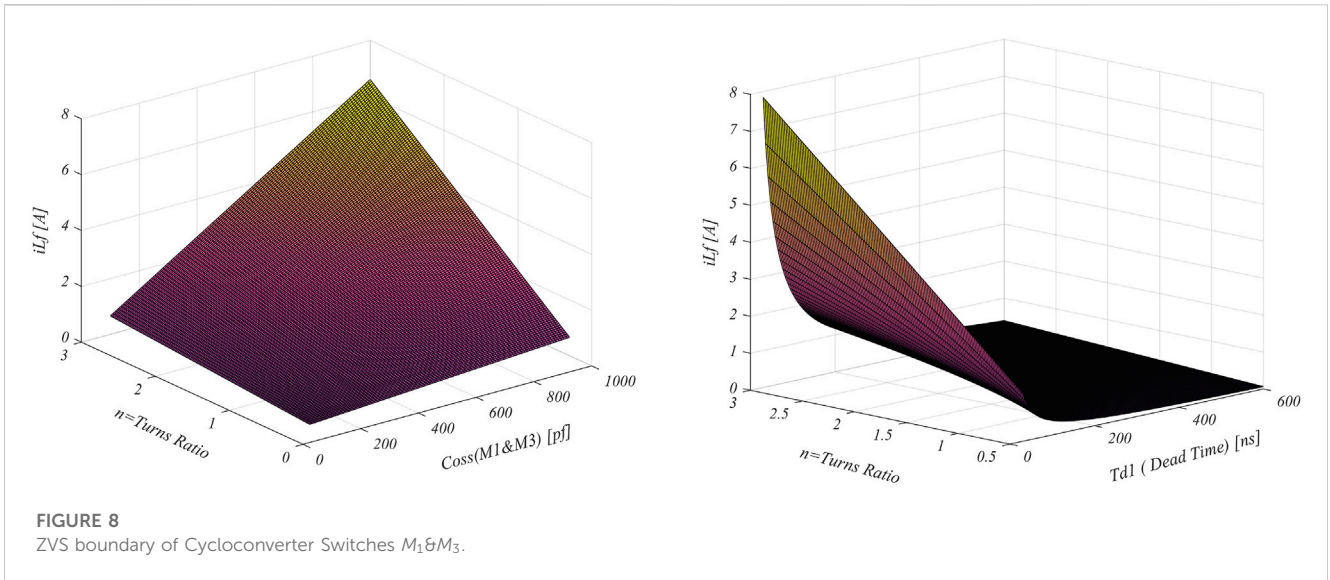
$$\begin{cases} \frac{1}{2}L_k i_{\text{Lk}}^2 > \frac{1}{2}\left(C_{\text{oss},S_2} + C_{\text{oss},S_3}\right)V_{\text{in}}^2 \\ \frac{1}{2}L_k i_{\text{Lk}}^2 > \frac{1}{2}\left(C_{\text{oss},S_1} + C_{\text{oss},S_4}\right)V_{\text{in}}^2 \end{cases} \quad (19)$$

Consequently, a substantial increase in the ZVS range can be achieved by increasing the value of the leakage inductance. Switch S_2

achieves (ZVS) during dead time t_{d3}. It is observed that increase in leakage inductance L_k value results in higher deadtime value. Thus (ZVS) of (FBAC) switches can be achieved with smaller leakage inductance L_k value. Figure 7B shows the ZVS of (FBAC) switches S_2 & S_3.

4.3 ZVS of cyclo-converter switches

The voltage across the parasitic capacitance of the cycloconverter switch is observed to be zero, which leads to the switches achieving the zero voltage switching (ZVS) state during the deadtime period t_{d1}, as depicted in Figure 7C. The ZVS condition referred to the upper switches (M_1 and M_2) of a cycloconverter can be attained by equating the voltage at points C and G. ZVS of cycloconverter switches depends on output voltage U_0 and output

FIGURE 8
ZVS boundary of Cycloconverter Switches M_1&M_3.

FIGURE 9
Key Waveforms **(A)** Gating Signals of Primary Side Inverter Switches (S_{p1}–S_{p4}) **(B)** Gating Signals of Clamper Switches (S_1–S_4) **(C)** Gating Signals of Cycloconverter Switches (M_1–M_4) **(D)** Waveform of Voltage U_G **(E)** Output voltage U_o.

FIGURE 10
(A) Comparison of output voltage U_o with UPWM and BPSM strategy **(B)** Comparison of Primary U_{ab} and Secondary Voltage U_{cd}, Comparison of steady state waveforms for Conventional (HFL) and Proposed Inverter **(C)** Proposed Inverter U_{cd} voltage **(D)** Conventional HFL inverter U_{cd} voltage **(E)** U_{cd} voltage with unipolar (PSM) **(F)** U_{cd} voltage based on Unipolar (PSM) without clamper circuit.

filter inductance L_f. Minimum value of output voltage U_0 ensures the wide ZVS range of cycloconverter switches (M_1-M_4). Figure 7C shows the ZVS waveform of cycloconverter switch M_1 and M_4

The boundary conditions ensuring ZVS condition of cycloconverter switches $M_1 - M_4$ are presented in Eq.20 & Eq.21.

$$-I_{lf}T_{d1} > V_{cd}(M_{1coss} + M_{4coss}) = nV_{dc}(M_{1coss} + M_{4coss}) \quad (20)$$

$$-I_{lf}T_{d1} > V_{cd}(M_{2coss} + M_{3coss}) = nV_{dc}(M_{2coss} + M_{3coss}) \quad (21)$$

ZVS boundary of cycloconverter switches, $M_1 \& M_3$ during Turn-on depends on values of output filter inductor current I_{lf}, dead time T_{d1}, parasitic capacitance C_{oss} of cycloconverter switches, and transformer turn ratio n. ZVS range can be extended with higher value of output filter inductor current I_{lf}, higher value of dead time

T_{d1} and with small value of parasitic capacitance of cycloconverter switches as shown in Figure 8. It is also observed the transformer turns ratio also effects the ZVS range of switches, at smaller value of transformer turns ratio, ZVS range of switches can be increased.

4.4 Steady-state waveforms

The driving signals for switches $S_{p1} - S_{p4}$ are identical to those of signals for $S_1 - S_4$ switches, with difference of a small amount of dead time incorporated between them; as shown in Figure 9A. The waveforms of the driving signals $M_1 - M_4$ and $S_1 - S_4$ switches are presented in Figures 9B, C. U_G is a bipolar PWM voltage at the
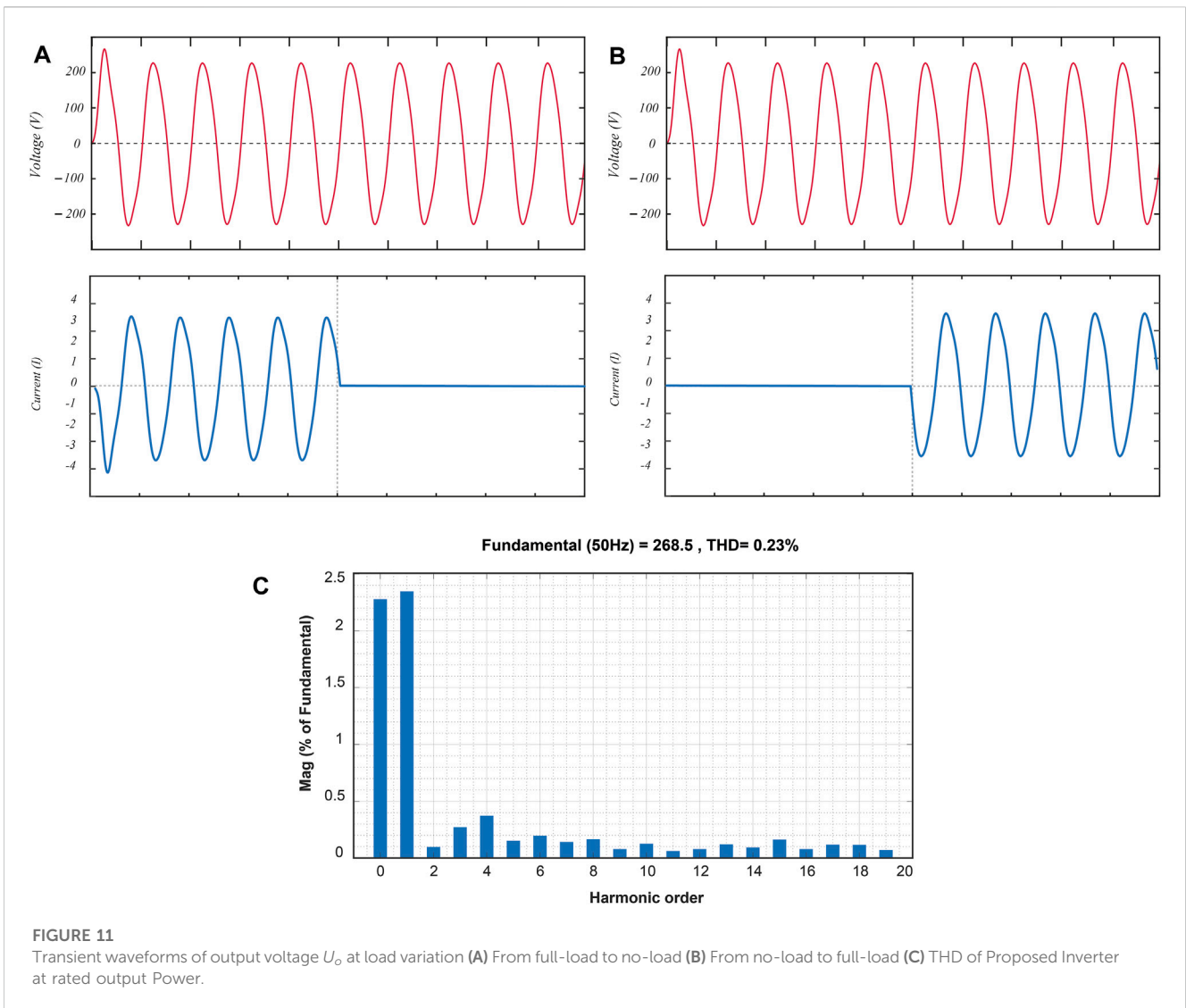
FIGURE 11
Transient waveforms of output voltage U_o at load variation **(A)** From full-load to no-load **(B)** From no-load to full-load **(C)** THD of Proposed Inverter at rated output Power.

output of the cycloconverter, it has a higher frequency. Waveform of U_G is shown in Figure 9D. It is clear that the proposed inverter produces a high-quality pure sine waveform without distortion. The simulation waveform of the output voltage U_o at a resistive load is shown in Figure 9E.

The following Eq. 22 can mathematically represent the U_o

$$U_o = \frac{nE}{2V_p} v_{in} \qquad (22)$$

Unipolar Pulse Width Modulation (UPWM) creates a narrow pulse at the zero crossing of the output voltage (Zhu et al., 2014). It is observed that if the rise-ON time of the semiconductor switch is higher than that of a narrow pulse, then this narrow pulse is lost. In the case of the BSPM, there was no loss of a narrow pulse. As shown in Figure 10A, V_{loss} shows the difference in voltage that is caused by duty cycle loss. The voltage between a full bridge inverter's leading and lagging legs, specifically U_{ab}, While U_{cd} shows the secondary voltage of the transformer. The comparison between U_{ab} and U_{cd}, proves that there is no loss of duty cycle on the secondary side voltage and is presented in Figure 10B. U_{ab} & U_{cd} in terms of duty cycle D are given as in Eq. 22 & Eq.23.

$$U_{ab} = DV_{DC} \qquad (23)$$
$$U_{dc} = (1-D)V_{DC} \qquad (24)$$

The comparison of steady state waveforms for a conventional high frequency link inverter and the proposed inverter is also presented in Figure 10. In Figure 10C, the transformer secondary voltage of the proposed inverter based on Bipolar (PSM) with a clamper circuit is depicted, which shows there is no any voltage spike on transformer secondary side voltage. Conventional high frequency link inverter when operated at high switching frequency without clamper circuit, high value voltage spikes are created, many times larger than nominal voltage, as shown in Figure 10D. The steady state waveforms for the conventional high frequency link inverter when operated under Unipolar modulation are presented in Figures 10E, F.

The transient behaviour of the proposed inverter is analysed from full-load to no-load and no-load to full-load conditions verified using the simulation results. Output voltage U_o waveform validates that the proposed inverter works well without creating any spikes on output voltage. The transient waveform, when resistive load is suddenly changed from 0 to full and *vice versa* is presented in

TABLE 3 Benchmarking of proposed inverter against dc-ac UPWM based inverter.

Ref	No. of active switches	No. of diodes	Modulation technique	Soft switching	Use of auxiliary components	Duty cycle loss	Efficiency (%)	Power density
Zhu et al. (2014)	12 IGBTs	2	UPWM	Partly ZVS	0	Yes	89	Low
Kan et al. (2014)	9 IGBTs,4 MOSFETs	0	UPWM	Partly ZYS	0	Yes	92	Low
Guo et al. (2018)	12 MOSFETs	0	UPWM	Wide ZVS Range	1 Auxiliary Inductor	No	93.6	High
Chen et al. (2016b)	3 MOSFETs / 4 IGBTs	1	UPWM	Partly ZVS	0	Yes	91	Middle
Mazumder et al. (2010)	20 MOSFETs	0	UPWM	Partly ZVS	0	No	92	High
Guo et al. (2016)	12 MOSFETs	0	UPWM	Wide AVS Range	2 Auxiliary Inductor	Yes	93	High
Zhu et al. (2022)	12 MOSFETs	2	UPWM	Hard Switched	0	Yes	93.5	Middle
Proposed	12 MOSFETs	0	BPSM	Wide AVS Range	0	No	95	High

Figures 11A, B. Harmonic spectrum of proposed inverter at rated power and output voltage is shown in Figure 11C. THD value is 0.23% at fundamental frequency.

4.5 Benchmarking against recent UPWM strategies

For the practical implementation of a High-Frequency Link Inverter (HFLI), it is imperative to consider the problems related to the realization of a wide ZVS range, voltage spikes on cycloconverter switches, duty-cycle loss, and high leakage inductance. Various solutions have been reported in the literature (Guo et al., 2018; Zhu et al., 2014); however, all require additional components (i.e., Diodes, Auxiliary inductors, and capacitors). Additional components make the topology more complex; therefore, practical realization is difficult. Moreover, sufficient leakage inductance energy is required to discharge the parasitic capacitance of semiconductor switches. Under light loads, an auxiliary inductor is required to achieve a Wide ZVS range. The proposed strategy uses magnetizing inductance to realize a wide ZVS range, without the addition of any auxiliary inductor.

Different Active clamp circuits (ACC) have been reported in the literature (Wang et al., 1999; Mazumder et al., 2010) to suppress voltage spikes. However, the control schemes for operating ACC are complex, and the ZVS of ACC switches is difficult to realize. The proposed Full Bridge Active Clamper circuit (FBAC) has 50% duty cycle control signals. It is possible to realize a wide range of ZVS without relying on the load current, and reduced conduction and duty cycle loss lead to higher efficiency and higher power density.

The features of our proposed (BPSM) based (CHFLI) with other recently developed topologies and modulation strategies are presented in Table 3.

The efficiency of the proposed inverter is shown in Figure 12. It can be observed that the highest efficiency of the proposed inverter is higher than that of the inverter in (Zhu et al., 2014), which simultaneously improves the power density. The proposed inverter is controlled using a simple modulation strategy that achieves zero voltage switching (ZVS) over a wide load range.
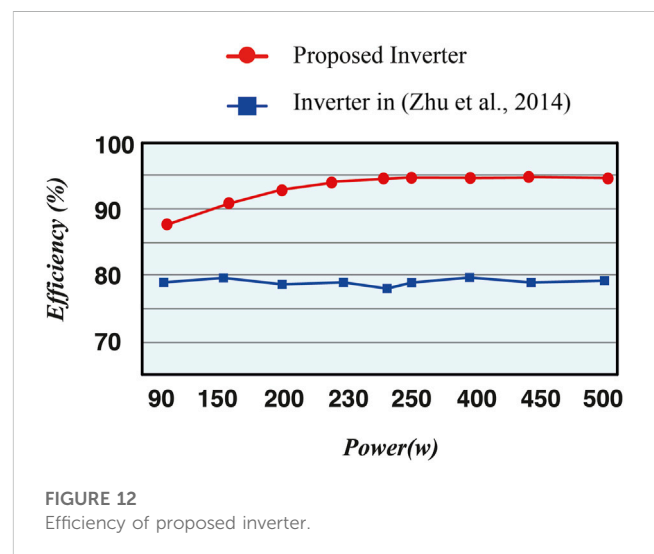

FIGURE 12
Efficiency of proposed inverter.

5 Conclusion

HFLI inverters are used for the integration of renewable sources with smart grid networks. Recently developed HFLI designs have auxiliary components; therefore, these strategies suffer from complex designs and high duty cycle losses. The proposed design focuses on a High-frequency link inverter featuring a novel bipolar phase shift modulation strategy (BPMS). To facilitate the operation of primary full-bridge inverter switches at 50% duty cycle while ensuring zero voltage switching (ZVS). The proposed design was comprehensively investigated through operational modes, modulation strategies, and soft-switching analysis of power semiconductor switches employed in circuit configurations. It is observed that the proposed topology experience lower duty cycle loss. The Full Bridge Active Clamper (FBAC) circuit was designed precisely to solve the problem of voltage spikes and stress on the secondary side of cycloconverter switches. One of the key advantages of FBAC is its ability to recycle energy from the output filter inductor back to either the DC or the AC side. The simulation results verified that the ZVS of semiconductor switches has been achieved without any auxiliary component. The proposed scheme achieves an efficiency of 95% and minimum duty cycle losses. In the future, the proposed modulation strategy can be extended to achieve a higher efficiency with advanced and sophisticated power electronic switches.

Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

Author contributions

Conceptualization AsA and JS. Writing, reviewing, and editing AsA GY, PH, visualization AsA, AmA. All authors contributed to the article and approved the submitted version.

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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