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A dual source fed eleven level switched capacitor multilevel inverter with voltage boosting capability

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This work introduces an 11-level switched-capacitor multilevel inverter (SCMLI) designed for solar photo-voltaic (PV) applications, capitalizing on the growing popularity of multilevel inverters due to their superior power quality. With a 1.67-times boosting capability, the proposed SCMLI employs 10 switches, 2 DC supplies, and 2 capacitors to achieve an 11-level output voltage waveform. The topology requires only seven driver circuits, incorporating 2 bidirectional switches and 3 complementary pairs of switches. The proposed inverter has intrinsic capacitor self-balancing features since the capacitors are connected across the DC voltage source at different times throughout a basic cycle to charge the capacitors at a level of input voltage. A thorough comparison between the topology and recently developed SCMLI's has been presented. The comparison demonstrates the effectiveness in terms of switches, capacitors, sources, efficiency, total standing voltage (TSV), and boosting capacity. To experimentally validate its performance, the suggested SCMLI undergoes testing using a frequency-based switching method. The topology exhibits low total harmonic distortion (THD) of 7.65% in its output voltage waveform and 0.89% in the output current waveform.

KEYWORDS

multilevel inverter, switched-capacitor topology, total standing voltage, voltage boosting, inverter, solar photo-voltaic

1 Introduction

In the advancement of electric vehicles (EVs), High-Voltage Direct Current (HVDC), renewable energy system, and microgrids technology the multilevel inverters (MLIs) play crucial and prominent role. The MLIs inverter has many distinguishing advantages over two-level inverters, including reduced dv/dt characteristics, improved efficiency, improved EMC, flexibility, and significant fault tolerance capabilities. The requirement for more switches, capacitors, diodes, dc sources, and other components increases under increased voltage stress. However, this significantly increases the size and cost of MLIs. There is a lot of discussion about traditional multilevel converters such as the cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) (Jayabalan et al., 2017; Khenar et al., 2018). These structures need a lot of components, which makes the system bigger, heavier, and more difficult to regulate. Thus, prompting

researchers to look towards structures with a lesser number of components (Gupta et al., 2016; Vemuganti et al., 2021).

Switched-diode, switched-source, and switched-capacitor MLIs (SCMLI) are the three main categories of reduced component structures (RCSs) with the fewest sources and larger boosting capabilities. According to Siddique et al. (2019), the switched-source structure has multiple sources, and the levels in the output voltage are produced by adding their magnitudes algebraically. In Hosseinzadeh et al. (2021), the second arrangement makes use of diodes to link several sources to the load. The third structure also uses capacitors and DC sources. The capacitors are kept at a constant ripple factor and discharge occur during the cycle of operation. The production of the necessary levels in Samadaei et al. (2019) and Iqbal et al. (2020) are achieved by the addition and subtraction of source and capacitor voltages. One method of charging the capacitors is to either connect them in parallel with the source, as shown in Mohamed Ali and Krishnasamy (2019) and Jagabar Sathik et al. (2020), such that the source voltage and the voltage of the capacitor are the same. Utilizing the redundant states of the inverter operation table, as shown in Vahedi et al. (2016) and Sharifzadeh and Al-Haddad (2019), is another option for charging the capacitors. These inverters may be used to integrate rooftop solar photovoltaic (PV) systems for home use into the grid or to power solar-powered irrigation systems (Ali et al., 2021).

Both symmetric and asymmetric RCSs are possible. For higher levels, sources of different magnitudes are often used. For instance, in Chappa et al. (2021), symmetrical sources may provide an output of 9 levels, but asymmetrical ratios of 1:2 and 1: 3 can produce outputs of 13 and 17 levels, respectively. Additionally, boosting may be accomplished with a lot of work by using the right sources and/or capacitor combinations (Ye et al., 2021). Ideal MLI should use lesser components and produce higher output voltage levels. The literature discusses capacitors and single-source asymmetrical inverters. The packed U-cell (PUC) inverter, which combines the CHB and FC topologies, is one of the simplest circuits (Ounejjar et al., 2011). The voltage across the capacitor is kept at half of the DC source ($V_{dc}/2$) or one-third of the DC source ($V_{dc}/3$), respectively, by using one capacitor, six switches, and one source to provide five or seven level output voltage, respectively. To maintain the voltage across the capacitor using the PI controller, a sensor is needed for a 5-level PUC, a sensor-less operation using redundant states was suggested in Vahedi et al. (2016). In Panda et al. (2021), the authors have used twelve switches and a total of five capacitors to develop an 11-level inverter, which employs an auxiliary circuit to handle the intricate control logic. The inventors of Priyadarshi et al. (2020) decreased the number of switches for the same number of levels to 10, but it still needs a lot of capacitors and diodes such as nine capacitors and nine are required. In Tayyab et al. (2022), the authors present an eleven-level inverter with a five-time boost. Although the topology has boosting ability, it has a higher THD and also uses a larger number of driver circuits as compared to the proposed topology. Thus, it increases the requirement for a larger size filter and also increases the overall cost of the inverter. Due to lower THD and fewer driver circuits, the requirement for filter size is reduced, which also makes the topology more cost-effective. For active and reactive power control of grid, the authors present a dual-source, asymmetrical, eleven-level inverter in Tayyab et al. (2023). Even though the topology has a higher efficiency and a lesser number of devices, it also has a higher THD of nearly 12.0%, no boosting capability, and a high minimum required input voltage to operate as compared to the inverter presented in this paper. For energy storage and smart grid applications, a novel switched capacitor multilevel inverter topology with lesser direct current (dc) supply requirement which can operate both in symmetric and asymmetric mode has been presented in Hussan et al. (2020) and a dual-source, cross-connected, asymmetrical 15-level switched-capacitor multilevel inverter novel topology with lesser switch count and number of drivers is presented in Hussan et al. (2021a). An eleven-level inverter topology using two DC sources, eight insulated gate bipolar transistors with antiparallel diodes, two bi-directional power semi-conductor switches, two diodes, and two capacitors is shown in this article.

The remainder of this work is structured as follows. The eleven-level MLI circuit and its functioning are covered in Section 2. Section 3 provides information on the inherent balance of capacitors and capacitance determination. The Nearest Level Control Pulse Width Modulation (NLCPWM) technique is covered in depth in Section 4 to improve the performance of the proposed inverter. The loss analysis of the proposed topology is illustrated in Sections 5. The suggested topology is also contrasted with current 11-level topologies in Section 6. The results were confirmed using MATLAB/SIMULINK and have been affirmed on an experimental setup in Section 7. The application of proposed multilevel inverter in solar PV system is discussed in Section 8. Lastly, Section 9 brings this article to a conclusion.

2 Proposed switched-capacitor topology and analysis

This section discusses the modelling and analysis of proposed 11-level SCMLI. Figure 1A depicts the suggested 11-level inverter topology. The following are the main elements of the proposed MLI: Two bi-directional (S_5 and S_6) and eight unidirectional switches (S_1, S_2, S_3, S_4, S_7, S_8, S_9, and S_{10}), two asymmetrical DC sources in magnitude ($V_1 = V_{dc}$ and $V_2 = V_{dc}/2$), two diodes, and two capacitors (C_1 and C_2), which inherently balance at V_{dc}. Figure 1B shows the 11-level output voltage waveform with a voltage boost of 1.6. The output voltage waveform has a voltage level of 0, $\pm V_{dc}/2$, $\pm V_{dc}$, $\pm 3V_{dc}/2$, $\pm 2V_{dc}$, and $\pm 5V_{dc}/2$ across the load. Three complementary switch pairs are included in the suggested topology: S_1 and S_2, S_3 and S_4, and S_7 and S_8. The switches should not be turned on at the same time in order to avoid short-circuit situation.

2.1 Operation of proposed 11-level topology headings

In this section, the operation of proposed 11-level SCMLI is presented. The conduction patterns for each switching condition are illustrated in Table 1 and Figures 2A–K. The impact of various switching states has been noted for easier understanding of proposed SCMLI. The entries “1” and “0” in Table 1 represents

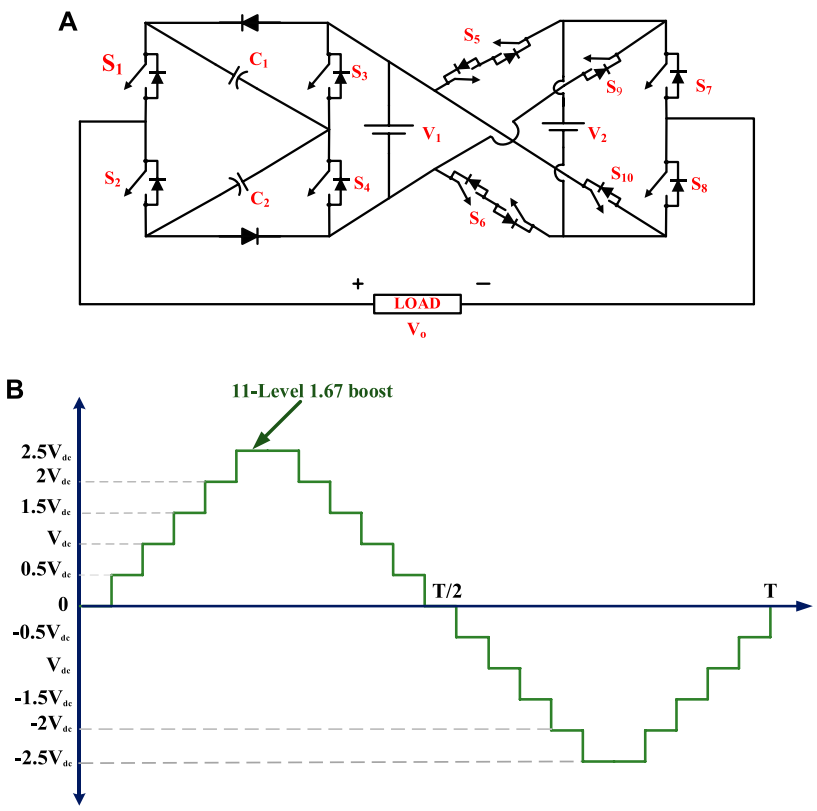

FIGURE 1
(A) Proposed 11-level inverter topology, **(B)** 11-level output voltage waveform.

TABLE 1 Switching State for proposed 11-Level SCMLI.

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	(V_o)	C_1	C_2
1	1	0	1	0	0	0	0	1	1	0	$2.5V_{dc}$	DCH	CH
2	1	0	1	0	0	1	0	1	0	0	$2\ V_{dc}$	DCH	CH
3	1	0	1	0	1	0	0	1	0	0	$1.5\ V_{dc}$	DCH	CH
4	1	0	1	0	1	0	1	0	0	0	$1\ V_{dc}$	DCH	CH
5	1	0	0	1	1	0	0	1	0	0	$0.5\ V_{dc}$	CH	NC
6	1	0	0	1	1	0	1	0	0	0	0	CH	NC
7	0	1	1	0	1	0	0	1	0	0	$-0.5\ V_{dc}$	NC	CH
8	0	1	0	1	0	1	0	1	0	0	$-1\ V_{dc}$	CH	DCH
9	0	1	0	1	1	0	0	1	0	0	$-1.5\ V_{dc}$	CH	DCH
10	0	1	0	1	1	0	1	0	0	0	$-2\ V_{dc}$	CH	DCH
11	0	1	0	1	0	0	1	0	0	1	$-2.5\ V_{dc}$	CH	DCH

the on and off states of corresponding switches. The letters "CH", "DCH," and "NC" stands for the respective capacitors' charging, discharging, and no change, respectively. The suggested topology voltage levels for the positive half cycle are shown in Figures 2A–F. The conduction route is shown by black lines, and the non-conducting path by grey lines.

2.2 Working of the topology for different voltage level states

In this section, the working of proposed SCMLI is discussed. The following steps are used to acquire the various positive output voltages:

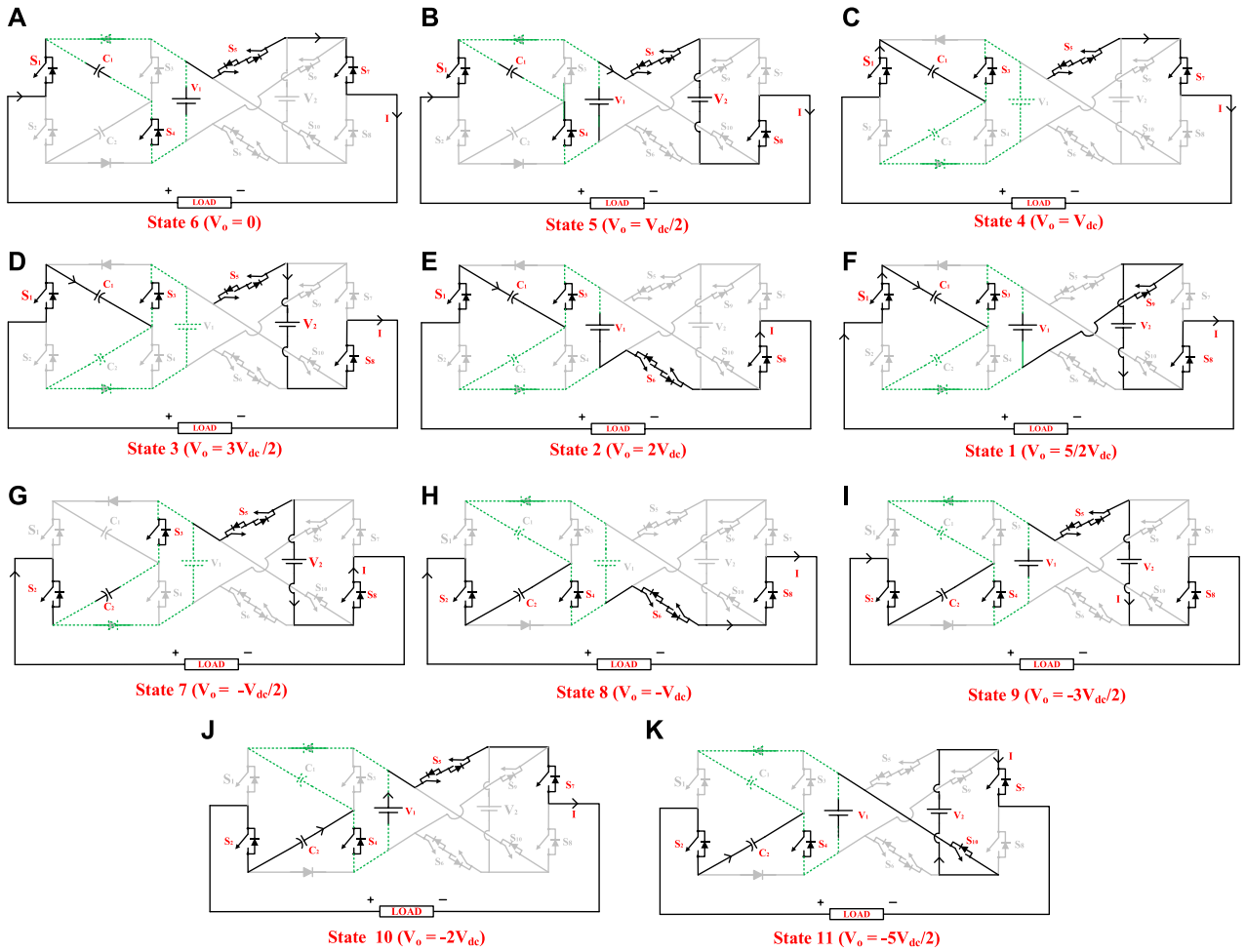

FIGURE 2
Positive and negative half cycle states of proposed 11-level inverter topology: **(A)** $V_o = 0$, **(B)** $V_o = 0.5V_{dc}$, **(C)** $V_o = 1V_{dc}$, **(D)** $V_o = 1.5V_{dc}$, **(E)** $V_o = 2V_{dc}$, **(F)** $V_o = 2.5V_{dc}$ **(G)** $V_o = -0.5V_{dc}$, **(H)** $V_o = -1V_{dc}$, **(I)** $V_o = -1.5V_{dc}$, **(J)** $V_o = -2V_{dc}$, **(K)** $V_o = -2.5V_{dc}$.

2.2.1 Zero voltage level

In this case, as shown in Figure 2A, only four switches (S_1, S_4, S_5, and S_7) are conducting according to the state number 6 of Table 1, so the output voltage across the load is 0. The output voltage can be zero only when C_1 is already charged to V_1. This can be understood by the given relation ($V_o = V_{C_1} - V_1$). In this state, the capacitor C_1 starts charging from V_{dc}.

2.2.2 0.5 V_{dc} level

The output voltage level for this state is $V_{dc}/2$, which can be achieved by turning on four switches S_1, S_4, S_5, and S_8 according to the state number 5 of Table 1. The conduction diagram for this level is shown in Figure 2B. In this state, C_1 is also conducting, and the two DC sources with different strengths are kept at V_{dc} and $V_{dc}/2$.

2.2.3 1 V_{dc} level

In accordance with switching state number 4 of Table 1, the necessary switches (S_1, S_3, S_5, and S_7) are turned on, utilizing the energy stored in capacitors C_1 to produce this level. The output voltage level for this state is V_{dc}, as illustrated in Figure 2C. In this state, the capacitor C_2 continues to charge.

2.2.4 1.5 V_{dc} level

The 1.5 V_{dc} level, whose conduction diagram is illustrated in Figure 2D, is generated by activating switches S_1, S_3, S_5, and S_8 as per the switching state number 3 of Table 1. During this state, the energy stored in capacitor C_1 is utilized to supply the required power to the load terminals.

2.2.5 2V_{dc} level

Figure 2E shows the conduction diagram for the level generation where the output voltage across the load is 2V_{dc}. This can be reached by switching on S_1, S_3, S_6, and S_8 as stated by state number 2 of Table 1and using the energy stored in capacitor C_1 along with the $V_1 = V_{dc}$ input supply.

2.2.6 2.5 V_{dc} level

This level is achieved by turning on four switches (S_1, S_3, S_8, and S_9) only, as well as utilizing the energy stored in C_1 and the two DC supplies (V_1 and V_2) as per using the switching state number 1 of Table 1. It's conduction diagram is depicted in Figure 2F.

Correspondingly, the conduction diagram for the negative half cycle is shown in Figures 2G–K. All possible levels can be achieved

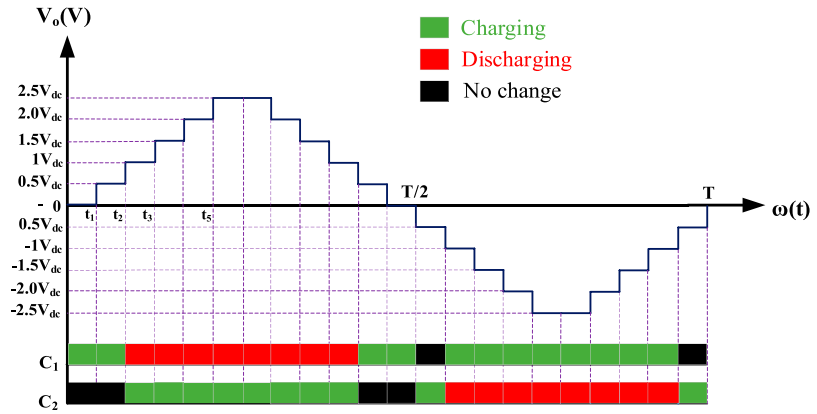

FIGURE 3
Staircase output with capacitor voltage pattern.

by turning on the respective switches seen in Table 1. The dotted green line depicted in the conduction diagram symbolizes the charging trajectory during each state of operation.

3 Capacitor voltage balance and capacitance calculation

Figure 3 displays each charging and discharging time period of the capacitors C_1 and C_2. Since the charging circuit of the proposed topology only contains diodes, switches, and capacitors; thus load characteristics have no impact on the charging interval of the capacitors (Hussan et al., 2021b). Therefore, in a cycle's capacitor charging and discharging periods are equal. As a result, regardless of the loading state, the self-voltage balance of both capacitors is maintained. The optimal value of the capacitors is determined by taking into account their Longest Discharging Period (LDP), nominal frequency, lowest voltage ripple, and highest fundamental load current.

The charging and discharging of the i^{th} capacitor's value may be calculated using Eq. 1.

$$Q_{C_i} = \int_{t_2}^{t_1} I_{lo}(t)dt \tag{1}$$

Where the LDP $= t_2 - t_1$

Using LDP for C_1, we can say that the maximum rate of discharge for capacitor C_1 during $[t_2, \frac{T}{2} - t_2]$ can be calculated using Eq. 2.

$$\Delta Q_{C_1} = \frac{1}{\omega}\int_{t_2}^{\frac{T}{2}-t_2} I_{lo}(t)dt \tag{2}$$

where the load current is represented by I_{lo} and ω is the output voltage frequency which is equal to $2\pi f$. Since, the LDP for capacitor C_1 is the same as that for capacitor C_2 i.e., $[t_2, \frac{T}{2} - t_2]$

$$\Delta Q_{C_1} = \Delta Q_{C_2} = \frac{1}{\omega}\int_{t_2}^{\frac{T}{2}-t_2} I_{lo}(t)dt \tag{3}$$

Using Eq. 3, the values of capacitors C_1 and C_2 can be calculated as

$$C_1 = C_2 = \frac{\Delta Q_{C_{1,2}}}{\Delta V_{C_{1,2}}} = \frac{1}{\omega \times \Delta V_{C_{1,2}}}\int_{t_2}^{\frac{T}{2}-t_2} I_{lo}(t)dt \tag{4}$$

The solution of Eq. 4 gives the optimal value of the capacitors by assuming the maximum permitted ripple voltage ΔV_C equal to 10% of the corresponding capacitor voltage.

4 Nearest level control pulse width modulation (NLCPWM)

Various control schemes have been tried and employed for multilevel inverters. The Nearest Level Control Pulse Width Modulation (NLCPWM) is a low-switching-frequency PWM approach, whose incorporation is simpler for higher levels (Hussan et al., 2020). Here, the suggested topology uses NLCPWM to govern the switching signals and generate the necessary output waveform. In NLCPWM, a sampled waveform is formed by comparing the standard sinusoidal waveform with the desired output waveform. To create switching pulses for the related IGBTs, the resulting waveform is then rounded off to the nearest level and analyzed using the switching logic shown in Table 1. Figures 4A, B depict the NLCPWM's operating system. For this 11-level topology, the standard signal, which is a sine wave, has an amplitude of 5 and is assumed to have a frequency of 50 Hz.

5 Power loss analysis

For the proposed SCMLI topology, three different forms of losses—conduction loss, switching loss, charging or ripple loss—are taken into account.

5.1 Conduction or ohmic loss (P_{cl})

The internal resistances of the devices infiltrate the conduction route and create an ohmic loss. P_{cl} for other levels can be computed using the corresponding circuit diagram for that level. Taking into

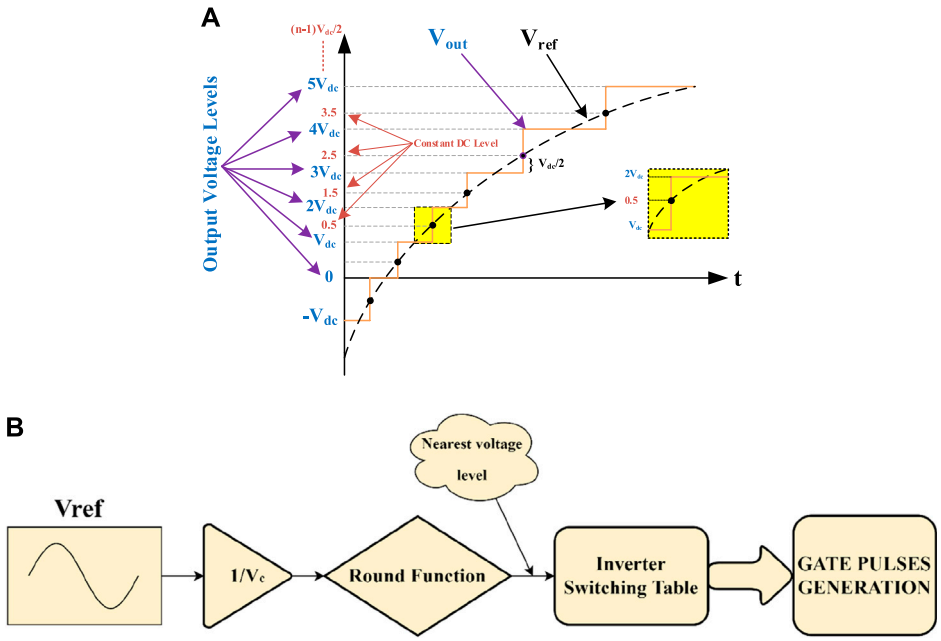

FIGURE 4
(A) Level generation method and **(B)** control scheme of NLCPWM.

account all voltage levels allow one to calculate the overall ohmic loss of the suggested topology. Ohmic loss is expressed as

$$P_{cl} = I_{lo}^2 (aR_s + bR_d + cR_c) \tag{5}$$

where in Eq. 5, I_{lo} = the load current, R_s is the on-state switch resistance, R_d is the diode resistance, R_C is the capacitor's internal resistance, and a, b, and c are the numbers of switches, diodes, and capacitors in the corresponding level's conduction route.

5.2 Switching loss (P_{sl})

Switching losses arise as a result of the switches' switching activity. Taking into account the voltage and current of a linear switch at the time of switching, the switching power loss during the turn-on operation can be written using Eq. 6.

$$P_{sl,ON} = f\int_0^{t_{ON}} v(t)i(t)dt = f\int_0^{t_{ON}} \left(\frac{V_s}{t_{ON}}t\right)\left(-\frac{I_k}{t_{ON}}(t - t_{ON})\right)dt = \frac{1}{6}fV_sIt_{ON} \tag{6}$$

Power loss during the switching off procedure may be stated using Eq. 7.

$$P_{sl,OFF} = f\int_0^{t_{OFF}} v(t)i(t)dt = f\int_0^{t_{OFF}} \left(\frac{V_s}{t_{OFF}}t\right)\left(-\frac{I'}{t_{OFF}}(t - t_{OFF})\right)dt = \frac{1}{6}fV_sI't_{OFF} \tag{7}$$

where I represent the switch current when it is turned on, I' is the current flowing through the switch when it is turned off, V_s is the switch's withstanding voltage, and f is the switching frequency. Overall switching loss of the suggested topology may be estimated by multiplying the number of on switching states (N_{ON}) by the number of off switching states (N_{OFF}) in one entire cycle by Eqs 8, 9, yielding Eq 10:

$$P_{sl} = \sum_{k=1}^{N_{SW}}\left(\sum_{m=1}^{N_{ON}} P_{sl,ON,km} + \sum_{m=1}^{N_{OFF}} P_{sl,OFF,km}\right) \tag{8}$$

5.3 Ripple or charging loss (P_{rl})

The loss occurring from the capacitor's charge is known as the ripple loss or charging loss. The voltage difference between the capacitor's current voltage and its intended voltage determines the magnitude of the charging current that flows through the capacitor during this time. The capacitors' ripple loss during a fundamental cycle may be written as

$$P_{rl} = \sum_{n=1}^{2}\left(\frac{C_n}{2}(\Delta V_{C_n})^2\right) \times f \tag{9}$$

where n is the total number of capacitors in the proposed circuit, f is the fundamental frequency, and ΔV_{c_n} is the ripple in capacitor voltage for capacitor number n. The following equation may also be used to determine ΔV_{c_n}.

$$\Delta V_{C_n} = \frac{1}{C_n}\int_0^t i_{C_n}(t)dt \tag{10}$$

Where time $[0, t]$ is the longest discharging period (LDP) and i_C is the charging current of the capacitor.

TABLE 2 Comparison of proposed inverter with recent topologies.

Published MLIs	N_{SW}	N_{DC}	N_L	N_{DR}	N_D	N_C	Gain	TSV (p.u.)	Power (W)	Efficiency (%)
Roy et al. (2019)	10	2	9	10	2	4	1.5	5.44	220	92.10
Lee et al. (2019)	12	2	9	12	0	1	2	5.50	150	96
Bana et al. (2020)	9	3	11	9	1	1	1	4.2	675	96
Alishah et al. (2016a)	14	2	13	14	4	4	1	5.3	1,200	91
Sandeep and Yaragatti (2018)	12	2	9	12	0	1	1	3.82	450	97
Zamiri et al. (2016)	10	2	9	10	2	2	1.25	2.62	375	91.5
Siddique et al. (2020)	10	2	13	10	1	1	1.67	3.5	1,000	96
Alishah et al. (2016b)	10	2	11	10	4	2	1	5.2	550	93.85
[Proposed]	**10**	**2**	**11**	**7**	**2**	**2**	**1.67**	**4.8**	625	**96.48**

N_{SW}, Number of Switches; N_{DR}, Number of driver circuits; N_D, number of diodes; N_{DC}, Number of dc source; N_C, Number of capacitors, TSV (p.u.), Per unit total standing voltage, NS, Not specified. The bold values indicates the proposed MLI.

6 Comparative analysis

To illustrate the aforementioned 11-level inverter benefits over existing topologies, a comparison with already reported 11-level topologies is made in this section. Table 2 presents a thorough assessment based on the number of switches (N_{SW}), diodes (N_D), DC sources (N_{DC}), levels (N_L), capacitors (N_{CP}), the voltage gain of the converter, efficiency and total standing voltage (TSV) in p.u. The summation of all peak voltage stresses throughout all switches is known as total standing voltage (TSV). The voltage ratings of the switches to be incorporated in the topology is determined by this. TSV (p.u.) is the proportion of TSV to the AC output voltage peak value. The topologies are described in details in Table 2 in terms of comparative parameters. The topologies presented in Bana et al. (2020) require fewer switches compared to the proposed topology to produce an 11-level output voltage, but they also require an additional DC source and driver circuit. Also, it has less boosting capability and efficiency than the proposed topology. Although the work published in Alishah et al. (2016a) produces a greater number of levels than the proposed topology (Alishah et al., 2016a), requires a greater number of additional components, such as more DC sources, switches, driver circuits, diodes, and capacitors, which increases the overall cost of the inverter and makes it less efficient in terms of cost and reliability. The proposed topology and the topologies presented in Roy et al. (2019), Zamiri et al. (2016), Alishah et al. (2016b), and Siddique et al. (2020) both used the same number of switches and DC sources, but (Roy et al., 2019; Zamiri et al. 2016) were only able to generate 9 levels, which is less than the proposed topology, while the topology presented in Alishah et al. (2016b) is able to generate an 11-level output voltage waveform, which is the same as the proposed topology, but (Alishah et al., 2016b) lags in total device count, TSV(p.u.) and in efficiency as well. Similarly, the work presented in Siddique et al. (2020) produces 13 levels, which is more than the proposed topology, but it lags in both the number of driver circuits and efficiency. The proposed topology validates its superiority in comparison in terms of the lower requirement for the number of driver circuits to make the gating pulses for the switches than all other topologies. The proposed SCMLI topology has a gain of 1.67, which is higher than other published topologies except the topologies presented in Lee et al. (2019), which makes it more applicable to use in those areas where the requirement for output voltage is greater than input voltage. Likewise, in terms of efficiency, the proposed topology performs well except for the one presented in Sandeep and Yaragatti (2018), making it more suitable for use in real-world applications than other topologies. Also, except (Bana et al., 2020), (Siddique et al., 2020), (Zamiri et al., 2016) and (Sandeep and Yaragatti, 2018) the proposed topology outperforms in terms of TSV (p.u.) comparison. Additionally, considering the resistive load (R-load), the comparison of power rating for different topologies has also been mentioned in Table 2. Hence, the superiority of the proposed topology can be validated from this. For a purely resistive load, the power factor is equal to 1.

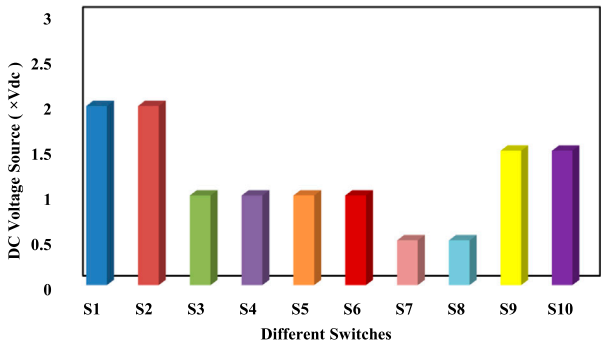

FIGURE 5
Voltage stress across the switches.

Overall, the choice of an MLI design depends on the specific application requirements, such as power rating, output voltage quality, circuit complexity, and cost-effectiveness. The studies presented in the table provide a useful reference for selecting the appropriate MLI design based on these considerations.

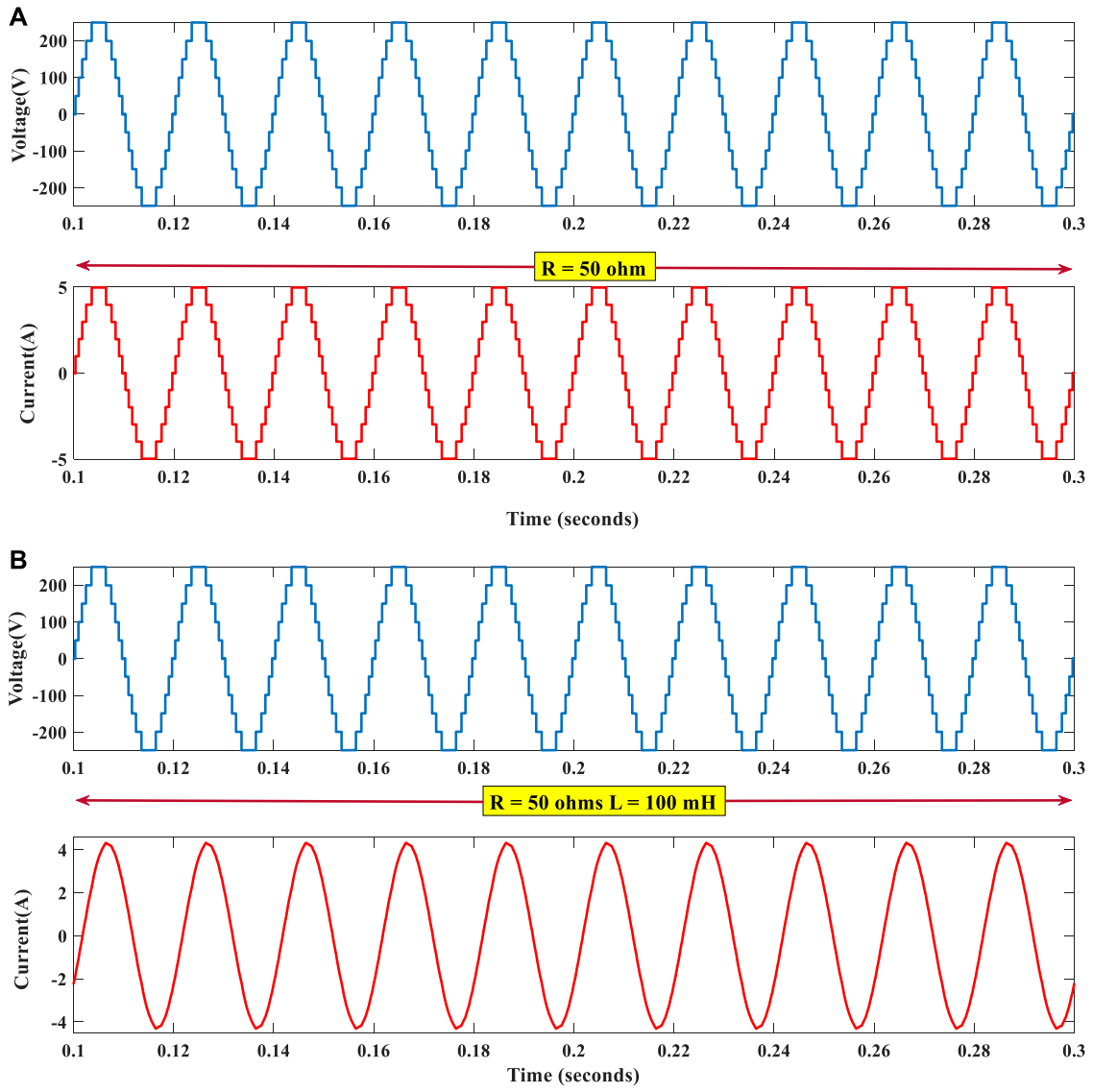

FIGURE 6
(Continued).

7 Results and discussion

This section presents the hardware and simulation results of the proposed 11-level inverter topology for various loading scenarios.

7.1 Simulation results

The voltage stress across the different switches used in the proposed topology has been shown in Figure 5. The suggested topology is simulated for 11-level using MATLAB/Simulink software. Figure 6 displays a variety of simulation results achieved for the 11-level SCMLI topology. Figure 6A depicts the output voltage and current waveforms of the proposed 11-level inverter for a purely resistive load (R = 50 Ω). As it is clear from Figure 6A, the output voltage waveform of the SCMLI has 11 levels, each level corresponding to a different voltage magnitude. The voltage waveform is a stepped waveform that approximates a sine wave and results in low harmonic distortion, which makes it suitable for applications that require high-quality voltage waveform. The current waveform also approximates a sinusoidal waveform with the same frequency as the output voltage waveform. Since the load is resistive, the current is proportional to the voltage, and the phase angle between the voltage and current waveforms is zero. The current waveform also has very low harmonic distortion, as the voltage waveform has low harmonic distortion and the load is purely resistive.

Figure 6B depicts the voltage and current waveform for an RL load with values of R = 50 ohm and L = 100 mH. Due to the inductance of the load, the voltage waveform is shifted in phase with respect to the current waveform. The degree of phase shift depends on the inductance value and the frequency of the voltage waveform.

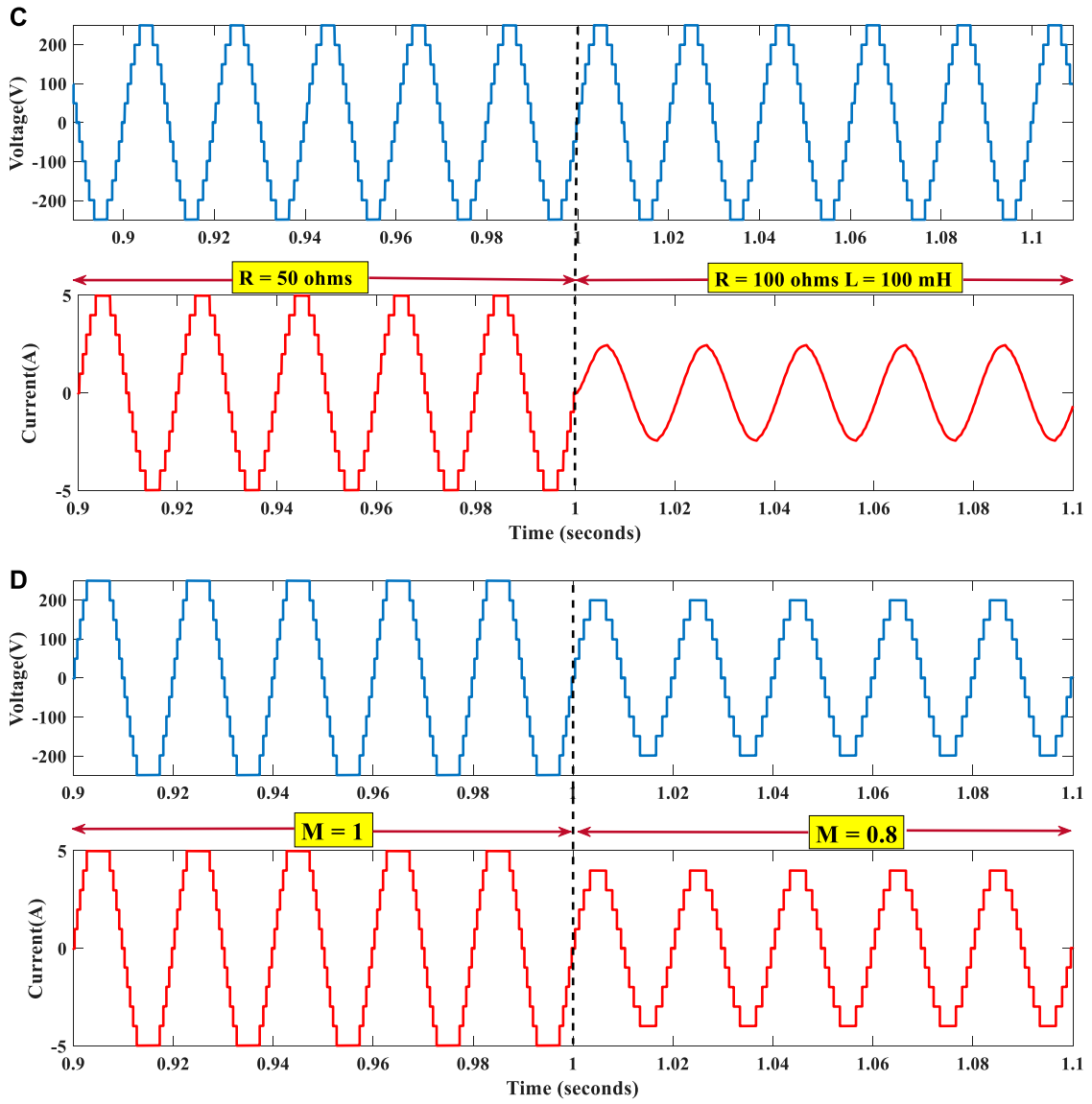

FIGURE 6
(Continued). Waveforms of the output voltage and current of the proposed 11-level inverter for the following loads: **(A)** a 50-Ω resistive load; **(B)** an RL load (R = 50 Ω, L = 100 mH); **(C)** a dynamic load change from R = 50 Ω to R = 100 Ω and L = 100 mH; and **(D)** a modulation change from M = 1.0 to M = 0.8.

The current waveform approximates a sine wave more than the voltage waveform with the same frequency as the output voltage waveform and results in low harmonic distortion.

Figure 6C depicts the voltage and current waveform with dynamic load change from load resistance, R = 50 Ω to R = 100 Ω and load inductance L = 100 mH. When the R-load is changed to an RL load, the dynamics of the circuit change. In an R-load, the load current is proportional to the voltage, and the power factor is 1. However, in an RL load, the load current lags the voltage due to the presence of inductance, resulting in a lower power factor. This change in the load impedance affects the operation of the SCMLI, which may require adjustments in its control strategy to maintain efficient and stable operation. Specifically, the switching frequency and duty cycle of the

TABLE 3 Simulation parameters.

Parameters	Values
DC sources voltage	50 V, 100 V
Output peak voltage	250 V
Inductance of load	100 mH
Resistance of load	50 Ω, 100 Ω
Capacitors	4,700 μF, 200 V
Fundamental frequency	50 Hz
Output frequency	50 Hz

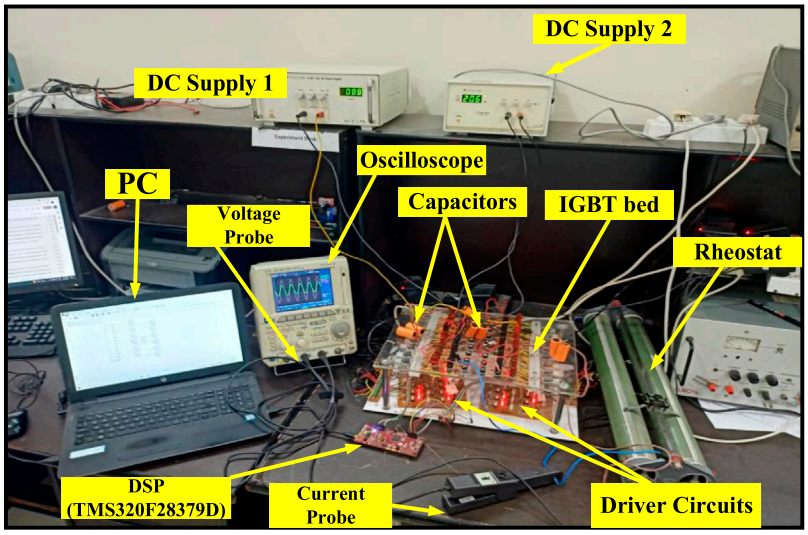

FIGURE 7
Experimental test bench of the proposed inverter.

TABLE 4 Experimental validation Parameters.

Parameters	Values
DC voltage sources	40 V, 20 V
Load resistances	40 Ω, 70 Ω, 80 Ω
Load inductance	40 mH
Output frequency	50 Hz
Capacitors	4,700 μF, 100 V, 4,700 μF, 100 V
Switching frequency	50 Hz

inverter may need to be adjusted to maintain a desired output voltage level and minimize harmonic distortion.

Figure 6D depicts how changing the modulation values from M = 1.0 to M = 0.8, affects the system. When the modulation index is changed from 0.8 to 1.0, the output levels remain same, but the amplitude of current and voltage waveforms are changed proportionally. This means that the output power is changed as well. However, the waveform shape and phase angle between the voltage and current waveforms will remain unchanged. Table 3 displays many simulation-related characteristics.

7.2 Hardware results

Figure 7 illustrates the hardware prototype that has been developed to evaluate the practicality of the proposed 11-level SCMLI. The circuit was developed using an insulated-gate bipolar transistor (IGBT) (FGA25N120). A gate driver circuit based on the TLP-250H was utilized to provide the gate signals for the individual IGBTs. Gate signals were created using the NLCPWM approach for fundamental switching. A digital signal processor (TMS320F28379D) was used to execute the NLC scheme for the suggested inverter. A FLUKE 435 Series II power quality and energy analyzer was used to test the experimental THD and efficiency percentages of the proposed MLI. The parameters for experimental setup are included in Table 4. For an input voltage of 40 V, the voltage gains of 1.67 is verified by the output voltage and output current waveform for the proposed 11-level topology, which is shown in Figure 8A. Figure 8B illustrates the transition in the load's nature, going from an R-load to an RL-load, or from a power factor of unity to a lagging power factor of 0.95. Figure 8B shows that when the load switches from an R to an RL, there is no change in the voltage, but the current does smooth out due to inductive nature of load. The suggested inverter has been examined for several modulation indices, some of which are shown in Figure 8C. The number of output levels is observed to decrease from 11 to 9 when the modulation index is altered from 1 to 0.8. For a modulation index of 0.92–1, eleven levels are achieved at the output; this number drops to nine for a modulation index range from 0.72 to 9. The output voltage and current THD are shown in Figures 8D, E. When a RL load of 50 Ω and 100 mH was taken, it was discovered that the output voltage THD is 7.65% and the output current THD is 0.89%. By employing a power quality and energy analyzer the plot of efficiency at various loads against output power is achieved in Figure 8F. The greatest efficiency is 96.48% at 500 W of output power, and it becomes inferior as output power gets bigger due to the reason mentioned in (Reddy et al., 2020). The self-balancing of the capacitor voltage is proven by all of these waveforms. Additionally, the suggested design performs well under various loading scenarios. Table 4 lists the parameters for experimental analysis and validation for the proposed inverter.

8 Application of proposed SCMLI

This section outlines the inverter current control method for injecting active and reactive power from sources of distributed power generation into the grid. The inverter is linked to the grid and has eleven levels. V_1 and V_2 are the input voltage supplies taken

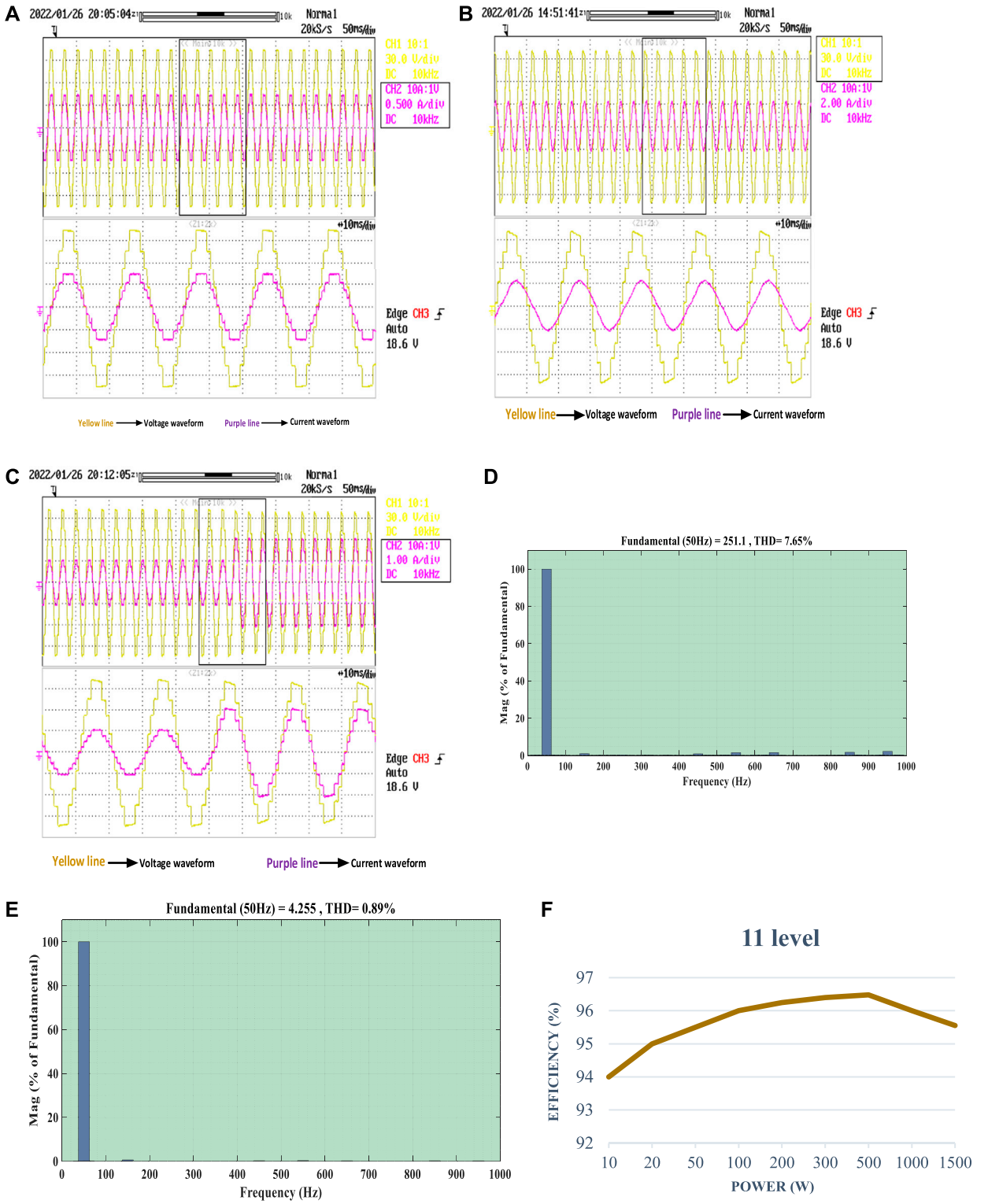

FIGURE 8
The output voltage and current waveforms of the proposed 11-level inverter for the following conditions: **(A)** a resistive load of 50 Ω; **(B)** an RL-load of R = 100 Ω and L = 100 mH; **(C)** a change in modulation from M = 1.0 to M = 0.8 **(D)** The output voltage's THD **(E)** The output current's THD and **(F)** efficiency under various loading scenarios.

from solar cells of the proposed multilevel inverter and the voltages are maintained at V_{dc} and $V_{dc}/2$. Figure 9 depicts the block diagram of the present control approach used to regulate the grid power injection.

The Phase-Locked Loop (PLL) block, which divides the grid voltage (V_g) into two components that are 90° apart, provides the grid voltage. The current controllers provide the NLCPWM block with a reference

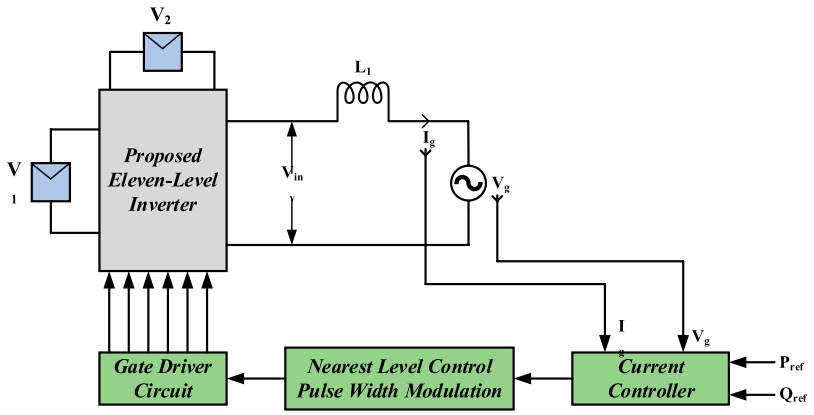

FIGURE 9
The grid-connected operation of the proposed eleven-level SCMLI.

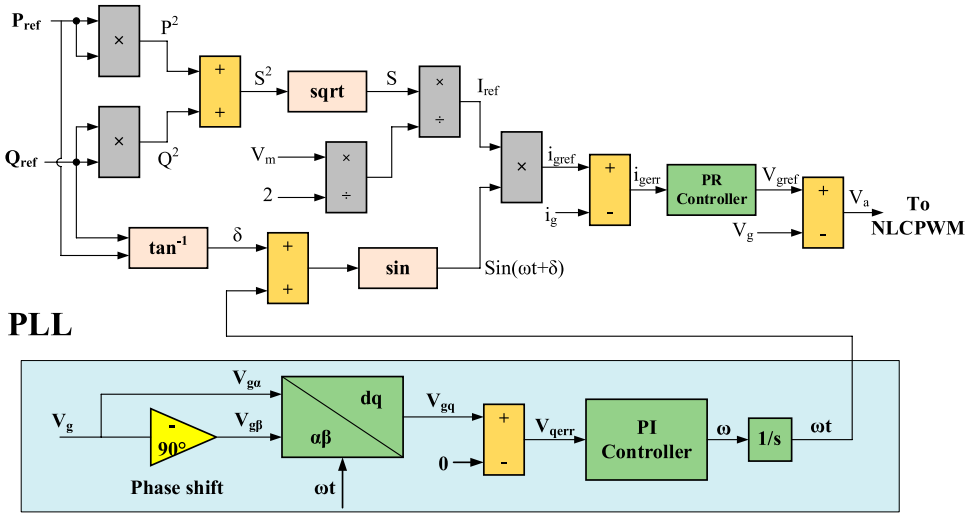

FIGURE 10
The technique for producing a reference sine wave for NLCPWM.

sine wave by delivering reference active (P_{ref}) and reactive (Q_{ref}) power in accordance with the varying active power and reactive power demand values (Monfared et al., 2012; Kar et al., 2022). Both active and reactive power are controlled using the proportional-resonant (PR) controller, which has a lower computational cost.

Figure 10 depicts the block diagram for the NLCPWM reference sine wave generation process. In order to supply the necessary gate switching pulses for the inverter switches, the current-controlled reference signal is fed back as the reference signal of the NLC-PWM method. The appropriate gate driver circuit of the inverter receives the switching pulse produced by the NLCPWM block.

9 Conclusion

The work proposes an 11-level switched capacitor multilevel inverter (SCMLI) topology for solar PV application. The proposed topology employing a dual DC-source configuration with 8 unidirectional and 2 bidirectional switches to accomplish 1.67 times boosted operation. A comparison study is carried out to ascertain the effectiveness of the suggested MLI with the recent converters. All the capacitors used in circuit are self-balanced, which lessens the control complexity. A simple basic modulation approach i.e., NLCPWM is used to generate the gating pulses for IGBTs. The validation of the suggested 11-level MLI is accomplished under diverse operating circumstances with the aid of an experimental prototype. The suggested inverter output voltage and current are having THD of 7.65% and 0.89%, respectively. The optimum efficiency attained by the SCMLI is 96.48% at 500 W of output power. In the future, SCMLIs may become more widely adopted in renewable energy systems such as solar and wind power, as well as electric vehicles and energy storage systems. Research efforts may focus on improving the design and control of SCMLIs to enhance their performance, reduce their size and cost, and increase their reliability. Furthermore, the development of new materials and components could enable the creation of more advanced SCMLI topologies with even greater efficiency and power density.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding authors.

Author contributions

MH: Conceptualization, Formal Analysis, Investigation, Methodology, Validation, Visualization, Writing–original draft. MT: Conceptualization, Formal Analysis, Investigation, Methodology, Supervision, Validation, Visualization, Writing–review and editing. AS: Conceptualization, Formal Analysis, Investigation, Methodology, Supervision, Validation, Visualization, Writing–review and editing. SA: Formal Analysis, Funding acquisition, Project administration, Validation, Visualization, Writing–review and editing. MP: Formal Analysis, Investigation, Validation, Visualization, Writing–review and editing. HM: Formal Analysis, Funding acquisition, Project administration, Visualization, Writing–review and editing.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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