frontiers in Energy Research

TYPE Original Research
PUBLISHED 05 October 2026
DOI 10.3389/fenrg.2026.1786735

Check for updates

OPEN ACCESS

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RECEIVED 13 January 2026
REVISED 24 August 2026
ACCEPTED 01 September 2026
PUBLISHED 05 October 2026

CITATION
Xie N, Wang J, Li S, Yang D, Cao X and Long L (2026) A three-level ANPC converter with differentiated Si/SiC hybrid switches in the inner and clamping positions.
Front. Energy Res. 14:1786735.
doi: 10.3389/fenrg.2026.1786735

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A three-level ANPC converter with differentiated Si/SiC hybrid switches in the inner and clamping positions

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Si/SiC hybrid-switch-based 3L-ANPC converters offer advantages such as high efficiency, balanced cost, and strong reliability. However, two major issues are still faced by traditional hybrid-switch-based 3L-ANPC converters: 1) some Si devices are operated at high-frequency switching, and 2) single clamp-leg conduction results in high conduction losses. To address these challenges, a novel H-Si/SiC 3L-HANPC converter topology is proposed, in which Si/SiC hybrid switches replace both the clamping and inner switches. By employing Si/SiC hybrid switch to optimize switching losses and simultaneously conducting both clamp branches during the zero-voltage state to reduce conduction losses, the proposed topology achieves improved efficiency. Furthermore, to overcome the low current utilization and high cost associated with using identical hybrid switches for the clamping and inner switches in conventional schemes, a differentiated Si/SiC hybrid-switch placement strategy is proposed. This strategy assigns devices to specific positions, effectively balancing cost and thermal performance in the H-Si/SiC 3L-HANPC converter. Finally, performance comparisons of various Si/SiC hybrid-switch-based 3L-ANPC topologies and configurations were conducted using experiments. The results indicate that, compared with traditional hybrid-switch-based 3L-ANPC converters, the proposed H-Si/SiC 3L-HANPC consistently achieves higher efficiency across different power factors and power levels. At the same time, the differentiated Si/SiC hybrid switches placement strategy simultaneously optimizes cost, efficiency, and thermal performance.

KEYWORDS
device losses, drive timing, efficiency, hybrid switch, modulation strategy, thermal performance, three-level active neutral-point-clamped converter

1 Introduction

Recently, Three-level Active Neutral-Point Clamped (3L-ANPC) converters have several notable advantages, including reduced output voltage and current harmonics, lower semiconductor device stress, decreased switching losses, and increased power density. These characteristics effectively minimize the size and weight of passive components such as filters, thereby facilitating their widespread deployment in industrial applications including grid-connected photovoltaic inverters, railway traction converters, and data center power supply systems. Consequently, the pursuit of further loss balancing among

power devices, improved conversion efficiency, and reduced output harmonic distortion has become a key research focus within both the industrial and academic communities (Barater et al., 2016; Lee and Lee, 2024; Zhuge et al., 2022; Zhao et al., 2025; Li et al., 2024; Li et al., 2023).

The ongoing trend of increasing system power density has led to a notable rise in the importance of high-frequency operation. However, conventional silicon (Si) devices are constrained by their intrinsic material properties, which hinders their ability to meet the evolving requirements of power electronic converters for high-frequency operation, high efficiency, and high power density (Sheng et al., 2020). This limitation has driven a growing demand for semiconductor devices capable of operating at high frequencies with minimal losses. Silicon carbide (SiC) is a representative wide bandgap (WBG) semiconductor material that offers distinct advantages, such as high switching speed and low switching loss. SiC is positioned as a key enabling technology to overcome the limitations of traditional Si-based devices by these properties. To balance cost and performance, the industry has introduced hybrid Si/SiC 3L-ANPC converters. However, the cost of SiC devices remains several times higher than that of their silicon counterparts. For example, in high-current applications, the price of a SiC MOSFET is typically six to eight times that of a Si IGBT and approximately twice that of a Si MOSFET (Luo et al., 2021; Xu et al., 2019; Hwang et al., 2023; Liu, 2023; Xu et al., 2023). At even higher current ratings, the cost of SiC MOSFETs increases exponentially. In high-power systems, a practical trade-off between efficiency and cost has been achieved by adopting hybrid configurations that combine a high current rated Si IGBTs with a lower current rated SiC MOSFET to replace fully SiC-based devices (Li et al., 2020), (Jiang, 2022). This hybrid switch (HyS) strategy has been widely implemented in 3L-ANPC converters, giving rise to the so-called HyS-based 3L-ANPC topology.

A variety of device placement configurations can be derived from the clamping, outer, and inner switches of the 3L-ANPC topology, enabling multiple HyS implementations. As reported in (Xia et al., 2025; Woldegiorgis et al., 2021; Woldegiorgis et al., 2020; Woldegiorgis and Mantooth, 2021; Liu et al., 2021; Xia et al., 2022), the inner Si IGBTs in the ANPC leg can be replaced by Si/SiC HyS, in which both S_2 and S_3 are configured as Si/SiC HyS, while S_1, S_4, S_5, and S_6 remain conventional Si IGBTs. This configuration, referred to as the 2-Si/SiC HANPC, is illustrated in Figure 1a. Its optimized modulation strategy enables the Si/SiC HyS of the inner switch to operate at high frequency, while the other power devices are fundamental frequency switches, thereby utilizing the low switching-loss characteristics of the SiC MOSFET in the Si/SiC HyS. As reported in (Liu et al., 2022) and (Liu and Zhao, 2021), the Si IGBTs in both the clamping and outer positions of the ANPC leg can be replaced with Si/SiC HyS. In this configuration, S_1, S_4, S_5, and S_6 are implemented as Si/SiC HyS, while S_2 and S_3 remain conventional Si IGBTs. This topology is referred to as the 4-Si/SiC HANPC, as illustrated in Figure 1b. The optimized modulation strategy adopted in this system allows the SiC devices of the outer switch and clamping switch to operate at higher switching frequencies, while the remaining switches function at fundamental frequency. This approach effectively mitigates switching stress on the power devices and achieves a more balanced distribution of device losses. According to (Feng et al., 2020), the Si IGBTs in the outer switches of the ANPC are replaced with Si/SiC HyS. In this configuration, S_1 and S_4 are implemented as Si/SiC HyS, while S_2, S_3, S_5, and S_6 remain conventional Si IGBTs. This topology is designated as the 2-Si/SiC E-HANPC, as illustrated in Figure 1c. The employed modulation strategy ensures that each power device undergoes high-frequency switching during specific intervals, resulting in a more uniform loss distribution compared with the previous two configurations. However, this improvement in thermal balance comes at the expense of a slight reduction in overall efficiency. According to Reference (Lou et al., 2022), the Si IGBTs in the outer and inner switches of the ANPC are replaced with Si/SiC HyS. S_1, S_4, S_2, and S_3 are all Si/SiC HyS, while S_5 and S_6 remain Si IGBTs. This configuration is referred to as the new 4-Si/SiC HANPC, as illustrated in Figure 1d. The corresponding modulation strategy enables the HyS to operate at high frequencies while other power devices function at fundamental frequency, resulting in improved efficiency and more balanced junction temperatures. As illustrated in Figure 1e, the initial all Si IGBT configuration has undergone no modifications, and neither efficiency nor losses have been optimized.

The above discussion summarizes several Si/SiC HyS based topologies proposed for the 3L-ANPC converter. However, in some configurations, power devices that are not replaced by Si/SiC HyS continue to operate at high switching frequencies. Moreover, certain topologies fail to achieve simultaneous conduction of both clamping loops during zero-state conditions. Consequently, the overall optimization of switching and conduction losses in these converters remains incomplete, indicating substantial potential for further improvement.

To address the above limitations, this paper proposes an H-Si/SiC 3L-HANPC and further investigates a position-differentiated configuration of Si/SiC HyS. The main contributions are summarized as follows:

1. An H-Si/SiC 3L-HANPC is proposed, in which Si/SiC HyS are employed at the inner- and clamping-switch positions, while Si IGBTs are retained at the outer-switch positions. By coordinating the redundant zero states with the switching process, high-frequency hard-switching events are mainly assigned to the SiC MOSFETs, while both clamping branches conduct during the zero state. Thus, the switching and conduction losses are jointly optimized.
2. A position-differentiated Si/SiC HyS configuration method is proposed according to the different RMS-current and loss distributions of the inner and clamping switches. Si/SiC HyS with a higher SiC/Si current ratio are employed for the inner switches, whereas lower-current-rated Si/SiC HyS are employed for the clamping switches, thereby improving device utilization and balancing efficiency, semiconductor device cost, and thermal performance.
3. Experimental and electrothermal evaluations are conducted to verify the proposed topology and differentiated configuration. The results demonstrate reduced converter losses and semiconductor device cost, together with improved junction-temperature distribution, compared with the corresponding conventional configurations.

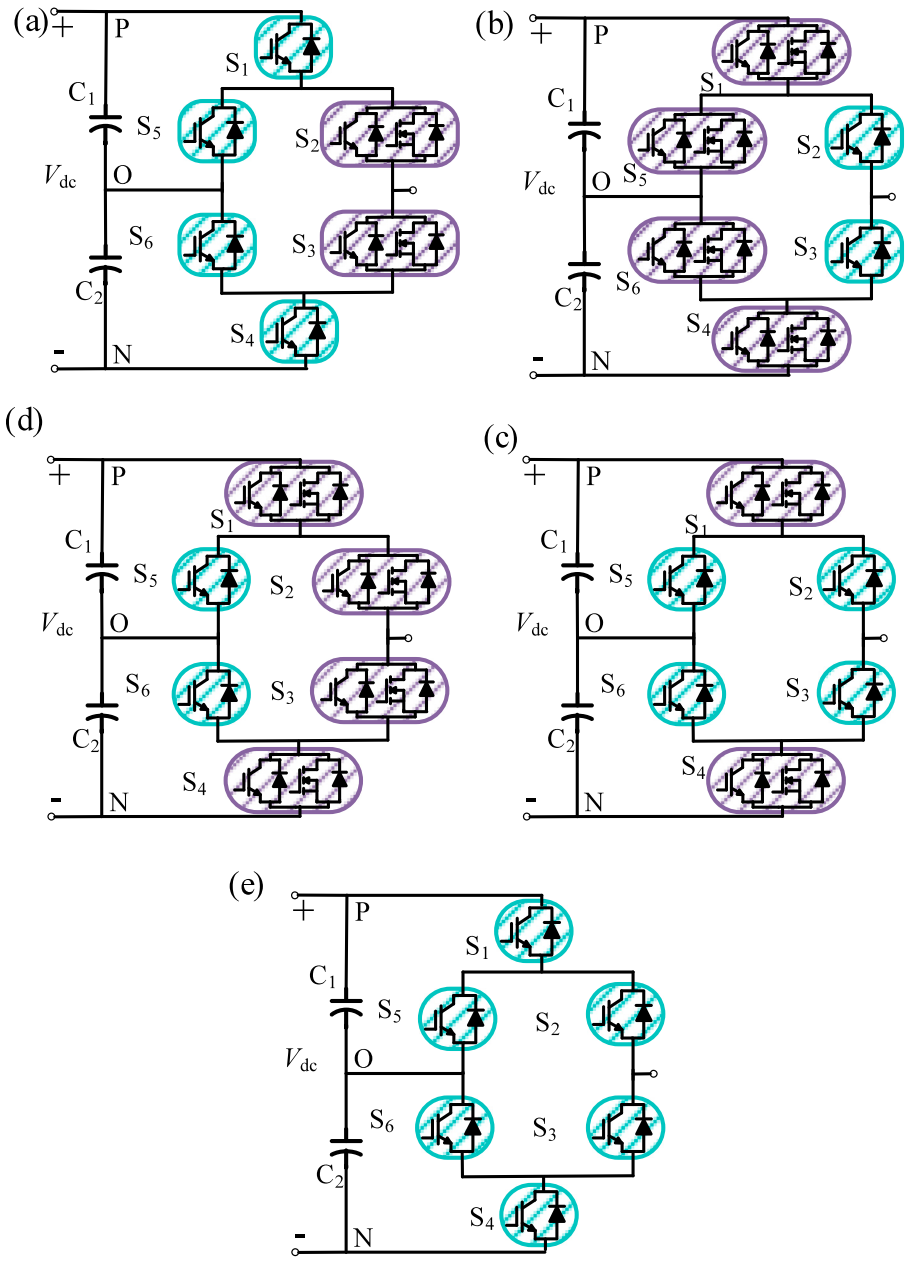

FIGURE 1
Topologies of various ANPC Structures. **(a)** 2-Si/SiC HANPC. **(b)** 4-Si/SiC HANPC. **(c)** 2-Si/SiC E-HANPC. **(d)** New 4-si/SiC HANPC. **(e)** Si ANPC.

2 H-Si/SiC 3L-HANPC topology and operating principle

2.1 Circuit topology

Compared with the conventional ANPC, the Si IGBTs in both the clamping and inner positions are replaced with Si/SiC HyS. Specifically, S_2, S_3, S_5, and S_6 are configured as Si/SiC HyS, while S_1 and S_4 remain Si IGBTs. This configuration is designated as the H-Si/SiC 3L-HANPC, and its topology is illustrated in Figure 2. As illustrated in Figure 2, the H-Si/SiC 3L-HANPC topology exhibits multiple redundant switching states in the freewheeling mode. The switch states are presented in Table 1. Consequently, the H-Si/SiC 3L-HANPC inverter exhibits multiple modulation degrees of freedom.

2.2 Gate drive timing of Si/SiC HyS

The switching losses of unipolar SiC MOSFETs are considerably lower than those of bipolar Si IGBTs, which suffer from slow switching transitions and tail-current losses. By employing an optimized gate drive timing strategy, the hard-switching events are assigned to the SiC MOSFETs, which exhibit minimal switching losses, while the IGBTs operate under zero-voltage

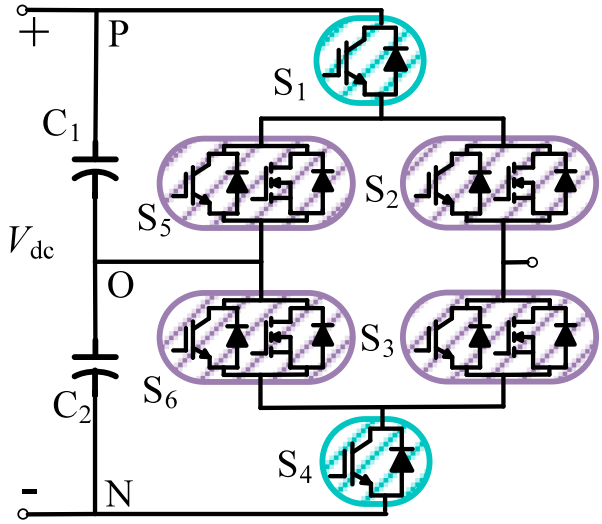

FIGURE 2
Topology of H-Si/SiC 3L-HANPC.

TABLE 1 H-Si/SiC 3L-HANPC topology switching states.

Switching state	S_1	S_2	S_3	S_4	S_5	S_6
P	1	1	0	0	0	1
OL	1	0	1	0	0	1
OL1	0	0	1	0	0	1
OUL	0	1	1	0	1	1
OU1	0	1	0	0	1	0
OU	0	1	0	1	1	0
N	0	0	1	1	1	0

switching conditions. The overall switching losses of the Si/SiC HyS are effectively reduced, and its efficiency is improved by this approach.

The gate drive timing for the Si/SiC HyS consists of four basic gate control sequences. The turn-on timing deviation between the two switches is defined as $T_{\text{on-delay}}$, while the turn-off deviation is defined as $T_{\text{off-delay}}$. A positive $T_{\text{on-delay}}$ indicates that the SiC MOSFET turns on before the Si IGBT, whereas a positive $T_{\text{off-delay}}$ implies that the SiC MOSFET turns off after the Si IGBT.

As illustrated in Figure 3, the SiC MOSFET is turned on before and turned off after the Si IGBT in Pattern 1. In this configuration, the Si IGBT is operated under zero-voltage turn-on and zero-voltage turn-off conditions, while hard switching is undergone by the SiC MOSFET. Consequently, the Si IGBT primarily contributes to conduction losses, whereas the SiC MOSFET dominates the switching losses. Pattern 2 exhibits a delayed SiC MOSFET turn-on relative to the Si IGBT and an earlier turn-off. Pattern 3 is characterized by both a delayed turn-on and delayed turn-off of the SiC MOSFET relative to the Si IGBT. Pattern 4 features an earlier turn-on and earlier turn-off of the SiC MOSFET compared to the Si IGBT.

This paper employs Pattern 1 consistently to ensure ZVS of the Si IGBT. This approach leverages the low switching losses of SiC MOSFET at high frequencies and the low conduction losses of Si IGBT.

2.3 Modulation strategy

The modulation strategy adopts phase-disposition (PD) pulse-width-modulation (PWM) schemes. When the reference voltage $u_s > 0$, the converter is operated by transitioning among multiple modes: P, OL, OL1, and OUL. Conversely, when the reference voltage $u_s < 0$, the converter transitions among the modes OUL, OU, OU1, and N.

The principle of pulse generation is shown in Figure 4. When u_s is greater than 0 and the carrier voltage is less than u_s, the converter output is P state (In the state P, switches S_1, S_2 and S_6 are turned on, while switches S_3, S_4 and S_5 are turned off) ; when u_s is greater than 0 and the carrier voltage is greater than u_s, the converter is switched by three states of OL, OL1 and OUL (In the OL state, switches S_1, S_3 and S_6 are turned on, while S_2, S_4 and S_5 are turned off. In the OL1 state, switches S_3 and S_6 are turned on, whereas S_1, S_2, S_4 and S_5 are are turned off. In the OUL state, switches S_2, S_3, S_5 and S_6 are turned on, while S_1 and S_4 are turned off), in which OL and OL1 last 0.5 μs.

2.4 Operating mode

Considering that the Si/SiC HyS is driven with a "SiC MOSFET turn-on-first and turn-off-later" sequence, multiple switching states of the Si/SiC HyS may occur within a single operating mode. Therefore, different switching states are analyzed, with only the positive half-cycle (i.e., positive reference voltage) taken as an example. In Figures 5a–c are the three device switching forms in the P state, (d) and (e) are the two device switching forms in the OL state, (f) is the device switching form in the OL1 state, (g) and (h) are the two device switching forms in the OUL state.

Firstly, in the P state, the SiC MOSFET is turned on first and the Si IGBT is turned on later in the S_2 HyS, and the SiC MOSFET is turned on first and the Si IGBT is turned on later in the S_6 HyS. At the end of the P state, the turn-off command of the Si IGBT is triggered first, and the turn-off process of the SiC MOSFET starts later, as shown in Figures 5a–c.

When the P state ends, it is switched to the OL state. At the beginning of the OL state, the current flows through the diode of S_3. Since the Si IGBT cannot be turned on in the reverse direction, after the SiC MOSFET is turned on, the total current only flows through SiC MOSFET and the body diodes of the Si IGBT, as shown in Figures 5d,e. When the OL state ends, it is switched to the OL1 state, and S_1 is turned off, as shown in Figure 5f.

When the OL1 state ends, it is switched to the OUL state, which is a dual current conduction loop. At the beginning, One current path flows through the SiC MOSFET and Si IGBT of S_6, and flows through the SiC MOSFET and the diode of Si IGBT of S_3. Another current starts from the SiC MOSFET and the diode of Si IGBT of S_5, and flows through S_2 SiC MOSFET. Subsequently, the Si IGBTs of S2 and S5 are turned on, as shown in Figures 5g,h.

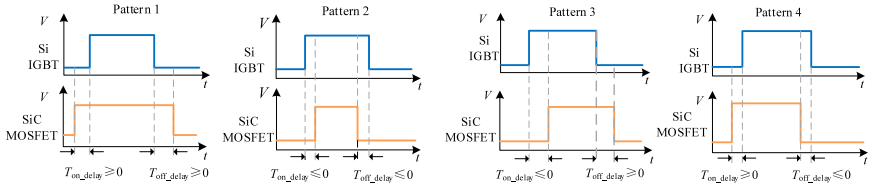

FIGURE 3
Multiple gate drive timing of Si/SiC HyS.

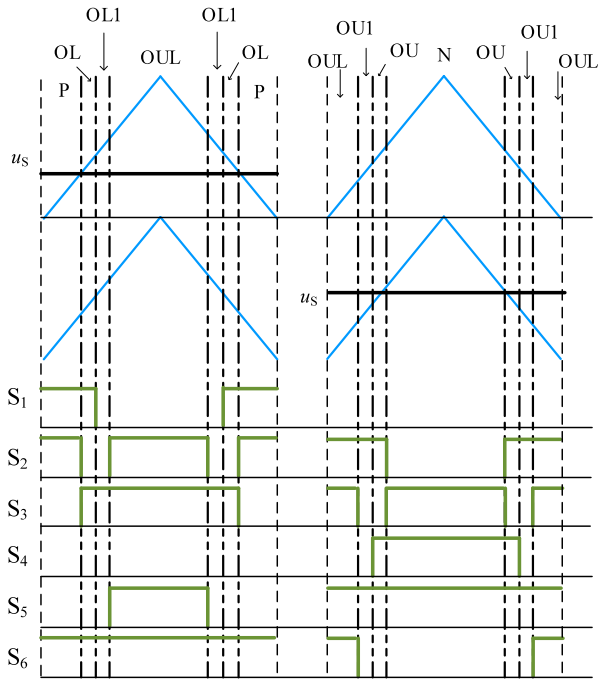

FIGURE 4
Pulse generation diagram of the H-Si/SiC 3L-HANPC modulation strategy.

3 Differentiated Si/SiC HyS configuration at specific positions in H-Si/SiC 3L-HANPC

3.1 Method for differentiated Si/SiC HyS configuration at specific positions in H-Si/SiC 3L-HANPC

At present, the Si/SiC HyS employed at different positions within the 3L-ANPC converter typically share identical specifications; that is, both their current ratings and SiC/Si current ratios are the same. (The SiC/Si current ratio of a Si/SiC HyS is defined as the ratio of the current rating of the SiC MOSFET to that of the Si IGBT within the Si/SiC HyS.) However, maintaining such a uniform configuration strategy results in low current utilization for certain Si/SiC HyS and consequently increases the overall system cost. To address this issue, a differentiated Si/SiC HyS configuration method for specific positions in the H-Si/SiC 3L-HANPC is proposed, which enhances the overall performance of the topology by adopting distinct Si/SiC HyS configurations for different positions.

Under the modulation strategy shown in Figure 4, the H-Si/SiC 3L-HANPC undergoes frequent transitions between the P (or N) state and the zero state, resulting in significant switching losses in the inner switches. Since the Si/SiC HyS adopt a switching sequence in which the SiC MOSFET turns on first and turns off later, the Si IGBT achieves soft switching. Consequently, the majority of the switching losses are concentrated on the SiC MOSFETs in the inner switches. Therefore, increasing the Si/SiC current ratio of the Si/SiC HyS in the inner switches can effectively enhance efficiency and reduce the maximum junction temperature of the power devices.

Furthermore, as illustrated in the operating mode diagram in Figure 5, the entire load current is conducted by the inner switches during the P state, whereas only approximately half of the total load current is carried by the clamping switches during the O state. Consequently, the RMS current through the inner switches is greater than that through the clamping switches. Therefore, Si/SiC HyS with different current ratings can be employed for the inner and clamping switches, respectively.

The following RMS-current analysis is specifically derived for the proposed H-Si/SiC 3L-HANPC under the modulation strategy shown in Figure 4. Neglecting the short transition intervals and dead times, the RMS currents of the inner and clamping switches are calculated according to their corresponding conduction intervals within one fundamental period. Therefore, the following expressions are modulation-dependent and are intended to characterize the current distribution of the proposed converter. The duty cycle of the non-zero state corresponding to any electrical angle θ is expressed as $D(\theta) = /M \sin\theta$ (where M denotes the modulation index). Accordingly, the duty cycle of the zero state OUL is given by$1 - D(\theta)$. Assuming the current flowing through the filter inductor is I_L, the RMS current flowing through the inner switches can be calculated as

$$I_{S2} = \sqrt{\frac{\int_0^{\pi} I_L^2(\theta) \times D(\theta) d(\theta) + \frac{1}{4}\int_0^{2\pi} I_L^2(\theta) \times (1 - D(\theta)) d\theta}{2\pi}} \quad (1)$$

The RMS current flowing through the clamping switches can be calculated as

$$I_{S5} = \sqrt{\frac{\frac{1}{4}\int_0^{\pi} I_L^2(\theta) \times D(\theta) d(\theta) + \frac{1}{4}\int_0^{2\pi} I_L^2(\theta) \times (1 - D(\theta)) d\theta}{2\pi}} \quad (2)$$

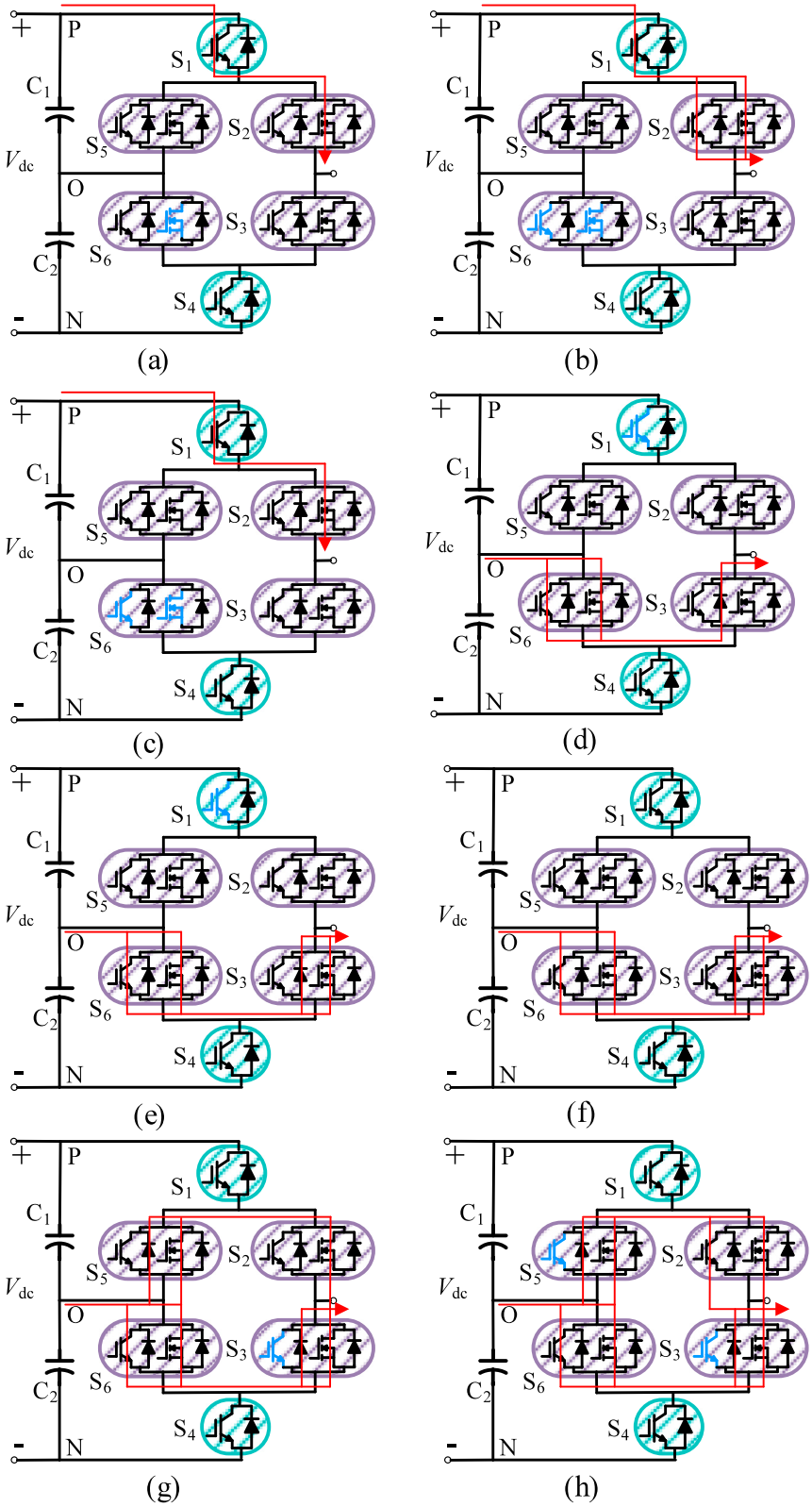

FIGURE 5
Current paths of the H-Si/SiC 3L-HANPC: **(a)**–**(h)** Eight switching states.

To improve the current utilization of clamping switches, it is essential to appropriately reduce the current rating of the clamping switches within a Si/SiC HyS configuration. The device current rating can be determined from the ratio of the RMS currents of the clamping switches and the inner switches. Optimally selecting the current rating of the clamping switches allows for a balanced trade-off between system efficiency and cost.

3.2 Differentiated configuration strategy of Si/SiC HyS for clamping and inner switches

Firstly, the Si/SiC HyS combination of the inner switches is selected. Because the on-state loss and switching loss of the inner switches are larger, in the combination I with smaller SiC/Si current ratio and the combination II with larger SiC/Si current ratio, the combination II with larger SiC/Si current ratio is selected, which can greatly reduce the loss of the power device and improve the efficiency.

Secondly, the clamping switches selects a cost-effective Si/SiC HyS combination due to the small effective value of the current. According to the characteristics of low on-state loss and switching loss of the clamping switches, the Si/SiC HyS combination III with the smallest current level of SiC MOSFET is selected for the clamping switches.

The final configuration is as follows: Combination III, with a lower current rating and lower cost, is adopted for the clamping switches, whereas Combination II, with a higher SiC/Si current ratio, is adopted for the inner switches.

The complete flow chart is shown in Figure 6. The design conditions used for device selection are as follows: the DC-link voltage is 800 V, the output phase voltage is 220 V, the output frequency is 50 Hz, and the switching frequency is 40 kHz. The full current Si IGBT uses Infineon's IKW75N60H3(600V, 75A). The Si/SiC HyS is composed of Infineon's IKW50N60H3(600V, 50A) and Wolfspeed's C3M0060065D (650V, 20A).

The available Si/SiC HyS combinations are selected according to the screening, as shown in Table 2. Among them, the combination I is cost-effective and suitable for cost-sensitive applications; combination II has a large Si/SiC current ratio and is suitable for high efficiency and high power density applications.

From Equation 1 and Equation 2, the RMS current of the inner switch to the clamping switch is about 1.7, and the current level of the clamping switches is calculated. Due to the discreteness of commercial power devices, the current ratings of the Si/SiC HyS combinations can only be approximated to 44 A. The minimum current rating for a 650 V SiC MOSFET is 16 A, such as C3M0120065D. Similarly, Si IGBT selects a series of similar IKW30N60H3. At this time, the current level of the Si/SiC HyS is about 46 A. Therefore, C3M0120065D and IKW30N60H3 are the optimal Si/SiC HyS combination III for the clamping switches.

In summary, the clamping switches employs combination III (C3M0120065D and IKW30N60H3), while the inner switches adopts the combination II (C3M0045065D and IKW40N60H3) with larger SiC/Si current ratio. The final configuration results are summarized in Table 3. In traditional scheme 1, Combination I is employed for both the clamping switches and the inner switches. In traditional scheme 2, Combination II is employed for both the clamping switches and the inner switches.

4 Experimental testing and validation

4.1 Experimental platform and parameters

This paper constructs a 3L-ANPC experimental platform based on a HyS mechanism to validate the effectiveness of the proposed strategy. The experimental setup is illustrated in Figure 7. In addition, Figure 8 displays the oscilloscope-captured modulation strategy waveform, which aligns with the positive half-cycle of the modulation strategy shown in Figure 4. Detailed parameters of the experimental platform are listed in Table 4.

4.2 Efficiency comparison of the Si/SiC HyS–based 3L-HANPC topology

All measurements were performed using the same HIOKI PW6001 Power Analyzer, with a basic power measurement accuracy of ±0.05%. The reported efficiency includes the losses of the inductor and output filter. The switching and conduction losses of the semiconductor devices under different topologies were experimentally evaluated, and the corresponding loss distributions are shown in Figure 9.

Analysis of Figure 9 indicates that, regardless of whether the power factor is 0.5 or 1, the efficiencies of the 4-Si/SiC HANPC and 2-Si/SiC E-HANPC are comparable at the same unit power factor. At PF = 1, the proposed H-Si/SiC 3L-HANPC topology achieves approximately 1.5% higher efficiency than the Si HANPC and about 0.2% higher efficiency compared with the 4-Si/SiC HANPC and 2-Si/SiC E-HANPC. At PF = 0.5, the H-Si/SiC 3L-HANPC exhibits around 3% higher efficiency than the Si HANPC, and roughly 0.2% higher than the 4-Si/SiC HANPC and 2-Si/SiC E-HANPC. In summary, across the full operating range, the H-Si/SiC 3L-HANPC converter is consistently shown to outperform the other compared topologies in terms of efficiency.

4.3 Cost comparison of different Si/SiC HyS configurations

As shown in Figure 10, the comparison results between the proposed Si/SiC HyS differentiation configuration scheme and the two traditional schemes show that the proposed scheme is between the two in terms of cost, showing a significant cost advantage.

4.4 Efficiency comparison of different Si/SiC HyS configurations

The efficiency of the proposed differentiated Si/SiC HyS configuration was compared with two traditional schemes, as illustrated in Figure 11. Compared with traditional scheme 1, the proposed scheme exhibits a slightly higher measured efficiency under heavy-load conditions, while only a marginal difference is observed under light-load conditions. This improvement arises from the selection of Si/SiC HyS with a higher Si/SiC current ratio for the inner switches, where the RMS current is relatively high,

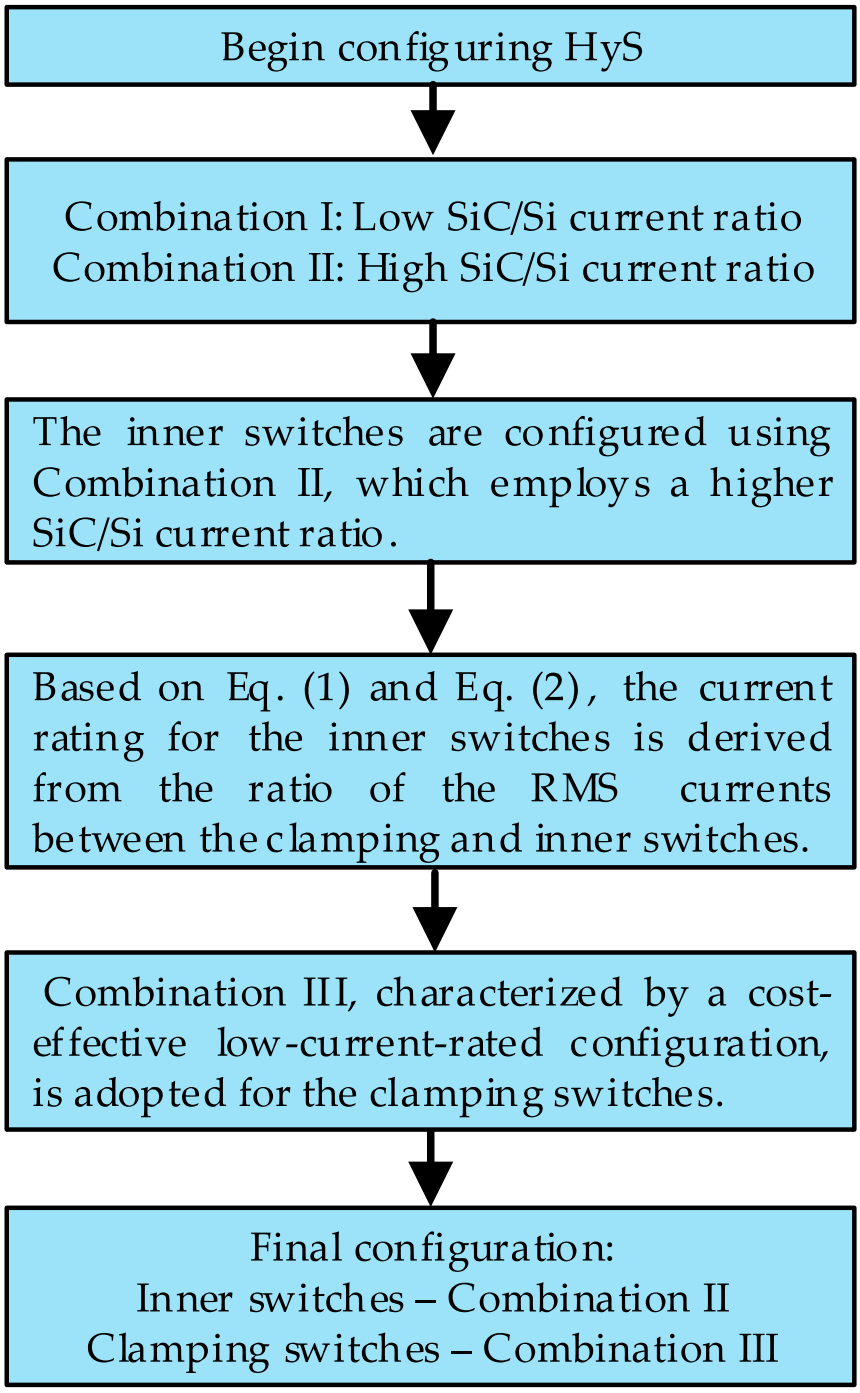

FIGURE 6
Flowchart of the differentiated configuration Scheme for clamping and inner switches.

TABLE 2 Si/SiC HyS combination.

Combination	The Si/SiC current ratio of a Si/SiC HyS	SiC MOSFET	Si IGBT	Cost (CNY)
I	1:2.50	C3M0060065D (650, 20A)	IKW50N60H3 (600V, 50A)	78.35
II	1:1.14	C3M0045065D (650V, 35A)	IKW40N60H3 (600V, 40A)	116.13

TABLE 3 Three configuration scheme combinations.

Scheme	The clamping switches combination	The inner switches combination	Cost of three-phase devices (CNY)
Traditional scheme 1 (Cost-sensitive)	C3M0060065D and IKW50N60H3	C3M0060065D and IKW50N60H3	1087.98
Traditional scheme 2 (high efficiency and high power density)	C3M0045065D and IKW40N60H3	C3M0045065D and IKW40N60H3	1541.34
Proposed scheme	C3M0120065D and IKW30N60H3	C3M0045065D and IKW40N60H3	1266.66

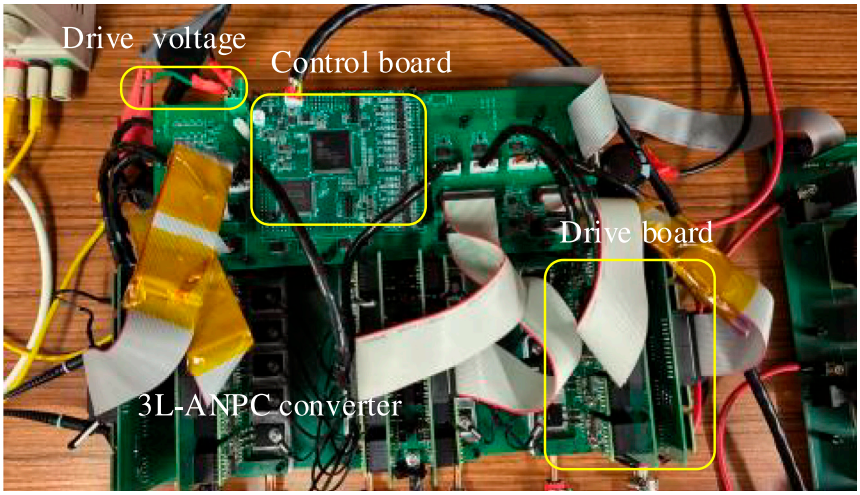

FIGURE 7
Experimental setup of 3L-ANPC converters.

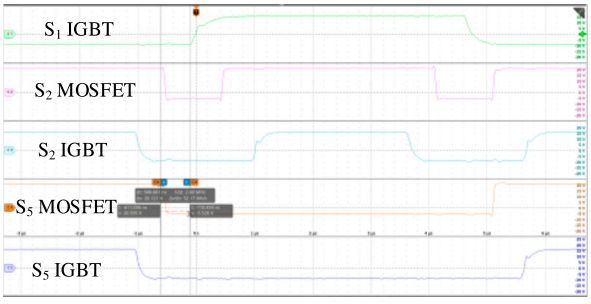

FIGURE 8
Modulation strategy waveform diagram for the 3L-ANPC converter.

TABLE 4 Test parameters for three-phase three-level ANPC converter.

Parameters	Value
DC voltage V_{dc}	400V
Output phase voltage V_{xn}	110V
Rated current I_{ac}	18A
Grid frequency f	50 Hz
Switching frequency fs	40 kHz
Filter inductor Ls	1 mH
Filter capacitor Cr	8 μF
$T_{on\text{-}d}$, $T_{off\text{-}d}$	0.5 μs, 0.5 μs

effectively reducing both switching and conduction losses in these branches. Meanwhile, Si/SiC HyS with a lower Si/SiC current ratio are used for the clamping switches, where the RMS current is smaller, thus controlling costs while still reducing the overall system losses.

In comparison with traditional scheme 2, the proposed scheme exhibits a slight reduction in efficiency. Both schemes employ identical power devices for the inner switches, resulting in similar performance; however, the proposed scheme uses Si/SiC HyS with a lower Si/SiC current ratio for the clamping switches. This choice slightly increases losses in these branches, leading to a minor decrease in efficiency. Nevertheless, a balanced trade-off between efficiency and cost is achieved by the proposed configuration, maintaining its competitiveness in terms of overall performance.

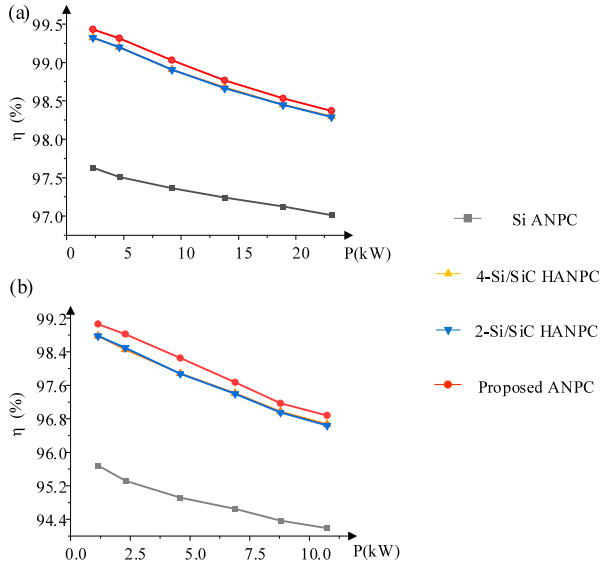

FIGURE 9
Pulse generation diagram of the H-Si/SiC 3L-HANPC modulation strategy. **(a)** PF = 1. **(b)** PF = 0.5.

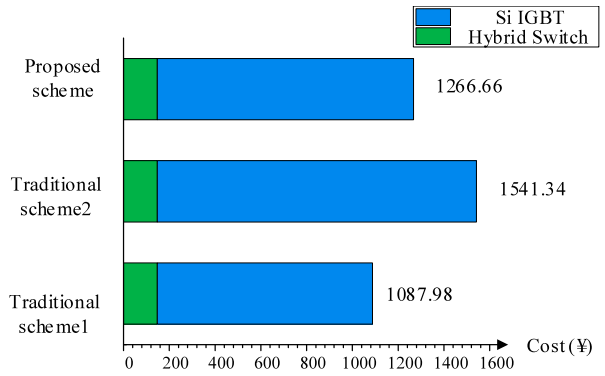

FIGURE 10
Cost comparison of the three H-Si/SiC 3L-HANPC schemes.

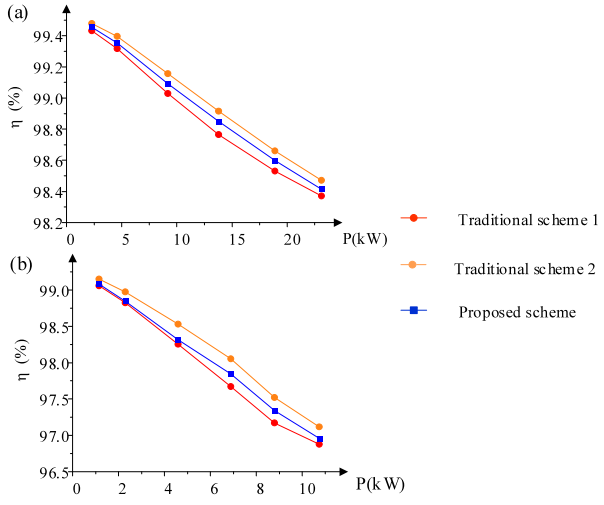

FIGURE 11
Comparative analysis of efficiency for three H-Si/SiC 3L-HANPC configurations at various power factors. **(a)** PF = 1. **(b)** PF = 0.5.

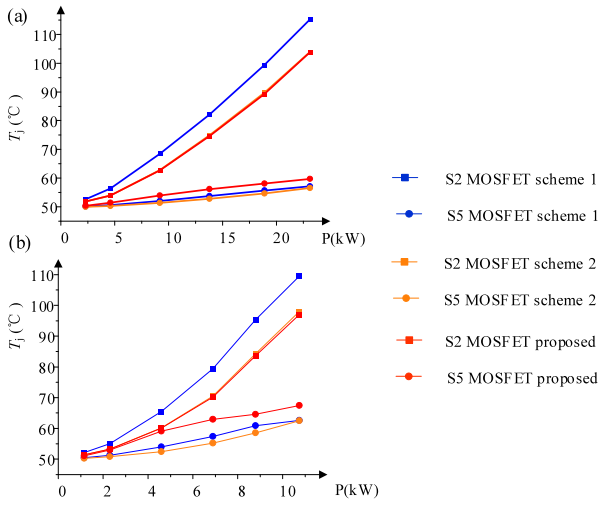

FIGURE 12
Comparative analysis of junction temperatures for three H-Si/SiC 3L-HANPC configurations at various power factors. **(a)** PF = 1. **(b)** PF = 0.5.

In summary, under both PF = 1 and PF = 0.5 conditions, the efficiency of the proposed scheme lies between the two traditional schemes, demonstrating a clear advantage in overall performance.

4.5 Thermal performance comparison of different Si/SiC HyS configurations

The junction temperatures obtained from PLECS simulation are used as a reference to compare the relative thermal performance of the three Si/SiC HyS configurations, as shown in Figure 12. Compared with Traditional Scheme 1, the junction temperature of the inner switches is reduced by 2 °C–12 °C in the proposed scheme, while the junction temperature of the clamping switches is slightly increased by 2 °C–5 °C. In comparison with traditional scheme 2, the inner switches are identical in both schemes, resulting in similar junction temperature performance. However, the proposed scheme employs lower-current SiC MOSFETs paired with Si IGBTs for the clamping switches, which increases losses in this branch and raises the clamping switches junction temperature by 2 °C–5 °C relative to traditional scheme 2. Overall, the junction temperature difference between the clamping and inner switches is effectively reduced by the proposed scheme, thereby enhancing the overall thermal balance of the system.

Based on a comprehensive comparison of cost, efficiency, and thermal performance between the proposed differentiated Si/SiC HyS configuration and two traditional schemes, it can be concluded that the proposed scheme not only integrates the cost advantage of traditional scheme 1 and the high-efficiency characteristics of traditional scheme 2, but also achieves further optimization in

thermal balancing. As a result, it maintains superior competitiveness in overall performance.

5 Conclusion

To address the incomplete optimization of switching and conduction losses in conventional Si/SiC HyS based 3L-ANPC converters, an H-Si/SiC 3L-HANPC converter topology based on HyS replacement of the "clamping switches + inner switches" is proposed. By analyzing its operational modes under the modulation strategy and utilizing Experimental data, the following conclusions are drawn:

1. By employing Si/SiC HyS in high-frequency positions and Si-based devices in fundamental-frequency positions, switching losses are significantly reduced. Additionally, conducting both clamp branches simultaneously during the zero-voltage state lowers the equivalent resistance of the current path, further reducing conduction losses in the Si/SiC HyS.
2. Compared with conventional hybrid-switch-based 3L-ANPC converters, the proposed H-Si/SiC 3L-HANPC converter achieves significant loss reduction across all power levels and at PF = 0.5 or PF = 1.
3. By selecting Si/SiC HyS with a higher Si/SiC current ratio for inner switches and lower-current Si/SiC HyS for clamping switches, it allows for minor efficiency trade-offs. At the same time, it further reducing costs and improving the thermal balancing performance of the H-Si/SiC 3L-HANPC converter.

In summary, the proposed H-Si/SiC 3L-HANPC converter, based on HyS replacement of the "clamping switches + inner switches", effectively enhances efficiency under various operating conditions and demonstrates high application potential in high-efficiency, high-power-density scenarios.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

NX: Methodology, Conceptualization, Software, Supervision, Writing – original draft. JW: Writing – review and editing, Validation, Formal Analysis. SL: Funding acquisition, Project administration, Writing – review and editing, Investigation. DY: Writing – review and editing, Resources, Visualization. XC: Writing – review and editing, Data curation. LL: Writing – review and editing, Writing – original draft.

Funding

The author(s) declared that financial support was received for this work and/or its publication. This work was supported by the Technology Project of China Southern Power Grid under Grant 000000KC24010028.

Conflict of interest

The authors declared that this work received funding from China Southern Power Grid Co., Ltd. The funder had the following involvement in the study: collection, analysis, interpretation of data.

Generative AI statement

The author(s) declared that generative AI was not used in the creation of this manuscript.

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