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Ferroelectric tunnel junctions: current status and future prospect as a universal memory

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The semiconductor industry is actively looking for an all-encompassing memory solution that incorporates the advantageous aspects of current technology. This features non-volatility, like that of Flash memory, high scalability, like that of both Dynamic Random Access Memory (DRAM) and Flash, quick operation, like that of Static RAM (SRAM), and durability, like that of both DRAM and SRAM. Ferroelectric thin films, which have electrically switchable bi-stable polarization, are one prospective technology that has the potential to revolutionize memory storage. However, due to difficulties with scalability and dependable industrial manufacturing, Ferro-Electric (FE) memory technology has not been able to effectively compete with DRAM and Flash. Research in this area has accelerated after the recent discovery of resistive switching in ferroelectric tunnel junctions (FTJs). For FTJs to be successful, it is important to overcome some obstacles, such as preserving bi-stability in ferroelectric thin films over the critical thickness. Additionally, the existence of interfacial layers, sometimes known as a "dead layer", between the electrode and the film can affect its characteristics. The article gives an overview of semiconductor memories with an emphasis on emerging technologies having the potential for future applications. It then goes into detail on the benefits of FTJ and its non-destructive reading capacity. The article also discusses the potential uses for FTJs in resistive switching while acknowledging their drawbacks and constraints.

KEYWORDS

universal memory, ferroelectric tunnel junction, resistive switching, non-volatile (NV) memory, hafnium oxide

1 Introduction

Information storage systematically evolved from the oldest memory devices such as "Analogue Rosetta Stone" to "Digital storage devices" that realize data preservation, data recovery, and document reconstruction. At present, the need for digital memory with greater capabilities is increasing at an exponential rate, and the semiconductor industry is changing to accommodate the future requirement of information technology. The Internet of Everything (IoE)works in a synchronized way with other technologies like artificial intelligence (AI), machine learning (ML), internet of things (IoT), big data, cloud, fog, edge computing and communication devices, routers, sensors, etc., cannot be powered without non-volatile semiconductor memories. Therefore, it would be incorrect to consider the semiconductor memory sector to be a matured technology devoid of offering extreme

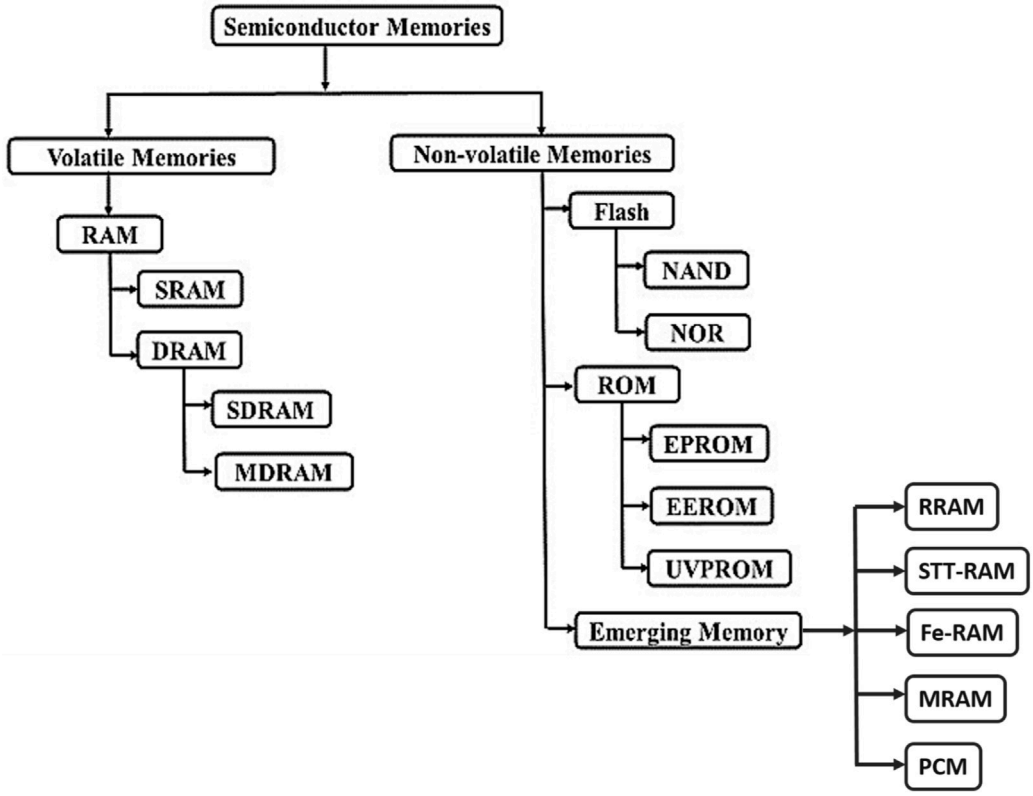

FIGURE 1
Classification of memory technologies concerning their functional aspects.

devices of current requirements. The power consumption of high-frequency operated logic and memory devices, smartphones, and microelectromechanical systems has increased as the number of transistors has increased by the vertical shrinkage in dimension. These devices have a smaller lateral die size and a gradually rising storage density. At present, any electronic system that uses memory to store information is based on a semiconductor substrate. Due to the demand for more storage density, memory technologies have been expanded into various types. To meeting the global demand for non-volatile data storage, there are memory technologies, that are emerging memories since the realization of proof of concept, like Ferroelectric RAM (F-RAM), Magnetic RAM (MRAM), and Resistive RAM (RRAM) (Jeong and Hwang, 2018; Chen et al., 2023; Cappelletti, 2015). However, the non-volatile memory devices that need to be created in the present scenario must be, quick, energy-efficient, dense, robust, and radiation-resistant to meet the long-term operational requirements.

Several semiconductor memory technologies are outlined in Figure 1 and are briefly discussed as follows before discussing the ferroelectric tunnel junction (FTJ) for high-density memories. These memories can be classified into two main groups, namely, volatile and non-volatile memories. Read-only memory (ROM) and random-access memory (RAM) are two categories of semiconductor technology embrace the aforementioned classification. Historically, RAM, a volatile memory, is utilized by the central processing unit (CPU) of the computers to write and read data in the predetermined order that involves a random draw of information from the memory. With this kind of memory, data can be stored and read numerous times at relatively high speed compared to secondary memory devices like hard disks. Volatile memory is a term used to describe memory that loses its contents when the power is switched off. Memory types that are volatile include, dynamic random-access memory (DRAM), Mobile DRAM (MDRAM), static RAM (SRAM), and Synchronous DRAM (SDRAM). One capacitor and one transistor make up basic cell of the DRAM's structure and 1 bit of information per cell is stored in the capacitors. When a capacitor is charged, it achieves logic "1," whereas a capacitor that has been discharged has a logic "0." However, six transistors are used in the construction of the SRAM, of which two are cross-coupled transistors and the other four are pass transistors. Memory bits are stored in the cross-coupled transistor pairs, which are Complementary Metal Oxide Semiconductor (CMOS) inverter pairs. In addition to this six-transistor arrangement, SRAM also has four other transistor configurations. High-impedance resistors are used to replace the p-MOS in this design. SRAM is used in cache memories, while DRAM is used in the primary memories. In contrary, even when the power is off, information is stored permanently in ROM and hence it is a non-volatile memory (Fujisaki, 2013). A computer's ROM contains the basic input/output system (BIOS) program, a software run fist when you start the computer. Erasable Programmable ROM (EPROM), Electrical Erasable Programmable ROM (EEPROM), ultraviolet programmable ROM (UVPROM) are other variants of ROM used for the information

storage. However, major development in the non-volatile memory category occurred at Bell Laboratory, by Kahng D and Sze SM. They originally proposed the floating gate transistor (FGT) as a non-volatile memory component in 1967 and that was the beginning of MOS's expansion into the nonvolatile device. Flash memory is built on FGT, a type of metal oxide semiconductor field emitter transistor (MOSFET) with one minor modification: an additional gate is inserted between the control gate and the body. This additional gate is referred to as a "floating gate" (FG). Since there are no electrical contacts and it is electrically isolated, any charge injected into the FG will stay there for many years. To encode data using a charge state, it enables flash memory devices to store data as a collection of charges. The FGT has two states: a) a negative charge; and b) a zero charge (Gerardin and Paccagnella, 2010; Hamdioui et al., 2017). A "0" bit value is assigned to the negative charge state and a "1" bit value to the zero-charge state. The two types of flash memory are NOR (huge cell size and direct write) and NAND (small cell size and page write). NAND flash memory frequently takes the place of storage memory in the form of a hard disc memory. When compared to DRAM, which is made up of 1T-1C, NAND flash memory's double gate transistors structure makes it appropriate for high-density memory storage with a smaller cell size. NAND flash is not a good choice for working memory due to its limitations on longevity (10^5 cycles) and slower writing speed (ms), apart from its ability to store data and programs without power. The most popular and reliable portable secondary memory type is flash memory. Solid-state memory technologies like DRAM, SRAM, and Flash have dominated the semiconductor memory market for the past 40 years of its development (Jeong et al., 2012). Figure 1 also shows the classification of various memories based on their functioning characteristics with additional reference to the new and emerging technologies. In the non-volatile memory category, emerging technologies for future memory formats includes resistive RAM (RRAM), phase change RAM (PCRAM), magnetic RAM (MRAM), Spin-transfer torque MRAM (STTMRAM), and ferroelectric RAM (Fe-RAM) aim to compete with DRAM and SRAM (Gerardin and Paccagnella, 2010; Hamdioui et al., 2017).

From the emerging memories, an intermediate endurance of 10^{10}–10^{12} and density in gigabyte (GB) can be achieved phase change random access memory (PcRAM or PCM). PcRAM's foundation is the materials like chalcogenides' reversible shift from low resistance (crystalline phase) to high resistance (amorphous phase). The design of the memory cell and the characteristics of the phase-change materials affect performance memory cell. PcRAM cells must be configured to meet the needs of increased thermal isolation, reduced reset current, easy processing, and power efficiency. Materials utilized in PcRAM with several nm thin-film thicknesses or nanoparticle diameters are used to exhibit the desired scaling behavior, which includes high crystallization temperature at a smaller dimension and decreasing thermal conductivity (Gerardin and Paccagnella, 2010; Law and Wong, 2021a). The substantial switching current restricts the linear dependency of the threshold voltage. Despite experimental testing using bipolar junction transistor (BJT) and diode devices, the efforts to shrink the cell size of phase-change random access memory (PcRAM) encountered obstacles such as electrode void development, elements segregation, and changes in mass density. However, the development showcased remarkable features, including a fast-switching speed of 100 nanoseconds and an endurance of over one billion cycles ($>10^9$) in the case of PcRAM (Fujisaki, 2013; Hamdioui et al., 2017). Nevertheless, PcRAM is unable to displace Flash memory or dynamic random-access memory (DRAM) primarily due to two factors: manufacturing costs and the continuous advancements within existing memory technology. Constant improvements in performance, density, and cost-effectiveness contribute to a competitive environment. These factors collectively make it difficult for PcRAM to surpass Flash and DRAM in terms of popularity and market dominance.

Apart from the aforementioned phase change memory (PCM), resistive random-access memory (RRAM) has been investigated for creating synaptic devices inside 3D cross-point designs. RRAM is a good contender for memory operations because the ion-based process controlling inductance in it mimics the synaptic plasticity seen in biological systems (Fujisaki, 2013). Operations for filamentary conductive-bridging RRAM (CBRAM) and oxide RRAM (ox RAM) (Goux, 2019; Garbin et al., 2015) are controlled by the growth and breakdown of a conductive filament (CF) made of oxygen ions and cations diffused through the material. The homogenous movement of oxygen ions/vacancies across the layer stack is a key component of the oxide RRAM, influencing aspects like the tunneling/Schottky barrier's thickness and barrier height. However, the precise process causing barrier modulation is still being debated. A number of options are being investigated, including phase change, redox/oxidation, electrostatic effects, and modifications to the local oxide stoichiometry. A multiscale modeling platform is used to relate the performance of electrical devices to atomic material attributes in order to comprehend the behavior of RRAM devices (Larcher and Padovani, 2017; La Torraca et al., 2019; Padovani et al., 2017). This platform accounts for the individual contributions of ions and vacancies/drifts and their effects on power dissipation and local temperature. Consideration of different charge transport processes such tunneling, drift and diffusion, and hopping also accounted. Aside from the bond deformation, breaking, chemical reactions, diffusion of atomic vacancies and interstitial ions, and phase shifts, the modeling also takes into account material variations at the atomic level.

Emerging memory is motivated by overcoming these problems and is the subject of active research (Law and Wong, 2021a; Lankhorst et al., 2005). However, characteristics like low power consumption, non-volatility, density, and speed are necessary for the development of future semiconductor memories. Such a memory prowess might lead to the development of a "universal memory" that will combine the non-volatile properties of FLASH, the long durability of DRAM and SRAM, the fast speed of SRAM, and the great scalability of DRAM and Flash (see Tables 1 and 2). The ferroelectric capacitor of ferroelectric RAM, also known as FRAM or Fe-RAM is one of them, where ferroelectric material is sandwiched between two metal electrodes. With the ferroelectric layer replacing the dielectric layer, it is similar in design to DRAM and functions similarly to flash memory in terms of the non-volatility of the stored information (Law and Wong, 2021a). James Scott contributed significantly to the advancement of ferroelectric memories as the co-founder of Symmetrix. He oversaw the development of integrated thin film ferroelectric technology suited for microelectronic devices from bulk ceramic

TABLE 1 The general characteristics of different memories available in the market.

	DRAM	SRAM	Flash	Fe-RAM	MRAM	PRAM	RRAM
Non-volatility	N	N	Y	Y	Y	Y	Y
Readout speed	50 ns	5–70 ns	50 ns	30–100 ns	30–100 ns	30–100 ns	10–100 ns
Writing Speed	50 ns	5–70 ns	10 m	30–70 ns	10–50 ns	100 ns	10–100 ns
Endurance	$>10^{15}$	$>10^{15}$	10^{6}	10^{12}	$>10^{15}$	10^{12}	?
Cell size	8 F^2	140 F^2	4 F^2	12–80 F^2	8–40 F^2	4–8 F^2	4–6 F^2
Integration with logic Circuits	YY	YY	YY	Y	Y	Y	Y

TABLE 2 The characteristics required for universal memory.

Memory hierarchy	Speed (write/erase time)	Scalability (cell size)	Endurance (cycles)	Energy efficiency
SRAM	High (0.3 ns/0.3 ns)	Low ($140F^2$)	High (10^6)	Volatile
DRAM	High (10 ns/10 ns)	High ($6F^2$)	High (10^6)	Volatile
FLASH	Low (1 m/10 m)	High ($10F^2$)	Low (10^5)	Non-volatile
Universal memory	High	High	High	Non-volatile

technology. The discovery that the Aurivillius class of ferroelectrics, illustrated by SrBi2Ta2O9 (SBT), does not suffer polarization fatigue a behavior different from that of traditional perovskite ferroelectrics was one of his major accomplishments (Chen et al., 2018). The drawbacks of FeRAM are the high manufacturing costs due to CMOS incompatible material and poor storage density compared to DRAM. Currently, Fe-RAM uses in motion control, process controls in industries, wireless data logging, gamma radiation in wireless memory, and radio frequency identification (RFID). Other applications include advanced metering, gaming, point-of-sale systems, automotive shift-by-wire, navigation, and anti-pinch control. The ferroelectric memory is set up with a ferroelectric field effect transistor and a ferroelectric capacitor, 1C, and 1T, respectively (Fe-FET). Due to the double-gate transistors NOR architectural construction, the memory has the potential to replace DRAM. The approach has not been implemented due to technical challenges like the need for thin enough ferroelectric thin films of less than 10 nm in the capacitor (Fe-RAM) and transistor (Fe-FET) forms. Ferroelectric layers make up the Fe-gate FET's dielectrics. Ferroelectric polarization in Fe-FETs is used in place of a floating gate, comparable to Flash memory (Shin, 2005; Prall, 2007). The thin doped HfO_2 films (< 5 nm) used in transistors and capacitors were developed by the Namlab in Germany. These are now accepted industrial standards, and doped HfO_2 will be moving toward this specific goal. Parts of "ferroelectric memory" include ferroelectric tunnel junction (FTJ).

This represents a significant advancement in the field since it shows that efforts have been made to match the properties and functions of doped HfO_2 with accepted performance and utility standards.

The ferroelectric tunnel junction (FTJ), a key element, plays a critical function in the larger field of memory technology. This component embodies the idea of ferroelectric memory, which uses tunneling mechanisms to store and retrieve data by manipulating the ferroelectric polarization state. In terms of improved data storage, preservation, and processing capabilities, FTJs represent a possible route for the development of memory technologies by utilizing the properties of ferroelectric materials. It is clear that the industry is expanding significantly outside the boundaries of known technologies in response to the rising demand for the newest memory solutions. This wave of development includes a variety of innovations, including:

The popularity of quantum dots (Q-dots) (Chauhan, 2007) is growing as a result of their distinctive electrical and optical characteristics. Through the use of efficient data manipulation techniques and high-density data storage made possible by quantum mechanical processes, quantum dots have the potential to revolutionize memory technology. A number of cutting-edge methods in memory technology are set to change how data is processed and stored. Zero-RAM stands out as a ground-breaking idea that goes against the grain of RAM technology conventions (Amo-Boateng, 2017). Zero-RAM promises to improve data access speeds while simultaneously lowering power consumption by focusing on eliminating intrinsic constraints. By tackling basic flaws and ushering in a new era of effective and high-performance memory systems, this dual approach has the potential to transform memory solutions. Stochastic Phase-Change-Based Memory (SPBMM), another ground-breaking challenger, makes significant gains by utilizing the concepts of phase-change materials. Optimizing data retention, increasing energy economy, and optimizing system performance are all objectives of SPBMM's design (Tuma et al., 2016). By utilizing the distinct qualities of phase-change materials, SPBMM has the ability to satisfy the requirements of contemporary computer environments, which call for dependable, quick, and energy-efficient memory solutions.

By introducing transformational capabilities, as demonstrated by this combination, memory technology and its applications across multiple industries could undergo a revolution. Together, these cutting-edge memory technologies herald an exciting new era of technological development, promising to revolutionize how data is

stored. Collectively, these cutting-edge memory technologies herald an exciting new era of technological development that will push computing as know it to new heights by revolutionizing how data is stored, accessed, and processed (Lankhorst et al., 2005). The spike in interest and investment in these next-generation memory technologies highlights the industry's acknowledgment of the necessity for cutting-edge solutions as the market continues to diversify and adapt. These developments have the potential to completely alter the memory technology landscape, opening up new opportunities for data-driven enterprises and altering the course of technological development.

1.1 Universal memory

Technologies like SRAM have outstanding read and write speeds (0.3 ns/0.3 ns) and require less power (Sharma et al., 2021; Liu et al., 2021). Since it requires a lot of foot print area due to the huge size of the cell typically six transistors, makes it unsuitable for embedded applications. DRAM has a denser architecture than SRAM since it only has one transistor and one capacitor per cell. For updating the bit state in DRAM every few milliseconds, constant power is required. This serves to stop the leaking of charges that are stored in the capacitor. DRAM in portable electronic devices shorten the battery life due to its high-power consumption. However, Flash memory provides information storage that is not volatile. The production process is complicated despite its high density and requirement for high-voltage driving circuits for embedded applications. This also results in slower write and erase operations (1 ms/0.1 ms) (Hemavathy and Meenakshi, 2017). The use of DRAM with a single transistor, commonly known as zero-capacitance RAM, is necessary to overcome some scaling challenges (Fujisaki, 2013). Although this kind of memory solves the scaling issues, its use as universal memory is constrained by the drawbacks such volatile ionization ignition and the need for high operating voltage. Therefore, scientists are working to create memories that get around these constraints by developing memories that are non-volatile like FLASH memory, highly scalable like DRAM and FLASH, fast like static random-access memory (SRAM), and durable like DRAM and SRAM. It has long data retention, scalability to meet growing technological demands of high density, quick access times for quick data retrieval, and durability to survive repeated read and write operations. This perfect memory 'universal memory' would incorporate the greatest attributes of many memory kinds. By meeting these objectives, researchers hope to create a memory technology that transcends the constraints of available choices and provides a flexible and effective solution for a range of applications.

Magneto resistive RAM (MRAM) (Sousa and Prejbeanu, 2005; Suzuki and Swanson, 2015; Senni et al., 2016) is promising with universally appealing properties like, high read and write speeds combined with non-volatile memory that has limitless endurance. The magnetoresistance of CoFeB/MgO/CoFeB based magnetic tunnel junctions found to be 230% or more is ideal for the high density MRAM (Chen et al., 2023). However, most obvious issues are the long-term stability of magnetic layers, ultrathin tunnel barriers, and data retention. With a high breakdown voltage and a very thin layer of aluminum oxide as the tunneling barrier in MRAM found to be stable (Åkerman, 2005; Yuasa and Djayaprawira, 2007). Over time, the inter-diffusion layers between the magnets have an impact on the switching performance. According to the results of the accelerated test, the switching performance of MRAM will not change over the course of 10 years (Kokado and Harigaya, 2003). Motorola unveiled the single transistor and tunnel junction MRAM in 2002 with Read-and-write cycles of 50 ns For many years, companies like Siemens, Motorola, Hitachi, and Hewlett Packard have done extensive studies on the problems with MRAM addresses. However, the memory producers are still not ready to begin mass-producing MRAM. One such difficulty is the non-uniformity of the insulating barrier. This is so that both the barrier's thickness and the direction of relative magnetization are impacted by the resistance of tunnel junctions. Due to thermal fluctuations, super-para-magnetism with small magnetic particles raises concerns about the loss of magnetic information. For the discovery of fully universal memory based on magnetic tunnel junction, significant advancements are required. The production of Spin-Transfer Torque (STT) MRAM (Sharma et al., 2021; Marinella, 2014), in which individual electrons are used to represent 1s and 0s to adjust the magnetic orientation of cells in MRAM, has been jointly undertaken by Samsung, IBM's Flexible Foundries of Memory and IBM's Spin-Transfer Memory. This could expand the application's market to include more mobile and IoT devices in addition to the sensor controller of Sprite Sats. Thus, a basic strategy for strengthening and upgrading the performance of current MRAM technology is required to realize "universal memory" with magnetic tunnel junctions.

The Laboratory of Functional Materials and Devices for Nano electronics at the Moscow Institute of Physics and Technology (MIPT) has information on the potential of the insulator hafnium oxide (Fabian et al., 2017; Ambriz-Vargas et al., 2017a; Abuwasib et al., 2015). The MIPT memory technology has been demonstrated to be faster than SRAM and to have a lower potential power consumption and non-volatile similar technologies. Hafnium dioxide is used as the storage medium in these developments at Sema Tech research centers (Bettinger et al., 2020; Kingon et al., 2000). It was accomplished by modifying the resistance using conductive filaments. RRAMs made of titanium dioxide have not yet reached commercialization despite 8 years of study by Hewlett Packard and Hynix, a major memory manufacturer in Korea.

FRAM is another contender for global memory that Texas Instruments (TI) has developed (Abdullaev et al., 2020; Mueller, 2018). With the elimination of memory hierarchy and the ability to sense vibration, pressure, temperature, motion, humidity, and pollution, TI has been converted into a compact microcontroller that may be used for field data loggers. As a challenger to SRAM that offered Fe-accelerating RAM's speed, reduced power requirements, non-volatility of flash, and decreasing DRAM size, TI pitched Fe-RAM as a high-performance memory architecture that could also function as universal memory. The inventors of magneto-electric memory technology are from the Cornell University (Roco et al., 2011). By using electric potential alone, the magnetic and ferroelectric properties of MRAM and FRAM, based on multiferroic material, can flip from 1 to 0 with less energy. In more recent research, interest in ferroelectric memory has been intensified due to the ferroelectric characteristics of CMOS compatible doped HfO_2 and $HfZrO_2$ ultra-thin films in tunnel

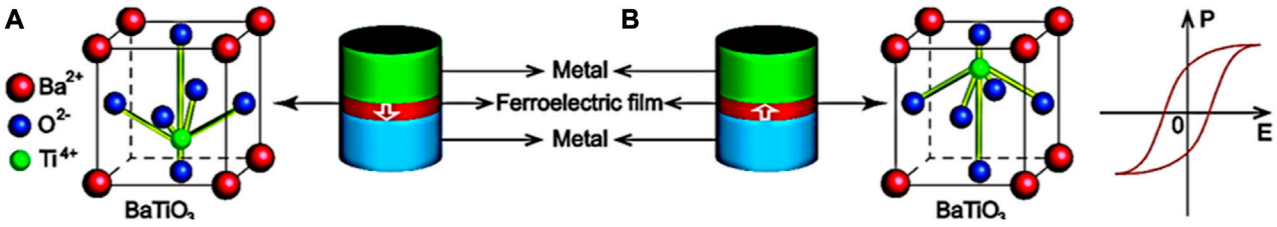

FIGURE 2
The basic construction of a typical FTJ. **(A)** $BaTiO_3$ is used as an example to demonstrate the polarized ferroelectric barrier's lattice on the left and right sides, **(B)** The ferroelectric barrier's polarization-electric field (P–E) hysteresis loop.

junction (Chen et al., 2021; Hur et al., 2022). In the framework of 3D neuromorphic computing systems, ferroelectric tunnel junctions (FTJs) based on HfO_2 are being investigated for non-volatile memory applications (Tsymbal and Kohlstedt, 2006; Kolhatkar et al., 2018; Kolhatkar et al., 2019). The research shows simulation-captured hysteresis behavior in the form of tunneling I-V curves for FTJs based on 9-nm ferroelectric HfO_2 (Kim et al., 2023). In FTJ, polarization reversal allows for a change in tunneling resistance in ultra-thin films (< 3 nm). With an overview of the various resistance states, it is a possible application in non-volatile memory. Since FTJ is significantly more developed than FeFET, it is covered in detail in this study. This combination of silicon-based technology with ferroelectric thin film offers the possibility of combining DRAM's quick read and write capabilities while keeping the latter memory's size modest and non-volatile.

2 Ferroelectric tunnel junctions

Esaki was indeed ahead of his time when he proposed a polar switch in 1971 that used a switchable thin-film ferroelectric material (Maksymovych et al., 2009; Mikolajick et al., 2021; Mikolajick et al., 2022). However, there were constraints on experimental methods and the ability to create high quality ultra-thin film of ferroelectric materials that could act as tunneling barriers at that time. It was also widely accepted that the critical thickness needed for ferroelectricity in thin films was substantially greater than the thickness required for tunneling (Abuwasib et al., 2015). Ferroelectricity was thought to disappear at critical thicknesses considerably below the nanometer range, so it was disregarded for about 30 years. It was not until 2003 that nanoscale ferroelectricity in ultrathin films with a few unit cells of thickness was proven to exist (Gao et al., 2017; Jia et al., 2007). This discovery opened the intriguing possibilities for ferroelectric tunnel junctions (FTJs) by producing thin films with ferroelectric characteristics that are appropriate for tunneling, which was reported in the scientific literature (Jia et al., 2007). Polarization reversal caused by the application electric field can quickly affect the conductance of FTJ. When the applied field matches the coercive field of the ferroelectric, this will lead to resistive switching. At the electrode barrier contact, polarization reversal changes the sign of the polarization charges (Ambriz-Vargas et al., 2017b). The FTJ structure with the Ferroelectric (FE) barrier can be seen in Figure 2. These are anticipated to have different current-voltage properties than typical tunnel junctions with dielectric barrier layer (Park et al., 2015).

In 2009, scanning probe microscopy was used to observe the Tunneling Electro resistance (TER) effect experimentally in ultrathin $BaTiO_3$ (BTO) utilizing conductive tips and metallic oxides as the top and bottom electrodes (Gao et al., 2012; Dubourdieu et al., 2013). Following that, several FTJ structures with various ferroelectric materials and electrodes were suggested and elaborated in the literature. A ferroelectric ultrathin film sandwiched between two metals makes up the majority of an FTJ's (Huang, 2019; Fey et al., 2021) core structure (M/FE/M structure). Through the tunneling effect, the ferroelectric film serves as a barrier to control electrons to pass through. The cation's displacement from its centrosymmetric position results in a spontaneous polarization in the ferroelectric barrier. One of two directions can be chosen for this spontaneous polarization. By using an external voltage or mechanical stress, polarization change can be accomplished reversibly. The probability of electron tunneling differs for the two opposing polarization orientations due to the variation of the barrier potential profile caused by polarization switching. It causes the junction resistance to switch non-between a high (ON) and a low (OFF) level and is known as Tunneling Electro resistance (TER) (Kokado and Harigaya, 2003). The OFF/ON resistance ratio is known as the TER ratio, the more is better for the reliable operations memory cell. Since spontaneous polarization can persist in the absence of an external voltage, allowing the FTJ remain in the ON and OFF state permanently to be used in non-volatile memories (NVMs).

Two conditions must be met to create a reliable FTJ, i.e., the ferroelectric layer must be thin enough to allow for electron tunneling, thickness below the tunneling regime (< 3 nm). It is also necessary for two ferroelectric/metal interfaces (either side of the barrier layer) to be asymmetrical to provide different potential barrier heights for different polarization orientations. Following are the specifics of the operating principle. In the absence of an applied voltage, Figure 3 shows the potential profile of an FTJ for the opposing polarization orientations. In this case, two metals (M1 and M2) are made with different materials to create asymmetric interfaces. The potential profile changes when ferroelectric polarization is reversed, as already mentioned. The following factors, among others, affect the potential profile: i) polarization reversal; ii) variation in barrier thickness brought on by the opposite piezoelectric action; and iii) modification of barrier/

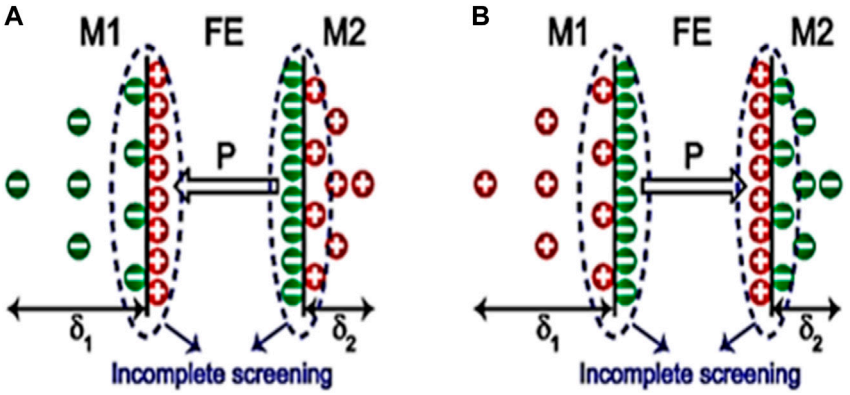

FIGURE 3
(A) Ferroelectric polarization, and **(B)** Depolarization caused by asymmetric charge screening (Wang L. et al., 2016; Yoon et al., 2019).

electrode interfaces brought on by insufficient polarization charge screening (Tsymbal and Kohlstedt, 2006). The third theme is thought to be the most important component causing the TER effect, as will be discussed later.

The ferroelectric polarization causes surface charges at the barrier/metal contacts, as seen in Figure 3A. The charges from the metals must screen out these surface charges. However, the screening is insufficient because, in each metal, the screening charges are typically distributed over a finite length away from the interface (shown by δ1 and δ2 in Figure 3), which is known as the screening length. The distribution of charges was predicated on the supposition that there is no other interface effect. Figure 3B shows that a depolarization field (E_{dep}) opposing the ferroelectric polarization is created in this situation by the imperfect charge screening at the barrier/metal contacts. It is further hypothesized that the only source of the tilting of the electrostatic potential within the ferroelectric film is the depolarization field. The electrostatic potential at two barrier/metal interfaces is then asymmetric since the screening lengths for the two metals M1 and M2 are not identical, as shown in Figure 3A. A straightforward Thomas–Fermi model can provide the electrostatic potential profile ($\varphi(x)$) in these circumstances if the FTJ is short-circuited as Equation 1 (Ricci, 2015; Wang, 2015; Boyn, 2016):

$$\varphi(x) = \begin{Bmatrix} \pm \frac{\sigma_s \delta_1}{\varepsilon_0} \exp\left(\frac{x}{\delta_1}\right), x \le 0 \\ \mp \frac{\sigma_s}{\varepsilon_0 d}\left[x(\delta_1 + \delta_2) - \delta_1 d\right], 0 < x < d \\ \mp \frac{\sigma_s \delta_2}{\varepsilon_0} \exp\left(-\frac{x-d}{\delta_2}\right), x \ge d \end{Bmatrix} \quad (1)$$

where δ_1 and δ_2 are the Thomas–Fermi screening lengths in the materials M1 and M2, σ_s is the screening charge per unit area, ε_0 is the vacuum permittivity, and d is the thickness of the FE film. The upper and lower signs signify situations with polarization toward M1 and M2, respectively.

With Equation 1 shown above, the opposite polarization orientations of the average potential barrier heights can be calculated as (Wang, 2015; Useinov et al., 2022; Cai et al., 2010):

$$\begin{Bmatrix} \overline{\varphi_{\leftarrow}} = U + \frac{\sigma_s}{2\varepsilon_0}(\delta_1 - \delta_2), \text{polarization towards M1} \\ \overline{\varphi_{\rightarrow}} = U + \frac{\sigma_s}{2\varepsilon_0}(\delta_2 - \delta_1), \text{polarization towards M2} \end{Bmatrix} \quad (2)$$

where U is the total of all additional contributions to the potential profile, excluding $\varphi(x)$.

As a result of δ_1 and δ_2, average potential barrier heights for the polarization orientations that are opposed to one another differ. As a result of the tunneling current's exponential reliance on the square root of the potential barrier height, there are differences in tunneling resistances as well (Wang, 2015). The electrostatic potential at the interfaces, i.e., $\varphi_1 \equiv |\varphi(0)| \neq \varphi_2 \equiv |\varphi(d)|$ varies depending on the length of the screening process. This results in an asymmetric potential profile. According to the dashed line, polarization switching caused variations in the ferroelectric layer's potential. Changes in junction resistance in a ferroelectric barrier are caused by polarization switching. The homogeneous polarization with relative displacements between ions of opposing charge is caused by the lattice distortion in bulk ferroelectric perovskites. According to reference (Samara and Morosin, 1973), the phenomena of the "soft mode" is indicated by the attenuation of both the restoring force and the occurrence of zero frequency. The idea of the soft mode encompasses the cooperative mobility of ions within bulk materials, symbiotically working with theoretical predictions of ferroelectric properties and their related dimensions. Therefore, it may be possible to scale this phenomenon down to work within the parameters of nanoscale activities. The depolarizing effect in ferroelectric films can be used to illustrate the theory underlying the critical thickness. The depolarizing field produced utilizing polarization charges stored on the film's surface. Between these two electrodes, a ferroelectric layer screens the charges (Figure 4). If the thickness of the ferroelectric film is further reduced, there will be incomplete screening, which will cause the ferroelectric state to become unstable because electrostatic charge (which is produced by the depolarizing field) will be able to overcome the energy gained from the ferroelectric ordering. Therefore, it is evident that the interfacial atom in a ferroelectric readily influenced the ferroelectricity. Due to the interfacial layer, there is a breakdown in symmetry, which results in electric dipoles at interfaces. Reduced

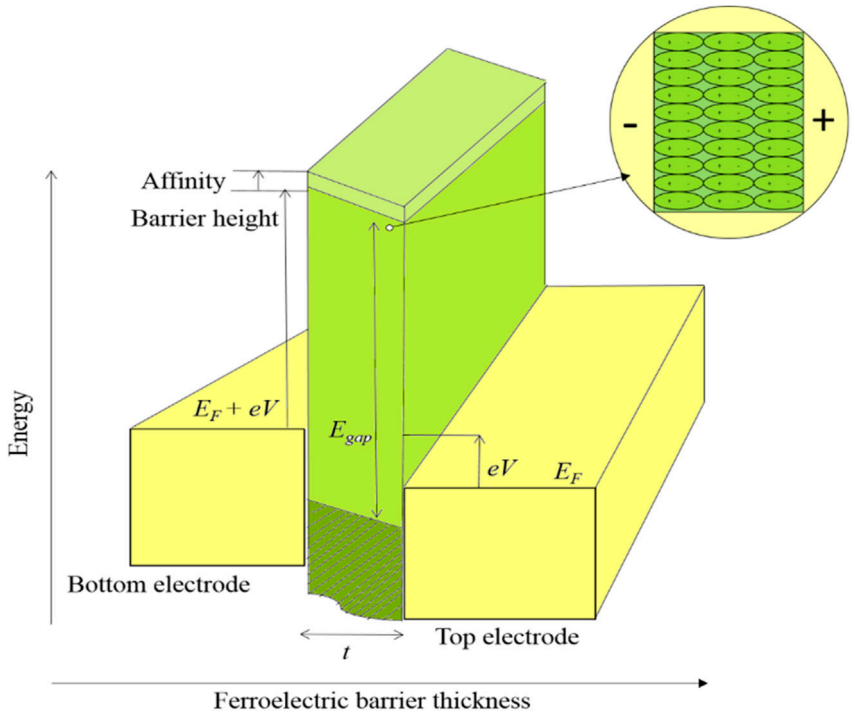

FIGURE 4
The pictorial representation of the ferroelectric tunnel junction with E_{gap} is the energy gap, E_F is the Fermi energy, V is the applied voltage, and t is the barrier thickness under the applied voltage (Tsymbal and Kohlstedt, 2006).

symmetry can occur for a variety of reasons, including straining at the interface, atomic rippling, changed valence, a different work function, and nonstoichiometric. It is also possible to discuss by applying the Ginzburg-Landau-Devonshire free energy per unit area to the density-functional calculation of interfacial polarization and its phenomenological description as follows (Richman et al., 2019; Taherinejad et al., 2012):

According to the results of the FTJ model Pt/$BaTiO_3$/Pt studied, the ferroelectric switching-dependent tunneling conductance is influenced by changes in the bonding at the interface, the rate at which evanescent states decay, and the electrostatic potential at the barrier. The barrier's inadequate screening as well as the FTJ's interfacial and strain effects are clarified by the transmission functions and attenuation constant, respectively. An interfacial layer existence is due to atoms bounded to the electrodes. It has an impact on the barrier's decay rate and, consequently, on the electron transmission through it. Barrier thickness changes and tunnel conductance are both impacted by the voltage applied across junctions (Tsymbal et al., 2012; Gruverman et al., 2009).

The polarization strongly depends on factors like strain, charge, and compositional variations and are the significant external factors. As discussed before, ultrathin barrier layers are necessary for the FTJ device's manufacturing. Characterization and comprehension of ferroelectricity's scaling are crucial. It was once thought that depolarization caused FE to vanish in films with a thickness less than 100 nm (Park et al., 2023; Morozovska et al., 2017). Because of this, FTJ was not practicable with oxide films thicker than 6 nm. Researchers, however, counter this with a minimum FE oxide thickness of 2.4 nm (Ezzaier et al., 2018; Martin et al., 2008). Wide gap oxide semiconductor also shows ferroelectricity. GaN or III-V, ZnO or II-VI with 3.4 eV, perovskite oxide BTO, $SrTiO_3$ with 3.2 and 3.6 eV, and PTO with 2.9 eV band-gap have all demonstrated the same assertion (McCluskey and Haller, 2018). The qualities of TJ can be improved by the by selecting proper FE material. The FE polarization's direction has an impact on resistive switching, making it possible to separate it from the well-known resistive switching of oxide materials (Wang et al., 2020; Pertsev and Kohlstedt, 2010). The $BaTiO_3$ (BTO) films have already shown ferroelectricity to a thickness of 1 nm and 75,000% electro-resistance. M. Bibes and A. Gruverman published the TER effect's initial experimental demonstration in 2009 (Tsymbal et al., 2012). BTO (Sulaev et al., 2015; Li et al., 2015) was utilized as an incredibly thin ferroelectric layer in both situations. The development of nondestructive polarization readouts as a result of the order 2 TER effect opened up new possibilities for nonvolatile memory technology. Although many oxides exhibit switching behavior, oxygen vacancies, grain boundaries, and dislocations can have an impact. The characteristics of the FE as a barrier layers influence the likelihood of transmission in the following ways: 1) piezoelectricity of the FE material of the barriers results in strain with applied voltage and changes the transport characteristics; 2) incomplete screening of the FE results in the electrostatic potential; and 3) B-site displacement results in the interface of atomic orbital hybridization that differs from orientation polarization, as in the case of the BTO/$SrRuO_3$ interface. The conductance effect of this displacement affects

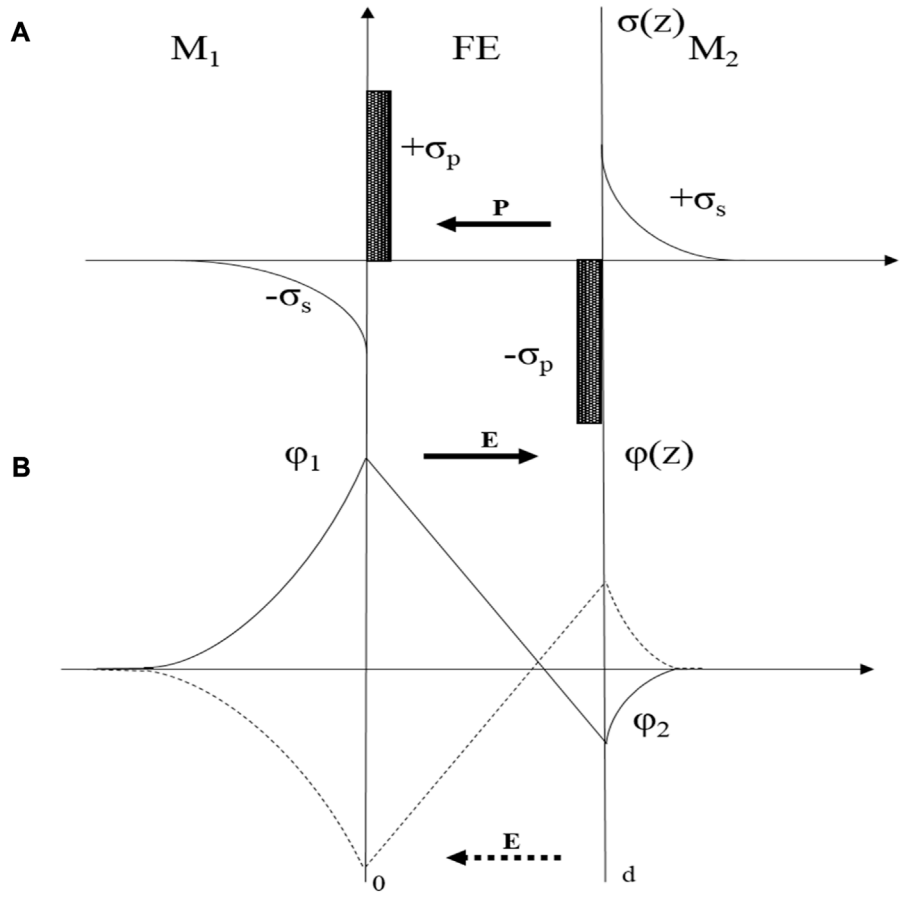

FIGURE 5
Electrostatic effect of M_1-FE-M_2: **(A)** The charge vs. distance distribution and their respective **(B)** profile of electrostatic potential vs. distance (dark line) (Gruverman et al., 2009).

the current-voltage characteristics of FTJ. The barrier/electrode interface is altered by the switch from +P to −P in polarization (as shown in Figure 5). It is difficult to determine whether polarization orientation and tunneling conductance are correlated. One of the issues with measuring conductivity with polarization changes and their experimental analysis utilizing the electro-resistance effect using the polarization control. Another challenge is the polarization stability of ultra-thin ferroelectric films barriers. Loss of polarization retention and relaxation of TER are brought on by the less effective polarization screening of oxide metal in comparison to normal metal. In line with the FE displacement of the barrier layer as BTO, the tunneling conductance significantly decreases. Apart from the inorganic oxides (Pb(Zr, Ti)O_3, BTO, BFO, and (Ba, Sr)TiO_3), TER effect was demonstrated by the organic barriers, specifically the copolymer films of polyvinylidene fluoride (PVDF) 70%-trichloroethylene (TrFE) 30% (Pawar et al., 2023). Researchers noticed the apparent change when the polarization was reversed and was accompanied by an I-V diode. The geometry suggested by Zhuralev et al. can be used practically and does not require the FTJ arrangement with electrodes (Wang et al., 2022). The tunnel profile in such a device is thought to represent a superposition of variable potential coming from the FTJ conduction band.

2.1 Resistive memory with FTJ

A few binary as well as complex oxide materials show resistive switching (Jeong et al., 2012). Chua asserted the existence of the circuit component based on flux-linkage to charge way back in 1971 and gave it the name memory resistor (memristors), a non-linear resistor (Mouttet, 2012). The physical processes that led to the emergence of memory resistance in a material includes self-heating, chemical reactions, spin polarization, phase transitions, and ionic transfer. The construction of an additional barrier in a semiconductor showed memristive behavior in a metal/ferroelectric/semiconductor FTJ by the tunnelling modulations (Ricci, 2015; Wen and Wu, 2020). Multilevel memory and logic devices use the benefits of huge resistance switching effect, control of transport spin polarization, low operating power, non-destructive reading, scaling down to the nanoscale range, and programmable resistance (memristive). With Co/Pb(Zr,Ti)O_3/$(La_{0.7}Sr_{0.3})MnO_3$, Pt/BTO/$SrRuO_3$, $(La_{0.67}Sr_{0.33})MnO_3$/$BiFeO_3$/$(La_{0.67}Sr0.33)MnO_3$, Cr/BTO/Pt, and Co/$BiFeO_3$/$LaNiO_3$, the behavior of TER may be investigated (Neumann et al., 2013; Zenkevich et al., 2013; Garcia and Bibes, 2020). The direction of polarization, which can be changed by an applied electric field, determines the resistance of the barrier. Because of

this tunnel electro-resistance, ferroelectric states are not damaged by the reading. Examples of interface barriers with electrodes are STO at the interface of BTO/SRO, CoOx layer with Co/BTO interface (Wang et al., 2016). The stable polarization was established by Triscone and his team in Geneva using a 4-nm epitaxial film of the FE perovskite $Pb(Zr_{0.2}Ti_{0.8})O_3$ (Guyonnet et al., 2011). Using synchrotron radiation on PTO with a thickness of 1.2 nm, the Argonne National Laboratory examined the FE properties (Petkov et al., 2007). The surface accumulation of charges corresponds to a minimal ON state capacitance. Due to the presence of the space charge zone, the capacitance measured to the OFF state should be lower than the ON state. Tunable OFF state suggests the use of hetero-configurations of metal, ferroelectrics, and semiconductors in memristive devices (Wen et al., 2014). HfO_2 and $HfZrO_2$ films with 2 nm tested both maintain their ferroelectricity to 5 nm. A current density of 75 A/cm^2 that is higher than previously reported values was measured at 0.1 V. This makes one of the promising applications for ultra-low-power NVMs due to the CMOS compatibility. Non-centrosymmetric orthorhombic structure of the thin films of HZO and HFO is responsible for the ferroelectricity (Sulaev et al., 2015; Li et al., 2015; Mo et al., 2018; Saitoh, 2020). Low ON/OFF ratio ferroelectrics have lower switching energies than those employing traditional junctions. The use of interfaces allows for a significant improvement in the ON/OFF ratio. Along with the FE barrier, these interfaces reduce depolarization field screening. This leads to polarization being unstable, which in turn affects the resistive switching's retention characteristics. Interface modulation as a result results in 105% ON/OFF resistive switching. The memristors consist of two terminals, where resistance can be continually modified using the amplitude, duration, and electrical impulses that have already been applied. The $Co/BFO/Ca_{0.96}Ce_{0.04}MnO_3$ (Fabian et al., 2017) (CCMO) fully integrated device was studied and large TER was observed. For calculating the potential, the model used Thomas–Fermi screening with a short-circuit boundary conditions screening tool. The electrostatic potential can be denoted as (Stengel, 2013; Hwang et al., 2020):

$$\varnothing(z) = \begin{cases} \varepsilon_0^{-1}\sigma_s\delta\, exp\left[\dfrac{(z+b)}{\delta}\right], & z < -b \\ -\varepsilon_0^{-1}\sigma_s\delta\, exp\left[-\dfrac{(z-b)}{\delta}\right], & z > a \end{cases} \tag{3}$$

Where.σ_s, screening chargeδ, Thomas–Fermi *screening* length of the electrode (assumed to be identical)a thickness of the *ferroelectric* layer.*b, the* thickness of the *dielectric* layer.*P,* the polarization of the ferroelectric layer.ε_f, dia the *electric* constant of the ferroelectric layerε_d, dia the *electric* constant of the electric layer

The interface potential and the screening charge can be determined from boundary conditions,

$$\begin{aligned} \sigma_s &= \frac{a\varepsilon_d\varepsilon_0^{-1}P}{a\varepsilon_d + b\varepsilon_f + 2\varepsilon_f\varepsilon_d\delta} \\ \varnothing(0) &= \frac{(\delta\varepsilon_d + b)a\varepsilon_0^{-1}P}{a\varepsilon_d + b\varepsilon_f + 2\varepsilon_f\varepsilon_d\delta} \\ \varnothing(-b) &= -\varnothing(a) = \frac{a\delta\varepsilon_d\varepsilon_0^{-1}P}{a\varepsilon_d + b\varepsilon_f + 2\varepsilon_f\varepsilon_d\delta} \end{aligned} \tag{4}$$

The tunneling conductance can be calculated using the Landauer formula for the FTJs per unit area:

$$G = \frac{2e^2}{h}\int \frac{d^2k_{\|}}{(2\pi)^2} T(E_F, k_{\|}) \tag{5}$$

The energy E_F at the Fermi level gives the transmission coefficient of $T(E_F, k_{\|})$ for a transverse wave factor $k_{\|}$. The potential developed across the boundary condition is obtained using the Schrödinger equation. The transmission coefficient of an electron moving with the potential $V(z)$ of the incoming wave can be normalized to a unit flux density. The solution obtained numerically for $V(z)$, the step-wise potential arises from the minimum conduction band and electrostatic potential superposition of $\phi(z)$ (Zhuravlev et al., 2009). The experiment showed the local transport of electrons on a thin ferroelectric film deposited on the metal layer using AFM. The controlled effect of the dielectric layer gives rise to new opportunities to modify TER. With the reversal of polarization, electrostatic potential changed and among the interface, non-polar film started acting as a switch for changing the barrier height from high to low values. It causes a change in transmission across FTJ. The orientation of the polarization-to-resistance ratio may reach large values (Zhuravlev et al., 2009). The current across the thick ferroelectric incorporates resistive and non-destructive readout of information with restricting miniaturization of circuits. The thickness of such ferroelectrics can be reduced to nanometers; hence their electric conduction enhancement becomes possible. The ferroelectric PTO tunnel barrier showed 50,000% TER through a 3.6 nm film (Bez and Pirovano, 2004; Fujisaki, 2013). When calculating the ER of a ferroelectric barrier film, the various transport mechanisms such as direct tunneling, thermionic injection, and Fowler-Nordheim tunneling (Chiou et al., 2001; Ikuno et al., 2011; Rumberg and Graham, 2013) are considered. These depend on the thickness of the barrier, the polarization's direction, and the ferroelectric and metallic properties.

Large ER are presented by the yield with direct tunneling and FNT presented by the 5 nm BFO film, among others (Wen and Wu, 2020). Theoretical calculations, synthesis, and ferroelectric material research have inspired a focused investigation into ferroelectric tunnel junction (FTJ) feature acquisition. A variety of cutting-edge thin film deposition techniques are used to create these films, including chemical vapor deposition (CVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE), and pulsed laser deposition (PLD).

The lattice mismatch between the substrate and the ferroelectric (FE) film must be considered while choosing substrate materials to enable strain control of the properties. The influence of compressive strain on the TER effect in $BaTiO_3/SrRuO_3$ (BTO/SRO) hetero-structures was examined by the researchers. They discovered that by applying epitaxial strain through the lattice mismatch of $NdGaO_3$ and $SrTiO_3$ with BTO and SRO layers, the ferroelectric polarization of BTO was enhanced, and the metallicity of the SRO films was raised. The reduced asymmetry in the tunneling barrier brought on by the shortened screening length of SRO under strain had a detrimental influence on the TER effect, even though the increased polarization was advantageous for the TER magnitude. The work emphasizes how crucial it is to consider both the

ferroelectric barrier's strain-induced polarization and the electrodes screening qualities to forecast and comprehend the TER effect in ferroelectric tunnel junctions.

The ferroelectric barrier is continuously tuned with domain switching resulting in the changing of tunneling resistance to some order of ON and OFF states in metal/ferroelectric/metal. The obtained characteristics, i.e., retention and endurance of Co/BFO/CCMO structure are 10 years via 10^3% ON/OFF resistance ratio. The inorganic binary oxides such as MgO_x, AlO_x, SiO_x, TiO_x, ZnO_x, HfO_x, MoO_x, CeO_x, YbO_x (Tsymbal and Kohlstedt, 2006; Kolhatkar et al., 2019; Hur et al., 2022) and more complex oxides like $LaAlO_3$, PCMO, BTO, BFO, STO, LC (or S)MO offers extreme switching characteristics with > 10^{12} cycles of endurance. There is a large (OFF/ON) of 300 with Co/$PbZr_{0.2}Ti_{0.8}O_3$/$La_{0.7}Sr_{0.3}MnO_3$ reported (Ogimoto et al., 2003; Yin et al., 2015) tunnel junctions with 220 nm diameter. The 10,000 value of ON/OFF was shown by the Co/BFO/$Ca_{0.96}Ce_{0.04}MnO_3$ configuration. The Pt/BTO/Nb: STO (Wen et al., 2014), device structure has continuously varying tunnel resistance affected by the polarity and amplitude. According to the capacitance measurement, the domain switching and semiconductor electrode in the ultrathin FTJ's regulate the width of depleted space-charge carriers on the surface. Only thin barrier layers can achieve steady polarization. The TiN/HZO/Pt (Dörfler et al., 2020; Yang et al., 2021; Cheng, 2021) hetero-structure with 20 nm thick $Hf_{0.5}Zr_{0.5}O_2$ developed on Si has been used as a representation of the experimental demonstration of perovskite tunnel barriers with CMOS compatibility. Pt electrodes with a thickness of 30 nm were used for the electrical characterizations. The examined structure has a TER of 15, which adds to HZO's standing as a strong contender for Si memory technology. One way to express the measured tunneling current density (J) is as follows as Equation 6 (Cheng, 2021):

$$J = -\left(\frac{4em}{9\pi^2\hbar^3}\right)\left(\frac{exp\left\{\alpha(V)\left[\left(\varphi_2 - \frac{eV}{2}\right)^{\frac{3}{2}} - \left(\varphi_1 + \frac{eV}{2}\right)^{\frac{3}{2}}\right]\right\}}{\alpha^2(V)\left[\left(\varphi_2 - \frac{eV}{2}\right)^{\frac{1}{2}} - \left(\varphi_1 + \frac{eV}{2}\right)^{\frac{1}{2}}\right]^2}\right) \times \sinh\left\{\frac{3}{2}\alpha(V)\left[\left(\varphi_2 - \frac{eV}{2}\right)^{\frac{1}{2}} - \left(\varphi_1 + \frac{eV}{2}\right)^{\frac{1}{2}}\right]\frac{eV}{2}\right\}$$

where,

$$\alpha(V) = \left[4d(2m)^{\frac{1}{2}} / \left[3\hbar\left(\varphi_1 + eV - \varphi_2\right)\right]\right]$$

ħ is reduced Plank constant

$$\varphi_1 = 1.86\,eV/2.75\,eV, \varphi_2 = 2.36\,eV/2.20\,eV$$

Electrode charge, *e*; effective electron mass, *m*; layer thickness, *d*; ferroelectric electrode interfaces, φ_1 and φ_2.

It is possible that a non-ferroelectric monoclinic phase exists when the HZO (Chen et al., 2018) material is thicker than 20 nm, which causes it to lose its ferroelectric capabilities. Ferroelectricity may, however, be maintained without any issues up to a thickness of 40 nm by increasing the number of stacked layers. Al_2O_3 is introduced to reduce leakage current, which results in a considerable decrease. When the ferroelectric (FE) barrier's polarization is reversed, the 6 nm Pb $(Zr_{0.52}Ti_{0.48})O_3$ film displays resistive switching. On the bottom electrode, lattice mismatch is reduced by employing perovskite crystal structures like PZT or BTO. SRO and BTO have fewer than 2% lattice mismatches. When the thickness of PZT is lowered to a minimal level, a phenomenon known as the passive layer effect or low dielectric layer effect occurs that causes the Remanent polarization (P_r) to decrease while the coercive field (E_c) to grow. According to earlier research, such as the Kay-Dunn law, E_c rises as thickness falls. Investigation of the properties of incredibly thin ferroelectric films is made possible by the Piezo force microscopy (PFM) method. Polarization is produced when a voltage is supplied to a metallic FE electrode, just like a regular FE capacitor. As a result, it is possible to characterize and manipulate polarization domains as well as comprehend stability, domain dynamics, switching speed, and reading and writing methods. The depolarization field can be used to explain why ferroelectrics have a critical thickness and why charges build up on the film surface. The charge polarization is screened by the interface between the metal electrodes. A state that is unstable results from insufficient screening, which causes the electrostatic energy associated with the depolarization field to overwhelm the energy acquired through FE ordering. Therefore, it is thought that the depolarization field reduces the critical thickness of the film.

The displacement of the soft mode is greatly influenced by the interlayer bonding at the interface. In the metal electrode, strong interface bonding prevents border atoms from moving about, preventing soft mode instability, and altering the displacement of other atoms. The local environment at the interfaces is different from the bulk, which furthers the disruption. A third obstacle to symmetry is the uneven local environment at the interfaces compared to the bulk. The second harmonic generation and the para-electric state are increased when the electric dipoles at the interface layer are reduced. The disruption of the tetragonal bulk soft mode between $SrRuO_3$ and Pt caused by bonding at the FE-metal interfaces and atomic displacement was shown using an ultrathin FE film of $KNbO_3$. Understanding the defect mechanism was aided using the TER effect and ferroelectric STO. The Pt/STO/Pt prototype contained a TiSr antisite defect, which boosts the conductance of electron tunneling. Ferroelectric materials can be polarized to control conductance, and ZrO_2, a nanoscale ferroelectric material, is what causes the polarization-induced negative capacitance (NC) in ferroelectrics. Due to the electromotive force that produces NC responses, multi-domain ferroelectrics are produced. A recent innovation called FTJ has the potential to take the role of CMOS-based RAM. FTJ operates in the sub-micrometer range, or at 100 nm or less, as opposed to CMOS, which has 15 nm technology (Zhao et al., 2022; Wang et al., 2015). The characteristics of the ferroelectric barrier material and the selected electrode must be carefully considered to maximize FTJ performance. After SRO showed stability in the RIE process, LSMO (Sandu et al., 2022; Wang et al., 2013) is proposed as a bottom electrode to address technical issues with its conductivity. Due to its long-lasting data retention and stable polarization, cobalt (Co) is a preferred material for a top electrode. A desirable ferroelectric tunneling barrier that is recognized by strain engineers is BTO (1 nm). In BTO/SRO-based FTJs, the top electrode of Pt has been characterized using PFM/c-AFM techniques. Further investigation is required to examine fully integrated circuits with enhanced switching, high-frequency dynamics, rapid pulse measurements, scalability, and reliability. The initial analysis of Ru/BTO/LSMO

TABLE 3 The various material configuration via literature on Emerging Memories.

Year	Main findings or conclusion relevant to the proposed research work			Remarks
	Bottom and top electrode	Ferroelectric barrier	Deposition technique (film thickness)	
2009 (Garcia et al., 2009)	$La_{0.67}Sr_{0.33}MnO_3$	BTO	PLD (1 nm)	Ferroelectricity in 1 nm highly strain BTO
	Cr/Pt			
2010 (Crassous et al., 2010)	$SrRuO_3$	PbTiO3	PLD (3.6 nm)	Giant TER effect FE of Retention of 72 h
	Conductive Tip			
2012 (Chanthbouala et al., 2012)	$La_{0.67}Sr_{0.33}MnO_3$	BTO	PLD (2 nm)	TER ratio = 64
	Co/Au			On/OFF cycles = 900
2012 (Pantel et al., 2012)	Au/Co	BTO	PLD (1.6 nm)	TER ratio = 300 at ± 0.4 V Brinkman model
	$PbZr_{0.2}Ti_{0.8}$ O_3			
2013 (Yamada et al., 2013)	$Ca_{0.96}Ce_{0.04}MnO_3$	BFO	PLD (7 u.c.)	TER ratio = 10^4
	Co/Pt			Retention = 68 h
				ON/OFF cycles = 10^3
2013 (Tsymbal and Gruverman, 2013)	Nb: $SrTiO_3$	BTO	PLD (4 u.c.)	Schottky barrier engineering enables TER varying from 400 to 8 × 10^5
	Conducting tip			
2014 (Boyn et al., 2014)	$Ca_{0.96}Ce_{0.04}MnO_3$	BFO	PLD (4.6 nm)	TER ratio = 10^3
	Co			ON/OFF cycles = 10^6
2014 (Zou et al., 2014)	$La_{0.67}Sr_{0.33}MnO_3$	BTO	PLD (6 u.c.)	TER ratio = 6,000 at ±0.2 V
	Graphene			
2014 (Jin Hu et al., 2016)	$La_{0.67}Sr_{0.33}MnO_3$	BTO	PLD (3 nm)	TER ratio of 1000 Brinkman model
	Cu			
2014 (Wen et al., 2014)	Nb-doped $SrTiO_3$	BTO	Sputter deposition (7 nm)	Continuous resistance modulation over four orders of magnitude
	Pt			
2016 (Wang et al., 2016a)	Nb: $SrTiO_3$	BTO	PLD (10 u.c.)	TER effect demonstration
	Au/Ti			
2017 (Ambriz-Vargas et al., 2017a)	TiN	$Hf_{0.5}Zr_{0.5}O_2$	Radio Frequency magnetron sputtering (6 u.c.)	CMOS compatible TiN, TER ratio of 15
	Pt			
2019 (Pawar et al., 2023)	In:SnSe	SnSe	Combining density functional calculation (8 nm)	2D ferroelectric tunnel junction with TER of 1460%
	Sb:SnSe			
2019 (Yoon et al., 2019)	TiN	$Hf_{0.5}Zr_{0.5}O_2$	ALD (4 nm and 5 nm)	TER analyzed using a direct tunneling model along with Wentzel-Kramers-Brillouin approximation
	Pt			

hetero-structures with PFM concentrated on the polarization switching of the tunnel junction and its amplitude.

From Table 3, the following articles pertain to the ferroelectric tunnel junctions (FTJs) research that is being contemplated. In 2009, it was discovered that sandwiched between bottom electrodes of chromium (Cr) and top electrodes of platinum (Pt), extremely strained 1 nm barium titanate (BTO) sheets displayed ferroelectric behavior. Strontium Ruthenate ($SrRuO_3$) bottom electrode and a ferroelectric barrier with a thickness of 3.6 nm were used in 2010 to produce the enormous Tunneling Electro resistance (TER) phenomenon in FTJs. Retention was shown by the TER effect to last 72 h (Law and Wong, 2021b; Dörfler et al., 2020). Cobalt and Gold electrode FTJ in 2012 had a TER ratio of 64 and withstood 900 ON/OFF cycles. This FTJ had a 2 nm BTO barrier between the electrodes. 1.6 nm top electrode made of cobalt and gold was used in another investigation in 2012. Another study from 2012 used a 1.6 nm BTO barrier, a top electrode made of both gold (Au) and cobalt (Co), and a TER ratio of 300 at 0.4 V.

In a study conducted in 2013, a cobalt (Co) bottom electrode and a bismuth ferrite (BFO) barrier with a thickness of 7 unit cells were

used. The results revealed a TER ratio of 10^4, retention of 68 h, and 10^3 ON/OFF cycles. By using a conducting tip on a niobium-doped strontium titanate (Nb: $SrTiO_3$) substrate and a BTO barrier, Schottky barrier engineering was used in 2013 to generate tunable TER ratios ranging from 400 to 8×10^5. The cobalt bottom electrode and a 10^6 ON/OFF cycle TER ratio were the main goals of the 2014 study. Cobalt as the bottom electrode and a bismuth ferrite (BFO) barrier with a thickness of 4.6 nm were employed in the 2014 study to focus on reaching a TER ratio of 10^3 and 10^6 ON/OFF cycles. The usage of graphene as a top electrode and a 6 unit cell. The BTO barrier was examined in the same year, and the results produced a high TER ratio of 6,000 at 0.2 V. As predicted by the Brinkman model, a copper top electrode and a 3 nm BTO barrier exhibited a TER ratio of 1000 in 2014. Using sputter deposition, a 7 nm thick niobium-doped strontium titanate (Nb: $SrTiO_3$) film was deposited on a platinum (Pt) bottom electrode in 2014, enabling continuous resistance modulation over four orders of magnitude. In FTJs with a Titanium bottom electrode and a niobium-doped strontium titanate (Nb: $SrTiO_3$) top electrode, the TER effect was proven in 2016 and the barrier had a thickness of 10 unit cells. A 2017 study used a ferroelectric barrier with a thickness of 6 u. c., a Titanium Nitride (TiN) bottom electrode, a platinum top electrode, and a hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$) ferroelectric barrier to achieve a TER ratio of 15. CMOS technology was discovered to be compatible with the TiN electrode. Based on density functional calculations, a 2D ferroelectric tunnel junction using Tin Selenide (SnSe) as the barrier material and doped with indium (In) and antimony (Sb) achieved a TER of 1460% in 2019. The TER in FTJs with a TiN bottom electrode, a platinum (Pt) top electrode, and a hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$) ferroelectric barrier with thicknesses of 4 nm and 5 nm were examined in another study in 2019. A direct tunnelling model and the Wentzel-Kramers-Brillouin approximation were used to analyze the TER.

3 Conclusion

The article discusses the prospect of creating a "Universal Memory" that combines the non-volatility of FLASH memory, the speed of SRAM, the great scalability of DRAM/FLASH, and the durability of DRAM/SRAM. The future of new memory technologies, including resistive RAM, magnetic RAM, phase change RAM, and ferroelectric RAM, is therefore examined. Among ferroelectric RAM, RAM based on FTJ is superior in terms of the density, retention, and speed. Since it can be produced in high density, with non-destructive read-out, and operated at high speed, FTJ, can be used to realize universal memory. If a ferroelectric material that is compatible with CMOS is found, FTJ has a lot of potential in the memory market. Non-volatile memories are still in the focus of extensive study in terms of manufacture, design, conception, and modelling.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

All authors listed have made a substantial, direct, and intellectual contribution to the work and approved it for publication.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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