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Lifetime prediction of copper pillar bumps based on fatigue crack propagation

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2.5D package realizes the interconnection of multiple dies through Si interposers, which can greatly improve the data transmission rate between dies. However, its multi-layer structure and high package density also place higher reliability requirements on the interconnection structure. As a key structure for interconnection, copper pillar bump (CPB) has small size, high heat generation, and thermal mismatch with silicon chips. The thermal fatigue failure of CPB has gradually become the main failure mode in 2.5D package. Due to the small size of CPB and the large proportion of intermetallic compound (IMC) layers, the lifetime prediction method of spherical solder joints is no longer suitable for CPB. Therefore, it is necessary to establish a fatigue lifetime prediction method for CPB. This paper establishes a method for obtaining the lifetime of CPB based on the basic theory of fatigue crack propagation. Using the extended finite element simulation method, the crack propagation lifetime of CPB under thermal cycling was obtained, and the influence of different IMC layer thickness on the fatigue lifetime of CPB was analyzed. The results indicated that the fatigue lifetime of cracks propagating in the IMC layer is lower than that of cracks propagating in the solder layer, and an increase in the thickness of the IMC layer leads to a significant decrease in the fatigue lifetime of CPB. The lifetime prediction method for CPB proposed in this paper can be used for reliability evaluation of 2.5D package, and has certain reference value for the study of the lifetime of CPB.

KEYWORDS

2.5D package, copper pillar bump (CPB), IMC layer, extended finite element simulation, lifetime prediction

1 Introduction

With the increasing demand for product miniaturization, high I/O density, and heterogeneous integration, higher requirements have been put forward for the front end and back end processes of semiconductors. But currently, the process of transistors is approaching the physical limit, and the benefits of relying on reducing semiconductor gate width to increase integration are decreasing (Wong, 2021; Watanabe, 2009). Therefore, more and more manufacturers are shifting the direction of improving

integration and reducing chip size from front end processes to back end processes, hoping to break through the physical size limitations of chips with more advanced packaging forms. Among them, the 2.5D package can package multiple chips with different functions and structures onto a Si interposers, achieving heterogeneous integration (Lancaster and Keswani, 2018; Zhang et al., 2021; Dale et al., 2020). Due to the shorter distance between chips, this package structure occupies less space, and it has lower power consumption and better electrical performance compared to traditional package (Liu et al., 2016).

In order to realize the vertical electrical connection of 2.5D package, various bump interconnection technologies are used, mainly including copper pillar bumps (CPBs) and C4 bumps (Liu et al., 2016; Zhang et al., 2015). Among these bump technologies, CPBs are the interconnect bumps with the smallest geometric size, shortest pitch, and highest density. Compared with traditional spherical bumps, cylindrical CPBs have higher aspect ratio and can solve the ultra-fine pitch problem of high-density package. At the same time, the CPBs also have excellent electrical and thermal conductivity properties, and the lead-free solder cap can also meet the ROHS requirements. Therefore, CPB technology is more and more widely used in various types of 2.5D and 3D package, and has gradually become a key link in the package.

However, as the size of CPB continues to decrease, the operating current continues to increase, and the working environment temperature is also getting higher, which leads to some problems in the application of 2.5D package. Due to the harmful effects of Pb-containing solders on the environment and human health, Pb-free materials such as SAC305 have been widely used as substitutes for interconnect materials under the National Electronics Manufacturing Initiative (Long et al., 2023). The solder cap material for CPB generally uses lead-free solder materials such as Sn-Ag or Sn-Ag-Cu. The solder joint is prone to producing rich intermetallic compounds (IMC) during use. Under long-term high-temperature action, the solder cap may even completely transform into an IMC layer (Rao et al., 2016; Na et al., 2022; Koo et al., 2007). With the emergence of the IMC layer, the mechanical strength and fracture toughness of the solder joints will decrease, causing crack in the welding helmet to expand more easily and reducing its fatigue lifetime (Gong et al., 2024). In addition, the 2.5D package has a high density and a large heat generation of the chip. The difference in thermal expansion coefficient between the copper pillar in CPB and the silicon material is significant, resulting in a serious thermal mismatch problem in this structure. As its size decreases, the failure of the CPB has become one of the main failure modes of 2.5D package (Jing et al., 2014). Therefore, studying the fatigue failure of CPB plays an important role in improving the reliability of 2.5D package.

Some authors have already noticed that the presence of IMC layers can affect the mechanical properties and reliability of CPB. Kwon et al. (2016) found that under thermal cycling conditions, an IMC layer is formed at the interface between solder and copper, and the thickness of the IMC layer also increases with time and temperature. When the z-direction stress caused by thermal expansion acts on the interface, the crack would propagate along the depletion zone, and eventually microcrack failure would occur. Ajay Kumar and Dutta (2018) analyzed the growth kinetics and shear deformation tests of IMC in thin Sn-3Ag-0.5Cu joints, and inferred that the increase in IMC content caused by heat treatment would lead to a deterioration of the mechanical properties of the joint due to the presence of initial microcracks. Zhu et al. (2020) conducted shear fatigue tests on CPB with different thicknesses of IMC layers and found that their fracture toughness decreased with increasing IMC thickness. They also applied the Coffin-Manon model to predict the fatigue lifetime of CPB, but the accuracy was slightly poor. Li et al. (2020) found that there are two locations for crack propagation at CPB, namely, Sn-Ag solder joint and IMC bump. They also compared the lifetime prediction results of the Darveaux model and Schubert model, and found that the latter should be more suitable for CPB, but both have significant deviations.

At present, many research has been conducted on traditional spherical solder joints. Based on different theoretical systems, lifetime prediction models suitable for different types of solder joints have been proposed. But among these models, most only consider the constitutive model of solder (Su et al., 2019). Generally speaking, in current 2.5D package, the diameter of the more commonly used CPB is about 30 μm, the diameter of the C4 solder ball is about 100 μm, and the diameter of the BGA solder ball is several hundred microns. The volume of C4 solder joints and BGA solder joints is hundreds or thousands of times that of CPB. The proportion of the IMC layer in CPB is much larger than that in BGA solder joints (Yu et al., 2024; Chen et al., 2022). The impact of the IMC layer on the thermal fatigue of CPB cannot be ignored. If the previous lifetime prediction model is completely applied, it may lead to significant prediction deviations. Therefore, it is necessary to develop a new life prediction method for CPB.

In this paper, the CPB within the 2.5D package is focused upon. An equivalent model was utilized to simplify the complex model, and thermodynamic simulation calculations were carried out. The accuracy of the simulation model was verified by measuring the warpage of the chip through moire interferometry. The extended finite element method was employed for fatigue simulation to derive the fatigue lifetime of the CPB. And an analysis of the impact of IMC layer thickness on the fatigue lifetime was also conducted. The proposed fatigue lifetime prediction method for CPB serves as a reference for the reliability assessment of 2.5D package designs.

2 2.5D package equivalent model simulation

2.1 Obtaining equivalent model parameters

The research object selected in this article is the high-density package vega 56 graphics card core produced by AMD. The number of through-silicon vias (TSVs), C4 solder joints, and CPBs in this device is very large, and the sizes of these structures are in the tens of microns. Compared to the entire package, they are all small structures. The method of establishing equivalent models can be used to simplify complex models into simple structures. The following structures need to be simplified: the interposers where the TSVs is located, the C4 solder joints with underfill, and the CPBs with underfill.

Taking the Si interposers as an example and referring to the equivalent parameter calculation methods in Chien et al. (2011)

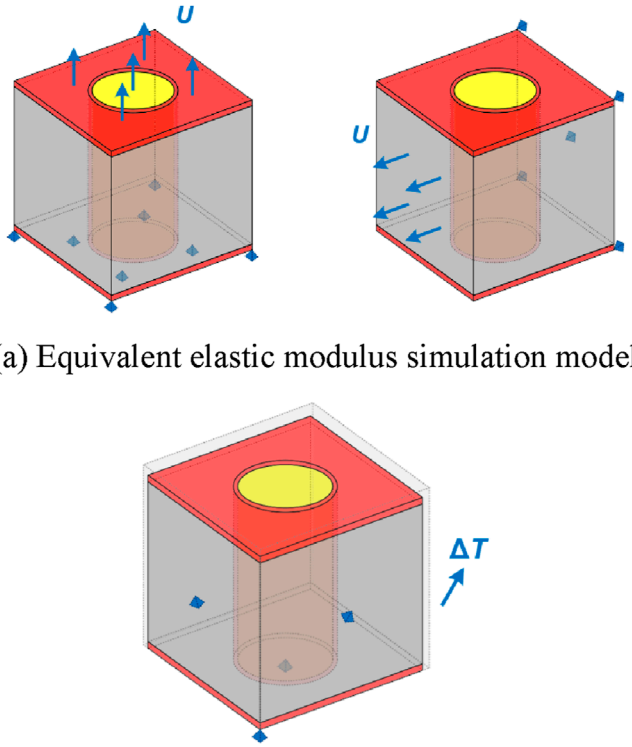


FIGURE 1
Equivalent simulation model. **(A)** Equivalent elastic modulus simulation model. **(B)** Equivalent thermal expansion coefficient simulation model.

and Chen and Wu (2015), the calculation formula of its equivalent thermal conductivity can be obtained as Equations 1, 2.

$$K_{eq,z} = \frac{\beta K_1 + K_2}{1+\beta} \tag{1}$$

$$K_{eq,x,y} = \frac{K_2(\beta K_1 + K_2)\sqrt{\pi/\beta + \pi}}{2K_2(1+\beta) + (\beta K_1 + K_2)\left(\sqrt{\pi/\beta + \pi} - 2\right)} \tag{2}$$

Where $K_{eq,z}$ and $K_{eq,x,y}$ are the equivalent thermal conductivity coefficients in the z-direction and x-y direction respectively. K_1 and K_2 are the thermal conductivity coefficients of TSV (Cu) and Si respectively, and β is the volume ratio of Cu to Si.

For the elastic modulus and thermal expansion coefficient, the finite element method is used to extract their equivalent parameters. Taking the TSV unit model (Figure 1A) as an example, a uniaxial tensile simulation is performed. A fixed constraint is applied to one side of the hexahedral unit, and a small displacement is applied to the opposite side. The support reaction force and stress strain of the unit can be obtained through finite element simulation. The equivalent Young's Modulus and Poisson's ratio of the unit is calculated using Equations 3–5.

$$E_z = \frac{\sigma_z}{\varepsilon_z} = \frac{F_z}{A_z \cdot \varepsilon_z} \tag{3}$$

$$E_{x,y} = \frac{\sigma_x}{\varepsilon_x} = \frac{F_x}{A_x \cdot \varepsilon_z} \tag{4}$$

$$\nu_{x-y} = \left|\frac{\varepsilon_y}{\varepsilon_x}\right| \tag{5}$$

Where E_z and $E_{x,y}$ are the equivalent elastic moduli in the z and x-y directions respectively, $\nu_{x\text{-}y}$ is the equivalent Poisson's ratio, σ_z and σ_x represents the stress in the z and x directions respectively, ε_z and $\varepsilon_{x,y}$ are the tensile strains in the z and x directions (or y directions), and F_z and F_x are the support forces in the z and x directions respectively. A_x and A_z are the cross-sectional areas of the unit model parallel to the x and z directions respectively.

The method for obtaining the equivalent coefficient of thermal expansion is as follows: set the normal degrees of freedom of the three adjacent surfaces of the model to 0, and set the temperature rise of ΔT, as shown in Figure 1B. The thermal expansion coefficient of the model is obtained from Equations 6, 7.

$$\alpha_{x,y} = \frac{\varepsilon_x^T}{\Delta T} \tag{6}$$

$$\alpha_z = \frac{\varepsilon_z^T}{\Delta T} \tag{7}$$

Where $\alpha_{x,y}$ and α_z are the thermal expansion coefficients in the x-y and z directions respectively, and ε_x^T and ε_z^T are the thermal strains in the x and z directions respectively.

The calculation process for density and specific heat capacity is relatively simple. According to the definition of

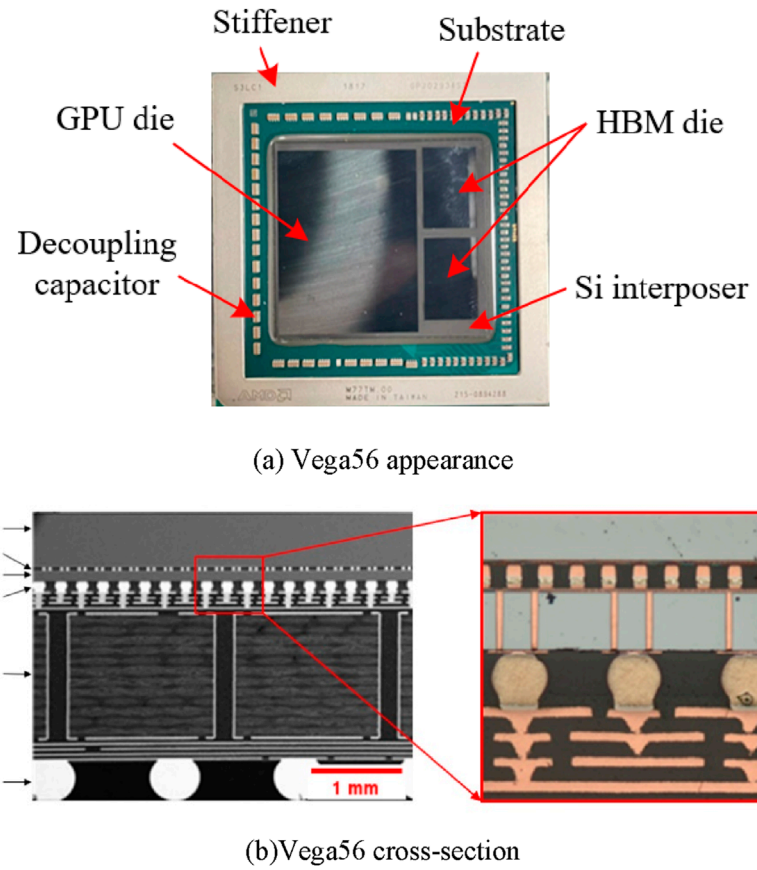


FIGURE 2
Vega56 appearance and cross-section. **(A)** Vega56 appearance. **(B)** Vega56 cross-section.

TABLE 1 Dimensions of Vega56.

Part	Dimensions (length × width × height/diameter × height, mm)
GPU	26.20 × 19.62 × 0.78
HBM	12.08 × 7.78 × 0.76
Si interposer	30.00 × 27.68 × 0.1
CPB	0.024 × 0.04 (pitch: 0.054)
TSV	0.01 × 0.1 (short pitch: 0.06; long pitch: 0.192)
C4 bumps	0.1 × 0.095 (pitch: 0.192)
Substrate	47.5 × 47.5 × 1.64
Stiffener	47.08 × 4.20 × 0.57

density shown in Equation 8.

$$\rho_{eq} = \frac{m}{V} = \frac{m_{Si} + m_{Cu}}{V_{Si} + V_{Cu}} = \frac{\rho_{Si} V_{Si} + \rho_{Cu} V_{Cu}}{V_{Si} + V_{Cu}} \quad (8)$$

Where ρ_{eq} is equivalent density, ρ_{si} and ρ_{cu} are density of Si and Cu respectively. Introducing the volume ratio $\beta = \frac{V_{Cu}}{V_{Si}}$, the Equation 8 can be simplified to Equation 9.

$$\rho_{eq} = \frac{\rho_{Si} + \rho_{Cu}\beta}{1 + \beta} \quad (9)$$

Similarly, the formula for calculating the equivalent specific heat capacity can be obtained as Equation 10.

$$C_{eq} = \frac{\Delta Q}{m\Delta T} = \frac{C_{Si} m_{Si} \Delta T + C_{Cu} m_{Cu} \Delta T}{m\Delta T} = \frac{C_{Si}\rho_{Si} + C_{Cu}\rho_{Cu}\beta}{\rho_{eq}(1+\beta)} \quad (10)$$

Where C_{eq} is equivalent specific heat capacity, C_{Si} and C_{cu} are heat capacity of Si and Cu respectively.

2.2 Simplified model thermal simulation

In this paper, the Vega56 graphics card core, a representative 2.5D package manufactured by Advanced Micro Devices (AMD), has been meticulously chosen as the subject of study. Vega56 contains a graphics processing unit (GPU) die and two high bandwidth memory (HBM) dies. The three dies are interconnected with the Si interposer through CPBs. The Si interposer is interconnected with the substrate through C4 bumps, and the

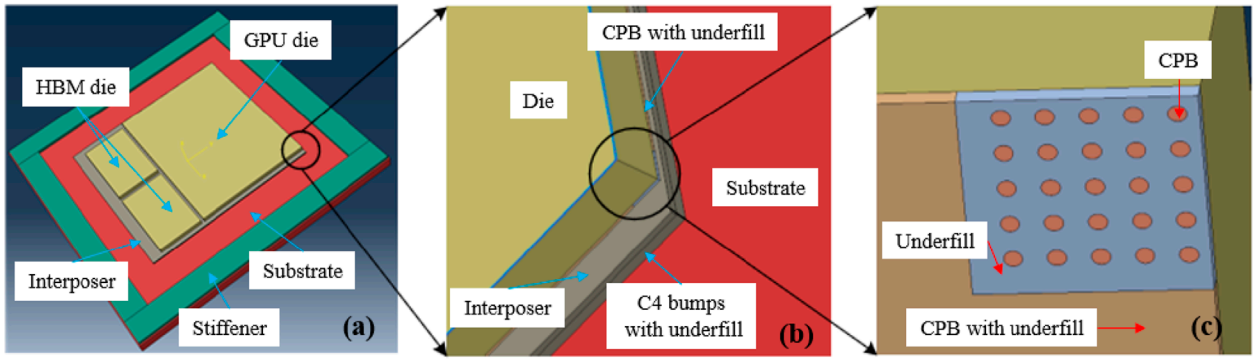


FIGURE 3
Simulation model of Vega56: **(A)** is overall view of the model; **(B)** shows the simplified model of interposer, C4 bumps with underfill and CPB with underfill; **(C)** shows the simplified model at corner of chip.

TABLE 2 Material parameters.

Material	E (Gpa)	ρ (g/cm^3)	α (1 × 10^{-6}/°C)	ν	C (W/(m×°C))
Cu	110	8.93	16.4	0.343	Table 3
Si	112.4	2.329	2.49	0.28	Table 3
Aluminum alloy	70.2	2.82	23.2	0.3	236.34
Substrate	18.75	2.44	10.2	0.12	16.5
Underfill	43.25	7.4	28.2	0.363	64.2
SAC305	54	7.38	40	0.363	50.3
Pb37Sn63	32.62	8.4	2.54	0.363	50
Interposers	E_Z:110.25 E_{xy}:110.529	2.395	$\alpha_{x,y}$:3.721 α_z:3.654	0.292	Table 3
C4 bumps with underfill	E_Z:40.05 E_{xy}:41.12	7.89	$\alpha_{x,y}$:2.52 α_z:2.51	0.363	$K_{eq,z}$:61.56 $K_{eq,xy}$:60.34
CPB with underfill	*Ez*:89.64 *Exy*:93.45	8.12	$\alpha_{x,y}$:4.89 α_z:4.57	3.592	$K_{eq,z}$:89.58 $K_{eq,xy}$:84.21

TABLE 3 Partial material thermal conductivity.

Material		C (W/(m·°C))			
		−55°C	0°C	25°C	165°C
Cu		431.8	401	398	389.9
Si		62.9	79.5	85.9	121.6
Interposers	$K_{eq,z}$	77.6	92.3	98.3	132.3
	$K_{eq,xy}$	53.8	67.3	72.6	101.8

substrate is connected to the computer motherboard through BGA solder balls. Its appearance is shown in Figure 2A, and its cross-section is shown in Figure 2B.

ABAQUS was used to conduct thermal simulation analysis of the model. The dimensions of each part of Vega56 are shown in Table 1. In light of the substantial quantity of CPBs, the construction of all individual CPBs would lead to exceedingly intricate models that demand considerable computational resources. In the thermal cycle, the dangerous solder joints of the chip are located at the center and corners, while the rest of the solder joints are relatively safe. Therefore, when constructing the model of CPBs in this paper, only the CPBs at the center of the chip and the four corners of the chip were constructed, and the rest was simplified using the equivalent model. In addition, the substrate, C4 bumps layer, and Si interposers were also simplified into rectangular shapes, resulting in the simulation model shown in Figure 3.

Based on the size and pitch of C4 bumps, CPBs, and TSVs, the volume ratio β could be calculated to be 20.532%, 15.514%, and 3.409%. Through (1)–(10), the material parameters of each structure

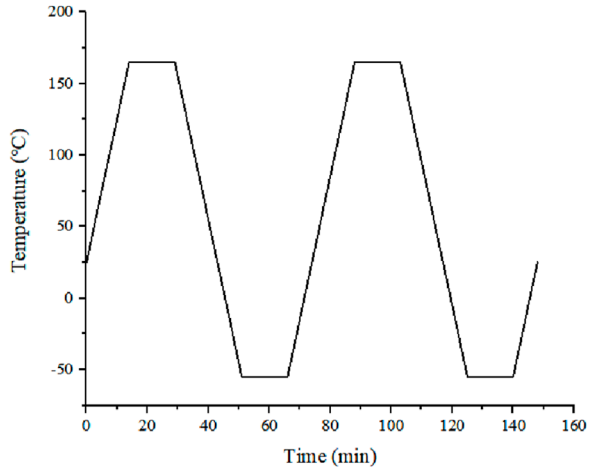


FIGURE 4
Thermal cycle curve.

in the model could be obtained, as shown in Table 2. The thermal conductivity of Cu, Si, and Interposers is temperature dependent, as shown in Table 3.

The simulation conditions for thermal cycling were −55°C~165°C, with a temperature change rate of 10°C/min, a temperature retention time of 15 min, and a cycle period of 74 min. In the thermal cycling simulation, the initial temperature was set to 25°C, with a cycle time of 2 h per cycle, culminating in a total duration of 148 min for the thermal cycling regimen. The thermal cycle profile is illustrated in Figure 4. During the static analysis segment, the boundary conditions were meticulously defined to incorporate fixed restraints at the vertices of the substrate's basal plane.

Eight-node hexahedral solid elements were used for meshing. During the transient thermal analysis, the DC3D8 unit was used, and during the static analysis the C3D8R unit was used. For thin-layer structures, the number of meshes in the z direction was controlled to two layers of meshes at least. The meshing results are shown in Figure 5.

The temperature field obtained from transient thermal simulation was put into static simulation as a predefined field to obtain the stress changes and warping deformation of the device under temperature cycling. The simulation results are shown in Figures 6A, B.

It could be seen that during the heating stage, the chip mainly experienced arching warpage, while during the cooling stage, concave warpage occurred. At the maximum temperature, the warpage was the largest, reaching 44.717 μm. At the minimum temperature, the maximum concave warpage value was −24.075 μm. Figure 6C shows the variation of the maximum warpage over time within a cycle, which was similar to the temperature change. From the GPU stress distribution, it could be seen that the maximum stress point was located at the corners, mainly due to the smaller thermal expansion coefficient of the silicon chip and the larger thermal expansion coefficient of the substrate. Therefore, the warpage stress on the GPU was mainly caused by the warping of the substrate.

2.3 Verification of simulation

Shadow moire interferometry (Zhu et al., 2018; Du et al., 2019; Yeh et al., 2019) is a non-contact optical technology for warpage full-field measurement. It uses interference between a reference grating and its shadow on the sample to measure the relative vertical displacement of each pixel position. This technology was used for experimental verification of the overall model in this paper.

The equipment used in this article is TherMoire AXP produced by akrometrix, as shown in Figure 7A. The sample was heated using infrared heating, and was fixed on a standard glass block with an ultra-low coefficient of thermal expansion (CTE). The bending radius of the standard glass is known, which can be used to calibrate the influence of the external environment during the experiment. A thermocouple was installed next to the sample to detect temperature changes in the sample. The experimental setup is shown in Figure 7B.

In order to maintain the device warpage in a steady state during experimentation, a heating rate of 10°C per minute was established, while the cooling rate was controlled to remain below −10°C per minute. The experimental setup included a maximum temperature of 165°C, with an ambient condition set at 25°C. Thermocouples were used to detect the surface temperature of the device in real time, and the temperature change curve was obtained as shown in Figure 8A.

During the experiment, the surface warpage of the sample was measured every 10 °C. Each measurement used the built-in three-step phase shift method of the equipment to obtain the surface warpage value. The experimental results are shown in Figure 8B.

The sample already had a warpage of 14 μm before heating, which perhaps caused by reflow soldering process. From Figure 8B, it could be seen that the initial warpage was arching warpage, that is, the center of the sample was higher than the four corners. As the temperature increases, the sample's arching warpage further intensified, and when the maximum temperature was reached, the warpage value increased to a maximum of 56 μm. As the temperature decreases, the warpage value gradually decreased and eventually returned to the initial warpage value.

The temperature change curve obtained from the experiment was input to the previous simulation model as a boundary condition, and the warpage of the device surface was obtained, as shown in Figure 8B. The simulation results were in good agreement with the relative warpage measured in the experiment. The error at the maximum warpage was 6.47%, and the maximum error does not exceed 20%, with an average error of 8.93%. This indicates that the simplified modeling and simulation methods used in this paper have sufficient accuracy.

3 Simulation of fatigue crack propagation of CPB

3.1 Boundary load curve extraction

In the process of model refinement, the specific CPB located in close proximity to the apex of stress concentration within the overall model was precisely delineated. Subsequently, a detailed submodel

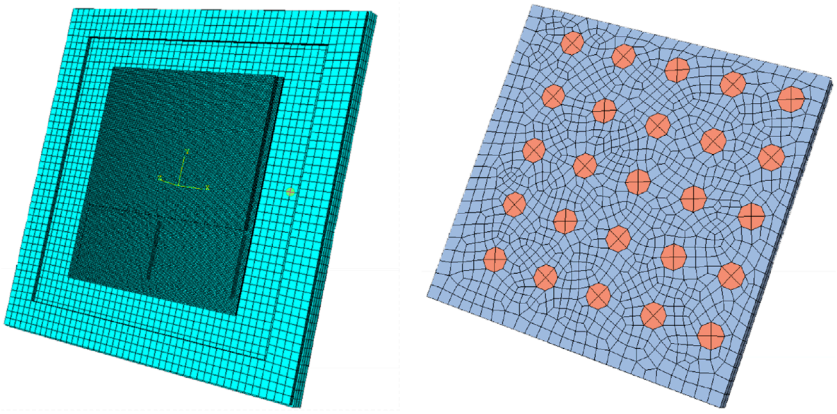


FIGURE 5
Meshing results of Vega56. **(A)** Overall model. **(B)** CPB.

encompassing this region of interest was extracted and delineated, as illustrated in Figure 9.

The solder layer material is SAC305, which is a viscoplastic material. Under thermal cycle conditions, plastic deformation and creep deformation mainly occur. The plastic constitutive model of SAC305 is shown in Equation 11.

$$\sigma = C_p \varepsilon_p^{n_p} \tag{11}$$

where ε_p is equivalent plastic strain, C_p and n_p are both time-dependent material parameters (Cheng et al., 2008), as show in Table 4.

The steady-state creep constitutive model is a hyperbolic sine creep constitutive model (Glane et al., 2023) as Equation 12.

$$\dot{\varepsilon} = C[\sinh(\alpha\sigma)]^n \exp\left(-\frac{Q}{kT}\right) \tag{12}$$

where Q is creep activation energy, T is temperature, n is stress exponent, k is Boltzmann constant, σ is applied stress, C and α are material constant, and $\dot{\varepsilon}$ is steady state creep strain rate. The relevant material parameters are shown in Table 4, and other material parameters are shown in Table 5.

Set the boundary conditions of the submodel as the displacement simulation results of the upper and lower surfaces. The boundary conditions for the submodel were established utilizing the displacement simulation outcomes obtained from the upper and lower surfaces. To achieve stable viscoplastic flow of the solder, the boundary conditions were cyclically loaded. The equivalent stress of the CPB was extracted for each cycle, with the stabilized equivalent stress serving as the boundary stress for subsequent analysis. Since the stress on the CPBs was mainly caused by the deformation of the dies, the external force was mainly on the upper and lower surfaces. The stress on the copper pillar was mainly in the *z*-axis direction, while the stress in the *x* and *y* directions was smaller. Consequently, in the simulation of fatigue crack propagation, the stress acting in the *x* and *y* directions was deemed negligible. The curve of the average principal stress on the outer surface of the copper pillar over time is shown in Figure 10.

3.2 Thermal fatigue crack propagation simulation

Under the influence of temperature, due to the expansion movement of atoms, two intermetallic compounds, Cu_6Sn_5 and Cu_3Sn, will gradually form between the solder and the copper pillar (Roy et al., 2022; Arafat et al., 2020). Generally speaking, the growth rate of Cu_6Sn_5 is greater than that of Cu_3Sn, so Cu_6Sn_5 is prone to forming undulating wave shapes, while Cu_3Sn generally forms relatively flat elongated shapes (An and Qin, 2016).

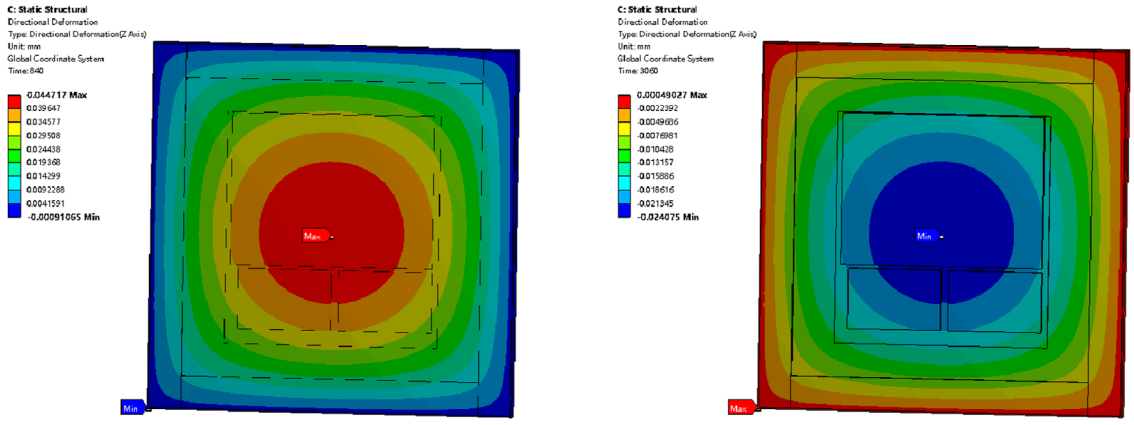
The IMC layer morphology characteristic parameters set in this paper are shown in Table 6. R_{rms} is the roughness of IMC layer, d_{ave} is the average thickness, λ_{ave} is the average distance between wave paeks.

Utilizing the MATLAB computational environment, a one-dimensional Gaussian random rough surface was meticulously modeled, with the explicit aim of synthesizing a stochastic rough surface profile that rigorously adhered to the specified parameters delineated within Table 6. Then, the rough surface data was imported into the CPB model, as shown in Figure 11A. During the crack propagation process, the CPE4R unit was used for simulation calculations. This unit can handle complex stress states and provide relatively high computational efficiency. The meshes are shown in Figure 11B.

According to the research in Li et al. (2020), there are two main ways of crack expansion in CPBs. Mode 1 is the crack propagation in SAC305, and Mode 2 is the crack propagation in Cu_6Sn_5, as shown in Figure 12.

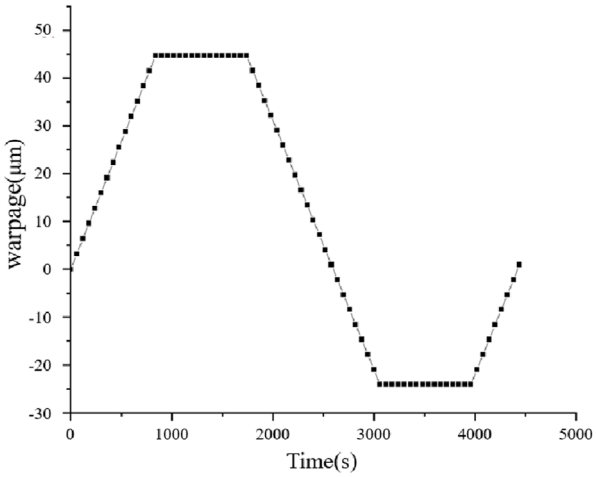
Two initial cracks with length a0 = 0.5 μm were constructed respectively. The first initial crack was located in SAC305 and was a horizontal crack used to simulate Mode 1. The second initial crack was set at the interface between SAC305 and Cu_6Sn_5, with an inclination angle of 60°, to simulate Mode 2. The constructed simulation models are shown in Figures 11C, D.

Crack propagation can be roughly divided into three stages: crack initiation stage, stable propagation stage, and unstable propagation stage. The crack propagation rate during the stable



(a) Warpage distribution at maximum temperature

(b) Warpage distribution at minimum temperature



(c) Variation of the maximum warpage over time

FIGURE 6
Warpage distribution and variation. **(A)** Warpage distribution at maximum temperature. **(B)** Warpage distribution at minimum temperature. **(C)** Variation of the maximum warpage over time.

propagation stage can be described using the Pairs formula (Rajaguru et al., 2019) as Equation 13.

$$\frac{da}{dN} = C(\Delta K)^m \tag{13}$$

where da/dN is the crack propagation rate; C and m are constants, which can be obtained by fitting experimental data; ΔK is the stress intensity factor amplitude.

The boundary load curve, as illustrated in Figure 10, was input into the model. The simulation of fatigue cracks was conducted through the direct cycle analysis step within the Abaqus software. Furthermore, the model parameters of the Paris formula was input, ensuring a comprehensive analysis of the fatigue crack propagation under the specified loading conditions. The parameters C and m in the Paris formula were obtained by fitting the experimental data in Tian et al. (2017), and the values of C and m are shown in Equation 14.

$$\begin{cases} \log C = -7.8 \\ n = 2.7 \end{cases} \tag{14}$$

The fatigue crack propagation results of Mode 1 and Mode 2 are shown in Figure 13. And the relationship curve between the crack length a and the number of cycle N in Mode 1 and Mode 2 were established, as shown in Figure 14. In the crack propagation of Mode 1, as depicted in Figure 13A, the crack initiates from an initial flaw and propagates in a direction parallel to the upper surface of the CPB solder layer. This propagation continues until the crack traverses the entire solder layer, which is in close agreement with the Mode 1 crack propagation path for CPB as shown in Figure 12A.

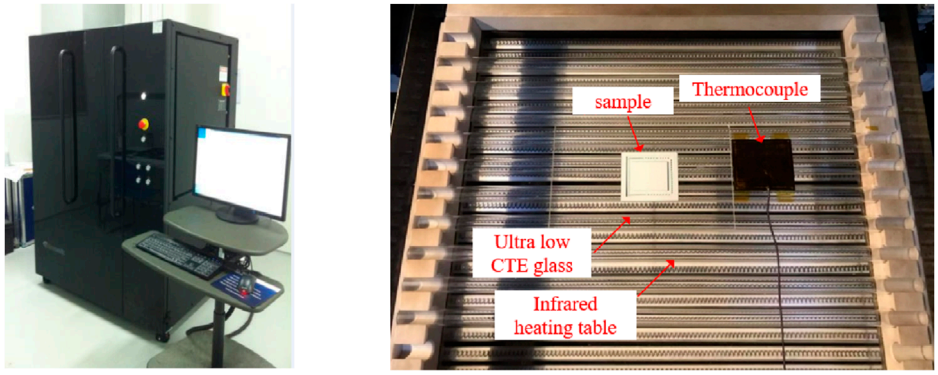


FIGURE 7
Equipment and experimental setup. **(A)** TherMoire AXP. **(B)** Shadow moire interferometer heating platform.

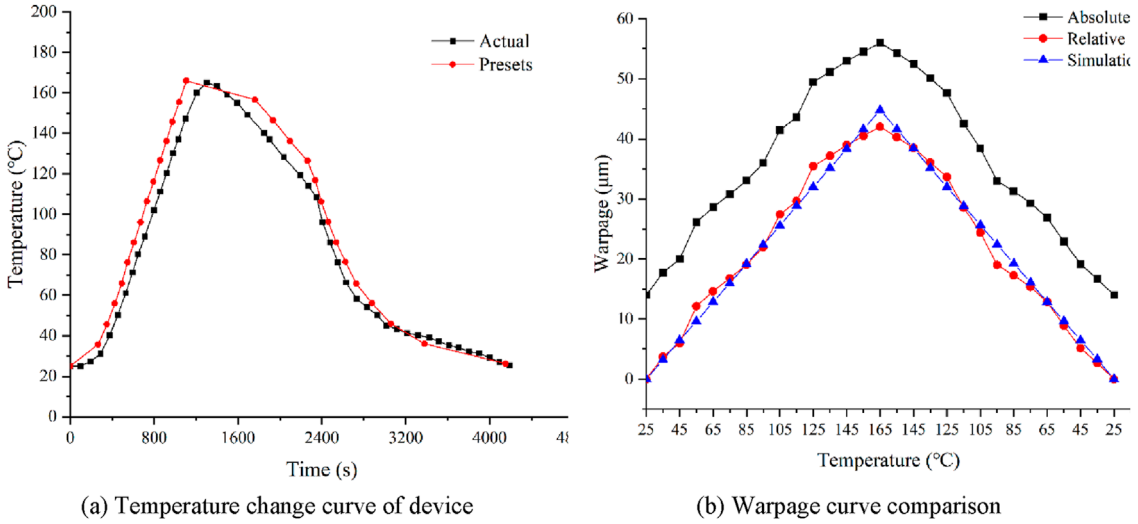


FIGURE 8
Temperature change curve and warpage curve comparison in the Verification experiment **(A)** Temperature change curve of device. **(B)** Warpage curve comparison.

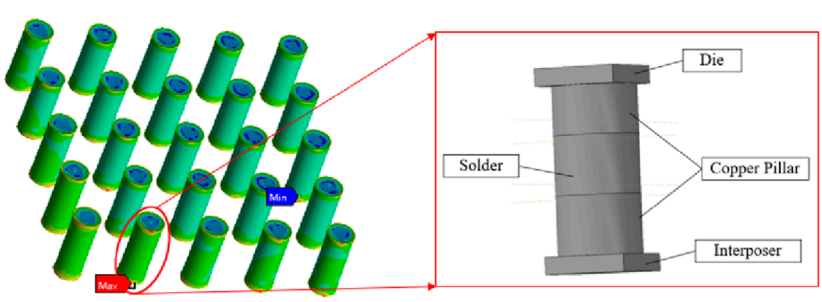


FIGURE 9
CPB submodel.

TABLE 4 Plastic and creep parameters of SAC305.

Material	Plastic parameters		Creep parameters			
SAC305	C_p	n_p	C	α	n	Q/k
	121.6–0.4 × T (°C)	0.29–0.00046 × T (°C)	441,000	0.005	4.2	5,412

TABLE 5 Other material parameters.

Material	P (g/cm^3)	E (Gpa)	ν	CTE (1 × 10^{-6}/°C)	C (W/(m×°C))
SAC305	7.38	54	0.363	28.2	50.3
Cu6Sn5	7.96	129.01	0.3	21.3	78.6
Cu3Sn	8.12	144.50	0.28	18.6	87.3

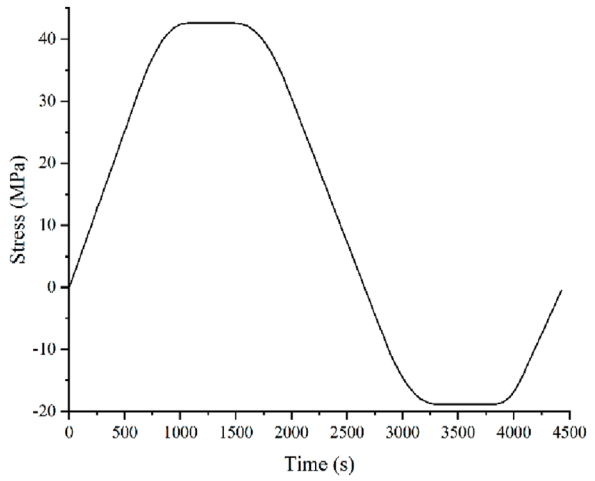


FIGURE 10
CPB boundary stress.

TABLE 6 Morphological characteristics of IMC layer.

Material	R_{rms} (Ra)	d_{ave} (μm)	λ_{ave} (μm)
Cu_6Sn_5	0.95	5.3	2.32
Cu_3Sn	0.53	1.97	4.56

This behavior is likely attributed to creep damage in the solder layer proximate to the upper copper pillar. In contrast, for Mode 2 crack propagation, as illustrated in Figure 13B, the initial crack is situated near the IMC layer within the solder. The crack then crosses the interface between the SAC305 solder and the IMC layer, entering the Cu_6Sn_5 phase and propagating parallel to the lower surface of the copper pillar. This propagation continues until the crack laterally spans the entire IMC layer, closely aligning with the Mode 2 crack propagation path depicted in Figure 12B. Moreover, the crack propagation rate for Mode 2 was observed to be faster than that for Mode 1.

3.3 Fatigue lifetime prediction

The fatigue crack propagation life is the number of cycles that a crack undergoes from the initial length a_0 to the critical length a_c. The critical length a_c is closely related to the stress intensity factor K at the crack tip and the fracture toughness K_C of the material. When $K \geq K_C$, the crack will experience unstable propagation and quickly reach the life limit of the structure (Wang et al., 2023; Alter et al., 2020). The unstable propagation of cracks can be determined by Equation 15, 16.

$$K_{\max} = f\sigma_{\max}\sqrt{\pi a_C} \leq K_C \tag{15}$$

$$a_C = \frac{1}{\pi}\left(\frac{K_C}{f\sigma_{max}}\right)^2 \tag{16}$$

where f is the geometric correction coefficient, and σ_{max} is the maximum value of applied stress.

In this paper, f is 1.121, σ_{max} is 43.13 MPa, and the fracture toughness of Cu_6Sn_5 is 0.481 MPa·m$^{1/2}$ (Ghosh, 2004). The critical length of Mode 2 could be determined to be 21.78 μm. From the a-N curve in Figure 14, it could be concluded that the fatigue lifetime of Mode 2 is 1,470 cycles. When the number of cycles in Mode 1 reached 1900, the crack almost penetrated the entire CPB, indicating a fatigue lifetime of 1900 cycles.

4 Discussion

From the lifetime prediction results of Mode 1 and Mode 2, it could be seen that when the crack propagated in the IMC layer, the fatigue lifetime of CPB was shorter than that of the crack located in the solder, and the difference between the two was significant $\delta=(N_1-N_2)/N_1 \times 100\% = 22.63\%$. This indicated that IMC had a significant influence on the fatigue lifetime of CPBs.

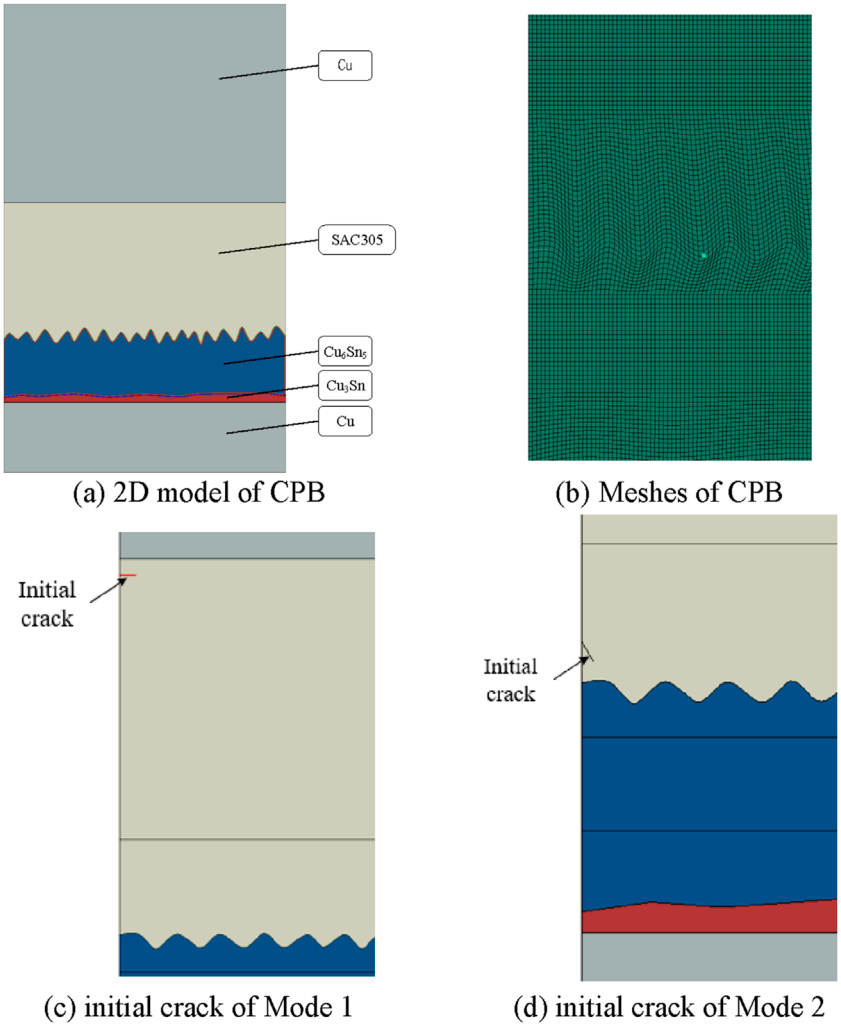


FIGURE 11
2D model and Meshes of CPB and initial crack simulation model. **(A)** 2D model of CPB **(B)** Meshes of CPB **(C)** initial crack of Mode 1**(D)** initial crack of Mode 2.

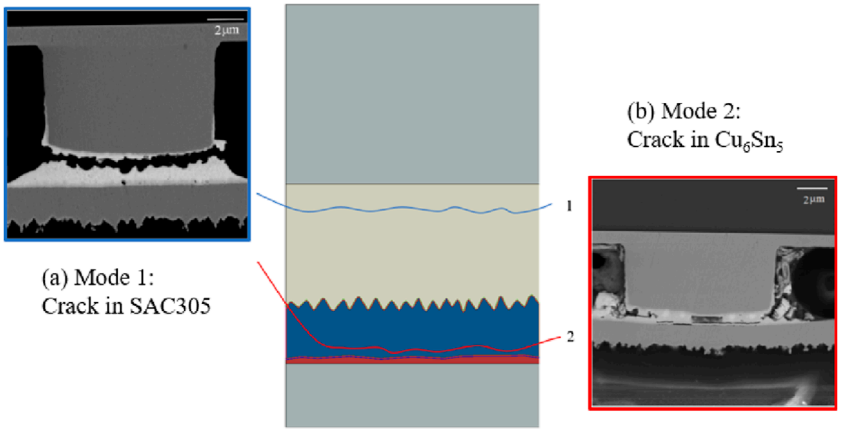


FIGURE 12
Schematic diagram of crack propagation: **(A)** Mode 1 crack is located in SAC305; **(B)** Mode 2 crack is located in Cu_6Sn_5 (Li et al., 2020).

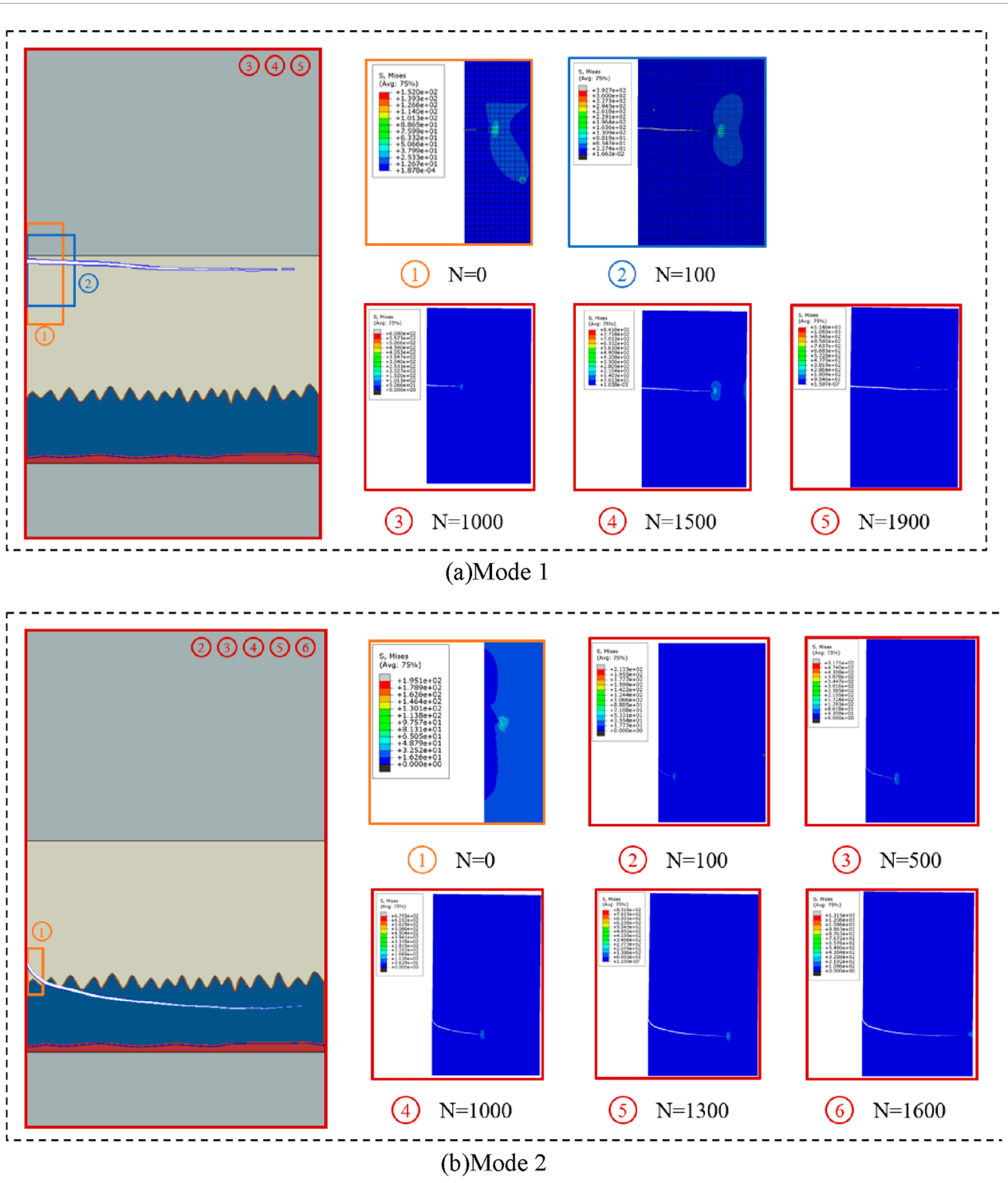


FIGURE 13
Fatigue crack propagation path of Mode 1 and Mode 2. **(A)** Mode 1. **(B)** Mode 2.

To investigate the effect of IMC layer thickness on the fatigue life of CPBs, this paper constructed simulation models with different IMC layer thicknesses. Due to the significant impact of the IMC layer, only the fatigue lifetime of Mode 2 was simulated. The a-N curves of CPBs with different IMC layer thicknesses are shown in Figure 15. And the fatigue lifetime prediction results of CPBs with different IMC layer thicknesses are shown in Table 7.

From Figure 15, it can be seen that as the thickness of the IMC layer increased, the shape of the a-N curve remained basically unchanged, but the rate of crack propagation increased rapidly. It can also be seen from the lifetime prediction results that as the IMC increased, the fatigue lifetime of CPB will decrease significantly. When all the solder layers were converted to IMC, its fatigue lifetime decreased from 1,470 cycles to 825 cycles, a decrease of 43.88%.

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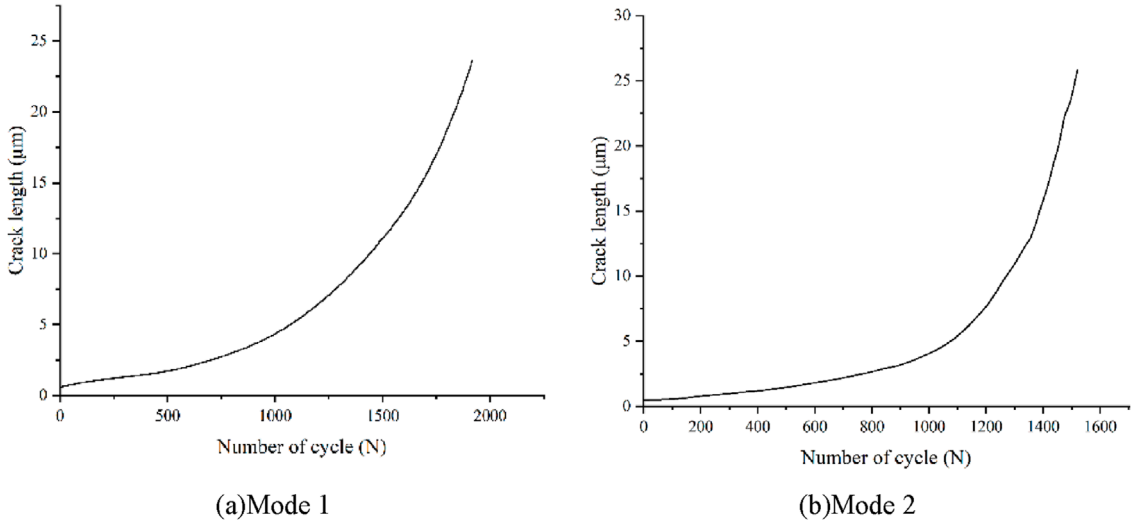

FIGURE 14
A–N curve of Mode 1 and Mode 2. **(A)** Mode 1. **(B)** Mode 2.

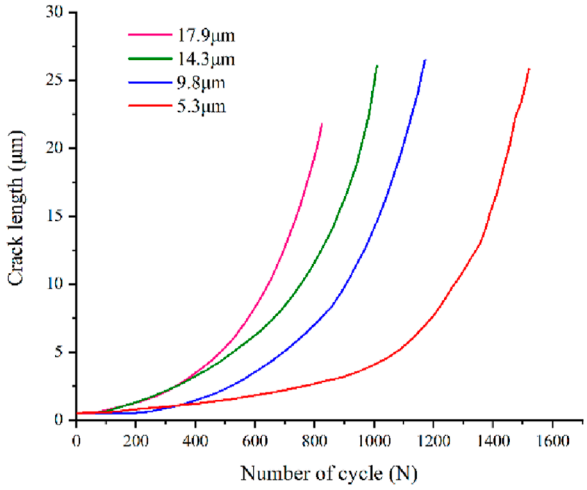

FIGURE 15
a-N curves of CPB with different IMC layer thicknesses.

TABLE 7 Fatigue lifetime of CPBs with different IMC layer thicknesses.

IMC layer thicknesses (μm)	5.3	9.8	14.3	17.9
Fatigue lifetime (cycle)	1,470	1,119	977	825

These results indicate that the existence of the IMC layer accelerates the fatigue crack propagation of CPB, which will seriously reduce the fatigue lifetime of CPB, and the thickness of the IMC layer is one of the key influencing factors. Therefore, in the preparation process of CPB, it is necessary to choose appropriate process parameters to ensure that the IMC layer is thin, and attention should also be paid to the growth of the IMC during service.

5 Conclusion

This paper takes the CPBs in 2.5D package as the research object, and establishes a method for obtaining the lifetime of CPBs based on the basic theory of fatigue crack propagation. Using the extended finite element simulation method, the fatigue lifetime of CPBs with different IMC layer thicknesses under thermal cycling was simulated, and the influence of IMC layer thickness on the fatigue lifetime of CPBs was analyzed. Through the simulation results of fatigue crack propagation at CPBs, it was found that when the crack propagated in IMC, the fatigue lifetime of CPB was smaller than the lifetime when the crack propagated in the solder layer. This indicates that the influence of IMC layer on the fatigue lifetime of CPB is significant. And as the thickness of the IMC layer increases, the fatigue lifetime of the CPBs also significantly decreases. When the thickness of the IMC layer reaches 100% of the solder layer height, the fatigue lifetime of CPB will decrease by 43.88%. Therefore, when predicting the lifetime of the CPBs, it is necessary to consider the impact of the IMC layer. In addition, there may be defects such as voids in the IMC layer of CPBs, which have a certain impact on predicting crack propagation lifetime. In future research, initial defects can be incorporated into simulations to establish more accurate lifetime prediction methods.

Data availability statement

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

Author contributions

YZ: Conceptualization, Investigation, Methodology, Writing–review and editing. QL: Data curation, Software,

Validation, Writing–original draft, Writing–review and editing. TM: Data curation, Formal Analysis, Validation, Writing–review and editing. SL: Data curation, Software, Writing–review and editing. XZ: Data curation, Software, Writing–review and editing.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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