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# Physical modeling of HZO-based ferroelectric field-effect transistors with a WO<sub>x</sub> channel

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The quasistatic and transient transfer characteristics of Hf<sub>0.57</sub>Zr<sub>0.43</sub>O<sub>2</sub> (HZO)based ferroelectric field-effect transistors (FeFETs) with a WO<sub>x</sub> channel are investigated using a 2-D time-dependent Ginzburg-Landau model as implemented in a state-of-the-art technology computer aided design tool. Starting from an existing FeFET configuration, the influence of different design parameters and geometries is analyzed before providing guidelines for nextgeneration devices with an increased "high  $(R_H)$  to low  $(R_I)$ " resistance ratio, i.e.,  $R_{\rm H}/R_{\rm I}$ . The suitability of FeFETs as solid-state synapses in memristive crossbar arrays depends on this parameter. Simulations predict that a 13 times larger  $R_H/R_I$  ratio can be achieved in a double-gate FeFET, as compared to a back-gated one with the same channel geometry and ferroelectric layer. The observed improvement can be attributed to the enhanced electrostatic control over the semiconducting channel thanks to the addition of a second gate. A similar effect is obtained by thinning either the HZO dielectric or the WO<sub>x</sub> channel. These findings could pave the way for FeFETs with enhanced synaptic-like properties that play a key role in future neuromorphic computing applications.

#### KEYWORDS

HZO, FeFET, TCAD, ferroelectric modeling, device simulation

# **1** Introduction

It has recently been shown that ferroelectric field-effect transistors (FeFETs) can function both as integrate-and-fire (IF) neurons (Mulaosmanovic et al., 2017; Chen et al., 2019) as well as solid-state synapses (Mulaosmanovic et al., 2018; Sun et al., 2018). They could thus build the core of brain-inspired spiking neural networks (SNNs) and other neuromorphic processors. For example, 5-bit analogue synaptic cores made of  $HfO_2$ -based FeFETs and utilized as on-line accelerators have been demonstrated to outperform competing hardware solutions relying on conventional resistive random access memories (RAMs) by a factor of  $10^3$  to  $10^6$  in terms of speed (Jerry et al., 2017). Moreover, similar to spin-transfer-torque magnetic RAMs, the switching mechanism of FeFETs is extremely energy-efficient as it does not involve any material or structural changes. The resulting conductance modulation, which corresponds to the weight updates

of artificial neural networks (Zhao et al., 2011; Apalkov et al., 2013; Mulaosmanovic et al., 2015; Ali et al., 2018; Sun et al., 2018), occurs through the polarization switching of ferroelectric domains or grains. Hence, FeFETs are characterized by an improved reliability, as compared to synaptic devices taking advantage of ion-migration processes or phase-change materials.

Despite these impressive achievements, FeFETs have not yet reached their full potential: design guidelines that could lead to enhanced figures-of-merit are still needed. Device simulation, in particular technology computer aided design (TCAD), lends itself naturally to the creation of such guidelines. Here, the Sentaurus-Device (S-Device) TCAD tool has been selected to optimize the performance of FeFETs (Synopsys, 2019). It features a recently developed physical model that captures the switching of ferroelectric layers (Mulaosmanovic et al., 2015). The objective of this work is therefore twofold: first shedding light on the functionality of FeFETs and then carefully adjusting their design parameters in order to improve their behavior as solid-state synapses. The focus is on transistors with a  $WO_x$  metal-oxide channel combined with a  $Hf_xZr_{1-x}O_2$  (HZO) ferroelectric dielectric layer. Note that in all simulations conventional semiconductor transport based on drift-diffusion phenomena is assumed to describe the conduction mechanisms occurring in the amorphous oxide channel.

To accurately model the peculiarities of HZO layers, a two-to three-dimensional Ginzburg-Landau-type numerical approach is necessary (Chandra and Littlewood, 2007). Important is that it offers the possibility to explicitly account for the presence of grains displaying different polarization switching properties (Noh et al., 2019). In S-Device, such a model has been incorporated into a classical drift-diffusion solver which is employed to describe the electron and hole transport characteristics of the WO<sub>x</sub> semiconducting channel and to compute the resulting electrical currents (Selberherr, 1984).

Before providing novel design guidelines, the simulation procedure was first calibrated with the help of an existing back-gated Hf<sub>0.57</sub>Zr<sub>0.43</sub>O<sub>2</sub>-based FeFET incorporating a WO<sub>x</sub> channel similar to the one presented in (Halter et al., 2020). After a careful adaptation of the simulation parameters, a satisfactory agreement between the calculated and measured transfer characteristics of the FeFET testbed could be obtained, using a relatively simple 2-D geometry. In particular, a hysteretic window with a width of about 2 V was extracted from the simulation, a value similar to the experimental one, but with a slightly different shape. The slope of the current with respect to the applied voltage, i.e.,  $dI_D/dV_{GS}$ , was found to be more flat in experiments, a phenomenon that can be attributed to the formation of a high density of ferroelectric grains inside the HZO. The characteristics of the considered FeFET have then been refined by accounting for the presence of multiple ferroelectric domains. As the number of domains increases in the HZO layer, the slope of the hysteresis loop decreases, provided that the standard deviation of the Landau

coefficients between different domain exhibits a large enough range.

Such a calibration of the available physical models is essential before moving to the exploration phase, the optimization of FeFETs for neuromorphic computing applications. To act as solid-state synapses, FeFETs should fulfill very specific requirements: it should be possible to modulate their resistance (or conductance) over a large dynamic range by applying positive and negative electrical pulses (potentiation and depression). A high number of intermediate states, ideally equal to or larger than 32, should be reachable between the minimum ( $R_L$ ) and maximum ( $R_H$ ) values of the resistance, which correspond to the low (LRS) and high resistance state (HRS) of the device, respectively. Finally, the response of FeFETs to potentiation and depression stimulations should be as symmetric and linear as possible (Gokmen and Vlasov, 2016).

Here, we concentrate on the  $R_H/R_L$  resistance ratio, which should be maximized, while also considering the number of achievable states in between. The impact of various design parameters on these quantities will be thoroughly investigated. It will be shown that the  $R_H/R_L$  ratio increases as the thickness of the ferroelectric HZO layer decreases. This behavior can be explained by the enhanced gate control over the channel as the thickness of the ferroelectric layer is reduced. The same happens when the WO<sub>x</sub> channel is made thinner. Other design parameters will be discussed as well, among them the gate length and the introduction of a second gate contact, which provides the largest improvement among all considered options.

The paper is organized as follows: in Section 2, the simulation approach is presented, followed by the model calibration and multi-domain characterization in Section 3. Section 4 is dedicated to the influence of the different design parameters on the behavior of FeFET before drawing conclusions in Section 5.

# 2 Simulation approach

As technology computer aided design (TCAD) tool, the Sentaurus-Device (S-Device) package from Synopsys is employed to describe the physical characteristics of the investigated FeFETs (Synopsys, 2019). The simulation of such devices requires a special treatment due to the presence of switchable polarization within their dielectric layer. To address this issue, an electrostatic model based on the time-dependent Ginzburg-Landau (TDGL) equations and dedicated to ferroelectric materials and devices was implemented in S-Device (Synopsys, 2019). The TDGL equations extend Poisson's equation, while the transport properties are still captured by the drift-diffusion solver of S-Device.

The starting point of the S-Device TDGL model is the freeenergy density of ferroelectric crystals, as proposed in (Starkov et al., 2013). This approach takes into account the electrostatic potential-polarization coupling and is therefore very suitable for device simulations, where a gate voltage modifies the polarization of an oxide layer. The original formalism was extended to treat non-uniform polarizations (Chandra and Littlewood, 2007). To include the influence of the semiconductor material into this thermodynamic description, a variational principle of Poisson's equation is employed. The electronic charge density is incorporated into an energy functional  $\Pi$ , which represents the total potential energy of the system. It has the following form:

$$\Pi = \int_{\Omega} \left( \alpha_i P_i^2 + \beta_i P_i^4 + \gamma_i P_i^6 + g_{ij} |\nabla_j P_i|^2 + \nabla_i \psi P_i - \frac{\varepsilon}{2} |\nabla \psi|^2 + \psi \rho_q \right) d\mathbf{r},$$
(1)

where  $\nabla_j P_i = \frac{\partial P_i}{\partial x_j}$ . In Eq. 1, the Einstein's summation convention is used. The first three terms correspond to the Landau energy density due to the polarization  $P_i$  along the cartesian coordinate *i*. They depend on the Landau coefficients  $\alpha_i$ ,  $\beta_i$ , and  $\gamma_i$ . The fourth term of the Ginzburg-Landau theory accounts for an additional energy cost caused by non-uniform polarizations and is proportional to  $g_{ij}$ , where  $j = \{x, y, z\}$ . The fifth term is the electrostatic potential-polarization coupling, while the last two terms represent the electrostatic field energy, including the semiconductor charge contribution  $\rho_q$ . Finally,  $\psi$  stands for the electrostatic potential, the main unknown quantity.

Considering the stationarity condition for the functional in Eq. 1, i.e.,  $\delta \Pi = 0$ , a set of partial differential equations (PDEs) can be derived (Zienkiewicz et al., 2005). Differentiating and integrating by parts Eq. 1 gives:

$$\begin{cases} -\varepsilon_0 \Delta \psi = -\nabla \mathbf{P} + \rho_q, \\ 2\alpha_i P_i + 4\beta_i P_i^3 + 6\gamma_i P_i^5 - 2g_{ij} \Delta P_i + \rho \frac{dP_i}{dt} = -\nabla_i \psi. \end{cases}$$
(2)

In Eq. 2, **P** is the polarization vector and  $\varepsilon_0$  the vacuum permittivity.  $\rho$  corresponds to polarization viscosity introduced to represent the dynamics during polarization switching. The system in Eq. 2 can be solved in a device domain by applying the following boundary conditions:

$$\psi = V_G \quad \text{on} \quad \Gamma_C;$$
 (3)

$$\left(-\varepsilon_0 \nabla \psi + \mathbf{P}\right) \cdot \mathbf{n}_{out} = 0 \quad \text{on} \quad \Gamma_{ext}, \tag{4}$$

where  $\Gamma_C$  delimits the contour of the gate contact(s) and  $\Gamma_{ext}$  refers to the rest of the exterior domain boundaries. The **n**<sub>out</sub> vector is orthogonal to the boundary domain and normalized.

Due to its mixed formulation and possible discontinuities of the polarization field at interfaces, the space discretization of the system in Eq. 2 presents several numerical challenges. Typically, strong oscillations of the polarization vector inside the ferroelectric layer are observed when implementing a "simple" finite-difference discretization scheme on a staggered grid.

To avoid such spurious oscillations that may lead to divergences of the numerical solution, a stabilized discretization scheme is necessary. In S-Device, a



FIGURE 1

Epitaxial structure of the HZO-based, back-gated FeFET which serves as a calibration reference for this work (Halter et al., 2020). The ferroelectric HZO gate dielectric, the WO<sub>x</sub> channel, the source (S), the drain (D), and the gate (G) regions are indicated. The thickness of all layers and the channel length are given in nanometers and micrometers, respectively. Note that only 2-D structure is used during simulations.

discontinuous Galerkin finite element method is applied because of the stability it provides when dealing with problems of a similar form as Eq. 2 (Cockburn et al., 2002). The application of the Galerkin method requires rewriting Eq. 2 in a conservative form. This can be done by introducing an auxiliary flux corresponding to the displacement vector  $\mathbf{D} = -\varepsilon_0 \nabla \psi + \mathbf{P}$ . Gauss's law of electrostatics can then be enforced element-by-element in a conservative way, with properly formulated numerical fluxes that ensure the stability of the method.

The Landau coefficients  $\alpha_i$ ,  $\beta_i$ , and  $\gamma_i$  are inputs to the solver. They can either be extracted from capacitor measurements or computed from density-functional theory (DFT) (Sholl and Steckel, 2011). The same applies to the polarization gradient coefficient  $g_{ij}$ . The coupling to the electronic transport comes from the charge density  $\rho_q$ , which, in S-Device, is calculated at the drift-diffusion (DD) level. All equations derived from the expression one are solved self-consistently with the DD ones.

### 3 Results and discussion

#### 3.1 Model calibration

As starting point, the back-gated ferroelectric Hf<sub>0.57</sub>Zr<sub>0.43</sub>O<sub>2</sub> (HZO) field-effect transistor (FeFET) with a tungsten metaloxide (WO<sub>x</sub>) channel similar to (Halter et al., 2020) is examined. Its epitaxial structure is displayed in Figure 1. The channel width (along the z-axis) and length (along the x-axis) of the considered device are equal to 2  $\mu$ m and 0.8  $\mu$ m, respectively. The measurements of the FeFET in Figure 2 serve as a reference to calibrate all material parameters of the two-dimensional (2-D)



FIGURE 2

Experimental (solid blue line) and simulation (dash-dotted red line) DC characteristics for the FeFET in Figure 1 with an 8 nm-thick  $WO_x$  channel (Halter et al., 2020). (A) "Drain current  $I_D$  vs. gate voltage  $V_{GS}$ " hysteresis at  $V_{DS} = 0.2$  V; (B) "Polarization vs. gate voltage" data; (C) "Polarization vs. electric field" characteristics of the ferroelectric HZO layer. Only simulation results are available for this quantity.

TABLE 1 Principle S-Device material parameters for the considered HZO ferroelectric layer.

Parameter name in S-device	Description	Value
alpha1 (cm/F)	Landau's coefficient (x component)	1.3e12
alpha2 (cm/F)	Landau's coefficient (y component)	-9.889e10
beta1 (cm <sup>5</sup> /FC <sup>2</sup> )	Landau's coefficient (x component)	0
beta2 (cm <sup>5</sup> /FC <sup>2</sup> )	Landau's coefficient (y component)	2.007e20
gamma1, gamma2 (cm <sup>9</sup> /FC <sup>4</sup> )	Landau's coefficient (x, y component)	0
g1, g2, g6 (cm <sup>3</sup> /FC <sup>2</sup> )	Coupling coefficient for the polarization gradient	5e-7
epsilon	Relative permittivity	33
rho (Ohm cm)	Polarization viscosity	2.25e4

TCAD physical model of S-Device (Synopsys, 2019). Once this is done, only the geometry and shape will be modified in Section 4 to enhance the synaptic-like characteristics of the FeFETs. Note that due to the planar structure of the considered transistor, 3-D simulations were not necessary to capture the physics at play. No additional contact resistance was included in our simulations. High contact resistances are expected to impact the quasistatic and transient characteristics of FeFETs. However, for transistors with relatively long channel like the ones considered in this study, the contribution of the contact resistance to the whole device resistance is relatively moderate ( < 20%) (Halter et al., 2022).

The ferroelectric model relies on several material parameters, in particular the Landau coefficients  $\alpha_i$ ,  $\beta_i$ , and  $\gamma_i$ . The default parameters that are available in the S-Device library have been utilized as initial values. They have then been slightly adjusted to best match capacitance measurements. Consequently, the sole uncertainty in the calibration of the FeFET simulation model resides in the material parameters for WO<sub>x</sub>. To obtain them, we used the experimental WO<sub>x</sub> data presented in (Migas et al., 2010; Halter et al., 2020) and the values proposed in (Fountaine, 2015) for WO<sub>3</sub>. The most relevant material parameters for HZO and TABLE 2 Same as in Table 1, but for the WO<sub>x</sub> channel.

Parameter name in S-device	Description	Value
Eg0 (eV)	Bandgap	0.75
Epsilon	Relative permittivity	300
Chi0 (eV)	Electron affinity	4.5
mumax (cm <sup>2</sup> /Vs)	Electron mobility	0.016
mm	Effective mass for electrons	0.8
Nc300 (cm <sup>-3</sup> )	Conduction band density of states	1.8e19
Nv300 (cm <sup>-3</sup> )	Valence band density of states	7.1e19

WO<sub>x</sub> that were employed in our simulations are shown in Tables 1, 2. Note that since 2-D simulations are carried out in this study, all coefficients along the z-axis of the HZO layer are defined to be zero. The Landau coefficients  $\alpha_i$ ,  $\beta_i$ , and  $\gamma_i$  in the first five rows of Table 1 determine the polarization component  $P_i$  along the axis  $i = \{x, y, z\}$ , in case of anisotropic dielectric layer. Similarly, the  $g_{ij}$  coefficients refer to the polarization gradient factor that

influences the spatial derivative of  $P_i$  (Eq. 1). The polarization is assumed to be anisotropic to restrict the switchable component to the y-axis, which is the direction orthogonal to the gate of the transistor, whose structure is schematized in Figure 1. This feature is realized by defining positive  $\alpha_i$  values along the two other directions, i.e., the x- and z-axis. Generally, the polarization gradient coefficients  $g_{ij}$  is a symmetric 3 × 3 tensor, which has six independent components. It can therefore be expressed in a sixcomponent vector notation:  $g_1 = g_{11}, g_2 = g_{22}, g_3 = g_{33}, g_4 = g_{23} =$  $g_{32}, g_5 = g_{13} = g_{31}$ , and  $g_6 = g_{12} = g_{21}$  (Synopsys, 2019). Regarding the relative permittivity of WO<sub>x</sub>, a value higher ( $\varepsilon_{WO_x} = 300$ ) than the experimentally measured one ( $\varepsilon_{WO_x}$  = 189) had to be used to improve the quality of the fit. This discrepancy could possibly be attributed to the gate voltage-driven migration of oxygen vacancies from the HZO to the WO<sub>x</sub> layer. This mechanism has been experimentally shown to alter the resistive switching characteristics of FeFETs (Halter et al., 2022). It might also be at the origin of higher doping concentrations, modified dielectric properties, and/or reduced mobility. Moreover, the electron mobility was adjusted to best reproduce the experimental hysteretic curves, with a final value  $\mu_e = 0.016 \text{ cm}^2/\text{Vs}$ . Experimentally, it was determined to be about 0.19 cm<sup>2</sup>/Vs. This difference at least partially originates from the omission of parasitic capacitances in our simulations.

The simulated and experimental characteristics of the 2-D FeFET structure are shown in Figure 2. In sub-plot (A), the experimental " $I_D$  vs.  $V_{GS}$ " hysteretic loop is presented. The measured curve was shifted along the positive V<sub>GS</sub> direction by 1 V, as compared to the simulation data, to compensate for the accumulation of trapped charges, an effect that is not accounted for in our model (Muller et al., 2016). Apart from this rigid shift that must be applied, a good agreement between the calibrated TCAD results and the measured data can be observed. The simulated hysteretic window is about 2 V wide, similar to the experimental one. The flatter  $dI_D/dV_{GS}$  slope of the experimental measurement can be attributed to the formation of a high density of ferroelectric domains inside the HZO layer, as will be discussed in Section 3.2. In addition, the simulated and experimental "polarization vs. gate voltage (P vs.  $V_{GS}$ )" characteristics of the ferroelectric HZO layer agree very well, as shown in sub-plot (B). In sub-plot (C), the "polarization vs. electric field" behavior of the HZO layer, as computed with the TCAD model, is presented. No experimental data is available for this quantity.

#### 3.2 Multi-domain characterization

Based on this initial calibration, the agreement between the simulated and measured characteristics of the selected FeFET have been further improved by accounting for the presence of multiple ferroelectric domains. As the number of domains increases in the HZO layer, the  $dI_D/dV_{GS}$  slope of the switching hysteresis and the value of the ferroelectric

coercive field ( $E_C$ ) change, as compared to the single-domain case that has been so far assumed. When the required electric field and time for the polarization to switch are different in each ferroelectric domain, the slope of the electrical current  $I_D$  with respect to the gate voltage  $V_{GS}$  becomes more gradual, for both branches of the hysteresis. This indicates that polarization switching takes place in a sequential manner across all grains (Noh et al., 2019).

To include this effect, the ferroelectric HZO layer in the modeled FeFET structure was divided into  $N_D$  domains with equal size  $L_D$  along the x-axis. These domains join the source and drain contacts possess varying Landau's coefficients  $\alpha_{2n}$  along the y-axis, since  $\alpha_{2n}$  is closely related to the remnant polarization  $P_r$  and the coercive field  $E_C$  of the concerned domain, according to Eqs 1, 2. Here, the subscript of the Landau coefficient *n* corresponds to the index of the ferroelectric domain along y, n = 1 being the first one on the source side, and  $n = N_D$  the last one close to the drain contact. The  $\alpha_{2n}$  values were randomly chosen according to a Gaussian distribution function with a mean value  $\mu_{\alpha 2} = -9.889 \times 10^{10}$  cm/F and standard deviations  $\sigma_{\alpha 2}$  varying between 0 and 9.889  $\times 10^{10}$  cm/F.

The simulated " $I_D$  vs.  $V_{GS}$ " characteristics of four different HZO domain configurations ( $N_D$  and  $L_D$ ) are plotted in Figures 3A–D, together with the experimental reference. Note that the product  $N_D \times L_D$  remains the same in all cases, 0.8  $\mu$ m, which is equal to the total length of the WO<sub>x</sub> channel. It can be clearly observed that the slope of the hysteresis loop decreases when increasing  $\sigma_{\alpha 2}$ . Among all tested configurations, the one with  $N_D = 40$ ,  $L_D = 20$  nm, and  $\sigma_{\alpha 2} = -0.3\mu_{\alpha 2}$  in Figure 3C gives the best agreement with the measurement. Moreover, the simulation with  $N_D = 80$ ,  $L_D = 10$  nm, and  $\sigma_{\alpha 2} = -0.3\mu_{\alpha 2}$  leads to a similar result, but with slightly larger discrepancy. Since the domain size is generally smaller than the grain size (Hyun et al., 2018), this finding aligns well with the experimental observation of a mean grain size in HZO of 26.8 nm, as reported in (Lombardo et al., 2021).

Next, we focused on the transient response of the  $WO_x$ -based FeFET to a train of positive and negative electrical pulses applied to its source and drain contacts, while the gate is grounded. Desired is a gradual, multi-state modulation of the device resistance as a function of the number of applied pulses. As a first numerical analysis, the influence of  $N_D$  on the number of resistance states was investigated at a constant standard deviation value of  $\sigma_{\alpha 2} = -0.3 \mu_{\alpha 2}$ . Results are shown in Figure 4. The amplitude of the electrical pulses first increases from 0 to 4 V in step of 0.1 V before decreasing from 0 to -4 V with a step size of -0.1 V. As a consequence, the resistance first increases (depression) and then decreases (potentiation). The duration of the writing pulses is set to 10 µs, as in experiments (Halter et al., 2020). As expected, the number of available resistance states increases as more ferroelectric domains  $N_D$  are considered. The maximum number of resistance states (15) is reached with  $N_D$  = 40 and 80, which corresponds to domain sizes of 20 and



#### FIGURE 3

Experimental (solid line with crosses) and simulated " $I_D$  vs.  $V_{GS}$ " transfer characteristics of the FeFET in Figure 1 with an 8 nm-thick WO<sub>x</sub> channel (Halter et al., 2020), different number of HZO domains ( $N_D$ ), and varying standard deviations of the Landau coefficients ( $\sigma_{a2}$ ) at a source-to-drain voltage  $V_{DS}$  = 0.2 V (**A**)  $N_D$  = 12,  $L_D$  = 67 nm; (**B**)  $N_D$  = 20,  $L_D$  = 40 nm; (**C**)  $N_D$  = 40,  $L_D$  = 20 nm; (**D**)  $N_D$  = 80,  $L_D$  = 10 nm.



10 nm, respectively, the length of the channel still being equal to 0.8  $\mu {\rm m}.$ 

Continuing our analysis, the potentiation and depression behavior of the WO<sub>x</sub>-based FeFET is investigated for  $L_D = 10$  and

20 nm with varying  $\sigma_{\alpha 2}$ . Here, the same electrical pulse sequence as in the measurements is used (Halter et al., 2020). Their amplitude increases first from 1.3 to 2.7 V for depression and then decreases from -1.5 to -2.5 V for potentiation, with a step



Simulated and experimental depression and potentiation response of the  $WO_x$ -based FeFET of Figure 1 as a function of the number of electrical pulses at different standard deviations  $\sigma_{a2}$  for (A)  $N_D = 40$ ,  $L_D = 20$  nm; (B)  $N_D = 80$ ,  $L_D = 10$  nm domain configurations. The writing pulse train increases from 1.3 to 2.7 V for depression and then decreases from -1.5 to -2.5 V for potentiation, with a step size of  $\pm 0.1$  V. The experimental  $R_H$  and  $R_L$  values are both indicated. They correspond to the resistance at the beginning of the pulse sequence ( $R_L$ ) and at the end of the depression part ( $R_H$ ).

size of  $\pm 0.1$  V and a pulse duration of 10  $\mu$ s. The simulated results are summarized and compared to experiments in Figure 5. For  $\sigma_{\alpha 2} \leq -0.5 \,\mu_{\alpha 2}$ , the difference in  $R_H/R_L$  obtained at the two  $N_D$ considered here comes from the fact that the ferroelectric domains are not fully switched due to the relatively limited voltage swing of the applied pulses (from 1.3 to 2.7 V for depression and from -1.5 to -2.5 V for potentiation). The best agreement is obtained when  $N_D = 40$ ,  $L_D = 20$  nm, and  $\sigma_{\alpha 2} = -\mu_{\alpha 2}$ . These results can then be used to extract the  $R_H/R_L$ resistance ratio, where  $R_H$  ( $R_L$ ) refers to the largest (smallest) resistance occurring in the depression/potentiation curve in Figure 5. This ratio is found to be 1.6. It should be noticed that the best match between the measured and simulated depression and potentiation characteristics is obtained for a larger standard deviation  $\sigma_{\alpha 2}$  than in the optimal DC case in Figure 3C. In Figure 3C,  $\sigma_{\alpha 2} = \mu_{\alpha 2}$  produces a good agreement with the experimental " $I_D$  vs.  $V_{GS}$ " curve. This discrepancy could possibly be attributed to the fact that for durations longer than 3 µs, the energy of each pulse is potentially large enough to enable oxygen migration between the HZO and WO<sub>x</sub> layers, which increases the  $R_H/R_L$  resistance ratio as compared to the case where only polarization switching occurs (Halter et al., 2022). As the migration of oxygen atoms cannot be described by the current TCAD model, the discrepancy between the quasistatic and transient results corresponds to the difference between the calibrated standard deviations of Landau's coefficients. In addition, larger R<sub>H</sub>/R<sub>L</sub> are expected for pulse durations longer than 10 µs, as confirmed experimentally (Halter et al., 2022). Note that the orientation of the polarization is restricted to the y-axis in this study although the switching characteristics of the investigated devices closely relies on this parameter and its

variation across the multiple ferroelectric domains. This partly explains the differences between simulations and experiments.

# 4 Prospective performance enhancements

Starting from the calibrated simulation results of Section 3, the influence of various design parameters has been studied to enhance the FeFET performance. More specifically, our theoretical investigations aim at designing novel FeFET structures with improved  $R_H/R_L$  resistance ratios, i.e., with larger dynamic ranges, as compared to the device configuration reported in (Halter et al., 2020). The higher the  $R_H/R_L$  ratio, the more efficient is the training of a crossbar array incorporating such devices. If possible, the number of available resistance states between  $R_L$  and  $R_H$  should also be maximized. All channel resistances are extracted at  $V_{DS} = 0.2$  V by applying a DC IV-sweep from -200 to 200 mV at the drain contact, while keeping the source and the gate grounded, as in experiments (Halter et al., 2020). For simplicity, all subsequent simulations were carried out utilizing FeFETs with a single-domain HZO layer, as the number of ferroelectric domains is not expected to significantly affect the resistance ratio of the device, as can be seen in Figure 4.

Because pulse-response simulations are computationally relatively intensive, the resistance ratios of the modified device designs were estimated as a first approximation by scaling the  $R_H/R_L$  results in Figure 5 with the following factor:  $(I_{ON}/I_{OFF})_{new}/(I_{ON}/I_{OFF})_{orig.}$ . This factor can be extracted from the DC "current vs. voltage" transfer characteristics at



#### FIGURE 6

(A)  $R_H/R_L$  resistance ratio as a function of the channel thickness  $T_{CH}$ , estimated from the hysteretic FeFET characteristics at  $V_{DS} = 0.2$  V. (B) Corresponding  $I_{ON}$  and  $I_{OFF}$  as a function of  $T_{CH}$ , extracted from the DC transfer characteristics at 4 V and -4 V, respectively. (C) Surface potential  $\psi_S$  along the WO<sub>x</sub> channel at  $V_G = -4$  V and  $V_{DS} = 0.2$  V. The beginning of the source contact is situated at x = 0, the gate starts at x = 0.6  $\mu$ m and goes till x = 1.4  $\mu$ m.

 $V_{DS} = 0.2 \text{ V}$ ,  $I_{ON}$  ( $I_{OFF}$ ) being the current at 4 V (-4 V). Hence, ( $I_{ON}/I_{OFF}$ )<sub>new</sub> represents the simulated ratio between the ONand OFF-state currents of the updated design, while ( $I_{ON}/I_{OFF}$ )<sub>orig.</sub> is the same quantity for the original FeFET, as simulated in Figures 2, 3. As the  $R_H/R_L$  ratio coming from depression/potentiation measurements is expected to depend on the DC  $I_{ON}/I_{OFF}$  ratio, we believe that our simplified approach is sufficient to indicate which parameters have a positive or negative impact on the FeFET operation.

## 4.1 Impact of design parameters

#### 4.1.1 Channel thickness

As a first design parameter, the impact of the channel thickness,  $T_{CH}$ , was analyzed taking advantage of the calibrated model. The simulation results are displayed in Figure 6. It can be observed in sub-plot (A) that by decreasing  $T_{CH}$  from 8 to 4 nm, the  $R_H/R_L$  ratio, as estimated with the method outlined above, doubles. This finding has been confirmed experimentally, where an improvement by a factor 2 is obtained by halving the channel thickness of the FeFET (Halter et al., 2022). These results are not only encouraging, they also validate our approach, where only the DC FeFET characteristics are computed to approximate the  $R_H/R_L$  ratio. For  $T_{CH}$  thicker than 10 nm, the estimated  $R_H/R_L$  ratio drops to unity due to the relatively low energy barrier between the source and drain regions, which leads to a decreased  $I_{ON}/I_{OFF}$ .

It can be seen in subplot (B) and that the increase in  $R_H/R_L$ can be mainly attributed to a rapid decrease of  $I_{OFF}$  as  $T_{CH}$  is reduced before saturating. The ON-state current also diminishes, but at a slower rate. This behavior is a consequence of the fact that transistors with a thinner channel exhibit a better electrostatics control than thicker ones, thus allowing for a more efficient switching off of the device. Further reducing  $T_{CH}$  below 4 nm does not bring additional enhancement anymore because  $I_{OFF}$  remains almost constant. At this size,



 $I_{OFF}$  is limited by the electron carrier concentration of the channel, which is equal to  $1.01 \times 10^{20}$  cm<sup>-3</sup> in our case (Si et al., 2019). Moreover, the surface potential at the source/ channel interface is already negative at  $T_{CH} = 4$  nm, as can be seem in Figure 6C. It thus forms a potential barrier at the source-gate interface so that further reductions of  $T_{CH}$  have little impact on  $I_{OFF}$ . In conclusion, an enhanced  $R_H/R_L$  ratio can be achieved by carefully adjusting  $T_{CH}$ .

#### 4.1.2 HZO thickness

The transfer characteristics of the FeFET device have also been evaluated for different HZO layer thicknesses,  $T_{FE}$ . As shown in Figure 7, the  $R_H/R_L$  ratio increases as  $T_{FE}$  decreases. The underlying physical mechanism is similar to the one discussed in Section 4.1.1, i.e., the gate control over the channel becomes stronger as the ferroelectric layer thickness is reduced because the gate capacitance augments. The impact of  $T_{FE}$  is stronger on  $I_{ON}$  than on  $I_{OFF}$ , which leads to the observed positive effect on  $R_H/R_L$ . According to our simulations, if  $T_{FE}$  is reduced down to 5 nm, a further increase of  $R_H/R_L$  could theoretically be envisioned, but two major issues might



TABLE 3 Geometrical parameters of the double-gate FeFET transistor in Figure 8.

Parameter	Description	Value
$T_{FE}$ (nm)	Gate dielectric thickness (HZO)	10
$T_{CH}$ (nm)	Channel thickness (WO <sub>x</sub> )	8
$L_{CH}$ ( $\mu$ m)	Channel length	0.8
$L_{S/D}$ (µm)	Source/drain contact length	0.6

prevent such a positive outcome. First, thin HZO layers are known not to switch as efficiently as thicker ones (Vitale et al., 2010). Secondly, an ultra-scaled dielectric layer tends to be leaky and to induce large gate leakage currents. Note also that the benefit of thinning the HZO layer is less important than a reduction of the semiconductor channel thickness. It is therefore not the preferred option.

# 4.1.3 Gate length, channel width, and source/ drain extensions

Contrary to the two previous parameters,  $T_{CH}$  and  $T_{FE}$ , which directly affect the depression and potentiation behavior of WO<sub>x</sub>based FeFETs, the lateral dimensions of the structure, the gate length  $L_G$ , and the source/drain extensions  $L_{S/D}$ , have little influence on the  $R_H/R_L$  ratio. The ON- and OFF-state currents scale proportionally to "1/ $L_{CH}$ ", so that their impact on the  $R_H/R_L$  ratio cancels each other (KO, 1989). On the other hand, it has been observed that the length of the source/drain contact extensions,  $L_{S/D}$ , has a negligible influence on the simulated  $R_H/R_L$  ratios of the FeFETs.



#### 4.2 Double-gate architecture

Based on our simulation results as well as on experimental evidence, regardless of the device dimensions and channel doping concentrations (not shown here), it clearly appears that the originally proposed back-gated (BG) FeFET structure with a WO<sub>x</sub> channel cannot deliver  $R_H/R_L$  resistance ratios larger than ~4. As a consequence, to improve the performance, a different transistor design is required. Here, we propose a symmetric, double-gate (DG), WO<sub>x</sub>-based FeFET with a planar structure, as schematized in Figure 8. Its geometrical parameters are summarized in Table 3. Its dimensions are similar to those of the original BG FeFET, but with two instead of one gate contact and a length of the HZO ferroelectric layer that does not exceed that of the gates. In other words, the source and drain extensions are not covered by HZO.

The transfer characteristics of the proposed FeFET design are reported in Figure 9 and compared to those of the original backgated FeFET of Figure 1. With the same dimensions in both transistor configurations, the introduction of a second gate significantly improves the electrostatic control, which helps suppress the OFF-state current, while slightly improving the ON-state current by a factor of 1.6, as compared to the original structure. Hence, the DG device with an 8 nm WO<sub>x</sub> channel and a 10 nm HZO layer could theoretically deliver a 13 times higher  $R_H/R_L$  resistance ratio than the original one with a single back gate, i.e., 20.8 instead of 1.6. This improvement is expected to be accompanied by a significant increase of the number of intermediate resistance states between  $R_L$  and  $R_H$ . Obviously, reducing the  $WO_x$  channel thickness could further enhance the  $R_H/R_L$  ratio, but not as much as in the back-gated FeFET because the electrostatic control is already close to optimal with a double-gate architecture and  $T_{CH} = 8$  nm.

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# 5 Conclusion

The transfer characteristics of HZO-based FeFETs were simulated utilizing a 2-D, time-depedent Ginzburg-Landau ferroelectric model, as implemented in the S-Device TCAD tool. Starting from an existing back-gated FeFET with a WO<sub>x</sub> channel, good qualitative and quantitative agreements between the simulated and experimental DC performance were obtained after careful calibration. The influence of different design parameters (channel and ferroelectric layer thickness, gate length) and device geometries (double-gate architecture) on the  $R_H/R_L$  resistance ratio of these transistors were investigated. This ratio is a relevant figure-of-merit for neuromorphic computing applications because it is closely related to the dynamic range of the depression and potentiation characteristics and to the number of available resistance states that can be accessed by sending electrical pulses to the FeFETs. The  $R_H/R_L$  ratio should be as large as possible to enhance the learning capabilities of artificial neural networks based on memristive FeFET crossbar arrays. In terms of parameter screening, a channel thickness of 4 nm seems to be optimal, regardless of the device geometry. It should be combined with a ferroelectric layer as thin as possible, while maintaining good polarization switching properties and low leakage currents.

However, to avoid large surface-to-volume ratios and minimize the impact of surface roughness, as typically encountered in ultra-thin channels, a double-gate FeFET appears as a more promising approach. It provides the best electrostatic control over the WO<sub>x</sub> channel, and is predicted to provide a 13 times larger  $R_H/R_L$  ratio than that of the original back-gated transistor with similar geometrical parameters. From a fabrication point of view, a double-gate structure might be more challenging than a reduction of the channel or ferroelectric layer thickness, but the benefit is far greater. Hence, the HZO-based FeFET technology might be a viable alternative to phase change materials, valence change memories, or electro-chemical cells as solid-state synapses in future neuromorphic computing circuits.

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## Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

### Author contributions

XW and ML led the project. XW carried out the simulations. MH and LB-L designed and performed the experiments. XW and ML wrote and edited the paper. All authors contributed to the article and approved the submitted version.

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# Conflict of interest

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