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Editorial: Emerging memories, circuits, and systems for post-Moore computing applications in nanotechnology

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Editorial on the Research Topic
Emerging memories, circuits, and systems for post-Moore computing applications in nanotechnology

Continuing the advances in nanoelectronics in scaling while fulfilling the demand of high computing such as artificial intelligence (AI), machine learning (ML), Internet of Things (IoT), and hybrid systems, reducing the power consumption, and boosting the performance has become critical in the semiconductor community. The traditional Moore's law scaling technology, traditionally used in materials, devices, and systems, may no longer guarantee the computational demand of the conventional von Neumann architecture. It has become crucial for the electronics and systems era to subvert the bottleneck in current CPU architecture, i.e., von Neumann architecture. To tackle the new computing paradigms which subvert the memory wall in the von Neumann bottleneck, the new computing configurations, e.g., neuromorphic computing, edge computing, and in-memory computing, are attracting a considerable amount of attention. In this era, non-volatile memory technology using emerging new materials and device physics for the implementation of neuromorphic systems and data-centric computing are promising ways to achieve the goals and requirements of next-generation energy-efficient high-performance computing applications. Emerging memory can be categorized by switching mechanisms in materials and device physics, such as ferroelectric random-access memory (FeRAM), resistive random-access memory (RRAM), phase-change memory (PCM), and magnetic random-access memory (MRAM), which show great promise for next-generation storage and computational applications. Meanwhile, dynamic switch devices are considered candidates for new computational applications, such as ferroelectric field-effect transistors (FeFET), tunneling FET (TFET), and negative capacitance FET (NCFET) selectors, especially in high-density crossbar memory array applications.

The published articles in this Research Topic include four original research articles. The research paper by Liu et al. summarizes the advances in spintronic in-memory computing systems implementing the magnetic tunnel junction (MTJ) devices in trusted neural networks at a modest energy budget. The second research article in the Research Topic is by Kang et al. in which $CuO_x/HfO_x/WO_x$ (electro-chemical random-access memory)

ECRAM arrays are fabricated and the linear and symmetrical weight update capabilities in both fully parallel and sequential update operations are presented. The research by Wilson et al. describes the characterization of pre-formed resistive random-access memories to design physical unclonable functions and experimentally validate inherent properties such as tamper sensitivity and a self-destroy mode. The experimental results show that at least 91% of the cells can generate keys protected by the scheme, while 22% of the sensing elements are triggered. This Research Topic reports the developments in device- and system-level research towards emerging computational configurations, energy-efficient devices, and memory-based hardware security applications. The final research article by Hendy et al. describes a new design utilizing the delay of memristor RC circuits to represent synaptic computations and a simple binary neuron activation function. Synchronization schemes are proposed for communicating information between neural network layers, and a simple linear power model is developed to estimate the design's energy efficiency for a particular network size. We sincerely hope that the research in this Research Topic has the fundamentals that will inspire future experimental explorations in the post-Moore and next-generation computing era.

Author contributions

Y-CC led this journal collection and writing the editorial. Y-FC and AA organized the review process and editorial tasks. All authors contributed to the article and approved the submitted version.

Conflict of interest

Author Y-FC was employed by the company Intel Corporation.

The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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