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Nanotechnology-enabled energy efficiency in semiconductors: plasmon-induced super-semiconductors and ballistic transport devices

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The semiconductor industry consumes staggering amounts of electricity annually, surpassing the energy usage of over 100 nations. This immense consumption not only underscores the environmental impact but also generates substantial heat within semiconductor devices, adversely affecting their performance, lifespan, and reliability, posing significant challenges to the advancement of nanodevices. To address these challenges, reducing energy consumption through the use of advanced, energy-efficient technologies has become a priority. Energy-efficient electronics (EEE), enabled by nanotechnology, have the potential to drastically reduce energy consumption in semiconductor devices while simultaneously enhancing their performance. From this perspective, this discussion focuses on two nano-semiconductor technologies poised to advance EEEs: plasmon-induced metal-based semiconductors and ballistic transport in nanostructured semiconductors. For example, p-n junction diodes constructed with the metal-based semiconductors can reduce power consumption by 3-4 orders of magnitude compared with silicon-based devices due to their low resistivity; similarly, the excellent ballistic transport property of InSe FETs enables an energy-delay product of $\sim 4.32 \times 10^{-29}$ Js/ μm of the devices, one order of magnitude lower than the Si counterparts. This perspective examines the offerings of each of these disciplines and explores how nanotechnology can be utilized to conserve energy and enhance performance. Differences from traditional technologies and limitations in existing research will also be assessed.

KEYWORDS

nanotechnology, nanomaterials, energy efficiency electronics, plasmon resonance, ballistic transport

1 Introduction

With the rapid growth of tech companies in recent years, particularly driven by advancements in artificial intelligence (AI), global electricity demand has surged. In just 2023, companies like Google and Microsoft consumed an astonishing 24 TWh of electricity, surpassing the annual energy usage of over 100 countries, including Iceland, Ghana, and Tunisia (Shilov, 2024). In the future, as more tech companies fully integrate AI, electricity consumption is expected to rise significantly, underscoring the need for energy-efficient electronics (EEE). Moreover, over 50% of electricity is lost as heat dissipation in electronics, a problem that worsens as the power consumption of semiconductor devices continues to

rise. Excessive heat can cause significant issues, severely impacting device performance, including response speed and operating frequency, as well as compromising reliability, such as device lifespan and failure rates. Advances in nanotechnology-enabled energy-efficient solutions offer a promising path forward by significantly reducing energy usage while enhancing the performance and reliability of semiconductor devices.

2 Principles of energy loss in semiconductors

Semiconductor devices, from amplifier circuits to the chips in cell phones and computers, play a crucial role in every aspect of our lives. At their core, these devices are built from diodes and transistors. To fundamentally reduce power consumption and enhance energy efficiency, it is essential to focus on improving the performance and energy efficiency of these fundamental components. Several factors influence the power consumption of diodes and transistors, including operating voltage, resistance (Behabtu et al., 2013), switching frequency, mobility, temperature, and more. Among these, resistance and mobility are the most critical for energy efficiency. Joule heating, caused by the flow of current in solid conductive materials, is primarily a result of resistance. Lower resistance leads to reduced heat loss, as observed in superconducting materials, which exhibit negligible heat dissipation.

In solid materials, resistance is inversely proportional to mobility at a constant carrier density. Enhancing mobility reduces the collision rate between carriers and atoms, thereby decreasing resistance and minimizing heat loss. Moreover, higher mobility improves the response speed of semiconductor devices, further optimizing their performance.

3 Plasmon-induced metal-based semiconductors

Nanomaterials, with their unique size and structure, exhibit properties not found in bulk materials. Examples include localized surface plasmon resonance (LSPR) in metal nanostructures and ballistic transport in semiconductor nanodevices. These novel characteristics have had profound impacts on the development of EEE. As early as 1968, optical excitation of surface plasmon resonance (SPR) by the method of attenuated total reflection was demonstrated by Kretschmann and Raether (1968), Otto (1968). Based on its unique performance, SPR has been widely used in biosensors (Yang et al., 2021), cancer therapy, drug delivery, photocatalysis (Spata and Carter, 2018; Liu et al., 2021), and photodetection (Kunwar et al., 2020). Along with the development of nanotechnologies, a subarea of SPR research, localized surface plasmon resonance (LSPR), has garnered considerable attention. LSPR is dependent on the size, shape, and composition of the nanoparticles and nanostructures, as well as other external factors (Kang et al., 2019; Hang et al., 2024).

LSPR is a phenomenon that occurs when light interacts with metal nanostructures. When light shines on these nanoparticles, a strong resonance is generated if the light's frequency matches the natural oscillation frequency of the electrons. This resonance leads to

the formation of hot electron-hole pairs as photon energy is absorbed through metallic plasmon resonances (Brongersma et al., 2015). Due to their high energy, the mobility and velocity of hot electrons are far above those of free electrons. When the hot electron-hole pairs dominate the transport properties of the metallic nanostructures, semiconducting properties will be observed.

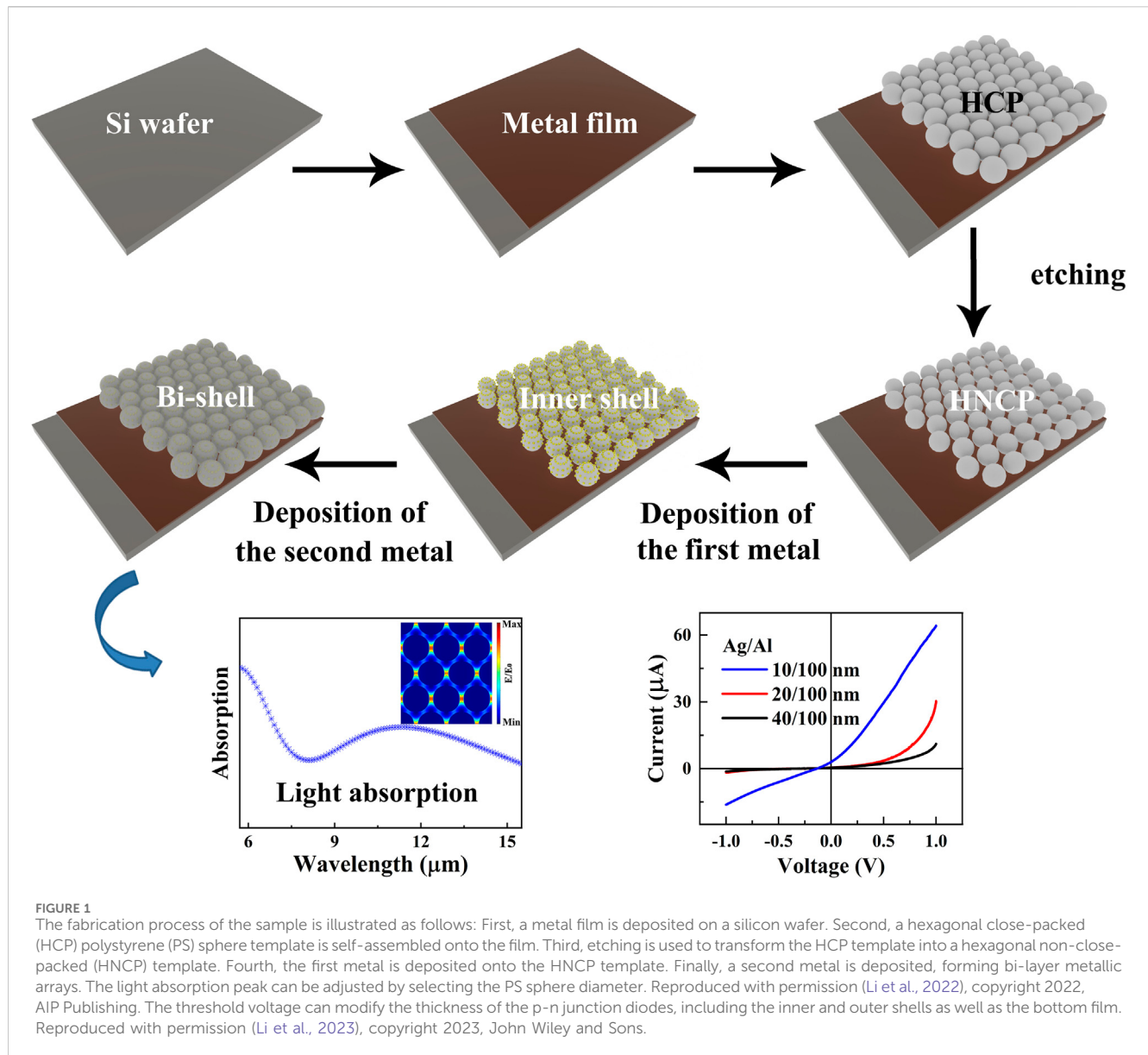
Recently, Li et al. designed an innovative immiscible bi-metallic shell array (Li et al., 2022) and applied LSPR to construct semiconductor devices, i.e., p-n diodes (Li et al., 2023). The inner shell consists of discrete metal nanoparticles responsible for metallic plasmonic resonance, while the outer shell is a continuous metal film that facilitates carrier transport, as illustrated in Figure 1. Notably, the light absorption peaks resulting from LSPR are highly dependent on the size and morphology of the metal nanoparticles (Kang et al., 2019). The inner shell structure, featuring metal nanoparticles of a specific diameter, can fine-tune these absorption peaks, such as those around 10–11 μm , allowing infrared light at ambient temperature to trigger a metal-semiconductor transition without the need for additional energy sources.

Thanks to the bi-metallic-shell nanostructure, typical semiconductor behaviors, such as p-type conduction and p-n junction diode characteristics, can be observed when hot carriers dominate current transport. The mobility of hot carriers is approximately 20–40 times higher than that of free electrons. This material with such an exciting phenomenon is referred to as a super-semiconductor (SSC), distinguishing it from traditional semiconductors due to its ultra-low resistivity ($\sim 10^{-8} \Omega \text{ m}$ at 300 K, which is 3–10 orders of magnitude lower than that of conventional semiconductors at room temperature) while exhibiting typical semiconductor properties within metals. The bandgap of SSCs is approximately equal to the photon energy (Li et al., 2022), which endows ultra-low-power semiconductor devices.

4 The ballistic transport properties in nanostructured semiconductors

At room temperature, the mean free path of a carrier in devices is approximately 10–20 nm. If the size of a nanodevice is significantly smaller than the mean free path, the scattering probability within the channel becomes negligible. This phenomenon, known as ballistic transport, allows the device current to be entirely controlled by carrier injection from the source into the channel. The limited scattering events during carrier transport substantially reduce heat loss in ballistic transport.

At room temperature, semiconductor carriers frequently scatter with lattice vibrations (phonons) on nanometer and femtosecond scales. This scattering causes electronic energy dissipation, known as Joule heating, and a loss of phase coherence and directionality, imposing significant limitations on the speed and energy efficiency of semiconductor devices. It is noted that the scattering probability is significantly affected by the device size (d) and the mean free path (λ). If d is much larger than λ , diffusive transport dominates, and the current can be well described by conventional mobility theory (Figure 2a). In contrast, when d is much smaller than λ , scattering within the channel becomes negligible. This regime corresponds to ballistic transport, where the device current is governed by carrier injection from the source into the channel (Figure 2b). When d is comparable to λ , the transport behavior falls into the quasi-ballistic regime (Figure 2c).



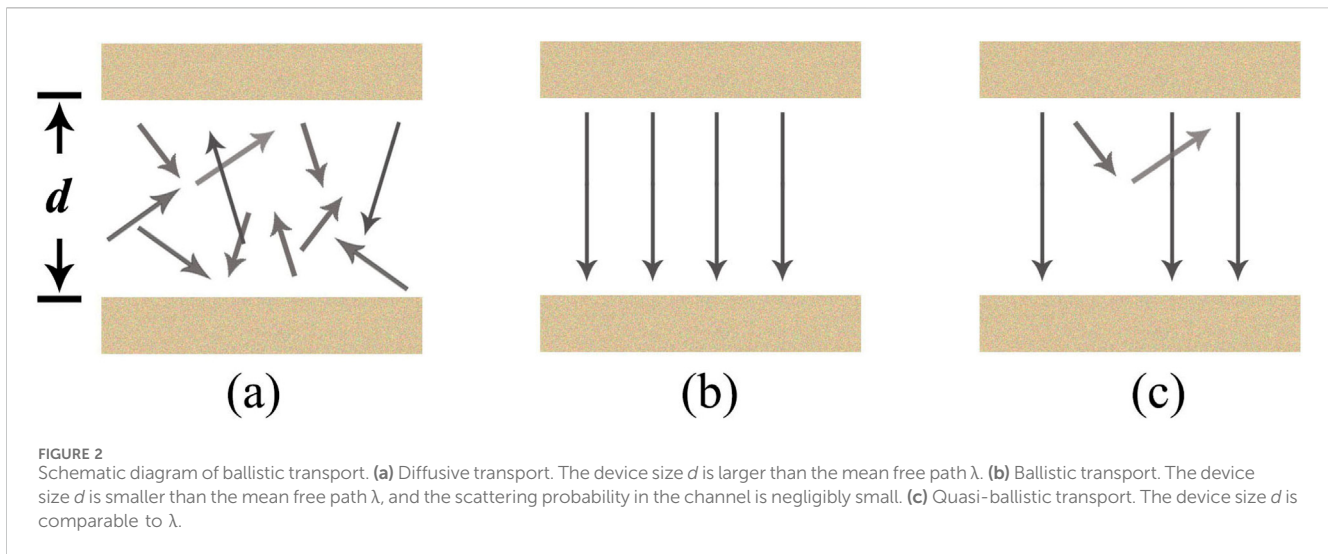
Early studies of ballistic transport focused on GaAs materials, which exhibit high mobility at low temperatures (Ruch, 1972; Maloney and Frey, 1977). Recently, with the rise of nanotechnology and two-dimensional materials (Du et al., 2008), transistors featuring room-temperature ballistic transport have garnered significant attention. Ballistic transport in nanostructured devices can significantly reduce thermal losses and enhance energy efficiency, making it a key strategy for improving energy efficiency and environmental sustainability.

5 Comparative analysis

5.1 Plasmon-induced metal-based semiconductors

SSC materials have been explored to construct p-n junction diodes (Ag/Al arrays) with a tunable threshold voltage by simply adjusting the

thickness of the inner Ag film. Notably, a near-zero threshold voltage can be achieved with an Ag film approximately 20 nm thick, enabling ultra-low-power p-n junction diodes, resulting in power dissipation of ~3 W per trillion diodes at a working voltage of 1 V or ~30 mW per trillion diodes at an operating voltage of 0.1 V (Li et al., 2023), better than that of superconducting diodes, achieved in a superconducting film (MoGe) patterned with a conformal array of nanoscale holes which typical power dissipation is ~100 W per trillion diodes at working voltage of 1 mV at 5.75 K (Lyu et al., 2021). Nevertheless, the power dissipation of a diode is of the same order of magnitude as that of a transistor made from the same material. The power consumption of silicon-based transistors is approximately 100 W per 10 billion devices. Therefore, SSCs can reduce power consumption by about three to four orders of magnitude in silicon-based devices, owing to the ultra-low resistivity and high mobility of hot carriers. This ultra-low power consumption fundamentally minimizes the heat dissipation of semiconductor devices, significantly improving their energy efficiency, device performance, and reliability.



Additionally, a built-in electric field in the SSC p-n junction is generated by infrared photons, resulting in a high breakdown field of $\sim 1.1 \times 10^6$ V/cm, comparable to wide-bandgap materials like SiC (2.5×10^6 V/cm) and GaN (2.9×10^6 V/cm) and significantly higher than Si-based materials (3.0×10^5 V/cm). The high breakdown electric field combined with the tuned threshold voltage of the SSC p-n diodes highlights the potential for ultra-low-power semiconducting transistors, integrated circuits, and chips.

5.2 Ballistic transport in nanodevices

Semiconductors can sustain ballistic wave-like energy flows over macroscopic distances at room temperature, enabling ballistic transistors, low-loss energy harvesting, and wave-based information technology. Using $\text{Re}_6\text{Se}_8\text{Cl}_2$, a van der Waals (vdW) 2-dimensional (2D) nanostructured superatomic semiconductor, Tulyagankhodjaev et al. demonstrated the formation of acoustic exciton-polarons, an electronic quasiparticle shielded from phonon scattering. They directly imaged polaron transport in $\text{Re}_6\text{Se}_8\text{Cl}_2$ at room temperature, revealing quasi-ballistic, wave-like propagation sustained for a nanosecond and several micrometers using ultrafast stroboscopic scattering microscopy (Tulyagankhodjaev et al., 2023). An above-gap, diffraction-limited visible pump generates excitons, and then a backscattering widefield probe (1.55 eV) slightly below the electronic bandgap spatially resolves how the excitons modify the local polarizability of the material. Shielded polaron transport leads to electronic energy propagation lengths orders of magnitude greater than in other vdW semiconductors, exceeding even silicon over a nanosecond.

Recently, Jiang et al. reported a field-effect transistor (FET) with 2D indium selenide (InSe) with high thermal velocity as channel material that operates at 0.5 V and achieves record high transconductance of $6 \text{ mS } \mu\text{m}^{-1}$ and a room-temperature ballistic ratio in the saturation region of 83%, surpassing those of any reported silicon FETs (Jiang et al., 2023). A yttrium-doping-induced phase-transition method is developed for creating ohmic contacts with InSe, and the InSe FET is scaled down to a channel length of 10 nm. The InSe FETs can effectively suppress short-

channel effects, featuring a low subthreshold swing of 75 mV per decade and a drain-induced barrier lowering of 22 mV/V. Furthermore, a low contact resistance of $62 \Omega \mu\text{m}$ is reliably extracted in 10-nm ballistic InSe FETs, resulting in a significantly reduced intrinsic delay and a substantially lower energy-delay product compared to the predicted limit of silicon. Moreover, the 10-nm-gate-length InSe FETs exhibit an energy-delay product of $\sim 4.32 \times 10^{-29}$ Js/ μm , one order of magnitude lower than the Si FET limit. The ballistic nanostructured semiconductor transistors could herald an era of essentially lossless nanoelectronics.

6 Challenges and future outlook

It should be noted that the fabrication process for bi-metallic shell arrays, as shown in the schematics in Figure 1, is straightforward and compatible with semiconductor technologies. Therefore, the scalability and reproducibility of the fabrication process are not technically challenging, as evidenced by the ability to control the size and distance of polystyrene sphere templates, as well as the deposition of different bi-metallic pairs (Li et al., 2022; Li et al., 2023). However, it is challenging to obtain defect-free polystyrene sphere templates at the wafer scale, including domain boundaries, voids, size polydispersity, and stacking faults. Uniformity issues can be improved by applying spin coating, substrate tilt for gradient-free assembly, and the Langmuir-Blodgett technique (Xia Y. et al., 2000; Jiang and McFarland, 2004; Kuncicky and Velev, 2008).

Furthermore, SSC devices can be fabricated on immiscible metal films using metal plasmonic resonance materials of various shapes, such as metallic quantum dots (Qi et al., 2023), nanoparticles (Scholl et al., 2012), and nanostructured arrays (Li et al., 2022), when a specialized laser tuned to the plasmon resonance absorption peak is applied. If an SSC device is triggered by infrared light at ambient temperature, the environmental temperature plays a crucial role because the wavelength of infrared light is dependent on temperature. This technology can also be utilized in optoelectronic detectors. Extended to semiconductor chip fabrication, compared with Si-based materials, it can reduce

power consumption by approximately 3–4 orders of magnitude due to the ultra-low resistivity and high mobility of hot carriers. Moreover, the hot carriers in SSC devices are influenced by nanostructure or particle size and light illumination rather than voltage, as in traditional semiconductor devices. This unique optical control capability introduces additional flexibility, paving the way for future multifunctional and ultra-low power nanodevice designs.

The ballistic transport property is particularly well-suited for nanodevices with dimensions less than 20 nm in thickness. However, the ballistic transport is sensitive to the monocrystal structure; the existence of defects or impurities will destroy the periodic structure, increase scattering, and reduce the efficiency of ballistic transport in FETs. By minimizing the elastic scattering of carriers, ballistic transport not only significantly reduces thermal losses caused by scattering but also enhances the overall performance of the devices.

In addition, both SSCs and ballistic transport devices are dependent on nanotechnology; in the long term, their stability will be influenced by various factors, including environmental temperature, current heating, oxidation, and atomic diffusion. For example, the SSC arrays are fabricated on polystyrene spheres, and the work temperature is limited to 70 °C. Above 50°C, its stability will be severely affected. However, it remains very stable at room temperature, and its rectification performance shows little to no degradation when stored for a year in a dry, room-temperature environment. Furthermore, the reliability of SSC devices at high temperatures will be significantly improved when high-temperature-resistant metal quantum dots are used for preparation.

7 Conclusion

Nanomaterials and nanotechnology will play a crucial role in the development of future energy-efficient electronics. Newly developed nanostructures, such as SSC and quasi/ballistic transport (scattering-free) features in semiconductor devices, drastically reduce energy consumption. Additionally, the high-mobility hot carriers in SSC and the reduced scattering in ballistic transport further enhance device performance. However, these technological advances have led to differences from traditional preparation processes, as well as variations in some intrinsic mechanisms. Similar to the SSC p–n junction, two types of carriers (hot and normal carriers) coexist, resulting in a built-in field and rectification effect that is considerably different from that of traditional semiconductor p–n junctions. The various mechanisms will increase the difficulty of preparing complex SSC semiconductor devices, as they are typically designed based on classical semiconductor theory. It is believed that with the continuous

advancement of research into new technologies, the unique nanoscale properties will offer significant advantages for developing EEE, providing performance enhancements and significantly alleviating the current energy consumption dilemma.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding authors.

Author contributions

ZL: Writing – original draft. BW: Conceptualization, Writing – review and editing.

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Conflict of interest

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