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EDITED BY
Syed Arshad Hussain,
Tripura University, India

REVIEWED BY
Ziang Chen,
Friedrich Schiller University Jena, Germany
Sherin Thomas,
Indian Institute of Technology Ropar, India
Sarappadi Narasimha Prasad,
Manipal Institute of Technology Bengaluru, India

*CORRESPONDENCE
Sachin Maheshwari,
maheshwari.sachin@ed.ac.uk

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Low-voltage programming of RRAM-based crossbar arrays using MOS parasitic diodes

Sachin Maheshwari*, Alex Serb and Themis Prodromakis

Centre for Electronics Frontiers, Institute for Integrated Micro Nano Systems, School of Engineering, University of Edinburgh, Edinburgh, United Kingdom

Due to their high density, scalability, and low-power properties, 1-transistor-1-resistor (1T1R) RRAM-based crossbars have been exploited in the past. However, the series resistance of the transistor is a major problem in 1T1R crossbar arrays. This limits the maximum current available for inducing resistive switching and degrades the array's performance. To mitigate this issue, we propose a new configuration—1-transistor-1-diode-1-resistor (1T1D1R)—in which diodes are used (including bulk source/drain parasitic diodes of the access transistor) to bypass the gating transistor during the programming operation ("write"). The proposed solution trades increased overhead in the layout area for a dramatic increase in the maximum achievable current drive on RRAM devices, resulting in the ability to deliver 1.5 mA+ with a voltage supply as low as 1.2 V using minimum-size devices (in our implementation). We designed a 32 × 32 crossbar array with on-chip peripheral circuitry in commercially available 0.18 µm triple-well CMOS technology for the proof of concept. We demonstrate bidirectional programming, showing a memristance change of ≈500 Ω for 120 and 80 pulses in positive and negative directions, respectively.

KEYWORDS

crossbar array, low voltage, RRAM, 1T1R, parasitic diode, programming, selector technologies

1 Introduction

With the evolution of data-intensive applications, from machine learning (ML) to deep learning (DL) (LeCun et al., 2015), processing and storing large amounts of data are the biggest challenges for the Von Neumann architecture. The Von Neumann bottleneck arises due to the long access time per operation in fetching both instructions and data from memory via a single bus. It thus limits the overall performance of a system, dissipating a large amount of energy. To solve this technological bottleneck, the emergence of non-volatile memory (NVM) became a new paradigm, with technologies that offer promising features over classical memory technologies, such as high density, low leakage power, scalability, and computing-in-memory (CIM) capabilities (Staudigl et al., 2022). There are numerous NVM technologies, including resistive random-access memory (RRAM), phase change memory (PCM), spin-transfer-torque magnetic RAM (STT-MRAM), and ferroelectric field effect transistors (FeFETs). Some have even become commercially available, such as TSMC's 40 nm RRAM (Chou et al., 2018) and Intel's 22 nm RRAM (Jain et al., 2019), TSMC's 40 nm PCM (Wu et al., 2018), Intel's 22 nm STT-MRAM (Wei et al., 2019), and Samsung's 28 nm STT-MRAM (Song et al., 2018), while doped HfO_2-based FeFET technology is also emerging, such as Global Foundries' FeFET at 22 nm (Dünkel et al., 2017).

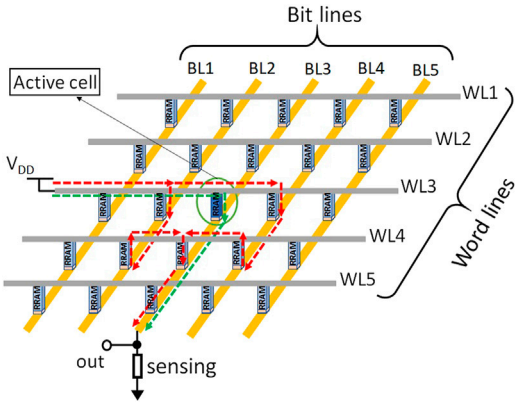

FIGURE 1
RRAM-based 5 × 5 "selectorless" crossbar array and the issue of sneak-path current. The dashed green signal is the actual current path, and the red signal is the sneak path.

Numerous studies have been conducted on the design of memory cells without using NVM technologies. Kim (2008) designed a single-bit memory cell using bipolar transistors, external Schottky diodes, and a capacitor. It was characterized by a lower word line loading, as it bypasses the transistors during programming. Prabhat and Myers (2020) demonstrate the use of the body bias technique to accommodate SRAM cells to operate at a lower operating voltage. Other SRAM-based designs also exist that use body bias technology to increase power efficiency (Mishra et al., 2021; Faraji et al., 2014). Houghton et al. (1998) designed a gain cell in a memory array using two transistors, one diode, and one capacitor. The main focus of their design is the gain cells used for the read-out operation and the diodes that prevent the conduction of the read transistor in the opposite direction.

RRAM/Memristor is considered a game-changing electronic device that can store multi-bit information at extremely low operational power (Stathopoulos et al., 2017; Chen et al., 2020). Moreover, due to its scalability, fast switching speed, and excellent cmos compatibility, it is considered competitive in next-generation memory devices (Berdan et al., 2014; Guan et al., 2012; Yu et al., 2012). RRAM-based crossbar arrays have been widely studied for in-memory computing and neuromorphic applications for their benefits in speeding computation and high area efficiency (Majhi et al., 2017; Lee et al., 2007). However, "raw" arrays suffer from "sneak current", also known as "sneak path current," whereby undesirable current flows through unselected or non-intended memory cells. This is demonstrated in Figure 1, where the green dotted path is the selected cell, while the red path results from unselected cells. Thus, the power which inherently compromises measurement accuracy in resistance states is drained, possibly even causing unintended writing on unselected cells. Multiple solutions exist, both at the biasing scheme and device levels. Biasing schemes (Chen, 2013; Deng et al., 2013; Li et al., 2021), effective at large write and read voltages, constrain leakage by applying some intermediate voltages to all the unselected cells within the array, thus preventing undesired disturbance to the stored data. Very recently, Chen et al. (2024) demonstrated that enhancing self-rectifying behavior in memristive cells offers better performance by characterizing the sneak path current in passive crossbar arrays. However, the dominant solution currently for circuit designers is using a selector— also known as an "access device"—connected in the path of the RRAM device, giving rise to the 1-selector-1-RRAM (1S1R) configuration. The selector may be a diode (1-diode-1-RRAM; 1D1R), a transistor (1-transistor-1-RRAM; 1T1R), or a mixed-ionic–electronic–conduction (MIEC) selector (Li et al., 2021; Huang et al., 2011; Burr et al., 2012; Chen et al., 2023). Transistor selectors are popular because they are directly implementable in cmos and have extra control flexibility via gate signaling. However, transistor selectors also bottleneck the high scalability of RRAM into high-density crossbar arrays and introduce significant series resistance, requiring compensation in the form of higher write voltages applied across the 1T1R stack. Dinh et al. (2016) used one transistor, one diode, and one RRAM to design a memory device. Here, the access transistor was switched on during programming and reading, while the parasitic diode was used during the erase mode. While this approach is interesting, the transistors' series resistance is a major bottleneck. Additionally, this approach cannot be used for bi-directional programming and multi-bit read–write at low voltages. Alshaya et al. (2023) and Fouda et al. (2018) found that the switching time for the 1T1R configuration is high and increases as the crossbar size increases.

To circumvent this, a new cell structure—1-transistor-1-diode-1-resistor (1T1D1R) uses metal oxide-semiconductor (MOS) diodes, including the bulk-S/D parasitic of the selector transistor, to bypass the selector during programming. The objective is to keep the voltage rating specification of the crossbar and its peripherals as low as possible (for example, operating under VDD = 1.8 V instead of requiring a 2.5 V supply for the programming process). Conversely, this can be thought of as improving the programming current drive in the 1T1R under fixed VDD. Programming through a diode allows significant current to pass with a voltage that does not significantly exceed the diode's "threshold"—in principle, capping the amount of switching voltage headroom that is consumed by the access device (the diode).

We have thus far successfully validated the 1T1D1R cell in the 0.18 μm cmos process at a 1.8 V supply, performing functionality tests for both programming and read operations. A comparison between the conventional 1T1R and the proposed cell in terms of the maximum achievable current drive on the RRAM device for the minimum-size MOS devices was made. To further show the efficacy of our concept, we constructed a 32 × 32 crossbar array and demonstrated the "programming" and "read" operations. This paper is thus structured as follows. Section 2 outlines the cell design. It demonstrates the overall working of the 1T1D1R cell, followed by an in-depth explanation of the programming and read operations and a simplified 2 × 2 array example. Section 3 presents a comparison of the proposed 1T1D1R with the 1T1R cell. This section also includes our in-house fabricated memristor model I-V characteristic (Maheshwari et al., 2021a). Section 4 demonstrates post-layout simulation results for a 32 × 32 crossbar array as a proof-of-concept, and Section 5 concludes the discussion.

2 1T1D1R memory cell design and operations

We propose a 1T1D1R structure, a tileable "memory cell" that when placed in an array configuration, can perform three basic

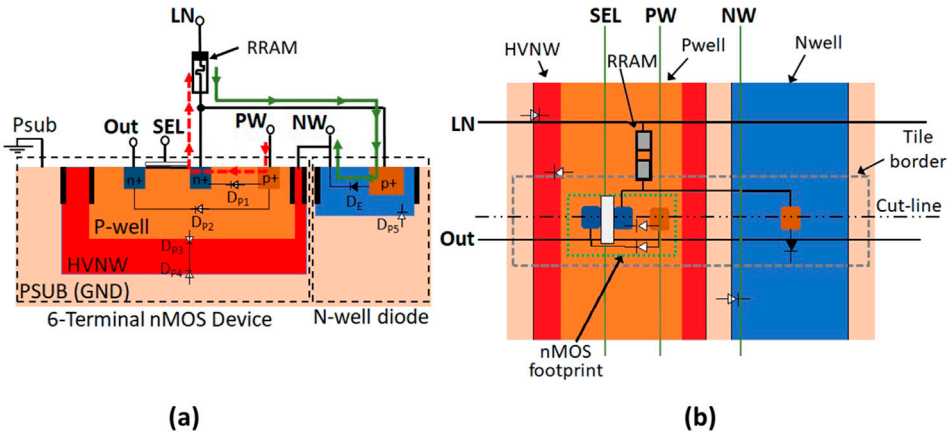

FIGURE 2
Layout view of 1T1D1R. **(a)** 2-D cross-section of 1T1D1R configuration along the cut line. Red dashed line and solid green line paths with arrows illustrate negative and positive programming directions, respectively. **(b)** Top view showing the nmos footprint.

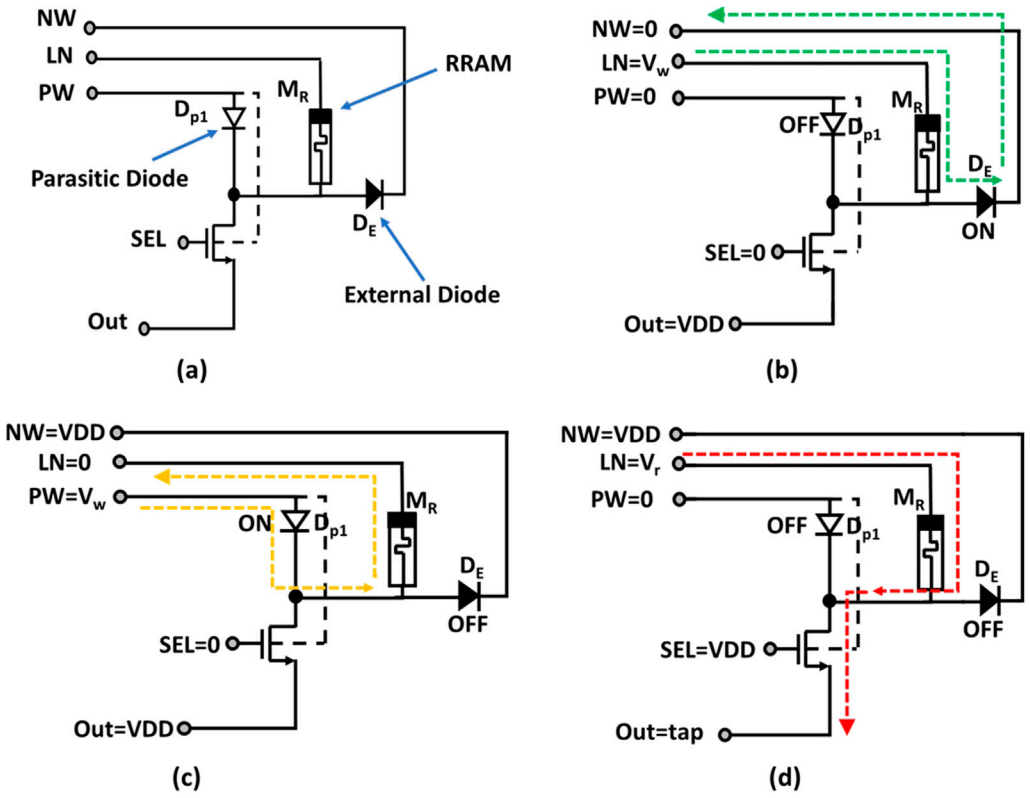

FIGURE 3
(a) 1T1D1R circuit diagram showing diodes and RRAM. **(b–d)** Terminal voltages for **(b)** "positive" programming with current direction from *LN* to *NW* (green dashed line); **(c)** "negative" programming with current direction from *PW* to *LN* (yellow dashed line); and **(d)** read operation with current direction from *LN* to *Out* (red dashed line).

operations: a) bidirectional (a.k.a. bipolar) programming/write; b) read; c) low-power idle mode (park). The 1T1D1R cell shown in Figure 2 has six terminals. Two of these arise as the nmos transistor sits on an insulated substrate formed by a nested *Pwell – Nwell* structure. In 1T1D1R, 1T represents a single triple-well nmos transistor with four parasitic diodes formed between differently doped regions: D_{P1}, D_{P2}, and D_{P3}, D_{P4}, with 1D as an additional diode D_E along with its parasitic diode D_{P5}, which is always reverse bias, and 1-R as our in-house fabricated $Pt/TiO_x/Pt$ VCM memristor model.

The two Nwells are connected via metal layers, and the terminal is named "*NW*." Figure 3a shows the equivalent circuit diagram for

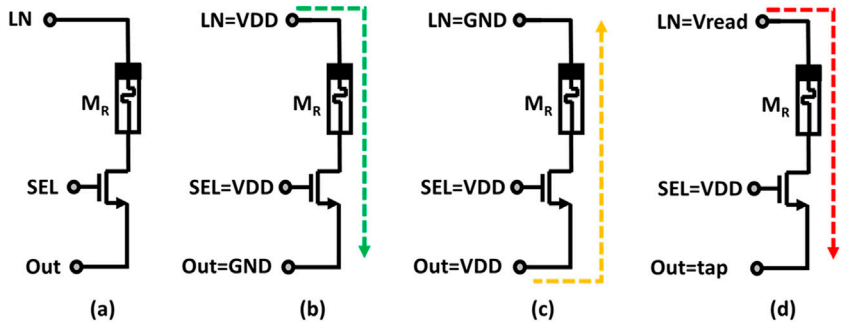

FIGURE 4
(a) Conventional 1T1R cell. Illustrates terminal voltages for **(b)** positive programming with the current direction from *LN* to *Out*. **(c)** Negative programming with the current direction from *Out* to *LN*. **(d)** Read operation with the current direction from *LN* to *Out*.

1T1D1R with five main terminals: transistor gate (*SEL*), transistor source (*Out*), Pwell (*PW*), high-voltage Nwell (*HVNW*), and the top electrode (*LN*). The sixth terminal (not shown) is *PSUB*, which is always connected to *GND*. In contrast, Figure 4a shows the conventional state-of-the-art 1T1R cell. The 1T nmos sits over the p-type substrate (PSUB) and has three main terminals: the gate (*SEL*), the top electrode (*LN*), and the source (*Out*). Figures 4b, c show cell terminal voltages and current direction for positive and negative programming, and Figure 4d covers the read operation.

2.1 Circuit operations

2.1.1 Programming mode

RRAM devices store data in their resistive states. Frequently, a "1" is stored as a suitably defined *low resistive state* (LRS) and "0" as a *high resistive state* (HRS). However, to program either of these values, potentially significant current must be passed through the RRAM device or "stuck-at" faults may occur.

In programming mode, terminal *Out* is connected to VDD, reverse biasing D_{P2}, and *SEL* is connected to ground (GND), shutting off the 1T device. For "positive" programming, we then set $NW = GND$, $LN = V_w$, and $PW = GND$, where V_w is the desired write voltage. This reverse-biases D_{P1}, bootstraps D_{P3} and D_{P4}, and drives current from LN to NW via D_E. Figure 3b shows 1T1D1R biased under the +ve prog mode. For "negative" programming, we set $NW = VDD$, $LN = GND$, and $PW = V_w$. This reverse-biases D_{P3}, D_{P4}, and D_E and drives current from *PW* to *LN* via D_{P1}. Figure 3c shows 1T1D1R biased under the -ve prog mode. Thus, programming occurs over a diode drop (as opposed to via the series resistance R_{on} of the 1T device), potentially achieving larger voltage drops across the RRAM and improving the chances of driving it to LRS or HRS. Note that D_{P1} is only used for *negative programming*, and the N-well/p-diffusion diode D_E is used for *positive programming*.

2.1.2 Read mode

For the read operation, the proposed 1T1D1R configuration maintains backward compatibility with standard 1T1R and offers multiple options. In all cases, *NW* and *PW* are connected to V_{DD} and GND, respectively, as per standard, and all diodes are reverse biased. In this study, we then set *LN* to a desired read voltage V_r, the 1T device is fully opened by setting $SEL = VDD$, and *Out* is connected to sensing circuitry, acting as a classical 1T1R configuration. Figure 3d shows 1T1D1R biasing during the read operation. Other options include reading via either of the write configurations or, indeed, under certain circumstances by setting $LN = VDD$ and $SEL = V_r$, causing the RRAM to be read at a particular (approximate) current. In this case, we could try sensing the voltage at the drain of the 1T via D_E or D_{P1}. However, these options lie outside the scope of this study.

2.1.3 Park mode

The memristors in the memory array are used as memory storage elements and are therefore electrically reconfigurable (they can be toggled repeatedly between their low and high conductance states called OFF and ON). There are several ways to "park" this circuit (switch it off). A possible configuration is with *LN*, *NW*, and *Out* terminals connected to VDD to ensure that the external diode (D_E) and diffusion well diodes (D_{P2}, D_{P3}, D_{P4}, and D_{P5}) are in deep reverse-bias mode. Terminals *SEL* and *PW* are connected to GND, ensuring that the nmos transistor is switched off and the D_{P1} well diode is in reverse bias mode. Thus, no current flows through the MOS transistors or through all the parasitic diodes, ensuring negligible power dissipation. The complete timing diagram for the programming (write), read, and park mode operation is illustrated in Figure 5. All the traces demonstrate voltage levels during the programming, reading, and park modes of a bit-cell.

2.2 Array design: no sneak current path

Here we examine the behavior of a 2 × 2 crossbar array structure and confirm the absence of sneak current paths. Figure 6 shows a 2 × 2 crossbar design with (2,1) as the active cell, with the remaining three inactive. Rows share the well (*PW* & *NW*) and the gate control (*SEL*) lines, whereas columns share the *LN* and *Out* lines. Each *Out* column line is connected to a sense amplifier. Unlike the 1T1R design, this configuration provides enough flexibility to program either a complete row or column independently. Table 1 reports voltage levels for all the operational modes of the 2 × 2 array. During programming, the

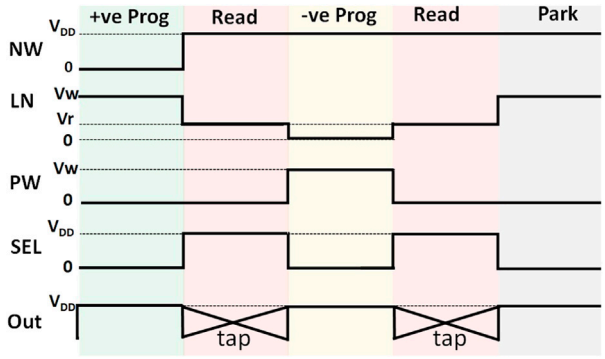

FIGURE 5
Timing diagram for programming (positive and negative), reading, and park operations. V_w and V_r represent programming and read voltages. During reading, the voltage/current is sensed from the *Out* terminal via read circuitry.

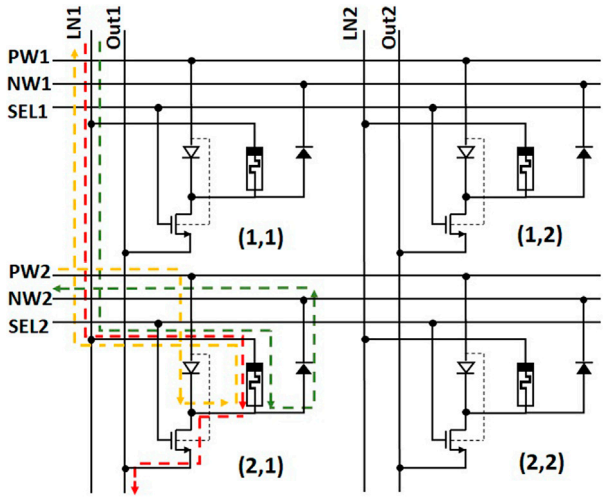

FIGURE 6
Programming and read paths of the target cell (2,1) in a 2 × 2 array. Green and yellow dashed lines represent *positive* and *negative* programming, respectively. The read operation is shown by the red dashed line. The diodes and the transistor effectively block all sneak paths.

RRAM memorizes either "0" or "1" via diodes, bypassing the 1T. The stored value is read through 1T via the *Out* terminal. Based on Table 1 and Figure 6, it is easy to deduce that there are no sneak current paths through semi-active/inactive cells. In parked mode, no significant current flows as all the diodes are in reverse bias and the transistor is switched off.

3 Memristor and 1T1D1R cell response

3.1 Memristor characteristics

Multiple memristor models exist in the literature (Kvatinsky et al., 2015; Messaris et al., 2017; Messaris and Serb, 2018). For this study, we use our in-house fabricated valance change memory (VCM) metal–insulator–metal structure $Pt/Tio_x/Pt$-based model, which can generalize to other flavors of VCM memories (Messaris and Serb, 2018). A Verilog-A memristor model utilising exponential fitting and experimentally extracted parameters for the RRAM range 10 $k\Omega$ –17 $k\Omega$ is reported in the appendix of Maheshwari et al. (2021a). The SPICE simulation for the same using the 0.18 μm cmos process is reported in Maheshwari et al. (2021b). The RRAM non-linear I-V characteristic and the testbench [inset] are shown in Figure 7. Input voltage values range in $[-1V, +1V]$, and the I-V curve shows pinched hysteresis characteristics. These particular devices exhibit very smooth switching, thus requiring no compliance control, although compliance can be added at the peripheral level if necessary. Here, we focus on the array core.

3.2 1T1D1R versus 1T1R under DC and transient response

RRAM device programming in both forward (positive) and reverse directions (negative) is done by setting the terminals *LN*/*PW* and *LN*/*NW* to a voltage up to 1.8 V for maximum current and the other terminals *PW*/*LN* and *NW*/*LN* to 0 V. The 1T1D1R cell is simulated for multiple memristance values, both within the model range and extrapolated outside the range to stress-test the configuration. The proposed structure is also compared with the conventional 1T1R structure. The test bench is constructed and operated as per Figure 5 for positive and negative programming. Figure 8a illustrates the voltage (V_{MR}) and current drive on the device for positive programming and Figure 8b for negative programming. The solid line represents 1T1D1R, and the dotted line represents the 1T1R structure. In positive programming, the 1T1D1R cell design shows ≈3.7× improvement in current drive and ≈ 450 mV more drop across RRAM vs. the 1T1R configuration at 1 kΩ. The diffusion diode used during the negative programming resulted in ≈4.7× improvement in the current drive and ≈ 500 mV more voltage drop. These current and voltage improvements are extremely significant and allow working at voltages lower than or equal to 1.8 V for RRAM devices working in this range. Furthermore, for our model and range (Maheshwari et al., 2021a), the transient response CAD simulation for 1T1R and 1T1D1R cells for alternate positive and negative programming trains of 5,000 pulses is shown in Figure 9. Each programming has a pulse width of 1 μs and is followed by a 9 μs read pulse width. During positive and negative programming, the memristive state converges to specific upper and lower boundary limits determined by the driving capability of the cell; this is a result of "the windowing" of memristive behavior (Slipko and Pershin, 2021). Figure 9 shows the boundaries significantly expanded for 1T1D1R configuration.

4 32 × 32 crossbar array design and analysis

4.1 Architecture design overview

For proof-of-concept, we designed a 32 × 32 crossbar array with on-chip row and column peripherals. The block diagram for the

TABLE 1 Voltage levels for the operation of a (2,1) target cell in a 2 × 2 array. Here, V_{DD}, *Vw*, *Vr*, and *GND* represent maximum, write, read, and the minimum voltage levels. The columns LN1, Out1, PW2, NW2, and SEL2 show the target cell operational voltage values.

Modes	LN1	PW1	NW1	SEL1	Out1	LN2	PW2	NW2	SEL2	Out2
Negative programming	GND	GND	VDD	GND	VDD	VDD	Vw	VDD	GND	VDD
Positive programming	Vw	GND	VDD	GND	VDD	GND	GND	GND	GND	VDD
Read	Vr	GND	VDD	GND	Tap	VDD	GND	VDD	VDD	VDD
Parked	VDD	GND	VDD	GND	VDD	VDD	GND	VDD	GND	VDD

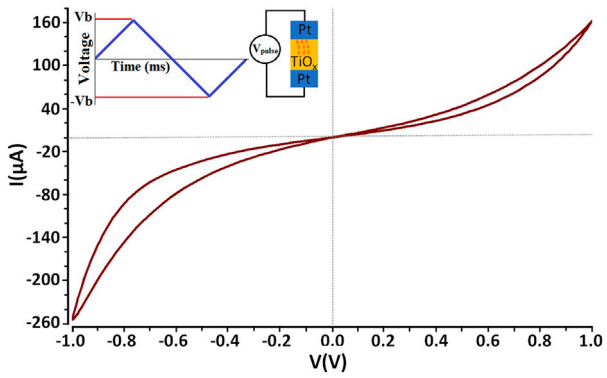

FIGURE 7
Typical I-V characteristic showing the pinched hysteresis loop of our in-house fabricated memristor model. The inset shows the test bench and the input voltage. The model's parameters are presented in the appendix of Maheshwari et al. (2021a).

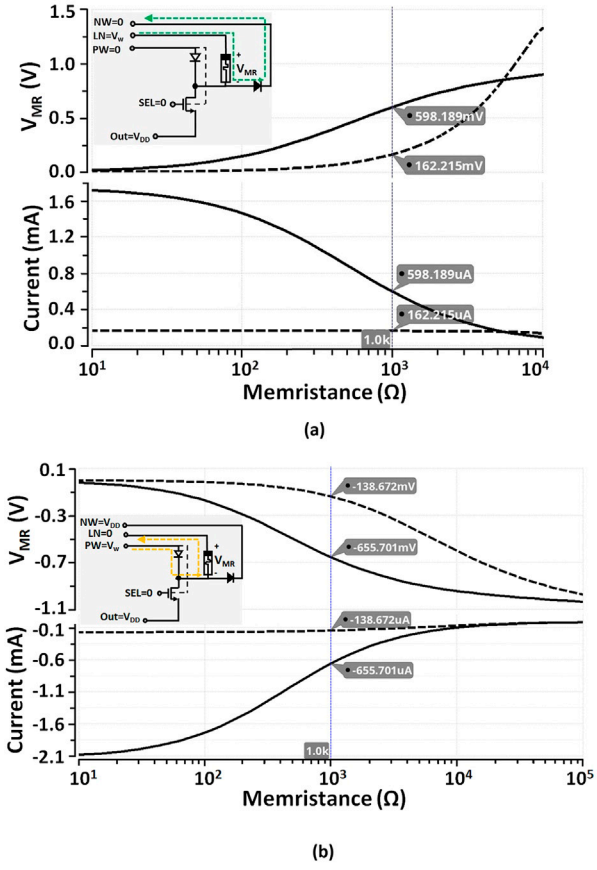

FIGURE 8
Current and voltage drive (V_{MR}) on RRAM device for memristance values ranging from 10 Ω to 10 k Ω for **(a)** positive and **(b)** negative programming. The solid and dashed lines signify the proposed 1T1D1R and 1T1R responses, respectively.

32 × 32 crossbar array is shown in Figure 10a. The fully integrated architecture with all the necessary interface circuitry is designed using a commercially available 180-nm cmos process. RRAM cells designed in this work are based on an experimental model developed by our research group (Messaris and Serb, 2018; Maheshwari et al., 2021a,b). All system components are powered with a 1.8 *V* power supply. The layout of a 32 × 32 crossbar array with on-chip peripheral circuitry is shown in Figure 10b. We note that we only have 4× metals available in the chosen technology (fewer than the number of major signal lines), leading to a high layout area. Using technologies with more metal layers can improve this, as the design is back-end-of-line (BEOL) limited.

The target cell is selected based on the row (*Row_addr*[1:32]) and column (*Col_addr*[1:32]) address. It is then programmed depending on the data (*Data*[1:32]) input. The *WEN* signal is active high for programming and active low for reading. Simultaneously, *Write* is a column programming signal that is active high when programming "1" and active low when programming "0" in the crossbar. As each column and row is independent of other columns and rows, the crossbar can also be used to one-shot-program an entire 32-cell row or column.

4.1.1 32 × 32 array design

To minimize the crossbar area, 32 nmos transistors are encapsulated inside *NW* (as they share rows) and are surrounded by *PSUB*, forming a 1 × 32 cell slab (Figure 11). The 16 external diodes are placed on either side of a 1 × 32 cell. These p-type diodes are here used with Nwell. Figure 11 also shows an inset of a single cell showing the active area where the memristor will be deposited, connected between the *LN* and the nmos drain (*D*) terminal. The RRAM device is placed above the transistor to maximize cell density. The dimension of the non-optimized layout cell of 1 × 32 cell array is 17.18 μm × 128.14 μm (Figure 10c). The integration of cmos with the memristive device is done using regular BEOL processes after the cmos substrate has been formed; this is explained in more detail in Section 3 of Mifsud et al. (2022). Each slab has *NW*, *PW*, and *SEL* terminals running horizontally, while the terminals *LN* and *Out* run vertically. The complete 32 × 32 array is designed to have 2× pages of 16 × 32 cells,

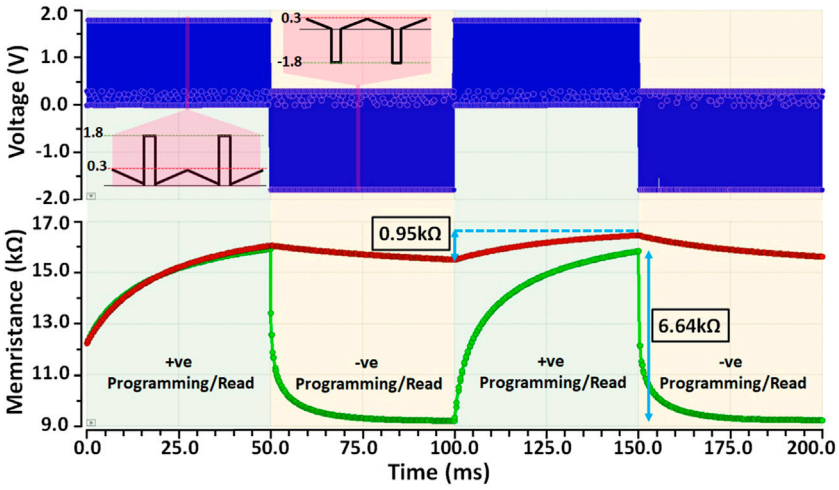

FIGURE 9
1T1D1R versus 1T1R transient response for programming and read pulse width of 1 μs and 9 μs, respectively. The programming and read voltage values used are 1.8 *V* and 0.3 *V*, respectively. The initial memristive state is set at 12.25 k Ω in the Verilog-A model. [TOP] Alternate voltage is applied in a single cell, and the [BOTTOM] memristive state is recorded for 1T1R (red trace) and 1T1D1R (green trace).

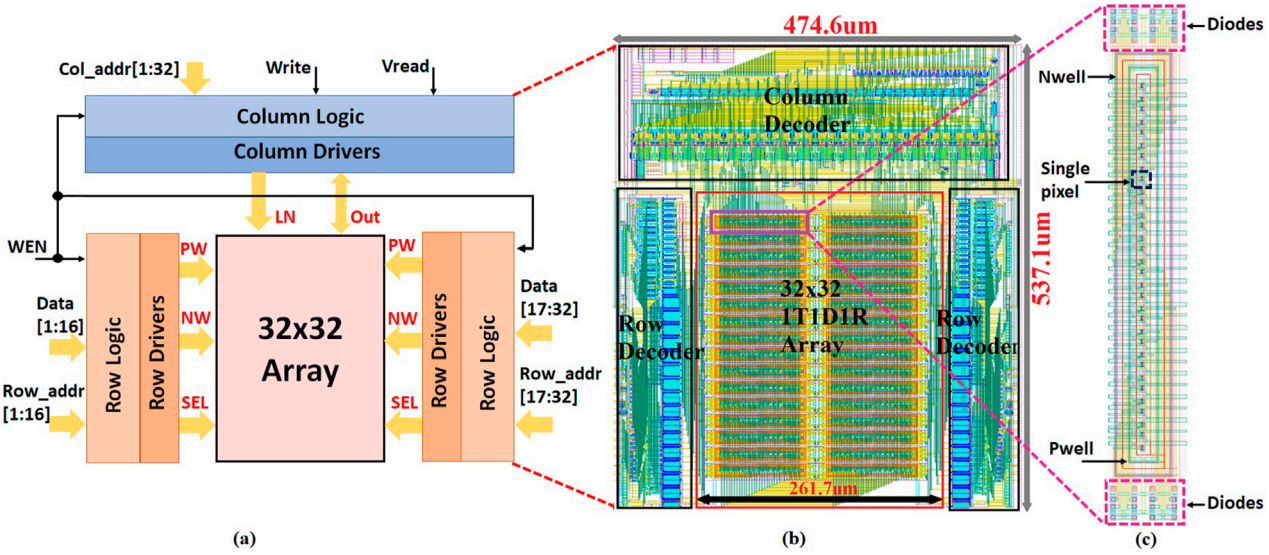

FIGURE 10
(a) 32 × 32 crossbar array architecture. **(b)** Layout with on-chip peripherals. **(c)** 1 × 32 cell slab showing external diodes (D_E).

where each page is constructed using a 1 × 32 cell slab. The 32 × 32 array has a layout dimension of 344.5 μm × 261 μm.

4.1.2 Row circuitry

The row circuitry (RC) constitutes logic for *NW*, *PW*, and *SEL* signals to the array. The 32-bit RC block diagram is shown in Figure 12; it consists of AND logic, muxes, and driver cells that can drive large capacitances and resistances on the row. The gate-level implementation of SEL, PW, and NW logic is shown in Figure 13, and its equivalent truth table is demonstrated in Table 2. The write/read enable signal (W/R enable) acts as a system reset. During programming and reading, it is held at logic "1" and "0" under park mode (reset). Once the system is enabled, the write enable (WEN) signal is enabled by setting it to logic "1" for memory write and "0" for read. The design is configured such that multiple cells, either row- or column-wise, can be programmed or read simultaneously. The +ve and -ve programming depend on the value of the data to be written in the memory cell. Each RC serves 2× pages of 16 rows, consisting of row logic on either side of the 32 × 32 array.

4.1.3 Column circuitry

The column circuitry (CC) constitutes logic for *LN* and *Out* signals connected to the array (again, logic and drivers). The "Out logic" is a bi-directional signal that allows current to flow through

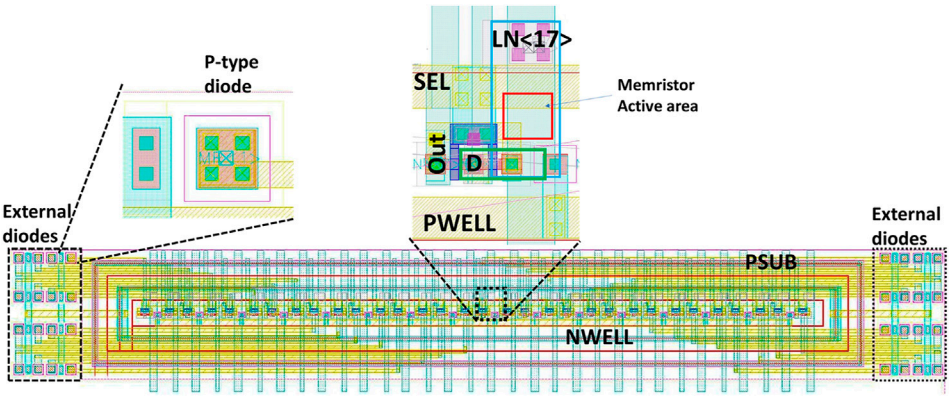

FIGURE 11
Layout of a 1 × 32 cell slab with external diodes (D_E). The inset shows a single cell with the memristor area and the p-type external diode.

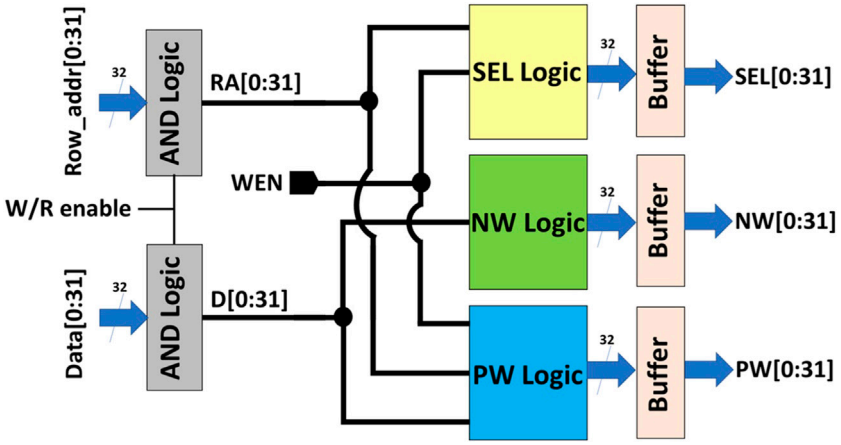

FIGURE 12
Implementation of 32 × 32 row circuitry, used to generate row signals SEL, NW, and PW. Input address and data are gated with a write/read enable signal.

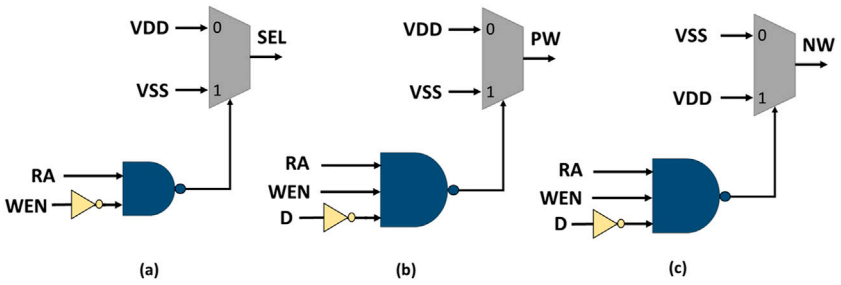

FIGURE 13
Gate-level implementation showing row logic circuitry. **(a)** SEL logic set either to VDD or GND. **(b)** Pwell logic used for negative programming. **(c)** Nwell logic used for positive programming.

the transistor during "read." The gate-level implementation of the CC is shown in Figure 14, and its equivalent truth table is shown in Table 3. Here, a single bit "write" signal is used which is activated by setting it to logic "1" during +ve programming, and "0" during -ve programming, and an appropriate value is set on the *LN* terminal. However, when the WEN signal is deactivated—that is, logic

TABLE 2 Row logic circuitry truth table generating SEL, PW, and NW signals for positive programming, negative programming, read, and park mode.

Modes	Inputs				Outputs		
	W/R enable	WEN	RA	D	SEL	PW	NW
Positive programming	1	1	0	1	0	0	1
	1	1	1	1	0	0	Vw
Negative programming	1	1	0	0	0	0	1
	1	1	1	0	0	Vw	1
Read	1	0	0	0	0	0	1
	1	0	1	1	1	0	1
Park	0	x	x	x	0	1	1

0 and 1 signify ground (GND) and supply voltage (V_{DD}), and Vw is the write voltage.

TABLE 3 Column logic circuitry truth table generating LN and Out signals for positive programming, negative programming, read, and park mode.

Modes	Inputs				Outputs	
	W/R enable	WEN	CA	Write	LN	Out
Positive programming	1	1	0	1	0	1
	1	1	1	1	1	1
Negative programming	1	1	0	0	1	1
	1	1	1	0	0	1
Read	1	0	0	x	1	1
	1	0	1	x	Vr	To Output PAD
Park	0	x	x	x	0	1

0 and 1 signify ground (GND) and supply voltage (V_{DD}), and Vr is the write voltage.

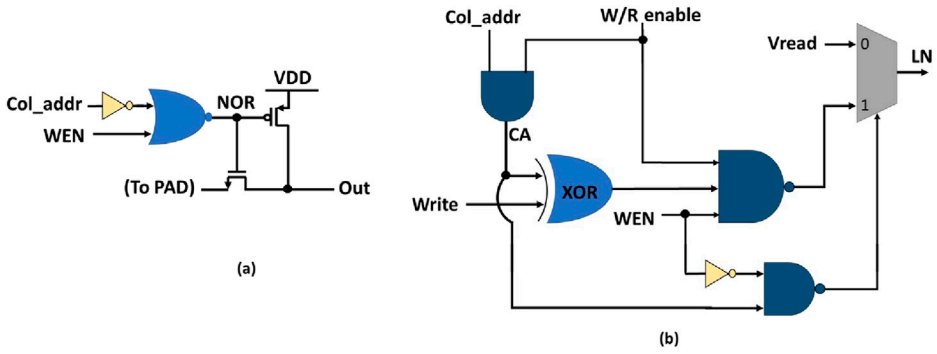

FIGURE 14
Column circuitry for reading either single cell or bunch of cells, either row or column-wise. **(a)** Out-logic for reading stored value in a cell. **(b)** LN logic for setting required voltage for writing and reading.

"0"—then irrespective of the "write" signal, the *Out* terminal is connected to the PAD where the current flows through the transistor to the external current amplifier for reading.

4.2 Timing analysis and evaluation

The post-layout simulated waveform for the 32 × 32 crossbar array is illustrated in Figure 15. According to Maheshwari et al. (2021a), the programming and read pulse widths are set to 1 μs and 9 μs, respectively. The selected target cell to demonstrate programming and read operations is M_{1024}. The respective row and column address of the target cell is selected (here *Row_addr* [32] = "1," *Col_addr*[32] = "1"). All other row and column addresses are set to "0." Initially, the system is in park mode as "W/R enable" is set to "0." To initiate programming and the read operation, the W/R enable signal is set to logic "1." The "*WEN*" signal is high only during programming operations. A read pulse follows every programming pulse. The column decoder biases "*LN*" depending on the column write signal *Write*, for +ve programming it is set to "1", and for -ve programming it is set to "0." Similarly, the row decoder generates "*PW*" and "*NW*" pulses depending on the *Data* input of a target cell in the row (similar to column write). Finally, memristance is measured by observing the current in the target cell. The initial memristance value is set to 11.25 kΩ. From Figure 15, we can see a memristance change of ≈+500 Ω over 120 pulses of positive programming and −510 Ω over 80 pulses of negative programming. We calculated the maximum voltage drops as +871 mV and −951 mV during positive and negative programming across the device.

The final comparison of 1T1D1R with 1T1R cell is shown in Table 4. Due to the two wells, the cell has a higher area; however, there is a negligible change in the programming energy consumption. The proposed design shows an increased current drive, recorded at 1 kΩ, of about 3.7× and 4.7× during +ve and -ve programming, respectively, compared to the conventional 1T1R. The key observation is the switching state from HRS to LRS, where the proposed 1T1D1R cell shows a change of ≈7× in comparison to 1T1R. The tabulated energy results for a 32 × 32 array include on-chip peripheral energy, which is responsible for ≈90% of the energy required to operate

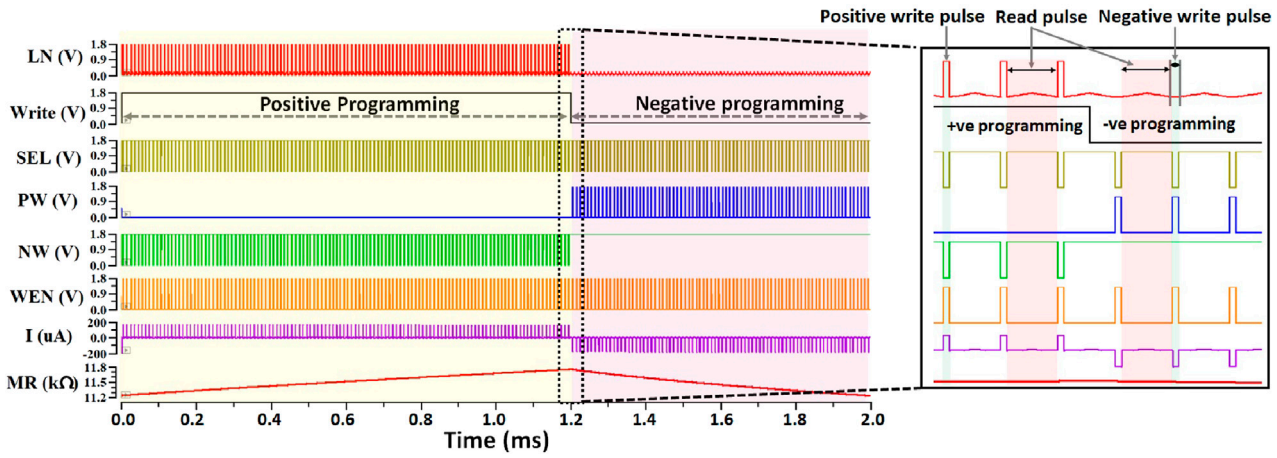

FIGURE 15
Post-layout simulated results for 32 × 32 cells with peripheral circuits. Write and read pulse widths are 1 μs and 9 μs respectively. Positive programming is applied during [0, 1.2]ms and negative programming during [1.2, 2].ms.

TABLE 4 Comparison of 1T1R and proposed 1T1D1R single cell and post layout result of 32 × 32 crossbar array.

Technology, supply voltage	180 nm cmos process, 1.8	
RRAM Technology (Messaris et al., 2018)	$Pt/Tio_x/Pt$ (10–17 kΩ)	
Single cell		
	1T1R	**Proposed**
Memristive range	0.95 kΩ	6.64 kΩ
DC current @ 1 kΩ (positive programming)	162.2 μA	598.2 μA
DC current @ 1 kΩ (negative programming)	138.7 μA	655.7 μA
Energy (positive programming)	28.44 pJ	27.99 pJ
Energy (negative programming)	1.22 pJ	1.88 pJ
Cell size[a]	5 × 2.28 μm^2	3.4 × 17.18 μm^2
32 × 32 Crossbar Array with On-Chip Peripherals		
Cell layout area	261.7 × 305.25 μm^2	
Total layout area	254,907.66 μm^2	
Single cell energy (positive programming)	230.9 pJ	
32-cell energy (positive programming)	10.59 nJ	
Single-cell energy (negative programming)	71.77 pJ	
32-cell energy (negative programming)	1.261 nJ	

[a]1T1R cell size @ 5 V supply.

the cell. The design was also simulated by programming the entire column of 32 memory cells. The +ve programming shows more drop across the diode; hence, more energy is dissipated than for the -ve programming. The difference in current drive capability for +ve and -ve programming results in higher energy consumption for the +ve programming. This energy can be reduced to the extent that resistive and capacitive parasitics can be moderated in the technology of choice (Chen, 2013).

5 Discussion and conclusion

We obtained a ≈3.5× improvement in the current drive at 1 kΩ and ≈7× improvement at 100 Ω resistance. We also obtained a ≈60% increase in programming voltage in one polarity and ≈3× in the opposite polarity at 1 kΩ memristance. The voltage increase at 100 Ω is ≈20% and is a very large factor in the other (the denominator is close to 0 in the 1T1R case—i.e., no drive voltage). This may make the difference between the presence or absence of viable resistive switching in a cmos/RRAM technology combination. We note, for example, that the relation between switching speed and electric field can be exponential; thus, small factor changes can cause dramatic effects (see the effect of a 30% change in voltage drive on switching in Figure 9). Crucially, because of non-linearities in the IV characteristics of our devices, even devices with relatively high nominal resistances (e.g., 10 s to low 100 s of kΩ measured at our standard of 0.2 V read-out voltage) present static resistance in the low kΩ range when high programming voltages are applied to them. Hence, we foresee that this technique will have much broader use than the headline figures might suggest (relevant to RRAM devices in the [0, 100]kΩ nominal resistance range, instead of the [10,10 k]Ω ranges quoted in Figure 8). In addition, our proposed solution can be readily implemented in any commercially available cmos technology, especially if it includes triple-well capabilities, and requires minimal modifications to peripheral circuit design. The cost is a significantly increased layout area, but with the principle proven, future versions—including silicon-on-insulator (Boni et al., 2023) or even the implementation of BEOL-diodes—the incurred layout cost could change very dramatically and potentially even render this technique mainstream. It will be very interesting to see which way the die is cast.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material; further inquiries can be directed to the corresponding author.

Author contributions

SM: Conceptualization, Formal Analysis, Investigation, Methodology, Validation, Writing – original draft, writing – review and editing. AS: Conceptualization, Project Administration, Supervision, Visualization, Writing – review and editing. TP: Conceptualization, Funding acquisition, Supervision, Writing – review and editing.

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Conflict of interest

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