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Fabrication of Silicon Sensors Based on Low-Gain Avalanche Diodes

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Low-Gain Avalanche Diodes are a recently-developed class of silicon sensors. Characterized by an internal moderate gain that enhances the signal amplitude and if built on thin silicon substrates of a few tens of microns, they feature fast signals and exhibit excellent timing performance. Thanks to their fast timing they are planned to be exploited in timing detectors in High-Energy Physics experiments, for example for the upgrades of the ATLAS and CMS detectors at the High Luminosity Large Hadron Collider (HL-LHC) at CERN. However, to achieve a spatially uniform multiplication a large pixel pitch is needed, preventing a fine spatial resolution. To overcome this limitation, the AC-coupled LGAD approach was introduced. In this type of device, metal electrodes are placed over an insulator at a fine pitch, and signals are capacitively induced on these electrodes. The fabrication technology is similar for the two LGAD families, although a fine tuning of a few process parameters needs to be carefully studied. Other R&D efforts towards detectors that can simultaneously provide good time and spatial resolution, based on the LGAD concept, are under way. These efforts aim also to mitigate the loss of performance at high irradiation fluences due to the acceptor removal within the gain layer. In this paper we describe the main points in the fabrication of LGADs and AC-LGADs in a clean-room. We also discuss novel efforts carried on related topics.

Keywords: silicon detectors, high-energy physics, impact ionization, fabrication process, timing, avalanche photodiodes

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1 INTRODUCTION

Detection of minimum ionizing particles (mips) is easily achieved with silicon-based detectors. In fact, High Energy Physics (HEP) experiments started using silicon strip detectors back in 1980 [1]. The amount of charge released by a mip is about 80 electron/hole pairs per micron of silicon traversed which gives origin to a fair signal that can easily be detected by modern read-out electronics. Even in the case of thin sensors, which may be preferred to limit both the applied voltage (especially after irradiation) and the Coulomb scattering, which deliver less charge while adding capacitance at the read-out node, such detection does not constitute an issue. For example the ATLAS [2] and CMS [3] experiments at CERN count millions of channels, and their innermost layers are populated with thin silicon sensors that undergo a severe irradiation. The front-end read-out electronics is typically based on a charge sensitive amplifier at the input stage followed by some filtering or shaping stage for noise reduction. Shaping times of a few hundreds of nanoseconds are typical; they are not chosen to maximize the Signal-to-Noise ratio (S/N) but to cope with the high rate of events expected.

However, in the future operation of the above mentioned experiments, an increase in luminosity is foreseen and multiple interactions are expected per bunch crossing. To distinguish tracks

belonging to different vertexes, the proposed solution is to add timing information to the tracks (in the order of tens of picoseconds) because the interactions are separated in time by that amount. If we are able to read-out at the necessary speed, we can disentangle multiple primary and secondary vertexes, reduce ghost tracks, and generally ease the reconstruction [4]. Thus far, this cannot be achieved with the standard silicon detectors used.

A new silicon detector, which has been under development for a few years, has been chosen for this application due to its timing performance [5, 6]. It is based on the Low-Gain Avalanche Diode concept (LGAD), a silicon sensor that can deliver fast pulses with the required timing resolution because of two properties:

- LGADs are fabricated on thin substrates across which the carriers drift in a short time to the electrodes.
- The signals are internally amplified (in the order of 5–100) which not only compensates for the reduced signal generated in a thinner substrate, but also makes the signal detectable when read-out by a high-speed front-end.

They have been pioneered by the Centro Nacional de Microelectronica (CNM, Barcelona, Spain) [7] and developed during the past few years within the CERN-RD50 community. Currently, the sensor R&D is still very active and many research facilities around the world are involved such as: Brookhaven National Laboratory (BNL, Upton, United States) [8], CNM, Fondazione Bruno Kessler (FBK, Trento, Italy) [9], Hamamatsu (Japan) [10], IHEP-NDL (Beijng, China) [11], Micron (Lancing, United Kingdom) [12]. It is worth mentioning that there are families of LGADs which are fabricated on thick substrates: iLGADs [13] are double-sided LGADs (multiplication layer on one side and hole-collecting fine-pitch electrodes on the opposite side of the wafer) which are fabricated on thick high-resistivity silicon wafers. As such, they loose the timing performance but, being the signals internally amplified, are still useful when soft X-ray detection is needed.

Internal charge amplification in silicon has been extensively used for the detection of light (mainly visible or UV) [14]. Avalanche PhotoDiodes (APD) are well-known and extensively used silicon devices with an internal amplification in the range 10–200, adjustable by applying a suitable external bias voltage [15]. They are used for scintillation light detection in High energy Physics experiments [16, 17]. In some applications, APDs are also used for soft X-ray detection [18]. APDs come in a variety of structures, some of which may not differ very much from the LGAD structure. However, since the kind of particle detected is different (photons for the APD and mips for LGADs), an ad-hoc development must be pursued to optimize the LGADs. One obvious difference is that in the case of an LGAD a gain higher than about 20 is not needed to achieve the sought-after timing performance (but higher gains are easily achievable). The fabrication of the LGAD may be greatly simplified since there is no need of an engineered entrance window (which is necessary if the APDs are used to detect light) as well as not requiring a deep or diffused junction [19] This will be explained in the following sections.

In this paper by describing the structure, the properties and the signal shape of LGADs, we point out the fabrication strategies that optimize their performance. After describing its limitations, we report some of the efforts carried on to overcome such limitations.

2 STRUCTURE OF AN LOW-GAIN AVALANCHE DIODE

LGADs are based on simple p–n junctions which are engineered to specifically detect mips traversing the substrate. Some pictures of LGADs viewed from the top and coming from different foundries are shown in **Figure 1**. As in a conventional diode-based sensor, mips generate electron/hole pairs into the substrate along their track; carriers that are generated in the volume with non-null electric fields (i.e. in depleted regions) promptly drift away following the electric field lines and induce signals at the electrodes according to Ramo's theorem [20]. As it is well known, electrons drift towards the n electrode (positive terminal) while the holes towards the p electrode (negative terminal). It is an intrinsic property of silicon that ionization coefficients are higher for electrons than for holes (for the same electric field). As such, in silicon device with internal amplification which do not work in Geiger mode, the drifting electrons are primarily responsible for the amplification. This is achieved by making them cross a high-enough electric field in which they undergo impact ionization. The electric field, on the other hand, is kept low-enough to avoid an important multiplication of holes and therefore preventing breakdown.

High electric fields can be simply obtained by creating a junction between two enriched layers of phosphorus and boron, from a fraction of micron to a few microns apart. Upon depletion, partial or total of one or both these layers, a high electric field is obtained. As mentioned previously, the electrons need to be multiplied so it is the boron implant that undergoes full depletion while the n-layer collects the drifting electrons. It is convenient to put the n-layer at the top of the wafer, for example by implantation of phosphorus, and to make a structure from the top n-layer to the back contact as in the example: $n^+/p/i/p^+$. In this case, p is the enriched boron layer which undergoes depletion, i is the high resistivity substrate, and p^+ is a low-resistivity contact for hole collection.

In the following sub-sections we detail the different parts making up an LGAD, which are depicted in **Figure 2**.

2.1 Substrate

To deliver a fast signal, LGADs must be fabricated on thin silicon substrates, usually in the range of 20–50 μm thick. For example, both experiments ATLAS and CMS plan to use 50 μm thick LGADs as sensors in their timing detectors. However, such thin substrates are impossible to process with equipment normally present in a standard clean-room. The thin active layer, which is depleted under normal operation and where the mips deposit the charge that is responsible for the creation of the signal, may be epitaxially grown over a thick low-resistivity handling wafer. The latter acts both as a mechanical support and as a ohmic contact. Being a sink for the holes, it must be p-type. It is convenient that the thin high-resistivity layer above the p-type low-resistivity bulk

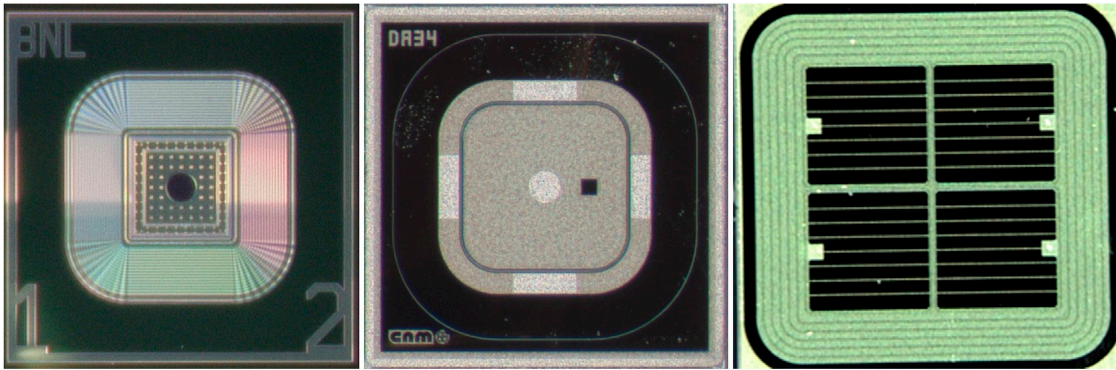

FIGURE 1 | Examples of LGADs produced by three different foundries: from left to right, BNL, CNM and IHEP-NDL.

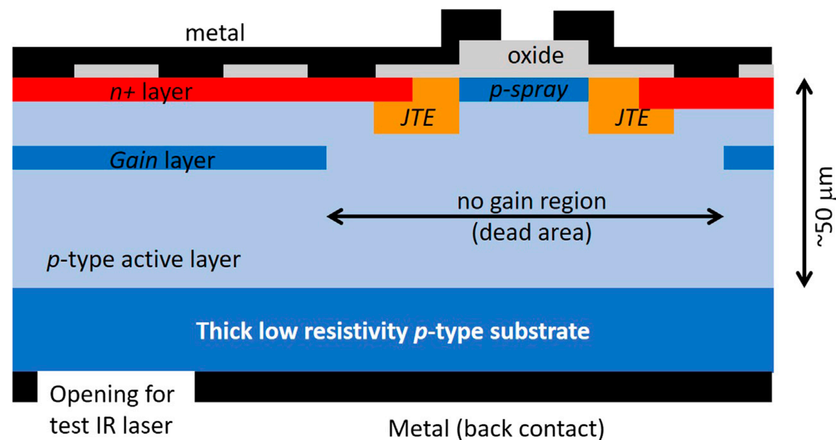

FIGURE 2 | Simplified cross-section of an LGAD, not to scale. The *p*-spray isolation implant between pixels can be replaced by a *p*-stop implant.

is *p*-type as well. This also prevents the charge-sign inversion after irradiation, commonly observed in *n*-type substrates, even after modest irradiation levels. Another way to handle such thin wafers is to bond two of them together. One of the wafers would be a thick low-resistivity wafer and the other being a high resistivity wafer which will subsequently be thinned down to the desired thickness by a standard process (e.g. wafer grinding followed by a polishing step, Chemical Mechanical Polishing (CMP) or dry polishing). In both cases, the handling wafer is a low-resistivity and no structures can be fabricated there. It comes that thinned LGADs for fast timing are intrinsically single sided devices: the only pattern that may be present on the back is a patterned metal to allow a laser beam through for testing purposes.

As mips deliver a charge proportional to the thickness of the traversed substrate, a lesser charge is generated in thin active layers and higher gains need to be engineered to achieve the same output charge.

2.2 n^+

An LGAD pixel or strip element is defined by an uniform, highly doped shallow n^+ region, usually obtained by means of a high-dose phosphorus implantation. This implant is then in contact, at least in part, with an aluminum metalization for the purpose of connecting to the external world by means of wire-bonding or bump-bonding (in which case an under-bump metalization (UBM) is required over the aluminum bump pad). Some n^+ regions may be covered by an oxide layer so that the metal contacts the n^+ in limited regions only. However, it is important that the resistance path that the signal sees, from the point in which the mip hits within the n^+ region and the metal, is negligible. From here the importance of having both a high-doped n^+ layer which offers a low resistance to the signal as well as closely spaced contacts. In fact, if LGADs are used for fast-timing applications, they are read-out with wide-bandwidth front-end electronics, order of 1 GHz. The RC associated with the LGAD must be well below 0.1 ns, which is of the same order as the rise time of the signal. The n^+ implant on the depleted substrate must be considered as a network of resistance and capacitances (towards the back) so that a signal that is generated at some point is "frozen" for a time RC in the area surrounding the hit position.

Also, ohmic contacts between n^+ and aluminum must present very low resistance, which can be achieved by a high-dose

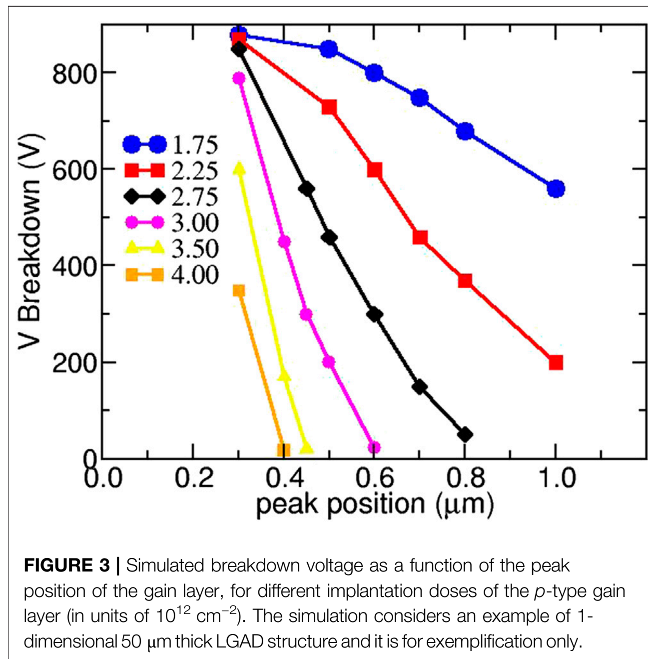

FIGURE 3 | Simulated breakdown voltage as a function of the peak position of the gain layer, for different implantation doses of the p-type gain layer (in units of 10^{12} cm^{-2}). The simulation considers an example of 1-dimensional 50 μm thick LGAD structure and it is for exemplification only.

phosphorus implantation properly annealed. In the extreme case, if an LGAD is fabricated with a low-dose phosphorus implant as n^+ and designed with distant contacts, one may be able to read-out only lower (and broader) signals as we will see in the following sections dedicated to the AC-LGADs.

2.3 Junction Termination Edge

At the border of the n^+ and ohmically connected to it, usually a Junction Termination Edge (JTE) is implanted [21]. This is a deep, low dose, phosphorus implant which serves the purpose of reducing the electric fields at the border and assuring that the maximum-value electric fields develop at the junction of the n^+/ gain layer. In this way, impact ionization in the device only occurs here. It is practical to do this implantation as the first implantation of the process so that it undergoes all the thermal cycles required. This increases the diffusion of the layer and its high-voltage handling capability. A way to implant the JTE deep, even with a sub-maximal implantation energy, is to exploit the channeling effect in silicon by implanting the phosphorus with zero tilt and rotation in a 100 oriented wafer. To still have a high doping concentration at the interface, multiple implantations can also be foreseen for the JTE, with low energies and high doses followed by higher energies and lower doses.

2.4 Gain Layer

The gain layer is a deep, low-dose boron implant, that undergoes full depletion during operation. Typically, the dose is anywhere between about 1.5 10^{12}–5.10^{12} cm^{-2} depending on a number of parameters such as substrate thickness and doping as well as profile of the gain layer and its depth. Since it is a critical parameter of the process, it must be carefully controlled and this is usually achieved by ion-implantation. High-energy implantations are best suited for this application. As a rule of thumb, a deeper gain layer requires less implanted dose than a shallower one, so that also the electric field in between the n^+ and the gain layer is lower. Since the ratio of the impact ionization for electrons and holes is a function of the electric field (the higher the ratio the lower the field), deeper gain layers are preferred when lower multiplication noises are sought-after. On the other hand, shallower gain-layers are advantageous when considering radiation hardness, because of their higher doping concentration peak. Since the gain depends on a complicated integral of a function of the electric field, the depth of the gain layer plays a crucial role in the gain of an LGAD. As seen in the example of **Figure 3**, obtained by means of TCAD simulations of possible LGAD structures, the breakdown voltage strongly depends on both the depth and the dose of the gain layer. A peak position in-between 0.4 and 1 μm are achievable with standard implantation energies (up to 400 keV). Given an implantation energy, i.e. a depth for the gain layer, the implantation dose that results in an optimal breakdown voltage (200–300 V) falls within a very limited range of values, so that every care must be taken to develop a consistent and reproducible process flow.

The gain layer must be contained within the border defined by JTE, otherwise high electric fields develop where the JTE ends due to its curvature. The tip of the gain layer can also be embedded into the JTE, which is usually more doped than the gain layer, provided the JTE is deep enough.

Usually, one wants to numerically simulate the process in order to limit the process splittings during prototyping. Standard impact ionization models in a TCAD simulator may not well reflect the process used and an ad-hoc definition of the parameters must be conducted. At least for the first productions, foundries prefer to process in parallel a few wafers that differ for just one parameter (e.g. dose of the gain layer, by keeping the implantation energy to a maximum) and tune the parameters of their simulations to fit the results.

2.5 p-spray

The gap between pixels is covered by an oxide layer. It is well known that fixed positive oxide charges naturally present at the interface and into the oxide itself induce an electron layer at the oxide/silicon interface. This layer shorts the n^+ pixels unless a boron layer, compensating for the electron accumulation layer, is placed in the gap. This problem is present in all silicon sensors and it is solved by implanting either a patterned layer around each pixel (p-stop) or a uniform layer (p-spray) all over the surface, usually at the beginning of the process. The p-stop is generally more doped, by about one order of magnitude, than the p-spray [22]. In LGADs the situation is slightly different, because the p-spray implanted in the active areas (i.e. above the gain layer) would interfere with the gain layer, being both p-type. One approach is to pattern also the p-spray in a fashion very similar to the p-stop case, and implant it just from JTE to JTE of adjacent pixels, while keeping its standard implantation dose, as shown in **Figure 2**. Being a very low dose implant (order of 2 10^{12} cm^{-2}), the p-spray can touch or be even embedded in the JTE, without the risk of breakdown. On the other hand, being that the p-stop is more doped, there must be a distance between the

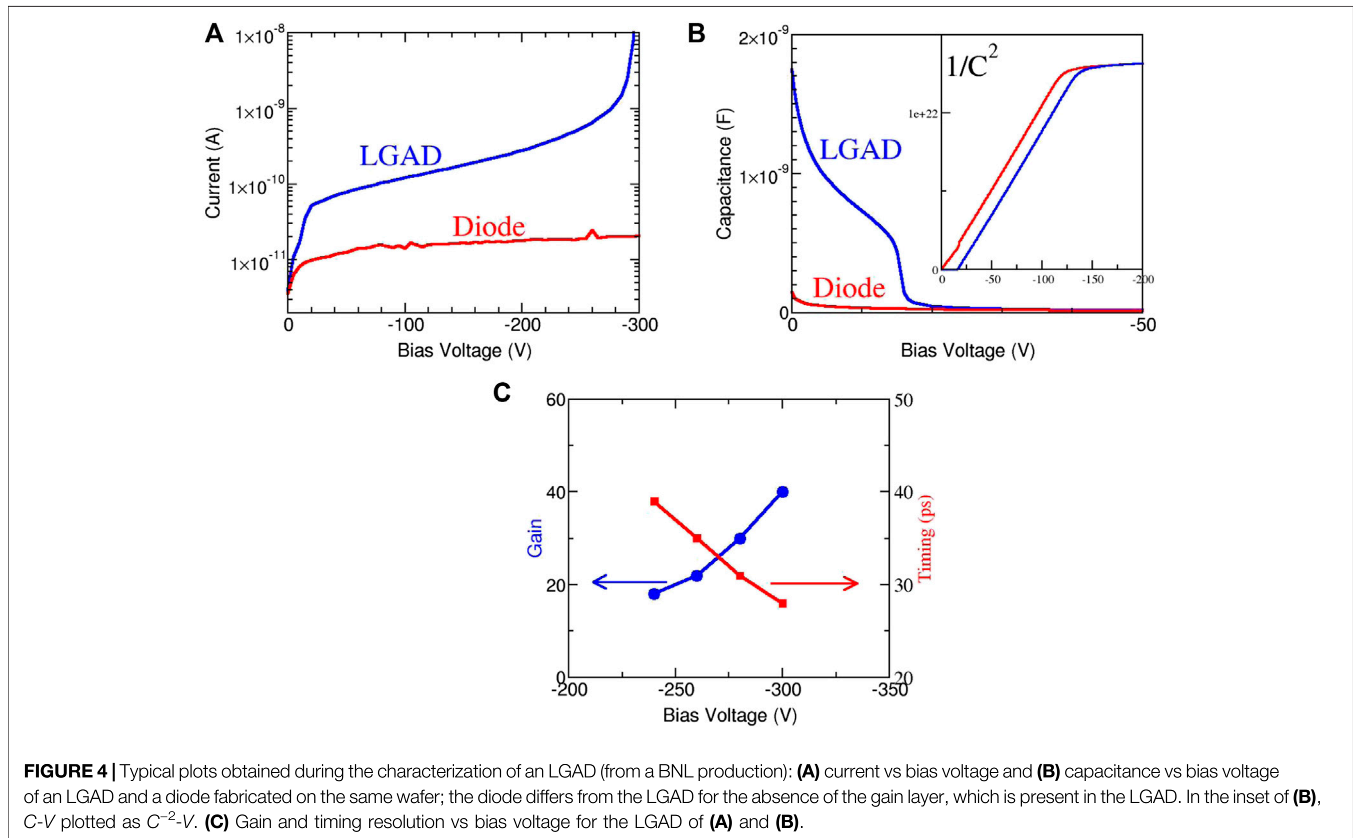

FIGURE 4 | Typical plots obtained during the characterization of an LGAD (from a BNL production): **(A)** current vs bias voltage and **(B)** capacitance vs bias voltage of an LGAD and a diode fabricated on the same wafer; the diode differs from the LGAD for the absence of the gain layer, which is present in the LGAD. In the inset of **(B)**, *C-V* plotted as C^{-2}-*V*. **(C)** Gain and timing resolution vs bias voltage for the LGAD of **(A)** and **(B)**.

JTE and the *p*-stop to avoid breakdowns. The distance increases the dead-areas of the LGADs, as discussed in the following sections.

3 ELECTRICAL CHARACTERIZATION OF LOW-GAIN AVALANCHE DIODES

After the completion of an LGAD fabrication batch in clean room, a static electrical characterization at the probe station follows. It is useful to place diodes and LGADs close-by on the same wafers. The devices should be perfectly identical, save of course for the presence of the gain layer in the LGAD. A current-voltage curve as the one reported in **Figure 4A** clearly shows the difference between the two devices. In the diode case, the I-V measures the leakage current dominated by the thermally-generated carriers in the deplete silicon bulk (surface currents are negligible), while for an LGAD this current is amplified by the gain layer. At high voltages, the electric fields between n^+ and gain layer are high enough to trigger the impact ionization for the holes, resulting in an avalanche breakdown (in the case reported in **Figure 4A** this happens at 300 V). Notice that at low voltages, below a few tens of volts, the gain layer is not depleted and the LGAD current is very small. At depletion of the gain layer, the LGAD current jumps up, giving a good estimate of the voltage at which the gain layer depletes. A better evaluation of it can be achieved by performing a capacitance-vs-voltage measurement, as the one shown in **Figure 4B**. While the gain layer is not yet depleted, the capacitance is very high; at the bias voltage at which it depletes a sharp drop in the capacitance happens (about 18 V in the figure): this feature in the curve C-V is commonly referred to as “foot”. Plotting the capacitance as C^{-2}-V, it is even more apparent where the foot voltage is: it is the voltage at which the curve starts rising linearly from zero. Note that the C-V of the LGAD is translated from the C-V of a diode simply by the foot voltage. From the C-V one can also extract the doping profile of both the gain layer and the substrate. In the devices considered in the figure, the doping concentration of the substrate is uncommonly high (about 7.10^{13} cm^{-3}, translating in a depletion voltage of 140 V); usually the doping concentration of the substrate is much less, order of 10^{12} cm^{-3}, as in any High-Resistivity (HR) substrate.

Functional characterization of an LGAD includes evaluation of the gain and timing resolution vs bias voltage (**Figure 4C**). This can be done by connecting the device to a fast transimpedance amplifier read-out circuit and exposing the detector to a beam of mips (in laboratory, these are provided by a ^{90}Sr beta source, for example). From the area of the current pulses, once the gain of the electronics has been calibrated, the gain can be extracted. For the timing, at least another device (a scintillator system or another LGAD) of known timing resolution has to be used. Mips are made crossing through all the devices and coincidences are looked at. The timing can be calculated with an off-line analysis. A gain in the order of a few tens is easily achievable before irradiation, while timing resolution, which strongly depends on the gain, can go a bit lower than 30 ps, for 50 μm thick devices.

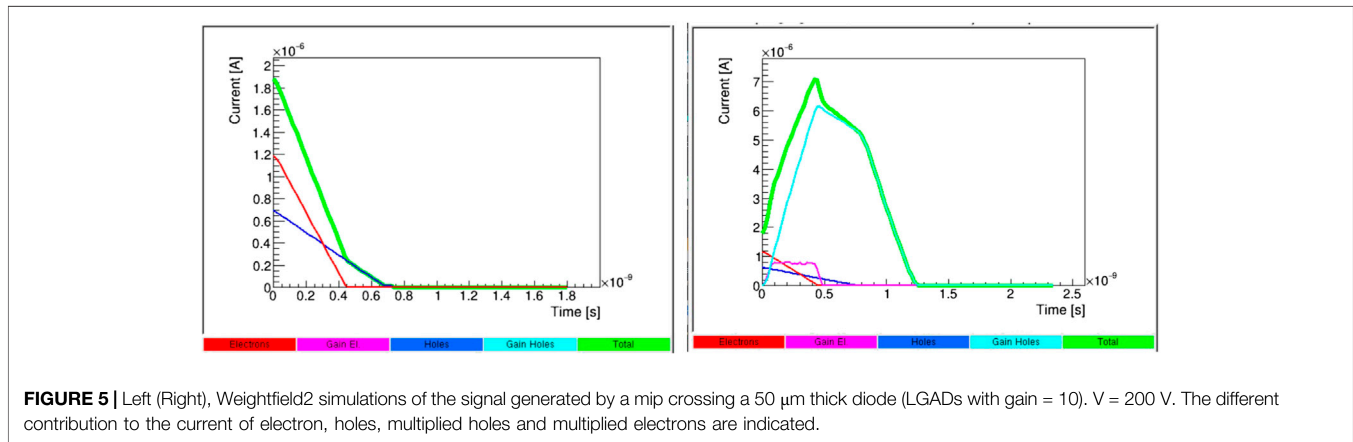

FIGURE 5 | Left (Right), Weightfield2 simulations of the signal generated by a mip crossing a 50 μm thick diode (LGADs with gain = 10). V = 200 V. The different contribution to the current of electron, holes, multiplied holes and multiplied electrons are indicated.

Figure 5 shows simulated signals generated by a mip vertically crossing either a diode or an LGAD, in this example having a gain of 10. The two devices are both 50 μm thick and are large enough to be considered, with good approximation, 1-dimensional devices. The simulations have been run using the software Weightfield2 [23]. Diodes exhibit a null rise time because the signal starts developing as soon as the carriers move into the bulk. The same is true for the LGAD whose initial part is generated by the same principle. In LGADs for later times, instead of decreasing with time as in the case of the diode, the signal increases because of the contribution of multiplied holes. It can be easily appreciated how most of the signal comes from the drift of the multiplied holes into the depleted substrate. Still, the full signal develops in about one nanosecond.

All electronics have a limited bandwidth that will introduce a non null rise time, also in the case of the diodes. Moreover, even front-end electronics with a large bandwidth, for example 1 GHz, will spread the relatively long signal of the LGAD signal further. As a consequence the signals of an LGAD or a diode will not be dramatically different, except of course for their amplitude. It must be noted that when reading at high speed, the noise varies as $\sqrt{B}$, B being the bandwidth and is large for a fast electronics. As a consequence, signals from diodes are beyond detection and only the gain provided by an LGAD makes the signal detectable.

An important parameter to have a fast signal is the electric field that is present into the substrate. While well below the threshold for impact ionization, it still needs to be high enough for the full signal to develop in a short time. For example, if multiplied holes have to drift 50 μm in less than one nanosecond, their drift velocity must be $v > \mu_h E = 5.10^6 cm/s$, and given the mobility of the holes μ_h, the electric field must be $E > 3.10^4 V/cm$. Considering the electric field constant, a voltage of 150 V must fall into the substrate. For operation at low temperatures, where the mobility and therefore the velocity are higher, this requirement is relaxed. But still, an operational voltage slightly in excess of 200 V (for 50 μm thick LGADs) is required for best performance. For thinner substrates, the voltage drop into the substrate scales accordingly to the thickness.

The importance of a high-enough electric field into the substrate is stressed by **Figure 6**, showing the total pulse currents (sum of the electron and hole contributions) in 1-D LGADs and diodes of different substrate thicknesses, and all biased at the same voltage of 200 V. An identical bias voltage makes the electric field higher, carriers faster and signal shorter (and therefore larger) in thinner devices. Differing from the case of diodes, in which in first approximation the amplitude is the same independently of substrate thickness, signal amplitudes in LGADs tend to decrease with thickness. On the other hand, if the same electric field was present into LGADs of different thicknesses, the current pulses would have the same amplitude [24]. In fact, the lower weighting potential in thick devices is exactly compensated by the larger charge deposited by the mip. The broader pulses in thicker devices are due to the longer time electrons and holes need to drift into the substrate and their integral accounts for the larger deposited charge. From **Figure 6** it can also be appreciated how, in LGADs, thicker substrates give origin to slower pulses which lead to worse timing resolutions.

5 TIMING IN LOW-GAIN AVALANCHE DIODES

As LGADs have been developed to address timing in mip detection, it is important to state the contributions to the total timing resolution (σ_t) and how this can drive choices in the layout and fabrication. The timing resolution of LGADs is defined by the following formula:

$$\sigma_t^2 = \left(\frac{\sigma_n}{\frac{dS}{dt}}\right)^2 + \sigma_{Landau}^2 + \sigma_{timewalk}^2 + \sigma_{ADC}^2 \quad (1)$$

To minimize the first two terms we can work on the LGAD properties, while the last two require efforts on the read-out electronics (front and back-end).

The first term is the jitter and accounts for the noise (σ_n) of the detector (LGAD + read-out electronics). It can be minimized with a good design of the front-end and by minimizing the input capacitance. The slew rate (dS/dt) can be increased using large signals (i.e. large gains) and thin substrates biased at voltages high-enough to achieve carrier velocity saturation, as the signals shown in **Figure 6** suggest.

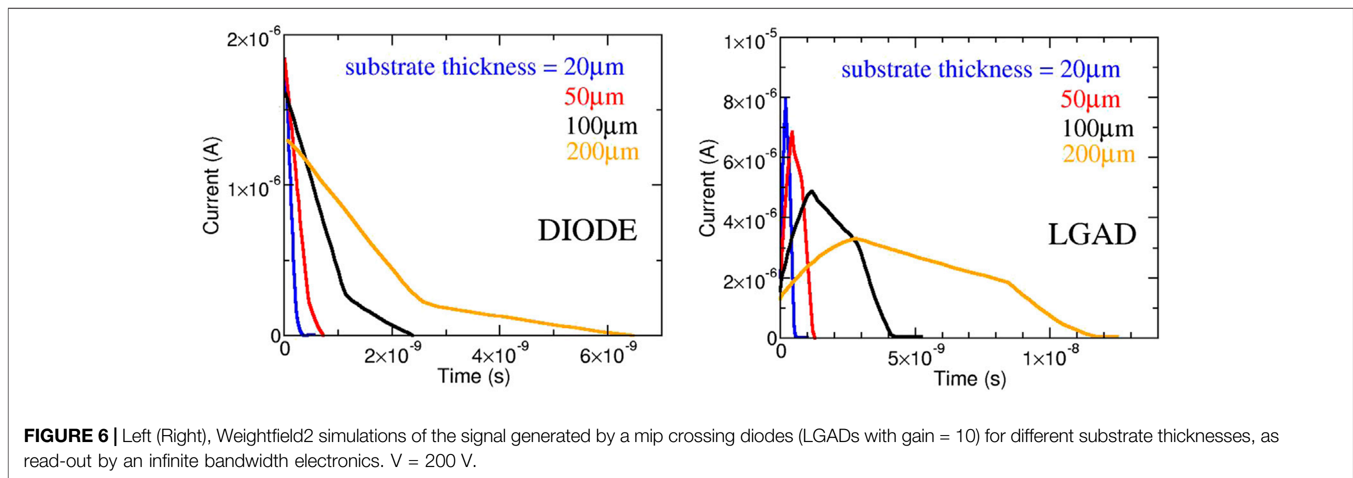

FIGURE 6 | Left (Right), Weightfield2 simulations of the signal generated by a mip crossing diodes (LGADs with gain = 10) for different substrate thicknesses, as read-out by an infinite bandwidth electronics. V = 200 V.

The Landau noise (σ_{Landau}) is due to the not-uniform generation of charge along the track of the mip, which generates a certain number of electron/hole pairs per micron of silicon that fluctuates around an average amount of 80. Thin substrates exhibit a lower Landau noise. With good electronics in a system where power consumption is not an issues, this is the dominant term. 3D sensors featuring electrodes perpendicular to the surface and therefore parallel to the mip direction, do not suffer from such noise source [25], although only in the particular case of particles crossing parallel to the columns. In this case, they can therefore be intrinsically faster than LGAD, at the price of an increase capacitance.

The time-walk noise is due to the statistical distribution of the signal amplitudes that are derived from the Landau distribution of the charge generated by the mips and the fluctuations in the gain. If the trigger is set at a certain threshold, then signals are detected after different times with respect to the time of arrival. While fast signals are less prone to this error, we can get rid of this effect by applying the Constant Fraction Discrimination method, in which normalized waveforms are triggered.

The last term takes into account the finite binning capabilities of the ADC. Usually this term can be made negligible.

Timing measurements performed with low-noise front-end electronics and sophisticated post processing, which therefore make the terms $\sigma^2_{timewalk}+\sigma^2_{ADC}$ negligible, show how σ_t is a strong function of the gain and reaches, for gains generally larger than 20, an asymptotic values due to the term σ_{Landau}. For 50 micron thick LGADs, as shown in **Figure 4**, this values can go lower than 30 ps, while for 20 micron thick devices it goes down to 15 ps.

6 LOW-GAIN AVALANCHE DIODES FOR ATLAS AND CMS

Both CMS and ATLAS experiments are upgrading their detectors adding a timing sub-detector to help resolve the tracks originating from the many vertexes expected in one bunch crossing: they are the MIP Timing Detector for CMS [26], placed in its Endcap Timing Layer (ETL), and the ATLAS High Granularity Timing Detector (HGTD) [27]. They are required to give a 30 ps timing resolution per track over the full lifetime. This task, which is hard to be accomplished by a single layer, can instead be achieved by having n sensitive layers, therefore having the timing resolution scaling as $\sqrt{n}$. This translates to a requirement of 52 or 60 ps/hit in the case of three or four independent timing measurements along the particle path [28]. This resolution is achievable with an LGAD of 50 μm active thickness or lower and until a fluence of about $3.10^{15} n_{eq}/cm^2$ is reached. After that the timing resolution of the LGAD has been measured to degrade to a value less than 60 ps, at which time a replacement detector is needed. The sensor pad size is driven by occupancy, pad capacitance, and the fill factor (FF). A unified pad size of 1.3 by 1.3 mm^2 in all detectors with an expected capacitance of 3.4 pF is found to fulfill the requirements. The pads will be arranged in arrays that take up a total area of about 20 by 40 mm^2 (15 × 30 pixels for ATLAS and 16 × 32 pixels for CMS) with a common backplane bias voltage connection.

CNM was the foundry that first started the fabrication of prototype thin LGADs in 2016, within an RD50 Common Project, for the ATLAS HGTD. They were fabricated on 4” wafers with 50 μm thick active area. The initial substrate was a silicon-on-insulator (SOI) type, with the back-side contact done through the inactive silicon wafer by means of deep wet-etch trench going through the insulator, however they later used Si-on-Si wafers. Splittings of the implantation dose for the multiplication layer were done, ranging from 1.8–2.0 10^{13} cm^{-2}. Such a high doping concentration was due to the long diffusion time at high temperature used by CNM to anneal the gain layer.

For both experiments, Hamamatsu Photonics (HPK) is delivering LGAD sensors manufactured on Si-Si bonded 6” wafers of 150 μm total thickness with a 35, 50 or 80 μm thick high resistivity float zone (FZ) active layer. Samples with different gain layer doses were produced, sharing the layout, to study the optimum parameters of the charge multiplication mechanism. Eventually a convergence toward 50 μm thickness has been reached. In the wafer layout, for test purposes, circular or square single channel devices have been inserted. Also small arrays are present, differing for the no-gain gap between the pixels.

FBK [29] has produced structures with different interpad distances and widths of the isolation *p*-stop implants, which are

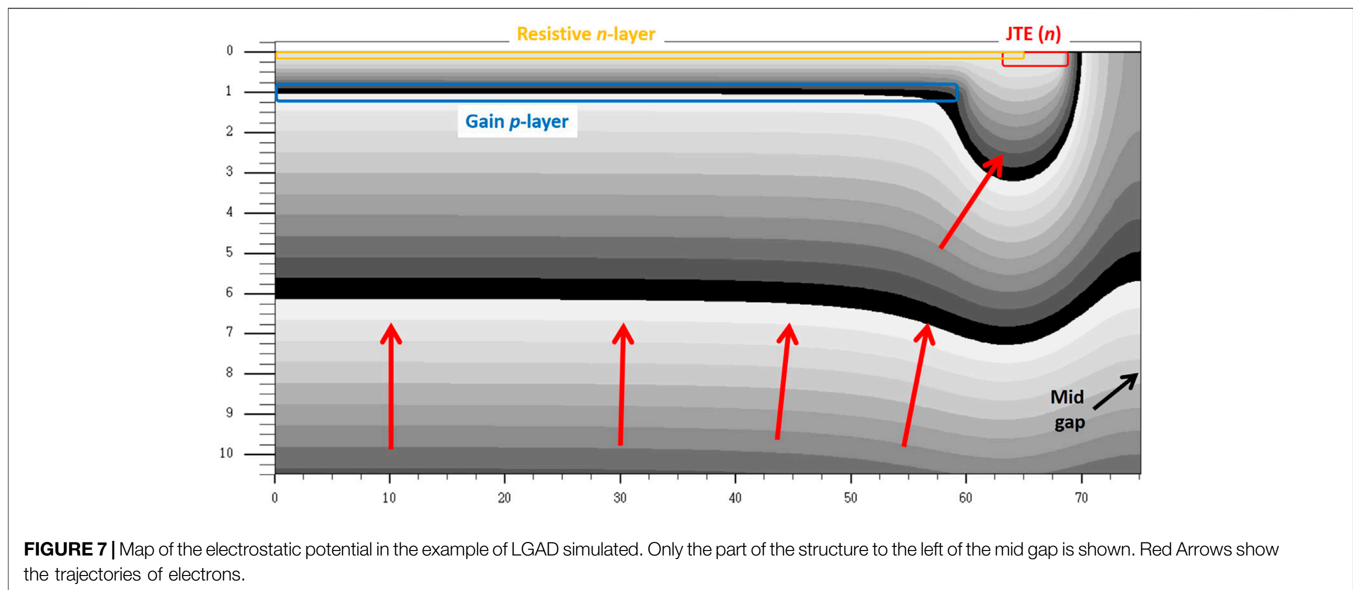

FIGURE 7 | Map of the electrostatic potential in the example of LGAD simulated. Only the part of the structure to the left of the mid gap is shown. Red Arrows show the trajectories of electrons.

aimed at maximizing the fill factor while keeping good isolation between pads. Besides doing several splittings of the gain layer dose to optimize the performance, they engineered the gain layer as to make it more radiation resistant. In some splittings, the boron of the gain layer has been replaced by gallium, in others a carbon implantation has been added to the gallium or boron implant. If on one hand doping with gallium resulted in a worsening of the overall performance, the carbon co-implantation seems to result in an increased radiation resistance while keeping the same timing performance, at the expense of an increased leakage current.

Recently, also IHEP-NDL has joined the effort of prototyping of LGADs structures (single pixels and arrays) for the ATLAS HGTD [30].

7 LIMITATIONS OF LOW-GAIN AVALANCHE DIODES

With the help of **Figure 7** let's consider what happens at the border of an LGAD pixel. The figure reports the electrostatic potential map of a 2-D LGAD, 50 μm thick. To simulate the interpixel capacitance and the charge sharing between two adjacent pixels, a pixel on the right of the one shown in figure has been included in the simulation. Being the two pixels identical, the boundary line at X = 75 μm is an axis of symmetry for the device. Far away from the JTE and well within the gain layer, electric field lines are vertical and parallel to each other. Electrons generated here drift to the n^+ and get multiplied as expected. If mips pass outside the gain layer (for X larger than 60 μm in this example), the generated electrons are collected by the JTE and are not amplified. For mips passing through this region, an LGAD behaves as a diode (gain = 1) and the signals will most likely be under the threshold for detection with fast electronics. There is an intermediate region where the electric field lines point to the JTE, so that electrons are partially collected here and do not go through the gain layer: the signal is subjected to a partial amplification. In **Figure 8** the current pulses and their integrals (i.e. total collected charge) generated by mips crossing at different X is plotted. In the LGAD, the signal generated by a mip crossing outside the gain layer is not different from the signal generated by a mip crossing at the center of a diode. Mips crossing close to the end of the gain layer (the gain layer in this example ends at X = 60 μm) give origin to a smaller signal, but still no net charge is collected by the nearby pixel. At X = 75 μm, which is mid gap, the same signal is induced in both pixels and the charge is shared between the two. This example makes apparent that a dead region at the border of an LGAD pixel exists, which can easily be larger than 20 μm. Fine pitch strip and pixels, with pitches in the order of 100 μm, are therefore excluded in the LGAD basic technology as the dead areas will be intolerably large. For example, LGADs to be used by either CMS or ATLAS have a pitch, as said above, of 1.3 mm.

To minimize the problem and still use the standard technology to fabricate an LGAD, one can use some design or system features. One can design the JTE as narrow as possible, or design the gain layer tip close to the JTE, or even use *p*-spray instead of *p*-stop to have the pixels closer. A high voltage tends to straighten the electric field lines and, therefore, increase the active area. Bringing the pixel closer usually means an increase to the interpixel capacitance which, due to the fast read-out, will add to the noise. In the next subsection we will see how this increase is negligible for an LGAD.

7.1 Capacitance of an Low-Gain Avalanche Diode

For a 1 × 1 mm LGAD fabricated on a 50 μm substrate, its capacitance toward the back is 2 pF. The simulations reported in **Figure 9** show that, also in the case of a gap of 20 μm, the interpixel capacitance for a 4 mm perimeter is about 0.2 pF, which is much less than the contribution of the capacitance toward the back. It is interesting to see how the interpixel

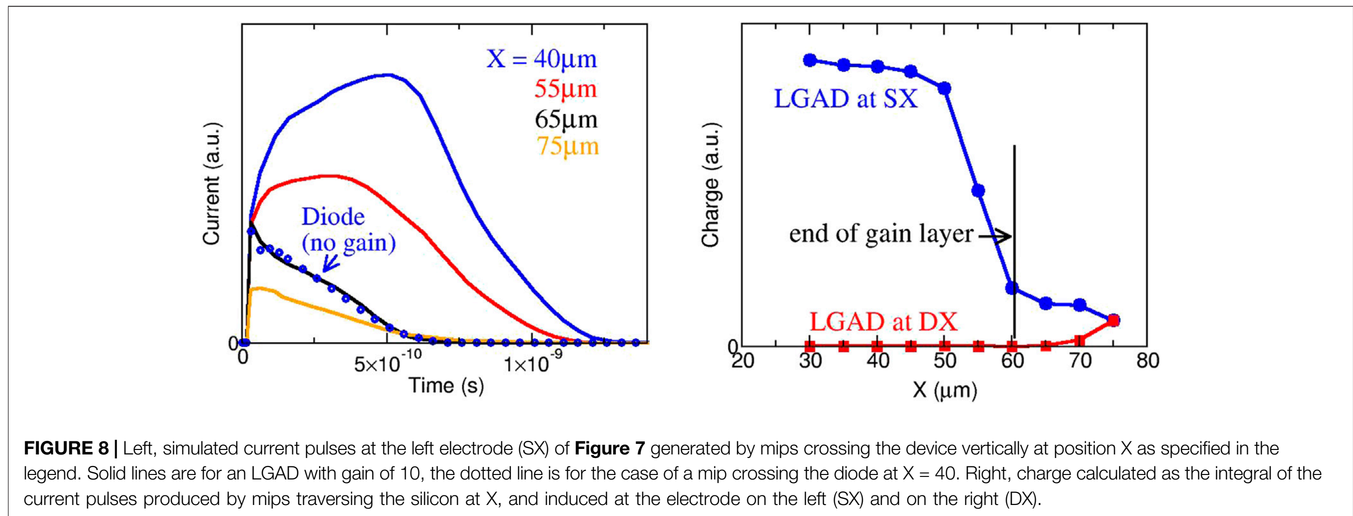

FIGURE 8 | Left, simulated current pulses at the left electrode (SX) of **Figure 7** generated by mips crossing the device vertically at position X as specified in the legend. Solid lines are for an LGAD with gain of 10, the dotted line is for the case of a mip crossing the diode at X = 40. Right, charge calculated as the integral of the current pulses produced by mips traversing the silicon at X, and induced at the electrode on the left (SX) and on the right (DX).

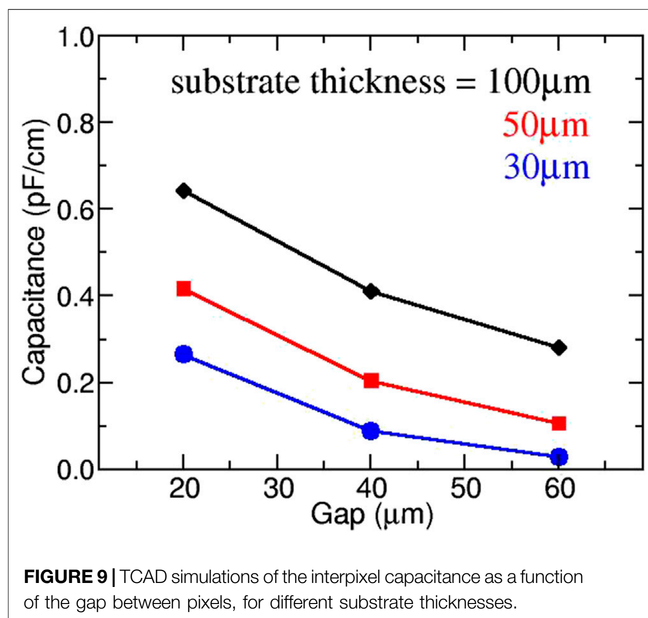

FIGURE 9 | TCAD simulations of the interpixel capacitance as a function of the gap between pixels, for different substrate thicknesses.

capacitance is strongly dependent on the substrate thickness. This happens because the substrate acts as an electrostatic shield from one pixel to the other and the shield is as more effective as it is closer to the pixels. The simulations consider the gap as depleted, which is usually not the case, being *p*-spray or *p*-stop is present. These resistive layers cause a long-range capacitive coupling between far-away pixels, which increases the interpixel capacitance. However, this contribution is frequency dependent and expected to be unimportant at high frequencies.

7.2 Radiation Hardening of Low-Gain Avalanche Diodes

To some extent, LGADs need to be radiation hard to be used in HEP experiments. Several irradiation campaigns clearly pointed out how the gain decreases with hadron fluence (proton irradiation being more damaging than neutron irradiation) [31]. The gain almost vanished at irradiation fluences of about $10^{15}\,cm^{-2}$. The effect is attributed to the effective acceptor removal in the gain layer [32]. By means of SIMS measurements [33] it has been shown that the boron ion is in the same position as before irradiation, and most likely inactivated by becoming interstitial and forming defect complexes with oxygen. To counteract this effect, two strategies have been tried: 1) replace the boron implant with gallium implant, and 2) implant a carbon spray over the gallium or the boron. The first option is motivated by the fact that the gallium atom may hardly form complexes, being less mobile than silicon. The second option is motivated by the fact that carbon can intercept interstitial silicon, and form Si-C complexes, which have been observed in irradiated silicon. It is measured [33] that a carbonated gain layer is at least a factor of two more radiation resistant than the equivalent non-carbonated gain layer, while gallium doping is less radiation resistant than boron doping.

Furthermore, narrower gain layer implants are more radiation resistant than wider implants due to the higher boron peak concentration of the former, suggesting to keep the annealing of the gain layer as the last thermal step of the process flow while keeping the temperature to a minimum (about 700–800°C).

Another important aspect of radiation hardness of LGADs is their leakage current. In unirradiated devices, the bulk thermally generated leakage current is approximately multiplied by the gain factor. During exposure to irradiation, the gain decreases, so the increase in leakage current is mitigated by the decrease of multiplication. A thin substrate will eventually have a leakage current close to the leakage of a standard, thicker device without amplification.

Furthermore, thinner LGADs (less than 50 µm) are more radiation resistant than thicker ones: while the gain layer contributes less to the electric field because of the acceptor removal process, acceptors are created in the bulk by the radiation. By increasing the bias, in parts of the substrate the electric field can reach the threshold for impact ionization and compensate for the gain layer.

8 TOWARDS 4D SENSORS

As discussed in previous sections, pixel dimensions must be by far larger than the substrate thickness to have a uniform multiplication and to maximize the fill-factor. With the current LGAD designs, position resolution in the order of 10 μm, as needed in 4D detectors, is out of reach. Other structures, still based on LGADs, can be developed to have both high spatial and timing resolution. In order to obtain a uniform amplification throughout the whole sensor area, together with high spatial resolution, it is possible to move the n^+ and gain layer on one side of the wafer (i.e. the top of the wafer) and the hole collecting electrodes to the opposite side (i.e. the bottom of the wafer) [13, 34]. The hole-collecting electrodes can be placed at a small pitch, without compromising the uniform multiplication occurring at the opposite side of the wafer. To safely process double-sided wafers it requires a wafer thickness of about 200 μm for 4" wafers, and thicker for 6" wafers. Such thicknesses will spoil the timing capability of the LGAD. As an example, the structure can be used for soft X-ray detection where timing information is not crucial.

Another solution to increase the fill factor, but without reaching 100%, is to separate the pixels by small trenches. In this case, pixels can be very close, order of 5 μm, since trenches can be narrower than 1 μm. A trench depth of a few microns is enough for this purpose and it is easily achieved since trenches with aspect ration of 20:1 are fairly common. Moreover, the JTE can be removed since trenches prevent the formation of high electric fields at the edge of the n^+. This solution has been implemented by FBK [35], reaching a dead area of only 7 μm between pixels, and has been addressed as "Trench-Isolated LGAD" (TI-LGAD). In their technology, segmented LGADs with pixel pitch down to 50 μm feature a fill-factor higher than 75%. The same parameters for the ion implantation dose and energy of the doped regions, as well as the thermal budget, used in standard LGAD productions are applied to fabricate the TI-LGADs. No detrimental effects due to the introduction of the trench have been experimentally observed.

A third solution will be discussed extensively in the following section: it is the AC-coupled LGADs (AC-LGADs for short), also called Resistive Silicon Detectors (RSDs), and is sketched in **Figure 10** [36, 37].

9 STRUCTURE OF AN AC-LOW-GAIN AVALANCHE DIODE

The AC-LGAD consists of a uniform gain layer that, as in the standard LGAD, is implanted deep below the n-implant: these two layers run seamlessly overall the active area [38]. The JTE is implanted at the border and within it a high-dose n^+-implant can be present, which is grounded during operation to drain the leakage current as well as the multiplied signal electrons. A main difference is that, in the AC-LGAD, the large uniform n-implant is about 10 or 100 times less doped than the n^+ implant of a standard LGAD. Its sheet resistivity is therefore much larger. The gain layer is implanted in the usual way as in the case of the LGAD, its tip can be either embedded in the JTE or stopped at a certain distance from it. Because of the relatively low implantation dose of the n implant, a non-negligible part of the n implant is depleted by applying the operation voltage. This results in the gain layer being effectively deeper (since the depth is measured from the undepleted n implant). As such, the ionization integral is higher for the same doping of the gain layer (i.e. same electric field) which lowers the value of the breakdown voltage compared to that of an LGAD which uses the same gain implant parameters. Therefore, it is necessary to re-calibrate the dose of the gain layer by lowering as much as needed to have a desired breakdown voltage. Notice that this calibration must be conducted for each new dose of the n-implant, although TCAD simulations can help in the selection of the correct dose once they are correctly tuned on the particular process used and reliable.

The n-implant is covered by a thin dielectric layer which is typically silicon oxide, silicon nitride, or both, while remaining grounded through a contact at its border. Over the dielectric, there are finely patterned metal electrodes (of arbitrary shape) visible in **Figure 11**, which will be connected to the read-out electronics. Signals are generated in the usual way and they induce a current pulse to the metal electrodes through the capacitance, whose parallel plates are defined by the metal electrodes and the n^+. A 100% fill factor is achieved, with uniform multiplication and no dead areas. Since the metal electrodes are separated from the n-layer by an insulator, they do not collect charge and the signal pulse is bipolar. Since two neighbor electrodes see, through the capacitance, a small resistance between them (due to the n layer), the pixels experience an important cross-talk. On one hand, this increases the position resolution by interpolation. On the other, it increases the occupancy. These effects must be carefully considered when designing the system, especially when a high count rate is expected.

There are a few components which are common in LGADs and AC-LGADs, i.e. the substrate, the JTE and the p-spray. The JTE is still placed at the border of the n-implant that defines the active area, while the p-spray is external to the active area and serves to insulate the JTE from the guard ring termination.

10 PULSE SHAPE IN AC-LOW-GAIN AVALANCHE DIODES

In an AC-LGAD, the signal develops in a very similar fashion as in a standard DC-coupled LGAD, with mip-generated electrons crossing the high-electric field and undergoing impact ionization. Multiplied holes then drift towards the substrate, generating most of the signal. In AC-LGADs, however, once electrons arrive at the n-implant they are not immediately collected by the read-out electronics. Instead they continue to generate signal as they move within the n-implant towards the n^+ electrode at the border. The resistive n-implant can be seen as a distributed RC network, made by capacitances towards the back and toward the AC-coupled metal electrodes. These capacitances are connected by resistances which account for the finite resistivity of the

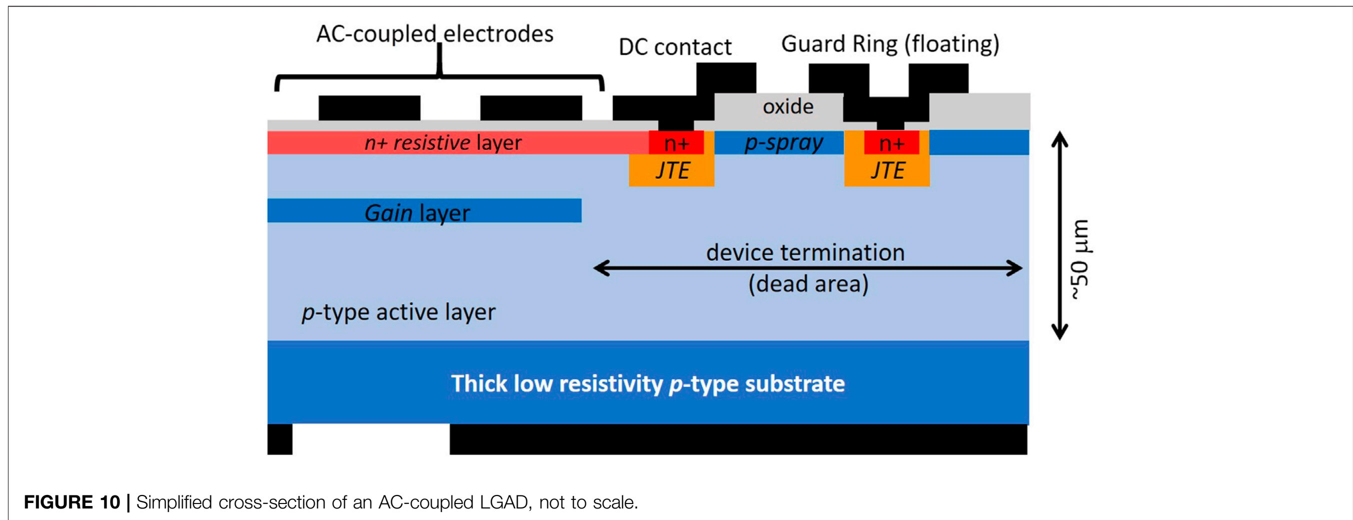

FIGURE 10 | Simplified cross-section of an AC-coupled LGAD, not to scale.

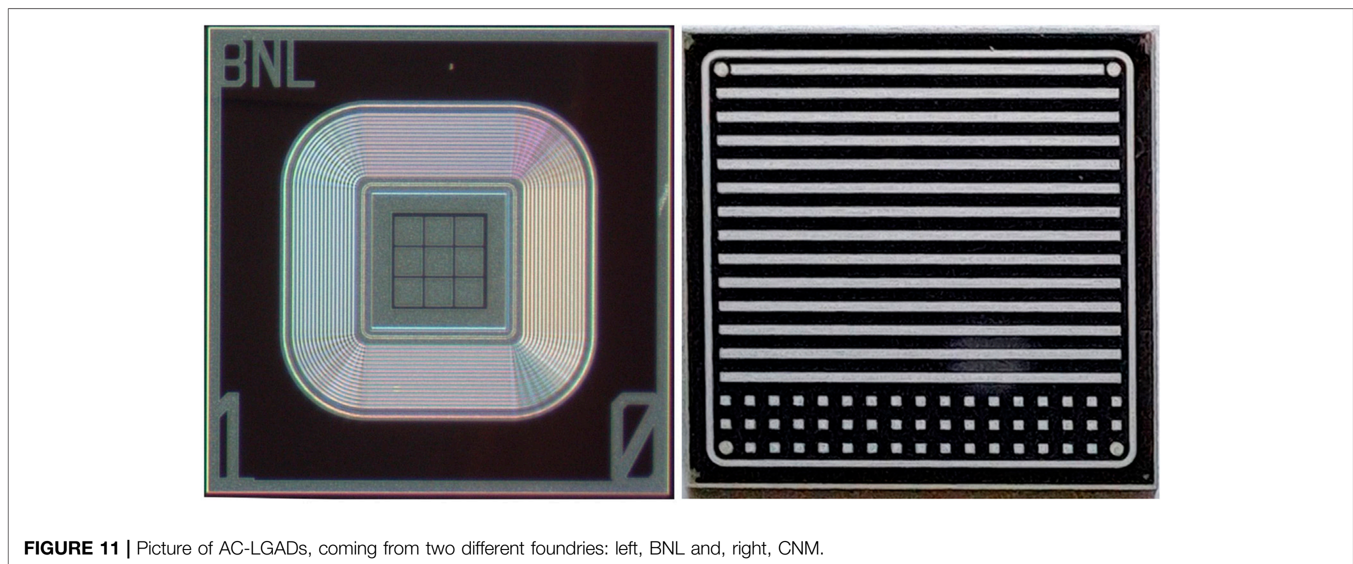

FIGURE 11 | Picture of AC-LGADs, coming from two different foundries: left, BNL and, right, CNM.

n-implant. Capacitances and resistances can, up to a certain extent, be tuned by means of the technology process flow. A large capacitance, for the same area of the AC-coupled electrodes, can be obtained using a thin insulator whose ultimate thickness is limited by the critical electric field that the insulator can stand. A large resistance, beside separating by design the metal electrodes, can be obtained by using a low-dose implantation for the *n*-layer. To avoid a full depletion of the *n*-layer, its dose must be larger than the integral of the acceptor concentration in the bulk, which include the *p*-type gain layer and the *p*-type substrate. The latter contribution is usually negligible. A minimum implantation dose for the *n*-implantation of about $1.10^{13} cm^{-2}$ is therefore needed.

For illustration purposes, a simplified 2-dimensional AC-LGAD structure has been numerically simulated, featuring five AC-coupled electrodes at a pitch of 100 µm and a grounded contact at the edge of the device. The value of the gap between two neighbour AC-coupled metals and the implantation dose of the *n*-layer have been varied. A mip vertically crosses the silicon in the middle of the device, at the center of the electrode labeled "hit strip" in **Figure 12** and in **Figure 13**, where some results are presented. It has been verified that the signal at the substrate is independent on the explored range of parameters (once the AC-LGADs are operated at the same gain) and closely matches the signal induced in a standard LGAD.

In the simulated configuration that considers only the particular case of a mip crossing at the center of an AC-pad, the signal sees a capacitance "*C*" toward the metal electrode of the "hit strip" [$Z = (\omega C)^{-1}$] and a resistance "*R*" towards the neighbour electrodes. The current signal splits according to the ratio of the two impedances, as in a conventional current divider. For example, the fast drift of the multiplied holes is fed through "C" unless "R" is very low. Electrons, once arrived at the *n*-implant, freeze on a limited area because of the non-null resistance of the *n*-implant and then decay with time constant

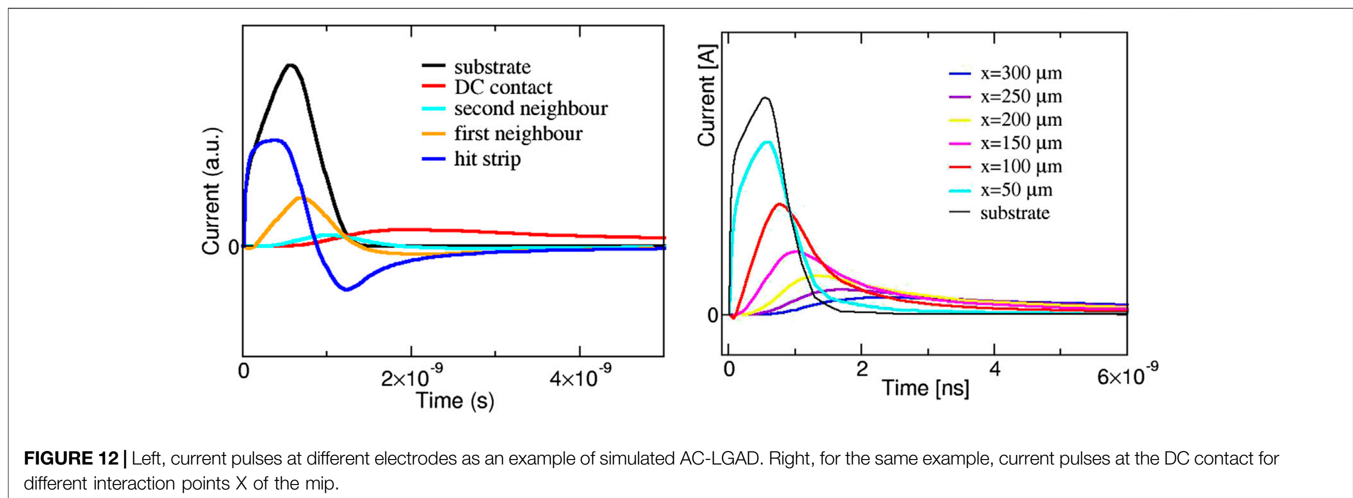

FIGURE 12 | Left, current pulses at different electrodes as an example of simulated AC-LGAD. Right, for the same example, current pulses at the DC contact for different interaction points X of the mip.

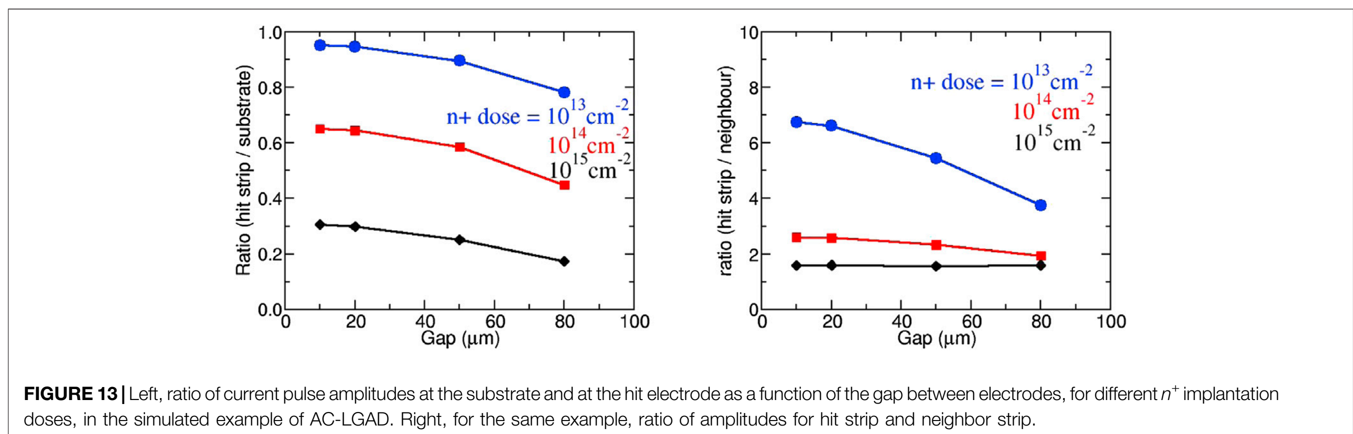

FIGURE 13 | Left, ratio of current pulse amplitudes at the substrate and at the hit electrode as a function of the gap between electrodes, for different n^+ implantation doses, in the simulated example of AC-LGAD. Right, for the same example, ratio of amplitudes for hit strip and neighbor strip.

RC. The motion of the electrons toward the n^+ contact, with the time constant RC, accounts for a negative lobe in the current pulse. It is found that the ratio $V_{hit-Strip}/V_{Substrate}$, with $V_{hit-Strip}$ being the pulse amplitudes at the hit strip and similarly $V_{Substrate}$ the pulse amplitude at the substrate, depends on the *n*-implant doping concentration, and decreases as the dose is increased. In fact, by increasing the dose, the effective interpixel resistance *R* decreases as it becomes comparable to $(\omega C)^{-1}$. A larger share of current is therefore induced at the nearby metals. An increase of the cross-talk is also calculated, which come at the price of lower signals at all electrodes. The effect of the gap is also visible. By reducing the gap, "R" decrease but at the same time "C" does not: the two effects compensate and a weak dependence on the gap is calculated showing that a pitch-to-gap ratio of 1:1 should be adequate in most applications. Further work is in progress aiming to optimize the geometry of the AC-pads. The signal formation in AC-LGAD itself is still debated and more rigorous study is needed to address the topic.

10.1 Considerations on Timing on AC-Low-Gain Avalanche Diodes

The current signal at the substrate is unipolar and essentially identical to the signal delivered by an LGAD, since electrons slowly moving within the *n* layer are far away from the substrate and marginally contribute to its signal. Since current signals are induced in multiple AC-coupled electrodes, for the same gain the signals at these electrodes necessarily have lower amplitude than in LGADs. Being the signals smaller, the jitter noise term in an AC-LGAD is therefore larger. Moreover, signals at neighbor strips, besides featuring smaller amplitudes, have longer rise times because of resistive effects. This produces even smaller slew rates and makes the jitter term much higher for these strips. On the other hand, profiting from the unavoidable presence of cross-talk, one can take the signals from two or more electrodes and average their time stamp. The timing resolution, in the case of equal noise contribution from the *n* different strips, scales as $\sqrt{(n)}$. However, for the sensor tested in [39], no significant improvement to the time resolution has been observed when combining measurements from multiple strips in the same cluster [39] which indicates that the former effects dominate.

10.2 Signal at the DC Contact

The DC contact to the n^+, which may be embedded into the JTE at the border of the active area, serves as drain for the leakage current and for the signal electrons. **Figure 12** shows interesting properties of the signal at the DC contact. Due to the RC network

introduced by the *n* implant, the amplitude of the signals at the DC pad decreases as its distance from the hit coordinate increases. Being the total collected charge is the same and independent from the distance, the smaller signals are broader. Timing resolution associated with this electrode is therefore very poor. On the other hand, mips that hit the active area very close to the DC contact originate pulses very similar to a DC-LGAD, and can therefore be used for gain estimation.

11 DISCUSSION

Leveraged by the interest of the HEP community in its fast timing performance, LGADs have reached an advanced stage of maturity. The physics reach of two mayor experiments in HEP (ATLAS and CMS) critically depends on the performance of meter-squared detectors based on this technology. A few foundries around the world are active in the development of the device, pursuing slightly different approaches in the fabrication but all converging toward the basic structure discussed above. During the years of research, several parameters have been explored, such as substrate thickness and doping of the gain layer, allowing an optimization and a deep understanding of the response of the device. Performance of LGADs coming from different vendors are very similar, although some process parameters such as the profile of the gain layer (mainly, the depth and, consequently, the dose) differ from one vendor to the other. Some other parameters are different as well, for example the depth of the JTE preventing early breakdown at the edges or the use of a *p*-stop rather than the *p*-spray, but the basic structure of an LGAD is essentially the same. A point of weakness of the device is its radiation tolerance, limited by the acceptor removal phenomenon which de-activates the boron of the gain layer, lowering the gain below the minimum value necessary to achieve a useful timing resolution. This limitation is particular severe in HEP experiments, where irradiation levels that destroy the gain are easily met. Some efforts are under way to extend the lifetime of the device by engineering the gain layer (carbon spray and low diffusion boron implant), and it is expected that a consistent effort in the LGAD R&D will focus on this topic in the near future.

Other lines of research equally originate from another fundamental limitation of the LGADs: their poor spatial resolution. In fact, LGADs are fabricated as large pixels (order of about 1 mm, much larger than the substrate thickness), thus preventing the possibility of having a device with very good spatial and timing resolution (a 4-D device). A device which has been conceived to solve this issue is the AC-LGAD (also called RSD). Its optimization is complicated by the fact that, besides the gain layer, also the *n*-layer plays a paramount role in its behaviour and the two implants are intertwined. An intense testing activity is necessary, and is under way, to characterize its performance. While radiation hardness of such devices has not been tested yet, it is expected to be at the same level as in the standard LGADs. 4-D detection is critical in other fields, such as X-ray detection or medical applications, and it may be that the development of such device (or other LGAD-based devices with different structures but similar capabilities) will be pushed from the outside of the HEP community.

AUTHOR CONTRIBUTIONS

The author confirms being the sole contributor of this work and has approved it for publication.

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Conflict of Interest: The author declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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