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Electronic global-shutter one-thin-film-transistor active pixel sensor array with a pixel pitch of 50 μm and photoconductive gain greater than 100 for large-area dynamic imaging

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In large-area dynamic imaging, an active pixel sensor (APS) is proposed. However, there is a trade-off between signal-to-noise ratio (SNR) and spatial resolution. To resolve this, a 256 × 256 active pixel image sensor array based on a 3-D dual-gate photosensitive thin-film transistor (TFT) is presented in this work, with a pixel pitch of 50 μm, pixel fill factor of 63%, photoconductive gain of 10^2–10^4 and spatial resolution of 505 ppi. An electronic global shutter is enabled by dual-gate biasing without additional a shutter TFT. Such an array is capable of dynamic imaging at a frame rate of 34 Hz.

KEYWORDS

large-area dynamic imaging, electronic global-shutter, one-TFT APS, sensor array, photoconductive gain

1 Introduction

Large-area optical image sensor manufactured by thin-film technologies can be found in numerous applications such as flat-panel X-ray detector and optical fingerprint scanning [1–11]. High sensitivity, high spatial resolution, and high speed of response are desirable particularly for dynamic imaging. Conventionally, a pixel consists of a photodetector (PD) and a thin-film transistor (TFT) switch in a passive pixel sensor (PPS) architecture. However, PPS is slow, suffers from low signal to noise ratio (SNR) and is incapable of supporting correlated double sampling (CDS) to remove the noise. To improve the SNR and enable the CDS, an active pixel sensor (APS) with an in-pixel amplifier is designed. APS integrates a PD with multiple TFTs

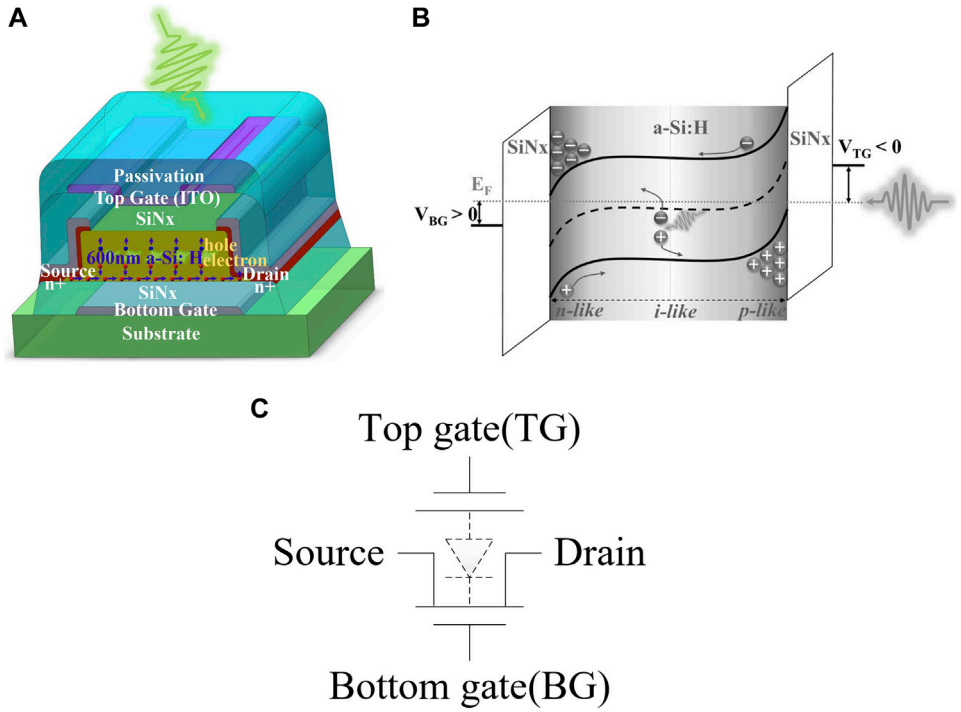

FIGURE 1
Diagram of pixel. **(A)** Pixel structure; **(B)** band diagram; **(C)** Equivalent circuit.

into one pixel. Consequently, it trades high SNR off against high spatial resolution and high fill factor [12–14]. The previous work reported one TFT APS aiming for high SNR, short sampling time, and high fill factor [15]. Even though it results in a decent increase in fill factor as opposed to the 3-TFT APSs, an integration capacitor is still needed to replace a reset TFT [15]. To take an image of a fast-moving object, a CMOS image sensor implements electronic global shutter. As for large-area dynamic imaging, a 4-TFT APS including one additional shutter TFT was proposed in the previous work [16]. However, it inevitably increases the pixel size and reduces the resolution. Despite all aforementioned efforts, the trade-off between SNR, fill factor, and spatial resolution still remains. To resolve the trade-off between SNR and resolution, we have proposed one-TFT APS concept for large area imaging applications [17–20]. This work presents an electronic global-shutter one-Thin-Film-Transistor active pixel sensor array with a pixel pitch of 50 μm and photoconductive gain greater than 100 for large-area dynamic imaging.

The design of the proposed sensor array is depicted in Section 2. The measured results and the performance summary are discussed in Section 3, and finally, we conclude this work in Section 4.

2 Design of sensor array

2.1 Pixel design of sensor array

In this work, we report an amorphous silicon (a-Si:H) TFT-based 256 × 256 image sensor array based on electronic-global-shutter one-TFT APS for high-resolution, high-sensitivity, and large-area dynamic imaging applications. Different from improving the spatial resolution by shrinking the TFT size in exchange for a smaller pixel, high resolution in this work is rather achieved by vertically embedding a PD and a switch to form a dual-gate photosensitive TFT.

The schematic pixel structure can be found in Figure 1A. In order to make the TFT photosensitive, a-Si:H channel layer is built in a three-dimensional (3-D) π-shape. Through externally biasing both gates, an internal electric field is created and accordingly separates photo-generated electron-hole pairs and makes the 3-D π-shape channel region become a “virtual” PIN-like PD as seen in the schematic band diagram in Figure 1B. The bottom-gate TFT is therefore PD-gated and its threshold voltage will be light-dependent due to quasi-Fermi level shift upon light exposure as shown in Figure 1B. Figure 1C is the equivalent circuit of the pixel. Such a 3-D dual-gate photosensitive TFT combines a PD, a storage capacitor, and a switch, making pixel fill factor of 63%. High spatial resolution

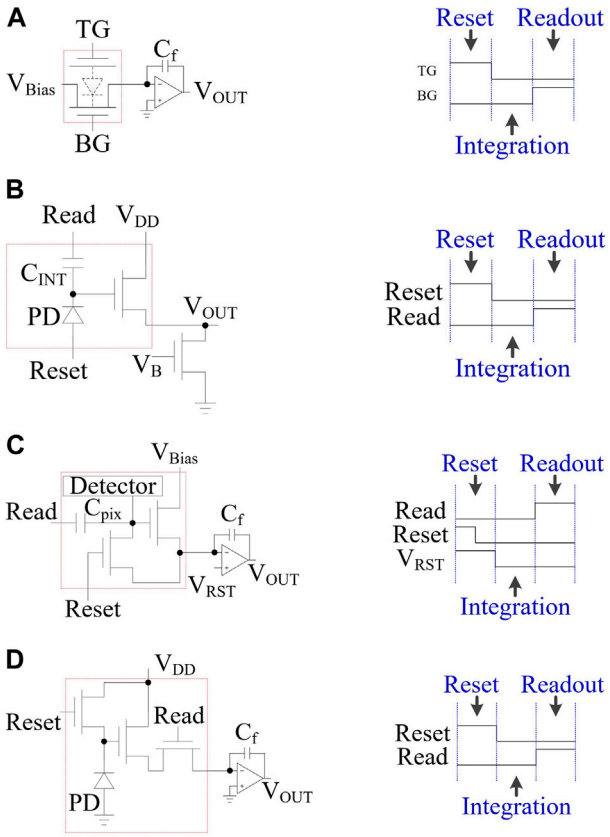

FIGURE 2
Architectures and timing of APS. **(A)** Proposed 1T APS. **(B)** 1T1C APS [15]. **(C)** 2T1C APS [13]. **(D)** 3T APS [14].

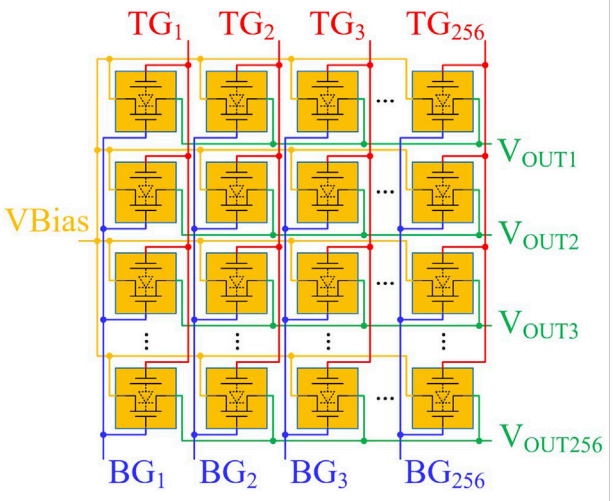

FIGURE 3
Diagram of sensor array.

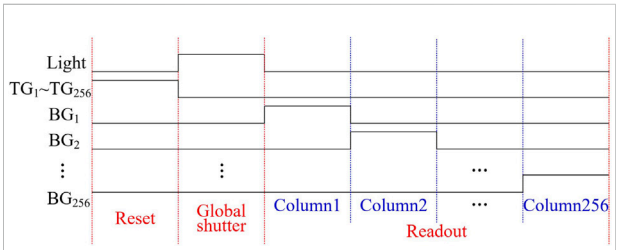

FIGURE 4
Timing diagram of electronic global shutter.

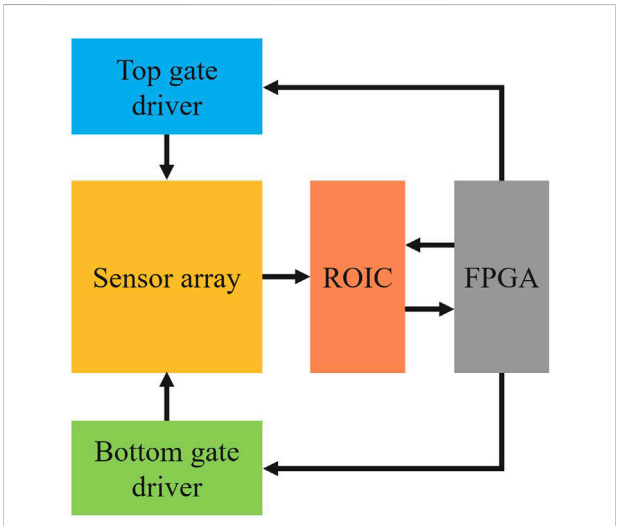

FIGURE 5
Block diagram of image acquisition system.

can be attained easily with only one TFT in the pixel. In this work, the image sensor array with 45 μm × 55 μm pixel size and 505 ppi resolution was successfully fabricated in an industrial G2.5 TFT-LCD mass production line.

2.2 Timing schemes of sensor array

Figure 2 plots the circuitry diagrams and timing schemes of the proposed one-TFT APS along with the other APS circuits. Similarly, the one-TFT APS presented in this work allows a three-phase pixel operation of reset, integration and readout and the CDS can be enabled by simply applying a reset pulse to the top gate for pixel resetting. The sampling time of the pixel is mainly governed by the resetting operation. Compared with the previous APSs, the proposed one-TFT APS removes the external reset TFT and the external PD as well, thus a reduced pixel sampling time is expected. With a small RC constant, the resetting in this pixel circuit can be done quickly, making it capable of very fast dynamic scanning.

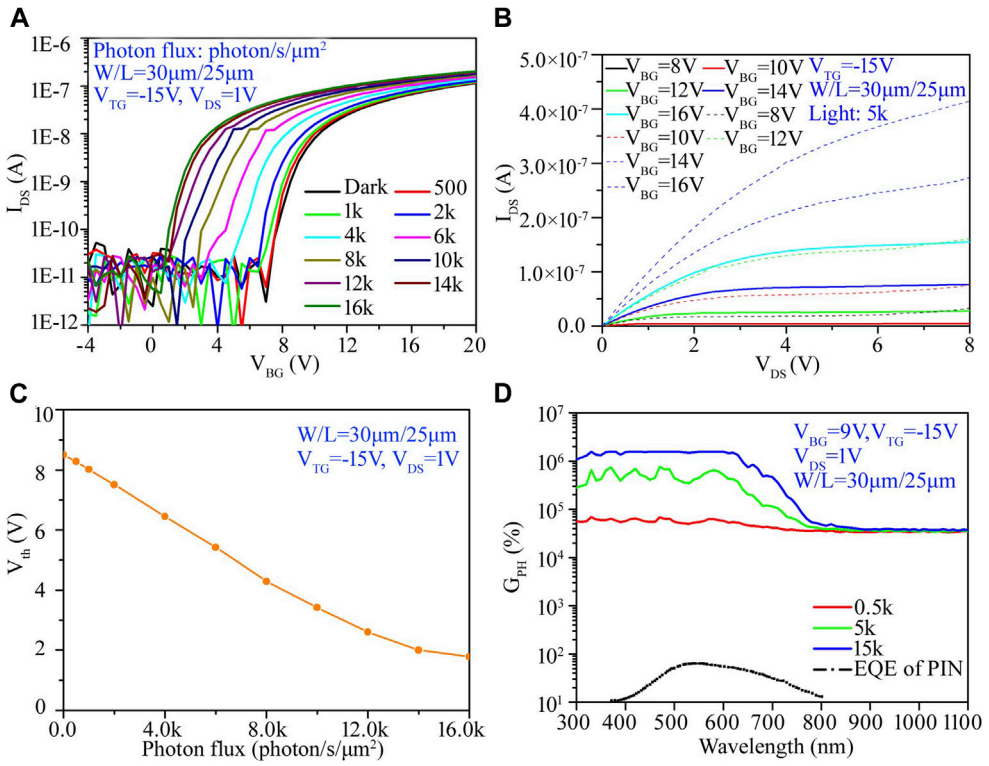

FIGURE 6
Characteristic curve of pixel. **(A)** Photo transfer characteristics. **(B)** Output characteristics (dot lines: light; solid lines: dark). **(C)** Photo-induced threshold voltage (Vth) decrease. **(D)** Gain (G_{PH}) spectra at various photon fluxes.

The response speed of dynamic imaging is also dependent on electronic shutter technique. The previous APSs mentioned in Figure 2 use electronic roller shutter to acquire images. In some cases of shooting a fast-moving object, the images would be distorted and/or a ghost image would be presented if the frame rate and/or the sensor were slow.

Figure 3 shows the diagram of sensor array. The array has 256 rows and 256 columns. The top gate lines of the pixels in each column are connected and routed from the top direction, the 256-column top-gated interconnects are named from TG_1 to TG_{256}. Similar to the top gate lines, the bottom gate lines of each column are named from BG_1 to BG_{256}. The drains of the pixels in each row are connected and routed from the right direction, which are named from V_{OUT1} to V_{OUT256}. The sources of all pixels are connected to V_{Bias} and routed from the left direction. BG_1 to BG_{256} and TG_1 to TG_{256} are used for timing control, V_{OUT1} to V_{OUT256} are used for signal output, and V_{Bias} is used for voltage bias.

Figure 4 shows the timing scheme of electronic global shutter in the proposed one-TFT APS. Since the photo-generated charges can be temporarily stored inside the pixel in the integration period through the dual-gate biasing, it is possible to realize electronic global shutter by simply implementing the designed timing scheme in Figure 3 even without a physical shutter TFT. After resetting the whole array, electronic global shutter is initiated by a pulse of light and followed by scanning and reading the array in a sequence.

2.3 Image acquisition system

Figure 5 shows the block diagram of image acquisition system where the sensor array is connected by a top-gated driver IC, a bottom-gated driver IC and a 256-channel readout IC (ROIC). The driver ICs are controlled by the FPGA to provide the driving timing, and the ROIC is controlled by the FPGA to collect analog signals and digitize the signals. The FPGA is used to synchronize the timing clocks and assure that the external ICs and the image sensor array work together well during the dynamic image acquisition.

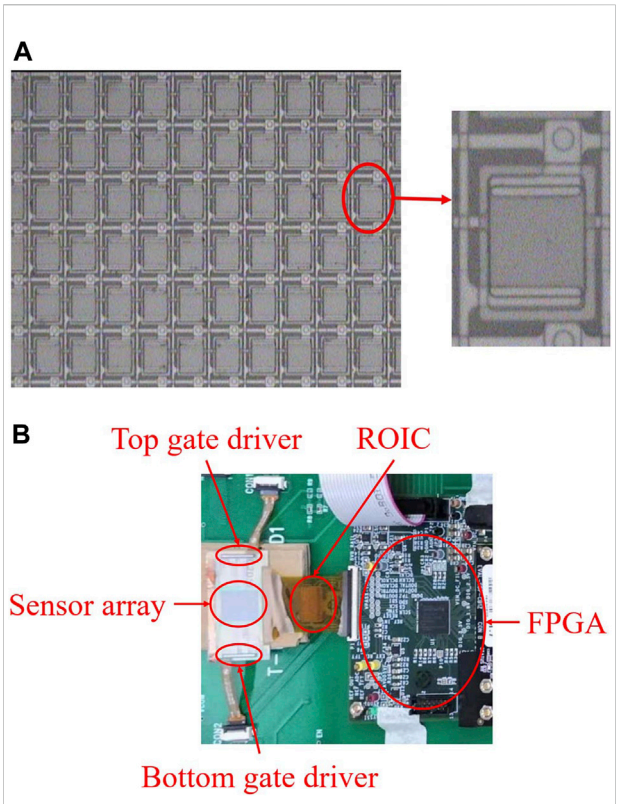

FIGURE 7
Die micrograph and system board. **(A)** Sensor array. **(B)** System board.

3 Example demonstration and discussion

Figure 6 illustrates device characteristics of the 3-D dual-gate photosensitive TFT. Upon light exposure, the transfer IV curves shift negatively, implying that the threshold voltage drops with light and accordingly the output photocurrent increases as observed in both transfer (Figure 6A) and output characteristics (Figure 6B). Further study unveils that the threshold voltage exhibits a quasi-linear relation with the photon flux (Figure 6C). In pursuing high sensitivity, the proposed one-TFT APS differs from the previous APSs in that the high SNR is achieved by operating the dual-gate photosensitive TFT in the subthreshold region where the output current is an exponential function of the threshold voltage. In another word, a small threshold voltage drop upon light exposure will lead to an exponential increase in the output current. As a result, the proposed photosensitive TFT demonstrates a high photoconductive gain of 10^2–10^4, nearly 2–4 orders of magnitude higher than the external quantum efficiency (EQE) of a typical PIN-type PD. It becomes even more important that such a high gain covers an entire studied spectrum with a wavelength ranging from 300 to 1,100 nm. The photosensitive TFT can therefore make a full utilization of all incoming photons in the studied wavelength range and outperform any a-Si:H based PIN-type PDs with an EQE generally below 85% (Figure 6D). Such a high gain can only be found in an avalanche photodiode where a strong electric field must be in presence to trigger avalanche electron multiplication (avalanche effect). However, shot noise also arises under such a strong electric field. Therefore, operating the photosensitive TFT in the subthreshold region becomes a possible approach to achieving high gain while suppressing the noise. Even though operation in the subthreshold region raises a concern of a narrow dynamic range, for low-level light sensing and low-dose dynamic X-ray imaging, high gain and full photon utilization are particularly more important. In the event that does need a wide dynamic range, the dual-gate photosensitive TFT can be tuned to operate in the linear or saturation region where gain is lower but dynamic range becomes wider.

TABLE 1 Comparison table.

	This work	Brown et al. [15]	Taghibakhsh et al. [13]	Karim et al. [14]	Roose et al. [12]
Technology	a-Si:H	CG-Silicon	a-Si:H	a-Si:H	a-IGZO
PD Type	Photosensitive TFT	Lateral PIN	Vertical PIN	Vertical PIN	NA
Gain or EQE of PD	$>10^2$	NA	<85%	<85%	NA
Critical dimension	5 μm	1.5 μm	10 μm	25 μm	3 μm
APS architecture	1T (dual-gate)	1T1C	2T1C	3T	3T1C
Pixel count	256 × 256	640 × 480	8 × 8	3 × 3	NA
Pixel size (resolution)	45 μm × 55 μm (505 ppi)	84 μm×84 μm (300 ppi)	100 μm × 100 μm (254 ppi)	250 μm × 250 μm (102 ppi)	100 μm × 100 μm (254 ppi)
Pixel fill factor	63%	NA	50%	50%	NA
Frame rate	34 Hz	30 Hz	NA	NA	50 Hz
Electronic shutter	Global shutter	Roller shutter	Roller shutter	Roller shutter	Roller shutter
Operating region of TFT	Subthreshold, linear, saturation	Linear, saturation	Linear, saturation	Linear, saturation	Linear, saturation

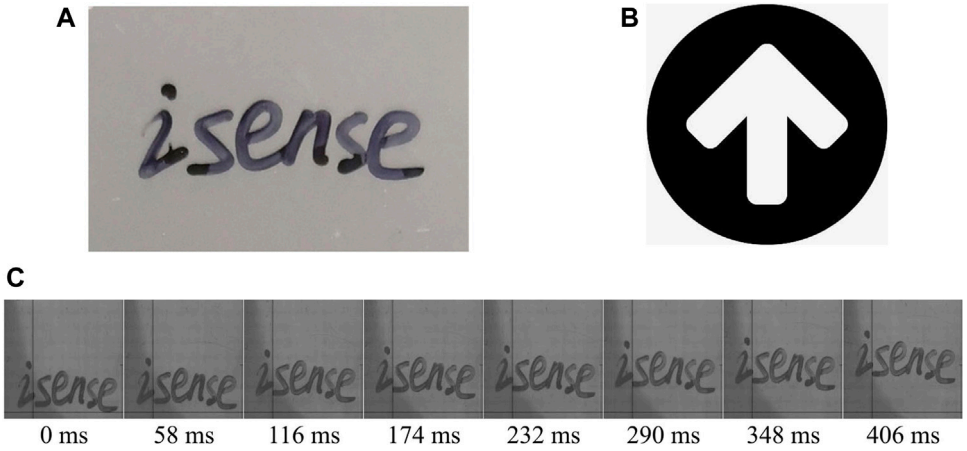

FIGURE 8
Example of dynamic imaging at a frame rate of 34 Hz under light exposure of 11 ms-pulsed green LED. **(A)** Target image. **(B)** Moving direction. **(C)** Sampling frames.

Figure 7 shows the micrograph of sensor array and system board where Figure 7A is a micrograph view of the array including pixels and traces and Figure 7B is a system board including driver ICs, ROIC, and FPGA. As shown, the top gates of each column are connected to the top-gated driver ICs, the bottom gates of each column are connected to the bottom-gated driver IC, and the signal outputs of each row are connected to the ROIC. The top-gated driver IC, bottom-gated driver IC and ROIC are all controlled by the FPGA. The image signal is sent to FPGA by ROIC.

One example of dynamic imaging using electronic global shutter is shown in Figure 8. Figure 8A is the target image with the characters of "isense" written on the transparent plastic. Figure 8B shows the moving direction of the target image. Figure 8C is a moving record of the target image, and the position of the target image is different at different times. In this example, the frame rate is 34 Hz.

A summary table and comparison with the previous works is given in Table 1. This work adopts a 1T APS structure, which has fewer devices than previous work, so it achieves the following advantages: smaller pixel size (45 μm×55 μm), larger resolution (505 ppi), better fill factor (63%), and higher photoconductive gain (>10^2). In addition, the array works in global shutter mode, and the frame rate can reach 34 Hz. Moreover, this work can operate in three regions (subthreshold, linear, saturation), while others can only work in two regions (linear, saturation).

4 Conclusion

In conclusion, we demonstrate a 256 × 256 active pixel image sensor array based on a 3-D dual-gate photosensitive TFT with a pixel pitch of 50 μm, pixel fill factor of 63%, photoconductive gain of 10^2–10^4 and spatial resolution of 505 ppi. An electronic global shutter is enabled by dual-gate biasing without additional shutter TFT. Such an array is capable of dynamic imaging at a frame rate of 34 Hz.

Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

Author contributions

YH: Designed the image acquisition system, performed the experimental work, and wrote part of the manuscript. YX: Captured the die micrograph of sensor array. JL: Processed image data. YQ: Tested the characteristic curve of pixel. KW: Conceived the project, organized the paper content, wrote, and edited the manuscript.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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