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4D-tracking in the 10-ps range: A technological perspective

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The present paper focuses on recent and ready-to-come advancements concerning high-resolution 4D-tracking with a perspective approach. Four-dimensional-tracking techniques (particle tracking with timing information for each detection point) have revealed a necessity for the next and next-to-next generations of high-energy physics experiments to cope with the increasing luminosity and consequent event pile-up in the beam collision region. Such a decisive challenge concerns both detection and processing technologies at an unprecedented level of difficulty. In addition to the high performance required in space–time measurement precision (some tens of picoseconds resolution in timing and about 10 μm resolution in space), an extremely high radiation hardness is demanded for such technologies together with an extremely high read-out and processing capability. Emerging experimental solutions for sensors and electronics against such challenges are presented here.

KEYWORDS

4D-tracking, pixels with timing, high space and time resolution, vertex detector, radiation hard detector, high data bit rate communication

Introduction

Following their path toward new discoveries, experimental techniques in high-energy physics (HEP) are now in need of an inevitable leap. Considering the research program for the next two decades and beyond, all the envisaged ways we could proceed further with high luminosity, future circular colliders, and muon colliders require an essential ingredient: high-precision timing in particle tracking with at least tens of picoseconds per detection point. However, high-precision timing alone is only one aspect of the problem. For brevity, the set of the tremendous technological requirements of an inner tracker for the next decade can be summarized as follows:

- R1. Space resolution $\sigma s \approx 10\ \mu m$.
- R2. Time resolution $\sigma t < 50$ ps
- R3. Radiation hardness against fluences $\Phi \approx 10^{17}$ 1-MeV n_{eq}/cm^2 (sensor) and total ionizing dose TID ≈2 Grad (electronics).
- R4. Data bandwidth density (readout and processing) DBW ≈ 10^2 Gbps/cm^2.

A complete solution satisfying all such requirements simultaneously does not exist yet.

Emerging solutions for future 4D-tracking

The pulsating heart of the system consists of two main parts, namely sensors and electronics, which are considered in the present section.

Among the several developments in sensor technologies, it is important here to highlight solutions having the technical capability to concurrently satisfy the previously listed requirements and, in particular, the items R1 to R3.

Sensors based on the internal gain by doping (LGAD [1]) can satisfy R2. Both the space and time resolutions must be accompanied by a high detection efficiency (ε), typically required to be above 99%. This limits the use of LGADs, where each pixel is bordered by a junction terminal edge (JTE) to isolate it from its neighbors. JTE can be fabricated with a size of approximately 10 μm, so that the minimum pitch of such sensors is limited to some hundreds of μm, in such a way to achieve a satisfactory fill factor of the sensing surface. This heavily violates R1. Several developments are being carried out to limit or even eliminate the effect of this feature, such as the use of trenches dug between adjacent pixels [2], or AC coupling through a resistive surface [3]. The latter solution has been already tested successfully on small matrices. It requires the acquisition of the amplitude information to extract timing and position with the due precision, and it is expected to be strongly limited to the detection rate due to the presence of the resistive plane.

However, the intrinsic limit in LGADs, which tendentially excludes them from our menu, is their weakness in operating at extreme fluences. Silicon sensors with gain are ruled out when it is necessary to sustain $\Phi > 5\ 10^{15}\ n_{eq}/cm^2$, as the p-doped gain layer is gradually deactivated by radiation [3], until it could not be compensated by the bias voltage increase anymore. Therefore, R3 also cannot be satisfied, unless new ideas are produced and experimentally demonstrated soon.

3D silicon sensors for 4D-tracking: no gain, but geometry

LGADs base their excellent timing performance (30 ps < σ_t < 50 ps typically) on two fundamental ingredients: minimizing the inter-electrode distance d (usually kept below 50 μm) and increasing the signal amplitude by gain. Gain is necessary to have an optimal signal-to-noise ratio (SNR) but turns out to be a very weak feature against high radiation fluxes. A completely different approach is demanded.

Presently, 3D silicon sensors are the only devices that show the capability to satisfy all the requirements from R1 to R3. The original idea of 3D silicon sensors dates to the late 1990s [4, 5]. It consisted in decoupling the sensor thickness from the electrode distance d. This idea is simple and clever and has three important effects:

a) keeping the charge carrier drift distance very short (20 μm or even less [6]).
b) Having a charge deposit thickness of some hundreds of μm and therefore enough signal amplitude (2 fC or more) to provide a good SNR.
c) The possibility to design the shape of the pixel volume, which, unlike planar devices, is not bounded by the size of d anymore. An accurate design can result in a timing-optimized pixel size, high electric field, and weighting field uniformity so to maximize speed and time resolution.

For this last reason, 3D sensors can also be named geometric sensors, as all their enhancement in performance depends on the specific electrode geometry.

The very short inter-electrode distance d has beneficial effects both on timing and radiation hardness, as the short carrier drift time also dramatically lowers the probability of defect trapping. Moreover, a small d produces a high electric field (and consequently high and more uniform carrier mobilities) even at small-to-moderate bias voltages ($V_{bias} \leq 100$ V). This enlarges the bias margin in case of performance weakening due to possible radiation damages at high fluences.

Present 3D geometric sensors have evolved considerably from the first designs, which were based on column-shaped junction electrodes fabricated at the center of square or hexagonal pixels. Bias electrodes were placed at each of the four (or six) pixel corners [5, 6]. Such "column geometries" are simpler to fabricate but are not optimized for timing and efficiency. They present zero-field spots between each couple of bias electrodes and very high field spots in the proximity of the central collecting electrodes. This causes a relatively large dispersion during charge collection times of the dE/dx deposits and consequently a worse time resolution.

In the last couple of years, excellent results in terms of timing have been obtained using an optimized or "trench geometry," also known as "TimeSPOT geometry" [6–8]. The bias (ohmic) electrodes are formed by a continuous trench on the two sides of the pixels, while the charge-collecting (junction) electrodes consist of a segmented trench at the center of the two continuous bias trenches. The TimeSPOT geometry maximizes the field intensity and weighting field uniformity while keeping the pixel capacitance under control (less than 100 fF at 55 μm pixel pitch).

The TimeSPOT geometry, with pixels of 55 μm pitch, has been widely tested under charged particle beams, showing intrinsic time resolutions $\sigma_t < 10$ ps and 99% efficiency in detection, while keeping hardness to fluences $\Phi \geq 2.5\ 10^{16}$ 1-MeV n_{eq}/cm^2 without any performance loss both in timing and efficiency [9]. Tests against higher fluences are presently in preparation.

TABLE 1 Target specifications for a pixel read-out ASIC suitable for future upgrades.

Specification	LHCbU2 Option 1	LHCbU2 Option 2	NA62 upgrade
Pixel pitch [μm]	≤55	≤42	≤300
Matrix size	256 × 256	355 × 355	40 × 45
Time resolution RMS [ps]	<50	<50	≤50
TID lifetime [Grad]	>2.4	>0.3/	0.07/year
ToT resolution/range [bits]	6	8	TBD
Power budget [W/cm2]	1.5	1.5	4.5
Power per pixel [μW]	23	14	<280
Pixel rate [kHz]	<350	<40	<700
Data BW per ASIC [Gbps]	<250	<94	<55
Material budget (per station)	<0.8% X0	<0.8% X0	<0.5% X0

The aforementioned results demonstrate that the challenge represented by the requirements R1–R3 can be considered basically won on the sensor side. Results have been obtained on small pixel matrices, and the work is still ahead concerning yield production issues on large devices and large-scale productions, but the intrinsic mechanism of the geometric sensors has convincingly proved its effectiveness.

The time measurements reported previously have been obtained with wide-bandwidth and high-power consumption electronics. Tests with such dedicated electronics were performed to study and understand the intrinsic behavior and performance of the sensors. It turns out that, at the system level, the limiting stage is by far the read-out electronics stage. This point will be addressed in the next subsection.

Electronics for high-precision 4D-timing

In a TimeSPOT sensor, the current signal induced onto the read-out electrodes has a typical total collection time of 200 ps with a standard deviation of 50 ps. For simplicity, a typical current signal can be approximated with a rectangular signal of 200 ps duration. It can be easily demonstrated [10] that the bandwidth of such a current signal is $f_{-3dB} \approx 2$ GHz, which corresponds to a time constant $\tau \approx 75$ ps for a first-order low-pass filter and $\tau \approx 40$ ps for a second-order one. These values can give a hint about the performance required for the front-end input stage to completely exploit the sensor speed. Such specifications have been fulfilled using discrete-components hetero-junction (Si-Ge) bipolar transistors and high-power consumption in trans-impedance amplifying stages [10]. Such electronics are implemented on printed circuit boards (PCBs) hosting few read-out channels, directly wire-bonded on the sensor pixels. A rise time of approximately 100 ps has been achieved at 70 mW per channel, with the corresponding intrinsic time jitter of approximately 6 ps. This solution can be considered a high-precision measuring tool and extremely useful in laboratory characterization of the devices under test, but it is clearly inappropriate in an experimental system at colliders. In such cases, high-density integrated electronics must be used, directly bonded on wide sensor matrices.

In high-density integrated electronics, the circuit design parameter space is limited by tough system constraints, as listed in Table 1 [11, 12]. Similar demanding requirements are presently at different stages of discussion and definition in other LHC developments (CMS-PPS [13], ATLAS AFP [14], and CMS run-5 [15]). The same trend, with even hardened specifications, will continue in future hadron collider experiments in the longer term [16].

Each readout channel, or electronics pixel, should integrate an amplifier and a fast discriminator. According to the average hit rate to sustain, a time-to-digital-converter (TDC) circuit should also be integrated per single channel or shared among a group of channels (2–8 typically). The need for a high level of integration obliges the use of small feature-size CMOS technologies.

The HEP community is decidedly oriented toward the choice of the CMOS 28-nm technology node for the next 5–10 years of developments in the field. This net choice is mainly due to the following reasons:

- The CMOS 65-nm node, which is used in the last ASIC developments [17], is not adequate for the level of integration required by the next generation of experiments. A gain in integration, speed, and power consumption is expected “for free” from the technology scaling.
- The CMOS 28-nm technology is the last “bulk” CMOS node before the subsequent FinFET generations. The latter are still very expensive and not “harnessed” enough inside the community to use them in very complex systems. In particular, their characterization against the total ionization dose (TID) is still preliminary.

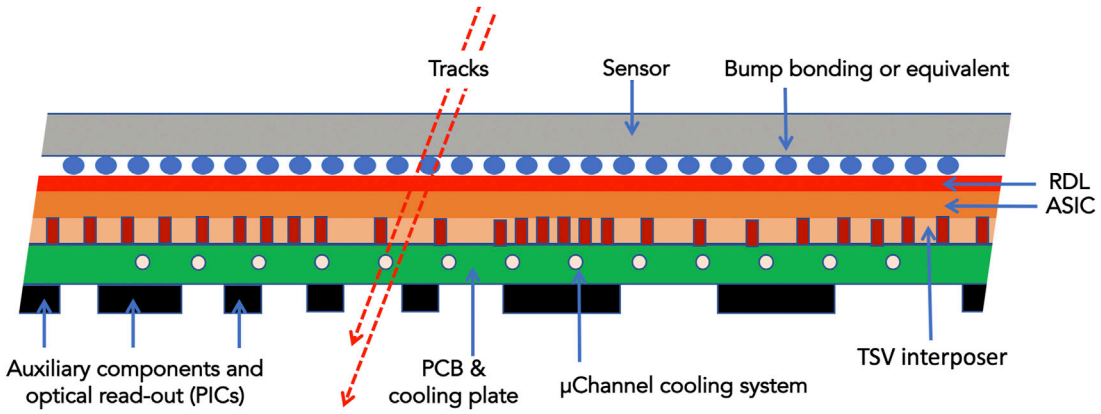

FIGURE 1
Schematic view of the envisaged tracker module spotting its levels of vertical integration.

- The CMOS 28-nm technology has been studied and characterized in the last years concerning TID resistance, demonstrating the maximum resistance to radiation TID when compared to other "adjacent" nodes (as, for example, the 65-nm and 22-nm nodes [18]).
- Characterization tests on the CMOS 28-nm demonstrate the possibility to use it at least up to a TID of 1 Grad. Moreover, a list of design recipes for better radiation resistance has been already identified [18], [19].

Among the several items listed in Table 1, the most compelling one is the small power budget allowed per electronics pixel. Such constraint is technically motivated by the present maximum capability to dissipate the power produced, which is approximately 1.5 W/cm^2 [11]. Compared to the aforementioned trans-impedance fast solution, a slower approach appears mandatory, allowing much less current flowing in the first stage and accepting a larger amount of signal integration and a much smaller slew rate. Recent developments in CMOS 28-nm have shown the possibility to limit the time jitter at the front-end level to approximately 20–30 ps within the power budget [20]. If 3D-trench silicon sensors are used, capable of an intrinsic $\sigma_t < 10$ ps, the sensor contribution to time measurement uncertainty tends to be negligible: the limitations to system performance depend by far on the electronics stage.

The pixel circuit must be completed by the TDC. Also, in this aspect, interesting solutions have been already developed, capable of suitable resolutions and low-to-moderate consumption [20].

The first developments in the front-end solution at the pixel level (amplifier, discriminator, and TDC) in CMOS 28-nm show that the target of 50 ps in system time resolution is feasible within the allowed power budget. The trickiest point about timing performance is the possible achievable accuracy in the wide distribution of the time reference (system) clock. This is particularly difficult and delicate already in small areas (mm^2) [20]. When the area of the ASIC is increased towards cm^2, extremely accurate floorplan and system distribution strategies must be elaborated, not to spoil the performance reachable at the single pixel level.

Data read-out and processing

The requirement R4 concerning a DBW ≈ 10 Gbps/cm^2 also demands very specific developments. While fast data serializers are under development in CMOS 28-nm [21], implementations of line-drivers are going in the direction of using Silicon Photonics-Integrated Circuits (PICs) [21]. The CMOS ASIC and PIC devices will have to form a unique system.

PIC devices implement a wavelength division multiplexing (WDM) technique. In each 28-nm CMOS front-end ASIC, several ring modulators, tuned at slightly different wavelengths, are driven at 25 Gbps, thus effectively multiplying the output bandwidth by the number of wavelengths. Those, in turn, are injected into the PIC using a single fiber [21]. The design of the PIC must be accomplished together with one of the CMOS ASICs, with particular care for their integration. A solution being investigated is the usage of a PCB interposer. The ASIC and the PIC are put in contact through a circuit using high-frequency low-loss material, such as Megtron 6 from Panasonic. Other solutions are being investigated, such as extending the TSV (through silicon vias) interposer foreseen for the ASIC-to-sensor integration to the PIC-to-ASIC integration [21].

Once the problem of transmitting data at 100 Gbps per single ASIC is solved, a further and major issue arises. We will briefly

address this point, concerning data handling, in the following Discussion section.

Discussion

Going back to the requirements R1–R4 and looking ahead to the final target of 4D-tracking, as defined at the beginning of this article, we can state that the R&D programs ongoing in recent years have already found many of the required experimental solutions.

3D-trench silicon sensors have time resolutions below 10 ps and excellent radiation hardness, having not shown their ultimate limit yet. Additional tests are needed to find it. The high performance of this sensor technology can be further pushed and exploited also in different applications, as, for example, high time resolution photonics or radiation detection in extremely harsh environments.

The high sensor performance is difficult to be matched at the system level by the integrated electronics stage, due to severe system constraints. The CMOS 28-nm technology appears as the largely favorite choice for HEP implementations of the next decade. Further characterization studies and design experience are needed to understand the limit of applicability of such technology in extremely high fluences. This can be important for the next-to-next generation of HEP experiments and also considering that subsequent technology nodes can be even less resistant to TID.

The path toward high DBW, although still long, appears already traced using integrated silicon photonics.

The complexity of the events and the aim to study very rare events in high-luminosity experiments led to the use of triggerless and data-driven acquisition systems. However, the huge amount of data produced is not trivial. The front-end system produces several peta-bps. The main problem with that is not so much the information storage but the time required for its processing. Fast and huge data storage facilities can only postpone the problem of data processing. Consequently, it is decisive to develop very sophisticated real-time analysis tools to process the events as soon as produced [22, 23].

In addition to the intrinsic performance of the single technologies involved, 4D-tracking is mainly a matter of system conception, where all the single components (sensor, read-out ASIC, cooling, data transmission, and data processing) must be intimately matched together implementing a unique, complex, highly integrated system (Figure 1). The success of such an endeavor relies on conceiving the system as a whole from the very early stages of the work.

Data availability statement

The original contributions presented in the study are included in the article; further inquiries can be directed to the corresponding author.

Author contributions

AL has been working on 4D-tracking developments for HEP for several years. He has been the Principal Investigator of the INFN TimeSPOT project (2018-21). He is now PI of the IGNITE project on electronics developments for 4D-tracking, which was recently approved and funded by INFN (2023-26). This study is mainly based on results and ideas elaborated within these two development programs.

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Conflict of interest

The author declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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