A GaN−Si hybrid integrated driver for narrow-pulse and high-current LiDAR applications

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Light detection and ranging (LiDAR) is the most important active remote sensing tool and is widely used in civilian and military fields. There are a number of methods to drive laser diodes; the most common circuit topologies are capacitor-discharge resonant circuits. However, the performance of the silicon (Si)-based switching device limits the development of Light detection and ranging, such as the large figure of merit (FOM) and the stray inductance. Although different methods have been reported to resolve these problems, there are still great challenges in reducing the pressure on Light detection and ranging driver design. Hence, this work presents a gallium nitride (GaN)−Si hybrid integrated driver for a Light detection and ranging system. In the circuit, the switching power device uses GaN instead of a Si-based device, because GaN enables much better performance for pulsed-laser operation due to its near-ideal switching performance. Furthermore, a GaN push−pull driver stage between the GaN power device and the Si-based driver integrated circuit (IC) was innovatively introduced, which is integrated in the same chip with the GaN power device, thereby effectively reducing the parasitic parameters of the signal chain and enhancing the system reliability. The design and implementation of the Si-based IC and GaN IC are based on 0.18 μm 80−120 V Bipolar-CMOS-DMOS (BCD) technology and 0.5 μm p-GaN technology, respectively. The experimental results suggest that the proposed driver circuit output pulse width is 12.6 ns, and it can normally operate at 10 MHz with turn-on/turn-off delay is 11.94 ns. In addition, the driver was capable of generating approximately 8.25 A current pulses through a low ohmic load with a pulse width of approximately 12.4 ns. This work plays a vital role in promoting the development of information equipment and aerospace equipment such as precise ranging, high-efficiency power supplies, and high-speed motors.

KEYWORDS

lidar, TOF, GaN, laser driver, narrow-pulse

1 Introduction

LiDAR, a radar system that detects the target position, speed, and other characteristics by emitting a laser beam, is widely used in military, automotive, medical, and other fields [1–7]. A typical LiDAR system consists of a laser transmitter, an optical receiver, and an information-processing system. The laser transmitter converts the electrical pulses into

optical pulses and emits them, and the optical receiver detects the optical pulses reflected from the target and restores them to electrical pulses, so that the distance between the emission source and the detected object can be calculated [8, 9]. This technique is also known as time of flight (TOF) detection.

Laser transmitters used in LiDAR systems are usually near-infrared semiconductor lasers, edge-emitting lasers, or vertical-cavity surface-emitting lasers [10]. These laser diodes behave similarly to rectifiers in terms of device electrical characteristics, that is, when forward biased beyond a certain threshold current, the device emits laser radiation with an output optical power roughly proportional to the forward current. Therefore, a pulsed-laser beam of corresponding intensity can be obtained by driving the laser with a certain intensity of current pulses. The pulse width and pulse amplitude of the laser determine the two most important technical parameters of the TOF LiDAR: ranging resolution and detection distance. A shorter pulse width gives better resolution while a higher pulse peak current increases the detection distance [11, 12].

The laser of a LiDAR is driven by a dedicated circuit, which supplies a large amount of current for a short period of time. The most common circuit topology to implement such a driver is a capacitor-discharge resonant circuit [13], as shown in Figure 1, where the power switch M_1 must be able to withstand high voltages, conduct peak currents, and respond in nanoseconds or less. However, the traditional Si-based switching device has become the limiting factor in the development of LiDAR systems for two reasons: first, the large gate charge due to the large power switch size needed to meet the current and voltage requirements greatly slows the turn-on of the metal–oxide–semiconductor field-effect transistor (MOSFET) [14]. Second, MOSFETs are vertical devices with connections on both sides of the die, so it is forced to use an external package form, which adds substantial inductance in both the power loop and the gate drive loop [15].

Recently, gallium nitride (GaN) power devices have attracted a lot of attention because of the heterojunction two-dimensional electron gas (2DEG) channel structure. These devices have several overwhelming advantages over silicon (Si)-based devices, such as higher operating frequency, lower on-resistance, and higher blocking capacity [16–18]. By comparing Si MOSFETs and GaN power devices at the same current rating, GaN power devices have a smaller figure of merit (FOM; $= Q_g \times R_{on}$. Q_g is the gate charge of the power device, R_{on} is on-resistance of the power device) and package inductance [19], which is especially suitable for high-frequency, high-integration, and energy-efficient LiDAR applications.

Some examples of laser drivers based on GaN power devices have been reported. Glaser [20] proposed a performance-optimized pulsed-laser diode driver based on a GaN FET. Ma et al. [21] proposed a digital-type GaN driver with a laser-diode peak-current-correction (LDPCC) loop and a current–pulse balancer (CPB) loop for LiDAR systems, which is a driver prototype that uses GaN high-electron-mobility transistors (HEMTs) as power switches, while the predriver and auxiliary
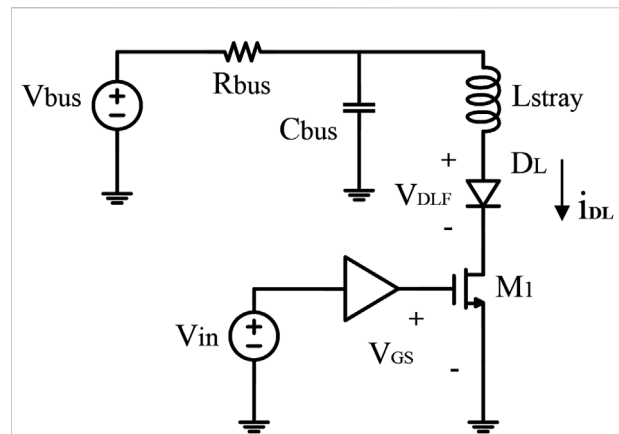

FIGURE 1
Conventional implementation of a capacitor-discharge resonant driver.

circuits use silicon transistors. Although a series of considerable research results has been achieved in optimizing drive circuit performance, there are still certain challenges in reducing the pressure on LiDAR driver design, specifically for reducing the parasitic inductance between driver output stage and the GaN power switch. Due to the existence of parasitic inductance, the gate voltage ringing during the whole pulse-generation cycle may cause it to exceed the safe-operating region, putting GaN power device reliability at risk [22].

This work presents a GaN–Si hybrid integrated driver based on the existing research. The circuit is a heterogeneous mixture of GaN integrated circuit (IC) and high-performance Si-based IC, which innovatively introduces a GaN push–pull driver stage between the GaN power devices and the Si-based driver IC. Through system-level optimization, this work minimizes the influence of the parasitic parameters, thereby stabilizing the power switch device turn on and enabling narrower output pulse widths and higher drive rates. This design has obvious advantages in narrow-pulse-width LiDAR applications that require extremely high performance with respect to output pulse width, drive rate, and stability. The experimental results suggest that the proposed driver circuit output pulse width is 12.6 ns, and the driver can normally operate at 10 MHz with turn-on/turn-off delay is 11.94 ns. The driver was capable of generates approximately 8.25 A current pulses through a low ohmic load with a pulse width of approximately 12.4 ns.

2 Materials and methods

2.1 Concept of the proposed architecture

As shown in Figure 2, an integrated driver of a heterogeneous mixture of GaN IC and high-performance Si-based IC is
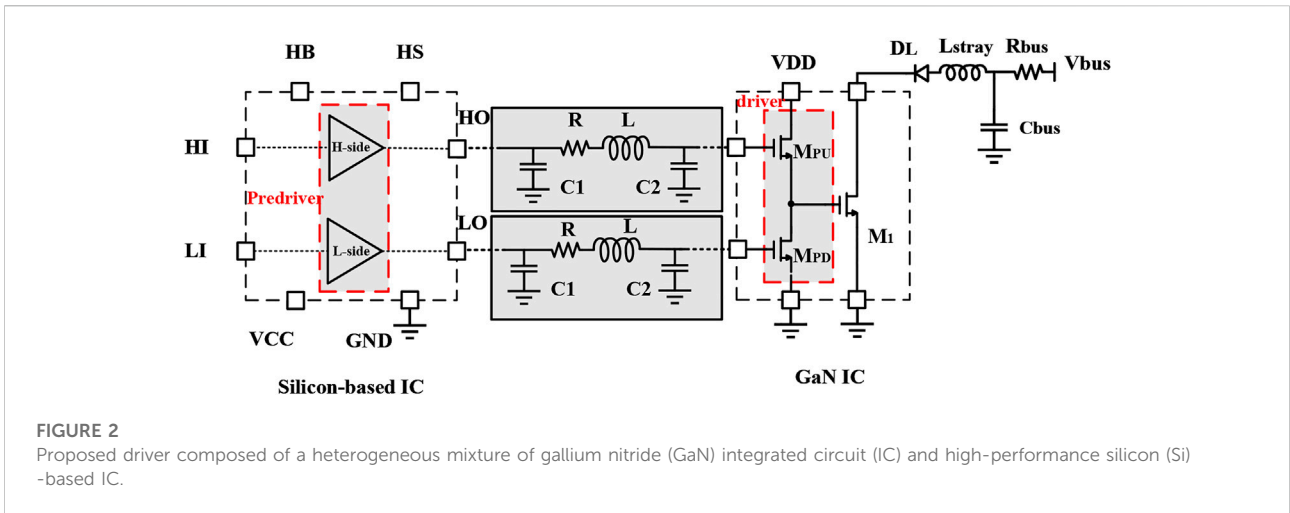
FIGURE 2
Proposed driver composed of a heterogeneous mixture of gallium nitride (GaN) integrated circuit (IC) and high-performance silicon (Si)-based IC.

proposed, where the main parasitic capacitance, inductance, and resistance are also illustrated. The parasitic inductance L and parasitic resistance R represent the bonded-wire components on the printed circuit board (PCB) circuit; C_1 is the equivalent parasitic capacitance of the Si-based IC output node and C_2 is the equivalent parasitic capacitance of the GaN IC input node.

The circuit includes two parts: the Si-based IC and the GaN IC. The Si-based IC is a high-stability and high-integration half-bridge predriver with high-side and low-side output channels, driving a GaN push–pull output driver stage M_{PU} and M_{PD}, respectively. VCC and GND is the power and ground of the low side, The voltage range of the low-side drive is 0V–5V. HB and HS is the power and floating ground of the high side. HB is generated off chip, we using Bootstrap circuit to generate high side power supply voltage HB. The voltage range of high-side driver is VDD to VDD + VCC. Specific circuits will be described thoroughly in Section 2.2.2. The GaN IC is composed of the driver stage and the power switch. They are integrated in the same chip to minimize the interconnection parasitic, and reduce the time constraint for charging the gate capacitance of the power switch device M_1. The enhanced GaN M_{PU} and M_{PD} form a push–pull output driver stage for M_1. M_{PU} and M_{PD} are much smaller than M_1, therefore the interconnection node between the Si and the GaN chip can be a position with lower parasitic capacitance in the signal transmission link, which can reduce the gate voltage ringing under the same parasitic inductance in the gate drive loop.

2.2 Circuit realization

2.2.1 GaN IC with push–pull driver stage

This work proposes a GaN IC with a push–pull driver stage and power switch on the same chip, as shown in Figure 3. Previous approaches have been reported for GaN ICs using
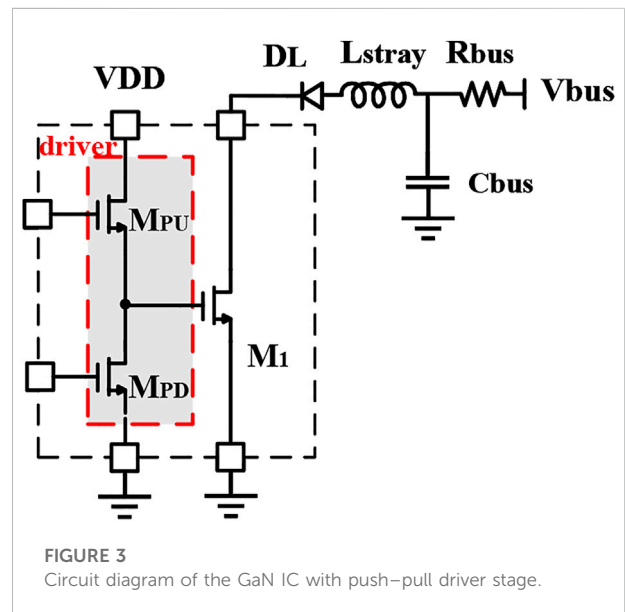

FIGURE 3
Circuit diagram of the GaN IC with push–pull driver stage.

p-type (p-GaN) -gate HEMTs [23]. However, complementary p-channel HEMTs are still not viable due to poor hole mobility in the GaN material [24]. Hence, the presented GaN IC driver stage is designed with two n-type enhanced GaN. To better appreciate the effectiveness of this solution, the Si-based IC uses a half-bridge structure to drive the enhanced GaN M_{PU} and M_{PD}. Because the half-bridge Si-based IC uses two signals with opposite phases that are non-overlapping, when the signals turn M_{PD} off, M_{PU} will turn on, and the M_1 gate node is pulled up. Similarly, when the signals turn M_{PD} on, M_{PU} will turn off, and the M_1 gate node is pulled down. The GaN IC is designed in 0.5 μm p-GaN technology, which uses a Si-based substrate, and the structure of the GaN FET is a p-type gate structure.
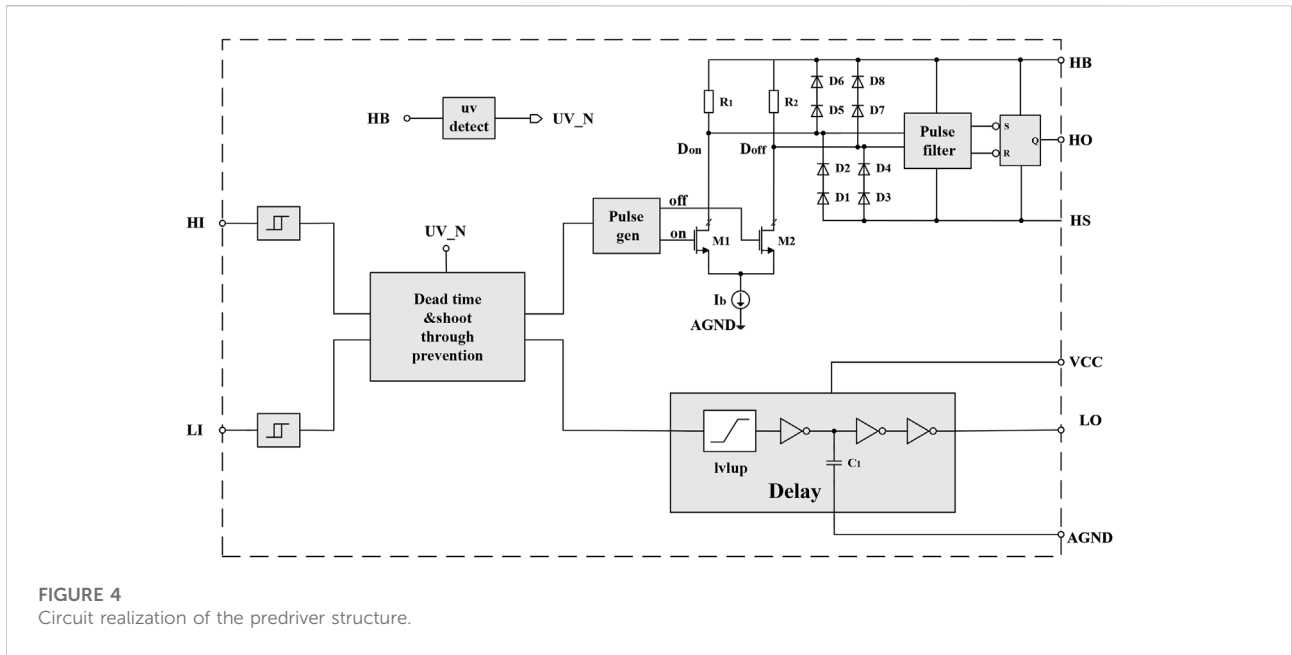
FIGURE 4
Circuit realization of the predriver structure.

2.2.2 Predriver

The topology of the predriver configuration is shown in Figure 4. The circuit is an integrated half-bridge predriver, which has high stability and high integration. It includes a Schmitt trigger circuit, dead-time control circuit, pulse generator circuit, level shifter circuit, pulse filter circuit, reset–set (RS) flip-flop circuit, and low-side predriver circuit.

2.2.2.1 Schmitt trigger

The role of the Schmitt trigger circuit is to reduce the interference of the input signal. As can be seen from Figure 4, input signals HI and LI are processed by Schmidt circuit, and the output signals HO and LO correspond to the input HI and LI through the logic levels. Because the Schmitt trigger has a hysteresis function, the entire logic circuit gives an anti-interference ability to the input signal.

2.2.2.2 Dead time control

The dead time setting prevents the high-side and the low-side power switches from being turned on at the same time, to avoid burning out. The dead time control circuit is divided into two parts: a dead-time generation circuit and a dead-time setting circuit. Figure 5 shows a block diagram of a dead-time generation circuit. The inverters with tail current sources I_1 and I_2 and the capacitor C_1 form a delay circuit to obtain a delay signal that inverts the rising edge of the high- and low-side signals. The inverted signal of the original input signal and the generated delay signal take part in the NOR operation to obtain the high- and low-side gate-switching signals with dead time. The UV_N signal is an under-voltage protection signal. When the high-voltage
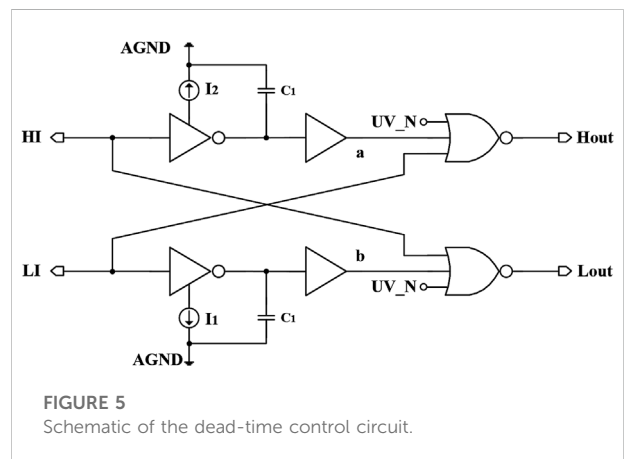

FIGURE 5
Schematic of the dead-time control circuit.

power supply HB has an under-voltage occurrence, the UV_N signal output is high, so that both the high- and low-side signals become 0 after passing through the dead-time control circuit.

The tail currents of the two branches on the high and low sides of the circuit are equal, that is, $I_1 = I_2$, so that when the high- and low-side power tubes are turned on, the dead time is equal. The expression for the dead time is as follows:

$$T_{DT} = \frac{(VCC - V_{th})C_1}{I_1} \qquad (2-1)$$

where I_1 is the tail current of the inverter, V_{th} is the flipping threshold of the buffer and VCC is the low-side power supply in Section 2.1.
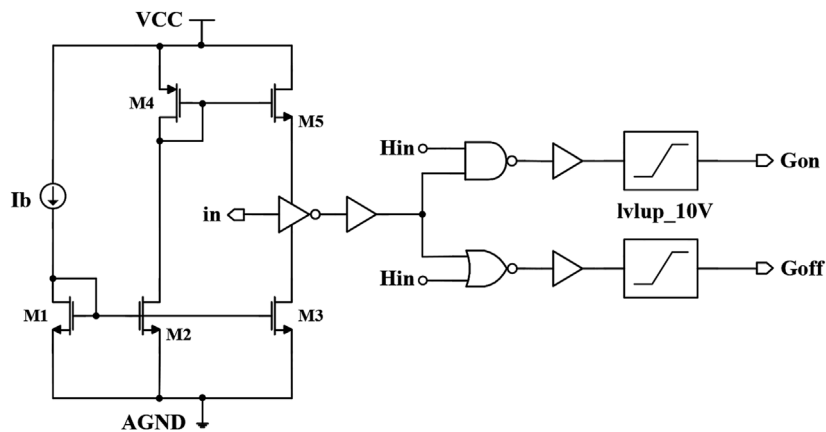
FIGURE 6
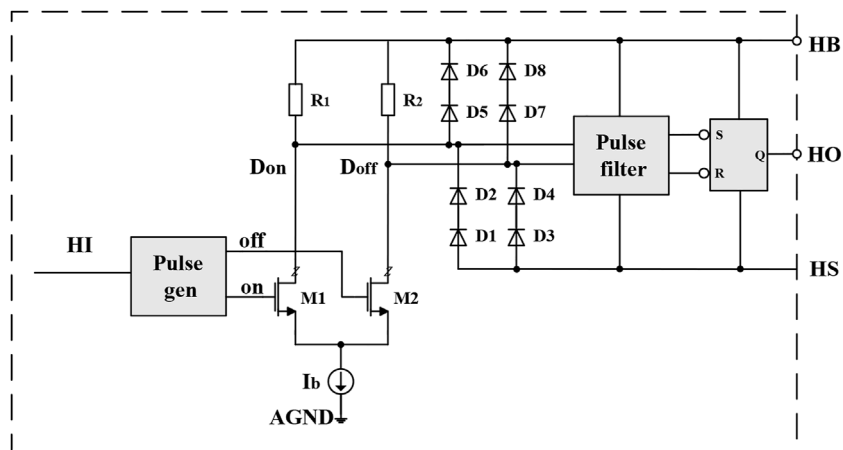Schematic of the pulse generator circuit.

FIGURE 7
Schematic of level shifter circuit.

2.2.2.3 Pulse generator

The pulse generator produces two pulses to drive the level shifter circuit formed by two high-voltage double-diffused MOSs (DMOSs). The generation of the two pulses reflects the rising and falling edges of the HI signal, respectively. Figure 6 shows the structure of the pulse generator circuit.

The principle of the pulse generator is to use a constant current to charge/discharge the capacitor, thereby controlling the width of the generated pulse signal. The pulse signal passes through the level conversion circuit and translates the voltage domain of the logic levels from low voltage to high voltage.

2.2.2.4 Level shifter circuit

The pulse signals G_{on} and G_{off} generated by the pulse generator are used to drive the level shifter circuit formed by two high-voltage DMOSs. When G_{on} and G_{off} turn on M_1 and M_2, the resistors R_1 and R_2 will generate a pulse D_{on} or D_{off}, which is low level relative to the floating level HS. After these two signals pass through the pulse filter, the RS flip-flop working on the floating level is set or reset. Figure 7 is a schematic diagram of the level shift circuit.

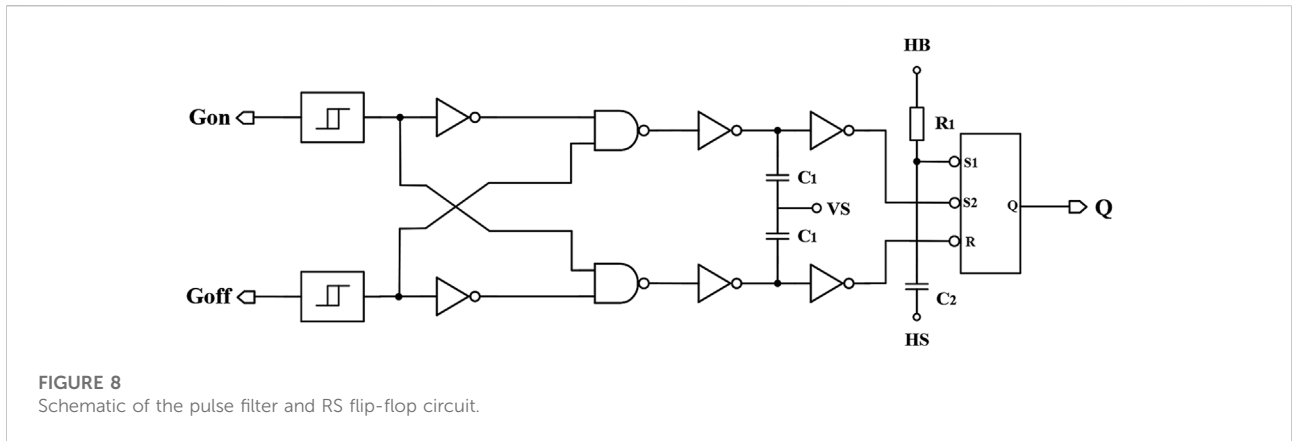When the DMOS M_1 or M_2 is turned on, the pull-down voltage on R_1 and R_2 can be expressed as:

FIGURE 8
Schematic of the pulse filter and RS flip-flop circuit.

$$\Delta V = I_b R_1 \qquad (2\text{–}2)$$

ΔV must be greater than the input inversion threshold of the subsequent pulse filter, but simultaneously not too large, to prevent the Zener diode from passing a large current and also prevent the diode from burning out. In the design, we choose I_b to be 1.5 mA and R_1, R_2 to be 4K Ω, then ΔV is 6 V, which is slightly larger than 5 V and satisfies the requirement.

2.2.2.5 Pulse filter circuit and RS flip-flop circuit

After the pulses D_{on} and D_{off} that are generated by the level shifter circuit pass through the pulse filter, the RS flip-flop on the floating level is set or reset. This series of actions resynthesizes the rising and falling edges of the HI signal into a complete pulse width signal, which is the entire process of converting the HI signal input at the logic reference level into the output drive signal HO at the floating level. Because each DMOS is only turned on for a short period of time when the RS flip-flop is set or reset, the power loss is much smaller than that of two DMOSs that are continually turned on, especially when the switching frequency of the system is very low. Figure 8 is a block diagram of a pulse filter circuit and an RS flip-flop circuit. Both the pulse filter circuit and the RS flip-flop circuit use HB and HS as the power supply and ground, and HS is the floating ground of the high side.

The introduction of R_1 and C_2 is to set the RS flip-flop during the power-on process. The high-side circuit realizes the conversion of the HI signal input at the logic reference level into the output drive signal HO of the floating level.

2.2.2.6 Low-side circuit

The low-side circuit converts the input low-level signal LI (5 V/0 V) into a driving signal (5 V/0 V) with driving ability, the delay block is to obtain the same delay as the high-side path.

Because there is no high-voltage power consumption and the problem of conversion such as suspension level, therefore, the
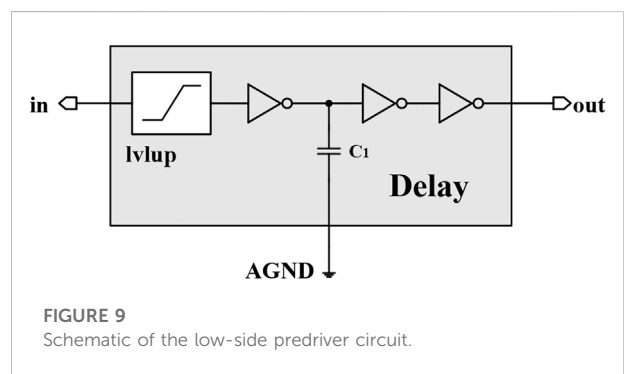

FIGURE 9
Schematic of the low-side predriver circuit.

low-side circuit can be greatly simplified. However, because the signal HI passes through the pulse generator, the level shifter circuit, the pulse filter, and the RS trigger circuit during the transmission of the high-side path, a delay module is required on the low-side path. The introduced delay module produces the same delay as that on the high-side path, so that after the HI and LI signals pass through the high-side path and the low-side path, respectively, the obtained delays are consistent. Figure 9 is a schematic diagram of the low-side predriver circuit.

3 Results

The implementations of the Si-based IC and GaN IC are based on 0.18 μm 80–120 V BCD technology and 0.5 μm p-GaN technology, respectively. Figure 10 shows the micrograph and testbench photos using the proposed structure. The layout of the PCB minimized the total inductance [25]. Moreover, a high-speed testing strategy is also used in this design, including a Kelvin connection for gate/drain and impedance matching with the sub-miniature A (SMA) connector at the gate/drain electrodes as well.
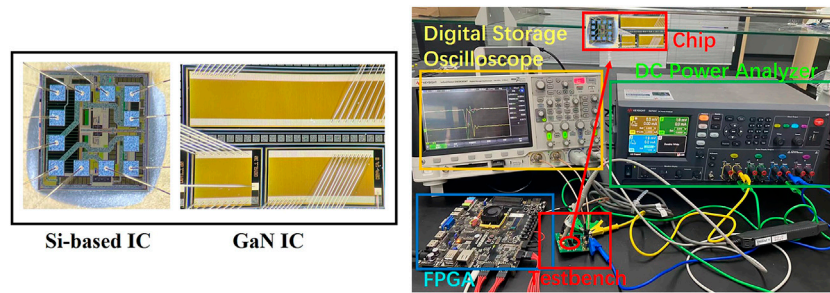
FIGURE 10
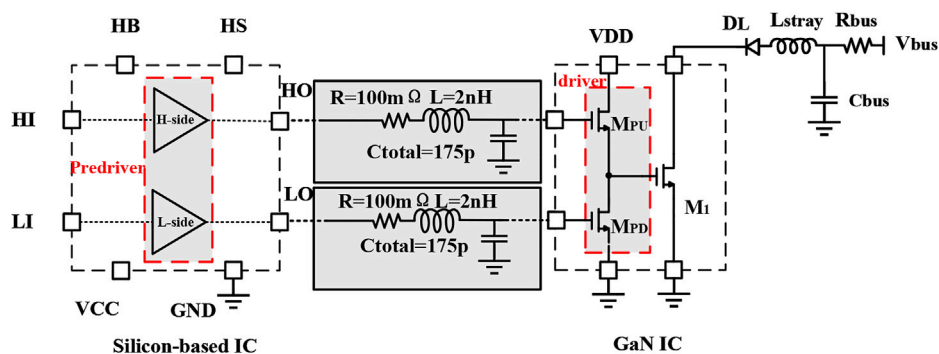Chip micrograph (left) and Testbench of the proposed driver circuit (right).

FIGURE 11
Diagram of the simulation model equivalent circuit.

3.1 Simulation results

Figure 11 shows the diagram of the simulation model equivalent circuit. The parasitic inductance L = 2 nH; the value of 2 nH is based on the estimated package inductance of the laser and the stray inductance due to the PCB. The parasitic resistance R = 100 mΩ; the parasitic capacitance and gate input capacitance are equivalent to C_{total}, which is 175 pF.

The design of the entire circuit was simulated and optimized using Advanced Design System (ADS) [17]. The parasitic inductances are estimated from the circuit layout. The simulated waveform results are shown in Figure 12. The conventional capacitor-discharge resonant driver simulation result is shown in Figure 12A; the equivalent capacitance between the driver stage and the power switch is 700 pF, which is the parasitic capacitance and gate input capacitance of power switch M_1 due to the size of the device. As we can see from the simulation result, the ringing of the gate voltage V_{M1_g} = 6.5 V, which is very dangerous for a GaN device, thereby affecting the stability of the system. Keeping the same circuit board inductance and resistance as for the conventional circuit, the proposed circuit

simulation results are shown in Figures 12B,C. It is clear that with the proposed circuit, the gate voltage ringing is significantly reduced, to 4.8 V. Because the size of M_{PD} and M_{PU} are much smaller than M_1, the equivalent capacitance between the driver stage and the power switch is 175 pF and the gate voltage ringing occurs at 5.487 V and 5.272 V, respectively, which are acceptable and significantly mitigated the harm to M_1. Therefore, the proposed circuit is a better choice for LiDAR applications.

3.2 Test results

Based on the simulation discussion in Section 3.1, the test comparison between the proposed circuit and the conventional circuit is shown in Figure 13. The test results of the proposed circuit are shown in Figure 13A; the input pulse signal generated by the field programmable gate array (FPGA) is 100 ns, the driver output width is 12.6 ns. Under the same test conditions for the input pulse signal, the conventional driver output width is 26.6 ns, as shown in Figure 13B.
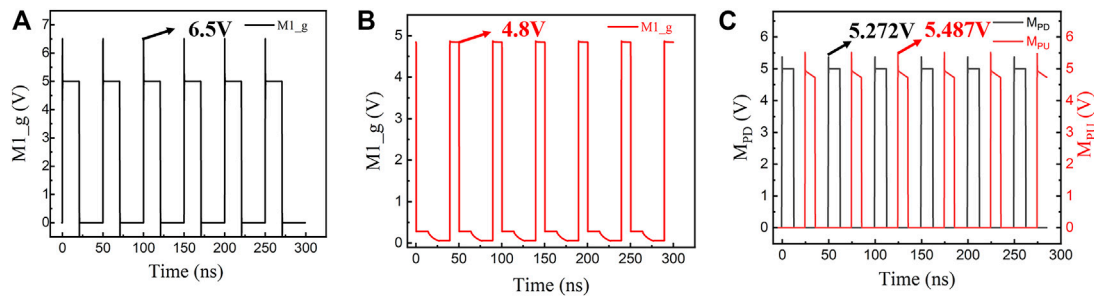
FIGURE 12
Simulation results comparing the proposed structure and conventional capacitor-discharge resonant driver circuit waveforms: **(A)** conventional capacitor-discharge resonant driver waveform of the M_1 gate; **(B)** the proposed driver waveform of the M_1 gate; **(C)** the proposed driver waveform of the M_{PD} gate (black) and M_{PU} gate (red).
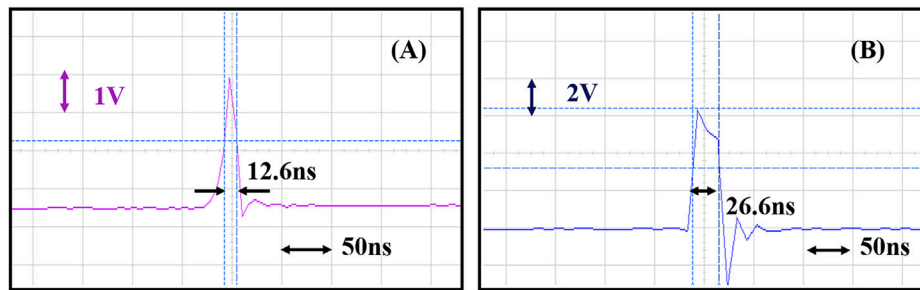

FIGURE 13
Experimental waveforms of the proposed driver and the conventional driver: **(A)** proposed driver output result; **(B)** conventional driver output result.

The proposed circuit has much smaller output width than the conventional circuit, which is consistent with the simulation results. However, there is still a slight deviation between the actual measurement results and the simulation results due to the power device conduction loss and switching loss.

The current drive capability was measured with a small resistor load; by measuring the drain voltage of the power switch M_1, the current can be obtained. In this case the peak value of the current pulse can be written as follows:
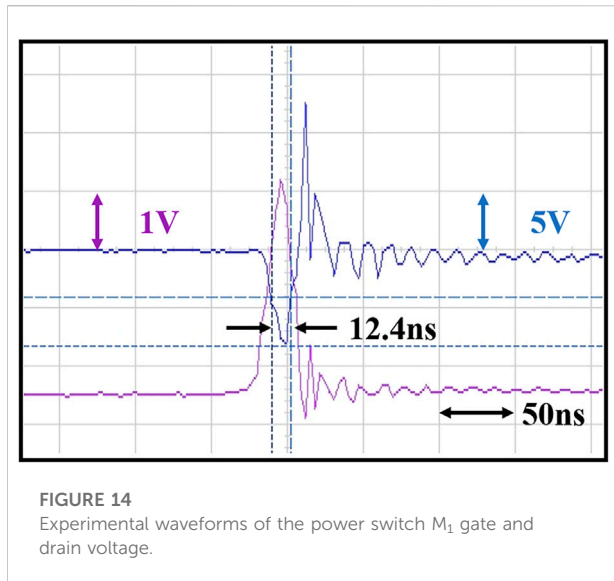
$$I_{peak} = \frac{V_{bus} - V_{M1\_d}}{R_{bus}} \quad (3\text{--}1)$$

Where V_{bus} is the supply voltage, R_{bus} is the resistor load, and V_{M1_d} is the drain voltage of the power switch M_1. Under the test conditions of $V_{bus} = 15$ V and $R_{bus} = 1\ \Omega$, the drain voltage of M_1 can be observed from Figure 14, which is 6.75 V when the pulse width is 12.4 ns. Based on Eq. 3–1, the peak current can be calculated as 8.25 A.

The propagation delay of the proposed high-side and low-side drivers at 10 MHz are shown in Figure 15. VCC is set to 5 V and VDD is 10 V, VCC is the low-side power supply and VDD is

the power supply of push-pull driver stage in Section 2.1. It can be observed from Figures 15A, B that the turn-on propagation delay of the high side is 11.94 ns, and the turn-off propagation delay is 11.7 ns. Figures 15C, D show the turn-on propagation delay of the low side is 8.44 ns, and the turn-off propagation delay is 18.6 ns. It is worth noting that the signal generated by the FPGA will be divided into two signals and preprocessed by an inverter to make sure the low side and high side signals will not be high at the same time, so the turn-off propagation delay includes the dead time of the inverter, which is 10 ns.

These experimental results indicate that with the proposed GaN–Si hybrid integrated driver, the power device ringing and spikes are significantly reduced, and the proposed structure has excellent performance in high switching frequency operation, and the propagation delay at 10 MHz is 11.94 ns. The driver generates approximately 8.25 A current pulses through a low ohmic load with a pulse width of approximately 12.4 ns. At this point, the pulse width of the input signal generated by the FPGA is 100 ns, and the output pulse width is 12.6 ns. When the pulse width of the input signal is adjusted to be narrower, this structure can be used to obtain a narrower pulse width output.

FIGURE 14
Experimental waveforms of the power switch M_1 gate and drain voltage.

FIGURE 15
Propagation delay of the proposed driver at 10 MHz: (A) turn-on delay of the high-side driver; (B) turn-off delay of the high-side driver; (C) turn-on delay of the low-side driver; (D) turn-off delay of the low-side driver.

4 Discussion

The design of a GaN–Si hybrid integrated driver for narrow-pulse and high-current LiDAR applications is presented. The experimental results suggest that the proposed driver circuit output pulse width is 12.65 ns, and the circuit can normally operate at 10 MHz with turn-on/turn-off delay is 11.94 ns. Additionally, the driver generates approximately 8.25 A current pulses with a pulse width of approximately 12.4 ns. By comparison with the conventional capacitor-discharge resonant driver structure, the ringing and spikes of the power device are significantly reduced, showing its future potential in a wide range of scenarios. The circuit driver is especially suitable to meet LiDAR applications for high resolution and increased detection range. However, to minimize the pulse width and to maximize the peak current the total parasitic inductance of the current loop should be minimized. This can be achieved by carefully designing the PCB and minimizing the length of the bonding wires.

Because this is still a non-monolithic driver, there are still inductances that cannot be avoided. During the switch turn-on cycle, the large time derivative of the currents through L cause a voltage drop on the power switch gate. The lower the gate voltage, the lower the maximum current that the power switch can handle when operating in the linear region, with low drain-source voltage V_{DS}. This may require compensating for the reduced current handling capability with an increase of the switch gate width or settling for a lower peak current specification. Therefore, future research on this work will be focused on an all-GaN driver solution, to further reduce the impact of parasitic inductance.
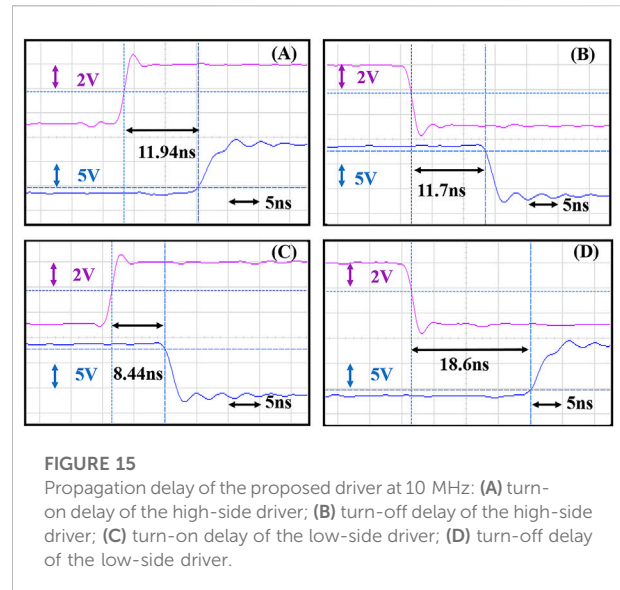
Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

Acknowledgments

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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