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# Amalgamation of high- $\kappa$ dielectrics with graphene: A catalyst in the orbit of nanoelectronics and material sciences

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In electronics, the size of transistors has been reduced to a few nanometers. Electronic devices' accuracy and authenticity face a major problem of leakage current. To solve this tricky situation, high- $\kappa$  dielectrics which have a huge band gap and permittivity are established to increase the capacitance and remove the leakage current. Three major properties are related to current flow: 1) band gap, 2) resistance, and 3) dielectric constant. High- $\kappa$  or higher dielectric constant shows how much charge a material can hold. A large band gap is needed to vanquish charge injection that causes leakage current. So, these are the insulating materials that store charges when placed in between metallic plates. The dielectric thickness of high- $\kappa$  can be enhanced without enhancing the capacitance, hence reducing the leakage current. These materials need to be functionalized. Materials with low physical and chemical barriers need to be functionalized with them. The best material to be integrated with these high- $\kappa$  dielectrics is graphene, as the goal of large area uniformity of electrical properties is achievable with this and easily separable graphene is also available. Here, we will scrutinize the current advancement in graphene electronics-based research on high- $\kappa$  dielectrics such as  $\text{Al}_2\text{O}_3$  (used as obstructing oxide in charge trap flash memory) with graphene. This article reviews the amalgamation of oxides such as high- $\kappa$  dielectrics with graphene, which are necessary for the understanding of top-gated electronic devices made by graphene which includes field-effect transistors and other electronic devices.

## KEYWORDS

graphene, van der Waals epitaxy (VDWE), heterostructures, high- $\kappa$  dielectrics,  $\text{Al}_2\text{O}_3$

## Introduction

The peeling or flaking (called exfoliation) of 2D [1] material known as graphene [3] from graphite has generated universal research interest in atomically fine materials over the last decade. Graphene is the first 2D material to be perceived; numerous materials existed in sheeted form with inter-sheet interactions controlled by Van der Waals (VdW) forces [4]. Flexible electronic applications of high- $\kappa$  dielectric insulators include touch panel displays, flexible OLED lighting, flexible photovoltaics, flexible transistors, flexible batteries, and supercapacitors [2], and all are the essential components in microchip technology. These applications require the consolidation of graphene into heterostructures containing very thin dielectric layers as tunnel barriers or gate dielectrics. So, it is vital to amalgamate graphene with oxides to recognize the vast spectrum of its electronic applications. Now, the challenge that comes into play is that receptive chemisorption sites on the perfect graphene surface are negligible [5]. Here, the role of Van der Waals (VdW) epitaxy becomes important. Easy transfer and cleavage of VdW epitaxy-grown oxides on graphene is an added advantage. So, grown oxides with redesigned properties can be transferred to other insulating substrates if needed. For electronic components, high- $\kappa$  dielectric material permits very high doping in graphene [6] and enhances the production of graphene field-effect transistors. Because of the caloric discrepancy between oxides and Si, only the polycrystalline or amorphous phase of STO is grown on Si. That means most of the oxides are not compatible with Si-based technology. This problem could be superscribed by growing oxides on graphene. For many electronic devices, we need high-quality oxide thin films on the surface of graphene. For example,  $\text{Ga}_2\text{O}_3$  grown on EG can be used for fabricating flexible, vertical solar-blind photodetectors [7].

The question might arise as to why this material was unknown until the 21st century. This is because nature rigorously prohibits the development of low-dimensional crystals [3]. Graphene research has increased greatly in the field of electronics because of its theoretically divine restrictions on properties: electron mobility concerning room temperature is predicted to be  $\sim 2 \times 10^5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  [8], it shows an inherent strength of 130 GPa [9] and Young's modulus of 1TPa, it is capable of carrying exceptionally high electric current densities which is  $10^5$  times more than that of copper, it shows an unreasonably elevated thermal conductivity (exceeding  $3,000 \text{ W mK}^{-1}$ ), gases cannot penetrate it, and it can also be synthetically functionalized. Graphene becomes more interesting for researchers in industrial applications when the reduplication of graphene gives the same superlative execution as the finest sample obtained in the research laboratory. Graphene can be synthesized by using three methods: micromechanical exfoliation [10], chemical vapor deposition (CVD) mostly carried out using a copper foil [11], and sublimation of SiC [12, 13]. With a zero-

band gap special electronic structure [14], graphene will improbably build into highly geared integrated logic circuits for a channel material. Both exfoliated and CVD graphene need to be transferred onto an insulating substrate, for example,  $\text{SiO}_2/\text{Si}$ , for significant electrical characterization and device fabrication. Transferred graphene generates an extra step and may also lead to some structural defects and contamination. An ideal template for oxides might be graphene as it is single crystalline, homogeneously thick over a large area, and does not need to be transferred. A list of dielectric constants for some high- $\kappa$  dielectric oxides used in DRAM and CPU is given below as follow [2] (in Table 1).

## Bigger is not always better

The electronic transfer of nanostructures is robustly controlled by the interface quality and lattice orientation [16]. In between the layers, epitaxy is required to manufacture highly accomplished and high-performance graphene-based nanomaterial. If the layered structures are not properly manufactured, then symmetry breaking occurs and dependency on in-plane charge transport increases [17]. Now, the stacking of 3D and 2D materials is because of the out-of-plane uniformity of the 3D network. 2D materials have weak interlayer interactions, so the manufacturing of 2D materials such as conductors, semiconductors, and insulators is done in a manner that enables the stacking and reduces the unsolicited impression on charge transfer due to weak Van der Waals interaction. A crucial criterion between the layers is epitaxy, if highly geared graphene-established nanoelectronics is to be manufactured [18]. More details about the high- $\kappa$  dielectric (such as its basics and some challenges) and a comprehensive discussion on the interpretation of some important high- $\kappa$  dielectrics (such as  $\text{Al}_2\text{O}_3$ ,  $\text{HfO}_2$ , and  $\text{ZrO}_2$ ) grown on graphene is presented in the following sections.

## Basics and challenges of novel high- $\kappa$ dielectrics

High- $\kappa$  dielectric is a material with a high dielectric constant dissimilar to  $\text{SiO}_2$  (as shown in Table 1). These materials are used in the semiconductor industry to manufacture semiconducting devices where they replace the dielectric layer of a device. We know that the scale integration of transistors in electronics has reduced to lower than a few nanometers because of which leakage current has become a problem for device dependability. To control this issue, materials that show huge permittivity and large band gaps are classified as gate dielectrics for increasing the capacitance and blocking this leakage current. A dielectric material is used to increase the electrostatic or AC coupling between adjoining metals and semiconductors. A dielectric

TABLE 1 List of High- $\kappa$  dielectrics with their dielectric constants and band gap [2].

High- $\kappa$ dielectric material	Dielectric constant- $\kappa$	Band gap in EV
BeO	274.80	10.11
NbOCl <sub>3</sub>	343.4	3.43
SrTiO <sub>3</sub> (Strontium Titanium Oxide)	288.12	3.01
NaNbO <sub>3</sub>	163.36	3.94
NaTaO <sub>3</sub>	167.76	3.55
AgTaO <sub>3</sub>	180.95	3.15
Li <sub>4</sub> CO <sub>4</sub>	62.39	7.83
CdTiO <sub>3</sub>	134.28	3.45
KTaO <sub>3</sub>	131.87	3.33
Y <sub>2</sub> Ti <sub>2</sub> O <sub>7</sub>	101.98	4.02
Cd <sub>2</sub> Ta <sub>2</sub> O <sub>7</sub>	112.80	3.53
TiO <sub>2</sub>	122.10	3.02
SrHfO <sub>3</sub>	49.92	5.19
Ag <sub>2</sub> Ta <sub>4</sub> O <sub>11</sub>	61.83	4.11
BaZrO <sub>3</sub>	54.57	4.62
HfO <sub>2</sub> (Hafnium Oxides)	34.3	6.12
PbZrO <sub>3</sub>	65.13	3.82
BiTaO <sub>4</sub>	56.17	4.23
PbHfO <sub>3</sub>	62.69	3.79
HfTe <sub>3</sub> O <sub>8</sub>	44.14	5.12
ZrO <sub>2</sub> (Zirconium Oxide)	38.53	5.71
K <sub>2</sub> W <sub>2</sub> O <sub>7</sub>	63.70	3.43
Sr <sub>2</sub> Ta <sub>2</sub> O <sub>7</sub>	50.30	4.25
AlO(OH)	28.82	8.03
NaIO <sub>3</sub>	48.84	4.94
BiTaO <sub>4</sub>	56.17	4.23
Al <sub>2</sub> O <sub>3</sub> (Aluminum Oxide)	9-11	6.044

insulator is a primary element in nanoelectronic devices such as dynamic random-access memory (DRAM), central processing unit (CPU), and flash memory. It is also used to vanquish the leakage current between electrodes which affects the energy utilization and authenticity of the devices [2]. Again, a question might arise in the context of why SiO<sub>2</sub> has been used for decades. That is because of its defect-free thin-film growth or because of its high-quality growth. The main issue with SiO<sub>2</sub> is that if its layers become very thin, then the quantum tunneling effect occurs and leakage current becomes a problem. High- $\kappa$  dielectric materials replace SiO<sub>2</sub> as they possess a high dielectric constant [19]. By using a high- $\kappa$  dielectric, the dielectric thickness can be enhanced at the same capacitance by suppressing the leakage current [20]. A perfect high- $\kappa$  dielectric should have a high dielectric constant and a high electronic band gap (E<sub>g</sub>) to vanquish the charge injection from electrodes in the dielectric.

An absolute high- $\kappa$  dielectric should have both a high dielectric constant and a high band gap.

So, why do we need to amalgamate these materials with graphene? There is a restriction in normal complementary metal oxide semiconductor (CMOS) scaling mechanics. Enhancement of the performance of field-effect transistors is required. For that reason, restructuring and recasting the structure of the transistors are maintained by amalgamating novel dielectric insulators with epitaxial graphene. Scaling of Si transistors forms high leakage currents in the SiO<sub>2</sub> gate oxides. So, dielectric materials of high permittivity are needed [21]. That is why high- $\kappa$  dielectrics such as hafnium oxide ( $k = 34$ ), aluminum oxide, ( $k = 9$ ), and ZrO<sub>2</sub> ( $k = 38$ ) are explored [22]. High- $\kappa$  dielectrics are used in graphene-based electronics due to lower Coulombic scattering of charge carriers and increased carrier mobility [23]. Challenges that are caused by integration with Si-based technology are mentioned [24]:

1. Appropriate band gap and permittivity with band arrangement for high- $\kappa$  dielectrics on Si.
2. Interfacial stability at high- $\kappa$ /Si

- Gate source voltage instability causing low performance of devices.
- Dielectric breakdown is a global issue in which dielectric material no longer has its insulating properties when receiving a high electric field for a long time.

The best-known example of dielectric breakdown is the electrical storm in which lightning is produced. Here, clouds/atm. air/earth forms an electrode/insulator/electrode system; in this system, when the potential difference between an electrically charged cloud and the earth reaches its limit, a sudden electrostatic discharge toward earth takes place. This is because the dielectric breakdown phenomena occurred naturally. When this electrical discharge vanishes, the insulating properties of air are reinstalled as shown in Figure 1H.

## Synthesis technique

The mobility of graphene can be enhanced by up to 22% by providing an appropriate layer of nucleation by atomic layer deposition (ALD) [22]. If graphene is covered by multilayers of high- $\kappa$  dielectric then a small degradation of graphene's electronic and structural properties occurs. High-quality films are grown by ALD. These films are grown for gate dielectrics, and these are grown at a temperature below 300°C [26]. ALD is a water-based technique which means graphene must permit surface preparation processes that will permit the depositing of the uniform dielectric film. The ALD technique is highly reproducible (see Figures 1A–F).

Many other synthesis techniques such as molecular beam epitaxy and pulsed laser deposition technique are used for the oxide growth on any type of graphene. MBE technique is discussed later.

The purpose was to grow SrTiO<sub>3</sub> on a graphene substrate using the molecular beam epitaxy technique. The sample was prepared before loading into the MBE chamber. Substrates of

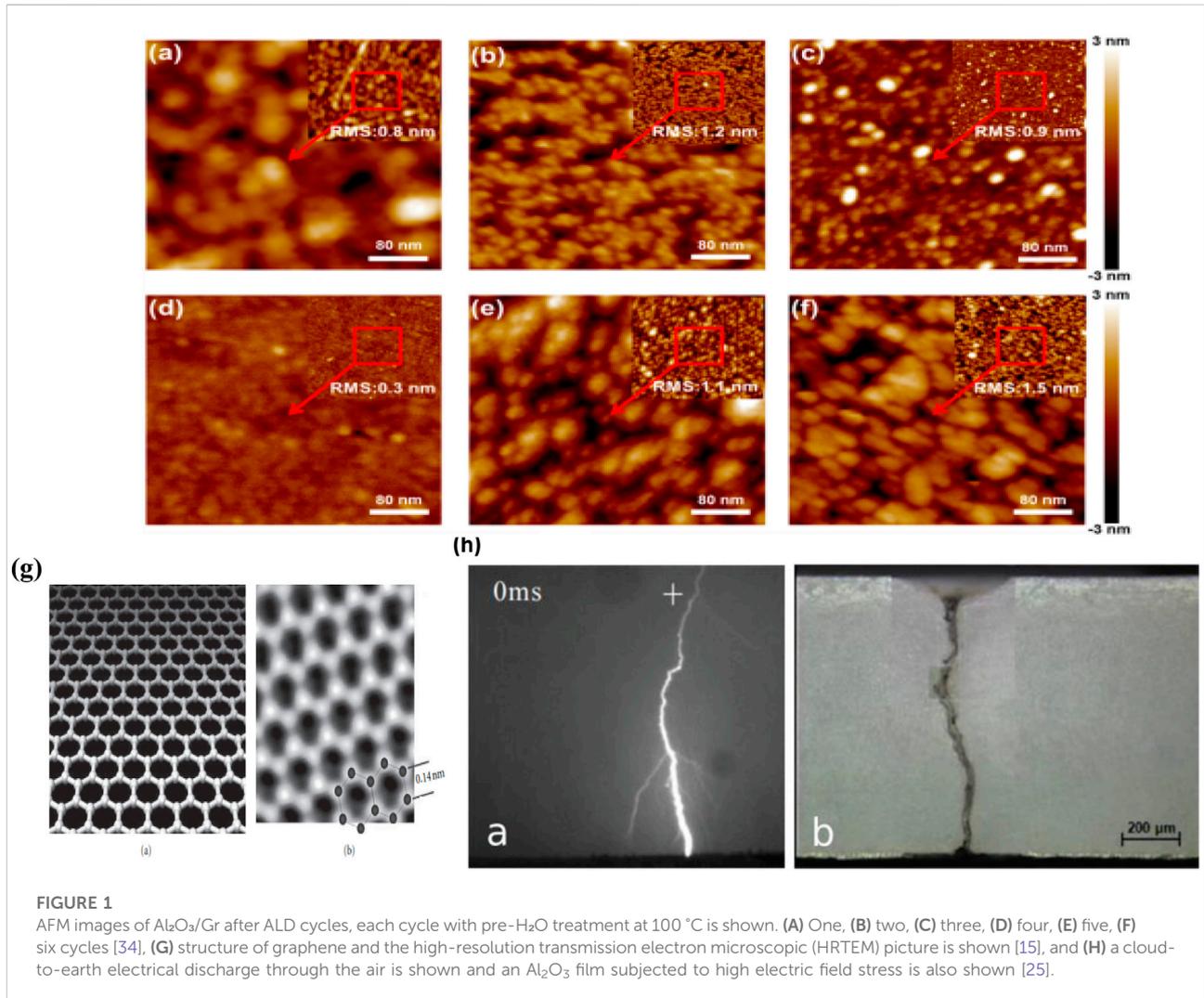
highly oriented pyrolytic graphite were prepared first by mechanical cleavage to expose a clean surface before loading in the MBE chamber. A base pressure of  $6 \times 10^{-10}$  Torr was created in the chamber. The next step was to remove the surface adsorbates. To attain that, the sample needed to be annealed at 600°C for 30 min. Sr was evaporated using the growth rate from 2 to 100 Å/min. Ti was deposited from an electron-beam evaporator with a growth rate of approximately 1 Å/min. SrO was deposited to grow to a thickness of up to 3 nm. It was grown by evaporation and co-deposition of Sr and Ti in the presence of molecular oxygen SrO. The morphology of the surface obtained and thickness of the grown film were characterized using atomic force microscopy (AFM). Crystal structure and orientation was determined using two important techniques, RHEED and XRD [40].

## high- $\kappa$ /graphene heterostructures

From the previous sections of this review article, we got to know the exceptional physical properties of graphene, the basics of high- $\kappa$  dielectric materials, and the challenges that arise with their integration with Si-based technology. Production of graphene in a large area is needed for the realization of graphene-based devices and the capability to amalgamate graphene with highly insulating thin films that act as gate dielectrics in field-effect transistors [22]. An attractive application of graphene is the field-effect transistor devices. These applications need the amalgamation of graphene into a composition that contains very thin dielectric layers. So, it is essential to amalgamate graphene with oxides to perceive the wide spectrum of its electronics applications as mentioned in the previous sections of this article. The properties of graphene can be regulated by overlayers. For electronic devices, high- $\kappa$  dielectric allows the ultra-high doping in graphene to enhance the performance of field-effect transistors which are based on graphene [22, 27, 28]. However, thermal fluctuation is another challenge of dielectric films on top of graphene, rendering

TABLE 2 High- $\kappa$  dielectric on graphene.

Material deposited	System/technique	Substrate	Reference
Al <sub>2</sub> O <sub>3</sub>	ALD	1. Gr on Cu foil	1. Raul Rammula et al. [5]
	ALD	2. Epitaxial graphene on Si face of SiC	2. N. Y. Garces et al. [33]
	ALD	3. CVD graphene	3. Li Zheng et al. [34]
	ALD	4. Gr on Cu foil	4. Gabriele Fisichella et al. [35]
	ALD	5. CVD graphene	5. Sang Hoon Chae et al. [36]
HfO <sub>2</sub>	ALD	CVD growth on Pt	Mengmeng Xiao et al. [37]
ZrO <sub>2</sub>	ALD	GNS from thermal reduction of GO	Jian Liu et al. [38]
STO	PLD	Gr on Cu foil PMMA	Sang A Lee et al. [39]
SrO	MBE	SrO/HOPG stack and EG	A.S.Ahmed et al. [40]
BaTiO <sub>3</sub>	PLD	Gr/SiO <sub>2</sub> /Si	Liyan Dai et al. [41]



manufacturing continuous dielectric/graphene interfaces tough [29]. The mobility of graphene integrated with high- $\kappa$  may be restricted due to phonon scattering [30], but still, graphene-based FETs amalgamated with high- $\kappa$  dielectrics perform very well [31]. This article is about fabricating layers of high- $\kappa$  dielectrics on the Si face of epitaxial graphene. These materials can be used to overcome some limitations noticed in Si-based nanoelectronic devices. Saturation current and switching speed are some parameters that can be improved [32]. Very few high- $\kappa$  dielectric materials have been grown on graphene until now, as shown in Table 2.

## Research issues and perspective

Raul Rammula et al. showed that 0.2–0.4 nm thickness of  $\text{Al}_2\text{O}_3$  seed layers were grown using the ALD technique at  $200^\circ\text{C}$ . As compared to the precursor, the TMA- $\text{H}_2\text{O}$  method of ALD did not

show much uniform growth. TMA- $\text{O}_3$  was much better as it resulted in a growth of dielectrics which was more uniform. However, it also caused some oxidation in graphene. The advantage of this ALD method was that it allowed the deposition of dielectrics on graphene in a single process [5]. Mengmeng Xiao et al. grew a very thin high- $\kappa$  dielectric on graphene using the ALD process. High-quality CVD-based graphene was grown on Pt. An amorphous layer of carbon was formed on graphene because of electron-beam scanning in the chamber of a scanning electron microscope. A uniform layer of dielectric was formed as a gate dielectric for top gate graphene FETs. The gate capacitance of up to  $2.63 \mu\text{F}$  per sq. cm was recorded. FET was fabricated with static carrier mobility of 2,500 sq. cm per volt per sec and negligible leakage current. The research was good for ultra-low power applications [37]. Jian Liu et al. developed nanocomposites of  $\text{ZrO}_2$  and formed the nanosheets of graphene by an atomic layer deposition (ALD) technique. Deposition temperatures were in the range of  $150\text{--}250^\circ\text{C}$ . By reducing the temperature, the crystallinity

was also reduced. This was a gradual decrease. The phase of the deposited sample was crystalline and amorphous at different temperatures. Both crystalline and amorphous phases were found in the ZrO<sub>2</sub>-GNS composite at 200°C [38]. Sang A Lee et al. used CVD graphene on Cu foil for such growth using pulsed laser deposition (PLD) at 700°C. A KrF laser of 248 nm was used for plume formation at a laser density of 2 J/sq. cm, and a repetition rate of 3 Hz was used. The atomic structure was characterized by HRXRD, and thickness, by XRR. Resistive measurements, Raman spectroscopy, and TEM were also applied. Graphene induced lower resistance on STO films, establishing a crystal structure and electric conduction [39]. A. S. Ahmed et al. grew the buffer layer for oxide amalgamation. A total of 25 nm SrO/HOPG was used, resulting in SrTiO<sub>3</sub> film having 001 orientation. Oxygen vacancies on SrO caused charge impurity scattering, resulting in Dirac point shifting and reducing the mobility [40]. Liyan Dai et al. used the PLD technique, and highly oriented BTO films were grown. Growth was achieved on graphene, which was covered with SiO<sub>2</sub>/Si substrates. These easily exfoliated films showed ferroelectric properties. Films followed Volmer–Weber mode. Wrinkles were obtained in graphene that showed nucleation sites at the initial stage of growth. BTO films were exfoliated using a metal Cr stressor [41].

## Graphene transistor fabrication

Three steps were involved in manufacturing a graphene-based field-effect transistor, abbreviated as GFET:

### Template (graphene) preparation

There are different approaches for obtaining monolayer and few-layer graphene sheets: 1) mechanical exfoliation, 2) epitaxial growth on SiC substrate, and 3) chemical vapor deposition (CVD). The best technique is to grow monolayer/bilayer graphene on the SiC substrate epitaxially. The SiC substrate is heated up to a specific temperature to attain the desorption of Si atoms in ultra-high vacuum. The first layer of carbon is not supposed to be graphene because of the strong bonding, and no Dirac spectrum is present in it [41].

### Deposition of dielectric material with a high dielectric constant in case of gated FETs

Since, now, the template is ready, the next step is to make the metal contacts and top gate. A minor value of gate capacitance is needed for some applications such as RF and digital applications. To achieve all this, one must use low leakage, thin, and uniform high- $\kappa$  dielectrics for the top gate. Dielectrics for gates are synthesized preferably using the ALD

technique, but deposition could also be done by thermal deposition. Now comes the challenging part as the ALD technique is water-based: The graphene plane of the base is hydrophobic, so it is difficult to deposit oxides such as high- $\kappa$  dielectrics mentioned in the previous sections. Also, graphene's surface is chemically inert, so it is more difficult to grow oxides on pristine defect-free graphene. The solution is to functionalize the sample of graphene to make it more reactive, for example, using NO<sub>2</sub> or O<sub>3</sub> [41].

### Contact formation with graphene (metal with graphene)

This section discusses the third step that has not yet been discussed in this article; it is the most important one. A simple method to make contact with graphene involves patterning which includes masking to transfer the pattern. This is achieved by a method called electron-beam lithography. Ti/Au, Cr/Au, Cr/Pt, Ni, and Co are normal metals used for making contact with graphene [42].

### Effect of insulating layers on performance of graphene transistors

SrO layers were fabricated on a graphene template by different deposition techniques as discussed previously. Now, to understand the effect of these layers on the electrical performance of graphene, some exfoliated SLG devices were fabricated on the SiO<sub>2</sub>(300 nm)/Si substrate. Before performing *in situ* electrical measurements, carrier density tuning was required. That was done using electron-beam lithography. Using the EBL technique, gold (Au) electrodes were patterned and a doped Si substrate was used as a back gate for tuning carrier density. Devices were then placed inside the UHV chamber for annealing at 100°C for 1 h. SrTiO<sub>3</sub> was deposited on graphene at room temperature. The growth rate used was 3 Å/min. Initially, the Dirac point (i.e., resistance maximum) was observed at the gate voltage of -5 V obtained through the four-probe resistance vs. the gate voltage curve. The slope of conductivity vs. gate voltage (VG) curve shows the field-effect mobility, which was 3,050 cm<sup>2</sup>/Vs. The Dirac point shifted to a value more negative than -90 V after deposition of 2 ML of SrO (3 Å/min). SrO has oxygen vacancies, and these vacancies were like charged impurities. If we assume that each oxygen vacancy donates two electrons and carrier density varies, each volt shift of the Dirac point corresponds to one vacancy per 42,000 oxygen atoms in 2 ML SrO. Future studies should focus on increasing mobility by increasing the SrO film quality through the reduction of oxygen vacancies and structural defects [40].

## Future outlook and challenges

Now we know about graphene and its electronic band structure. Because of its gapless electronic bands, the gate control is more challenging in comparison to its high off-state leakage currents for the fabrication of graphene-based transistors [42]. In the semiconductor industry, challenges for the size of MOSFETs are enhancing the importance of upcoming materials and devices which might improve the performance of MOSFET. This purpose requires material such as graphene with such electronic properties as discussed previously in this article. In this review article, we explored the challenges of high- $\kappa$  dielectric materials on graphene [42]. Here, in this review article, it is mentioned that the structural and electronic properties of graphene change based on the choice of dielectric material growth on graphene and deposition conditions for film growth. ALD depositions of  $\text{Al}_2\text{O}_3$ ,  $\text{HfO}_2$ ,  $\text{ZrO}_2$ , and PLD depositions of STO, BTO, and MBE growth of SrO were shown. The work in this article provides the building block for dielectric gate and/or tunnel barrier engineering that might help in the fabrication of graphene-based transistors in the future. However, most of the graphene used until now is CVD-based graphene. More well-defined growth could be maintained by using epitaxial graphene as a future template. A huge amount of regular work in the direction of the growth of diverse oxides has already been done. However, the growth of high-quality oxide layers on graphene is proving to be a serious issue. CVD-grown graphene is a very cost-effective and popular method. Most of the work is done on traditional CVD-grown graphene, which is polycrystalline, and exfoliated graphene which has limited-size flakes. As we previously discussed, both types of graphene need to be transferred onto some insulating substrate such as Si/SiO<sub>2</sub>. Also, this transferring process results in further defects/wrinkling in graphene. In such cases, the template does not act as an ideal substrate for the epitaxial growth of oxides due to inherent defects and multiple domains oriented in random directions and of limited size. This reduces the performance of the device due to haphazard oriented domains of graphene and adulteration at the interface. Ideally, if we want graphene as a growth template for epitaxial growth of oxides, then it should be single crystalline, should have homogeneous thickness over a large area (mm scale), and should not need to be transferred. Si sublimation from SiC and subsequent recombination of carbon atoms leading to epitaxial graphene has emerged as one of the best methods to achieve large-area single crystalline graphene with controlled layered thickness.

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## Conclusion

The quality of manufactured high- $\kappa$  dielectric films on graphene is analogous to the best quality of high- $\kappa$  films on Si, and it has great prospects for future graphene application in electronics. Here, in this review article, it was noted that the structural and electronic properties of epitaxial graphene change based on the choice of dielectric material growth on graphene and deposition conditions for film growth. There is only minimal degradation in the structural properties of epitaxial graphene. The work shown in this article is the building block for dielectric gate and/or tunnel barrier engineering that might provide help in the fabrication of graphene-based transistors in the future.

## Author contributions

Author made a substantial, direct, and intellectual contribution to the work and approved it for publication.

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## Conflict of interest

The author declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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