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Historical Perspectives, State of art and Research Trends of Single Photon Avalanche Diodes and Their Applications (Part 1: Single Pixels)

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The ability to detect single photons is becoming an enabling key capability in an increasing number of fields. Indeed, its scope is not limited to applications that specifically rely on single photons, such as quantum imaging, but extends to applications where a low signal is overwhelmed by background light, such as laser ranging, or in which faint excitation light is required not to damage the sample or harm the patient. In the last decades, SPADs gained popularity with respect to other single-photon detectors thanks to their small size, possibility to be integrated in Complementary Metal-Oxide Semiconductor processes, room temperature operability, low power supply and, above all, the possibility to be fast gated (to time filter the incoming signal) and to precisely timestamp the detected photons. The development of large digital arrays that integrates the detectors and circuits has allowed the implementation of complex functionality on-chip, tailoring the detectors to suit the need of specific applications. This review proposes a complete overview of silicon SPADs characteristics and applications. In this Part I, starting with the working principle, simulation models and required frontend, the paper moves to the most common parameters adopted in literature for characterizing SPADs, and describes single pixels applications and their performance. In the next Part II, the focus is then posed on the development of SPAD arrays, presenting some of the most notable examples found in literature. The actual exploitation of these designs in real applications (e.g., automotive, bioimaging and radiation detectors) is then discussed.

Keywords: single-photon avalanche diode (SPAD), quenching circuits, SPAD arrays, single photon counting (SPC), time-correlated single-photon counting (TCSPC)

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1 INTRODUCTION

Through the years, solid-state and especially single-photon imaging techniques have benefited from silicon electro-optical properties and integrability potential. In fact, a wide range of semiconductor optical detectors has been studied and employed.

Among such a variety of options, photodiodes figure as the simplest and cheapest ones [1]. To convert an incident radiation into an electrical signal, the diode is reverse biased and thus depleted from free carriers. When a photon is absorbed in the material, it transfers to the structure the energy necessary to generate an electron-hole pair, which is then collected by the readout circuit. However, when operating in photon-starving conditions proper to many fields of interest, such devices show a

critical signal-to-noise ratio mainly because of the readout electronics noise. Therefore, an internal gain multiplication is mandatory.

In Avalanche Photodiodes (APDs), being biased slightly below the breakdown voltage, photogenerated carriers undergo an impact ionization process, generating avalanche multiplication and a finite gain [2]. APDs operate in linear/analog mode and the maximum useful gain is limited by strong fluctuations in the multiplication procedure. Thus, they are unsuitable for time-correlated imaging techniques, where it may be required single-photon sensitivity and an effective time-gating of the detector operation.

Instead, single photons can be detected by APDs operated above the breakdown voltage (Geiger mode) [3]. Such sensors are known as Single Photon Avalanche Diodes (SPADs). When a photon is absorbed in the multiplication region of the device, a self-sustaining avalanche may be triggered and the current increases rapidly to a well-detectable level, marking with picoseconds time resolution the arrival time of the detected photon. An external circuit is then needed to quench the multiplication process and restore the SPAD to its original state, preparing it to detect a new photon [4]. The main drawback of SPADs with respect to analog detectors is the presence of a deadtime after each photon detection which limits the maximum count rate. To bring together the advantages of single-photon detection, typical of SPADs, and the photon number resolution, typical of analog detectors, solid-state photodetectors made of many SPADs connected in parallel, i.e., Silicon Photomultipliers (SiPMs), are widely exploited. The possibility to count each triggered avalanche is achievable both in an analog fashion (aSiPM), where each microcell employs a resistor for passive quenching of the SPAD, and in digital SiPM (dSiPM), integrating every SPAD with its own active or passive quenching and readout circuit [5].

Notwithstanding many single-photon sensitive devices already existed, SPADs stick out because of some advantages over the most promising one, e.g., Photomultiplier Tubes (PMTs) and Superconductive Nanowire Single-Photon Detectors (SNSPDs). Indeed, PMTs require high bias voltages, are bulky and sensitive to magnetic fields, and cannot be integrated with Complementary Metal-Oxide Semiconductor (CMOS) electronics, while SNSPDs require a cryostat to cool down the detector to a few Kelvins, making the system bulky and consequently limiting the application fields [6].

Arrays of SPADs are eligible for high-sensitivity imaging, superseding Charge-Coupled Devices (CCDs) and CMOS Active Pixel Sensors (APSs) when high-frame rates, gating, and photon timing capabilities are required. In fact, CCDs charge transfer readout results in a limited frame rate, whereas CMOS APSs, albeit being fast, do not detect faint signals, because they do not use internal amplification. More expensive Intensified-CCDs (I-CCDs) and Electron-Multiplying-CCDs (EMCCDs), having an internal gain, are employed to increase the signal [7, 8]; however, they cannot provide frame rates higher than few kframe/s and cannot be used in precise time resolved measurements. Eventually, arrays of SPADs and SiPMs are employed to overcome such tradeoffs.

From a historical perspective, single-photon detection by means of p-n junctions was first proposed by Haitz in Shockley Laboratory in the early 1960s [9, 10]. With the studies on the micro-plasma instabilities in silicon, he pioneered the understanding of avalanche breakdown and dark-current pulses, successfully modeling the first diode operating in Geiger mode. However, the evolution toward efficient Single Photon Detectors (SPDs) stepped forward with the development of the first epitaxial devices in the late 1980s [11], achieving good control of the electric field in the active region and thus its influence on dark counts, afterpulsing probability, and temperature dependence. Another milestone in the usage of SPADs was represented by the introduction of Active Quenching Circuits (AQCs), developed in 1981 by Cova [12]. By sensing the rise of the avalanche pulse and reacting back on the SPAD, these architectures force the quenching and reset transitions in short times (few nanoseconds) with a controlled bias-voltage source, paving the way for Single-Photon Counting (SPC) and Time-Correlated Single-Photon Counting (TCSPC) applications. A decade later, with ICs technology nodes miniaturization, custom fabricated SPADs combined with compact active frontend were developed [13]. Fully dedicated and flexible fabrication provided best-in-class performance in terms of detection efficiency, noise, and jitter. However, the impossibility of monolithic integration with processing electronics confined their application only in single- or some-(up to about one hundred) pixel arrays. Later on, thousands of SPADs have been assembled in arrays of a few millimeters square using the technological solution proposed firstly by Golovin [14]. The rising request for integrated circuits for control electronics in the 90s and early 2000s, set technological constraints fairly consistent with those set by SPADs, leading to the fabrication of on-chip integrated sensors in standard CMOS technology. Among the first attempts, in 2003 single pixel CMOS SPADs [15] and then fully integrated 2D arrays have been developed by A. Rochas et al. [16]. This allowed monolithic integration on the same silicon wafer of photodetectors, analog avalanche sensing and quenching, and digital electronics for SPC and TCSPC. In the last few decades, more advanced technologies such as 3D-stacking [17] have gained ground. Such architecture overlaps the sensor tier to the processing electronic, thus enabling independent optimization of each layer with dedicated processes, promising better sensitivity and more functionalities per pixel. Aull was the first to investigate 3D-stacked SPAD arrays in 2006 [18], while a decade later Mata Pavia [19] firstly demonstrated back-illuminated 3D-stacked SPAD image sensors based on standard CMOS technology.

SPADs stand out for their digital output, single-photon sensitivity, fast-gated operation, and picosecond precision, while remaining compact, low cost, and easy-to-integrate. Hence, they have been applied at first when intensity and time-dependent waveform of faint optical signals needed to be reconstructed. Beginning with academic research purposes in astrophysics [20], Adaptive Optics [21] and Fluorescent Imaging [22], during the years, the implementation on-chip of smart SPC and TCSPC increased the commercial and industrial appeal of such detectors, raising the interest of many big players (e.g.,

STMicroelctronics, Toyota, Sony, Samsung, Apple) in mobile/consumer electronics. Nowadays, several fields of applications are covered, spanning from biophotonics [23], Light Detection and Ranging (LiDAR) [24] and 3-D optical ranging applications [25], to quantum information technologies [26, 27].

Furthermore, arrays of SPADs and SiPMs tend to replace traditional PMTs in many radiation detection applications [28]. Large aSiPMs are already an established reality in indirect detection of gamma rays for Positron Emission Tomography (PET), offering a high fill-factor (FF), fast collection of highly energetic photons, and magnetic fields immunity [29]. However, dSiPMs are gaining more and more interest in Time-Of-Flight (TOF) PET, promising an improved coincidence time resolution, increased timestamp granularity and direct on-chip processing. Usage of 3D-stacked SPADs as detectors in X-rays radiation environments has also been recently documented [30].

The aim of this article is to review the main features of silicon SPADs and their figures of merit. **Section 2** covers the description of SPADs physics. **Section 3** is dedicated to the different frontend architectures, **Section 4** focuses on the main SPAD figures of merit while **Section 5** presents single pixels applications and their performance.

2 SPAD DETECTOR

2.1 SPAD Working Principle

SPADs consist of a p-n junction biased above the breakdown voltage (V_B) and are characterized by an intrinsic positive feedback, which is the fundamental mechanism behind their single-photon sensitivity. This condition happens when the electric field is so high to reach a critical value (>3.10^5 V/cm) due to the applied reverse bias across the p-n junction, overcoming the V_B with an overvoltage named excess bias (V_{EX}). In fact, SPADs operate in a bistable condition in which the device is either in a quiescent state or the avalanche is triggered. A SPAD must be able to remain quiescent, when biased above breakdown, for a sufficient amount of time (e.g., longer than ms), waiting for the avalanche current injection. Thus, the spontaneous generation-recombination phenomena, which would trigger the avalanche multiplication process independently of the light signal, must be kept as low as possible. As soon as an electron-hole pair is generated an avalanche current is generated, typically increasing with a rise time below 1 ns up to a steady current level in the mA range. The current converges to a self-sustaining level, as a consequence of a counteracting effect due to the generated free carriers in the depleted region, able to mitigate the electric field. The SPAD outcoming pulse due to a single-photon detection has a sufficient amplitude to be easily detected by a readout electronics; for this reason SPADs are considered SPD [31–34]. The high value of avalanche current in a SPAD risks to stress and damage the junction. Consequently, to stop this current and avoid breaking the device, it is essential to lower the electric field adequately below the critical value (≈3.10^5 V/cm), effectively quenching the avalanche. Thus, the frontend electronics has the task to detect the leading edge of the avalanche, generate an output pulse synchronous with the triggering, promptly reduce the SPAD bias to the breakdown voltage and finally restore the initial operative level. This circuit is usually referred to as a sensing, quenching and recharge circuit or simply quenching circuit [13]. In the current-voltage (I-V) characteristic, shown in **Figure 1**, the on-branch represents the sweeps after the avalanche has been triggered and the SPAD is being quenched, the off-branch, instead, the sweeps during the recharge phase.

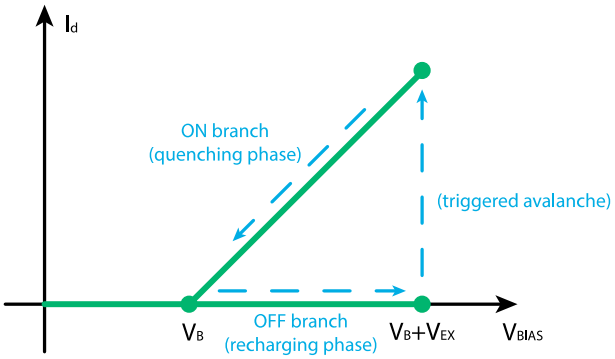

FIGURE 1 | SPAD I-V characteristic. The voltage V_{BIAS} is the reverse bias applied to the SPAD and I_d the SPAD current.

Quenching circuits are necessary to avoid SPAD damage by promptly interrupting the avalanche current flow through a reduction of the reverse voltage below V_B. Various are the proposed solutions for quenching that come with either passive or active components, or a mix of the two, answering to different design requirements (see **Section 3**).

2.2 Cross-Section in Different Technologies

The technology employed to fabricate the SPAD and the device cross-section, deeply influences the detector performance. SPADs can be fabricated either in Custom technologies or Standard CMOS technologies. A custom fabrication process was employed in the earliest published works on SPAD detectors [35, 36], achieving very good device performance. The main advantage of custom technology is the flexibility to act on dopant concentration and implantation energy, targeting the optimization of SPAD performance. Nevertheless, custom SPADs have high production costs, cannot be integrated with frontend circuitry and their parameters are not homogeneous on different production batches. Thus, this process is mainly employed for single devices or small arrays of the detectors.

Custom SPADs are gathered in two families: reach-through and planar devices. The typical structure of a reach-through SPAD is shown in **Figure 2A**. Considering a quasi-intrinsic p^- substrate, the high electric field region is at the junction created on one side by an n^+ phosphorous diffusion, while on the other side by a deeper p^+ boron enrichment. By applying an appropriate reverse bias, the depleted region extends into the entire p^- layer. This structure reaches high efficiency thanks to the wide depleted region and having the avalanche initiated by electrons (being a p/n^+ geometry), however the large area allows the triggering of the avalanche in different regions with a different propagation

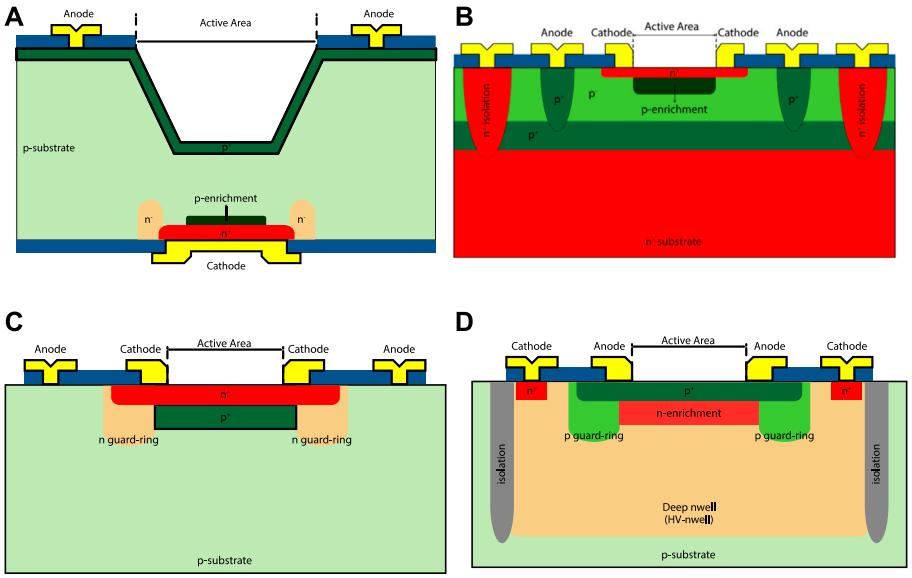

FIGURE 2 | SPAD cross-sections: reach-through custom SPAD **(A)**, planar custom SPAD **(B)**, non-isolated CMOS SPAD **(C)**, and isolated CMOS SPAD **(D)**.

time of the current, worsening the timing performance. The backside of the wafer is etched targeting a thickness of 25–40 μm. However, reach-through SPADs are not suitable for array implementation, being delicate and costly devices [3]. On the contrary, a planar structure is easier to fabricate [37–39]. A possible example of cross-section can be found in **Figure 2B**, the junction is relatively shallow, obtained through an n^+ phosphorous diffusion and an ion implantation p enrichment. The substrate is one of the main differences with respect to the reach-through SPAD. It is composed of an n^+ wafer plus the addition of a quasi-intrinsic p region and a p^+ buried one, both through epitaxy. The high doping n^+ region introduces a full electrical isolation and sharply reduces the diffusions tails. The planar structure requires a lower bias and assures very good timing response, making it possible to create arrays of detectors (still without frontend electronics). In order to obtain higher efficiency in the Near-Infrared (NIR) range, two different structures of custom planar SPADs have been engineered: red-enhanced [40, 41] and resonant-cavity-enhanced SPADs [42, 43].

Standard CMOS SPADs have clear advantages compared to custom devices. First of all, the possibility to be integrated into silicon wafers, optimizing the area employment with high resolution and low cost per pixel. As a direct outcome, integrated SPADs allow the design of arrays, up to massive size, together with the design of complex frontends, processing and readout. The main drawback of SPAD integration in well-consolidated commercial technologies is the rigidity of processes, since realizing the specific technology masks requires a significant economical effort. However, integrated SPADs have shown a key role in many applications, so they have been introduced alongside the core products of some foundries [44]. CMOS SPADs are divided into non-isolated and isolated devices [45]. The formers have a central cathode surrounded by the anode, which is directly in contact with the substrate (**Figure 2C**), resulting in a deep

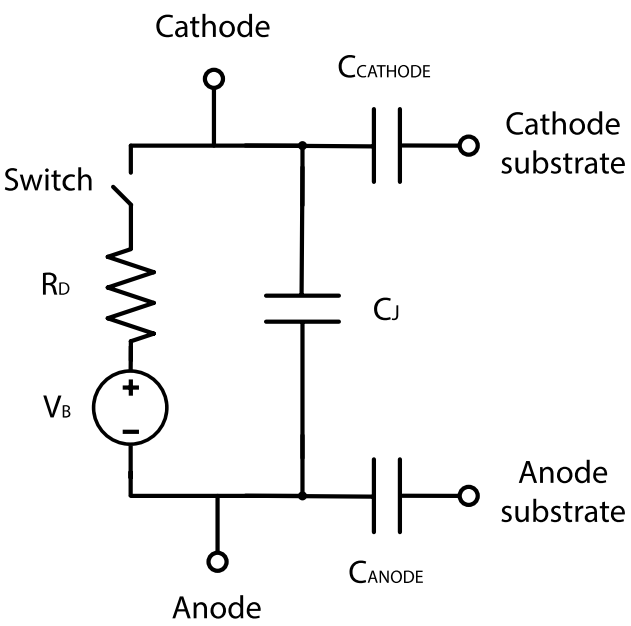

FIGURE 3 | SPAD model, which includes the breakdown voltage generator, the detector resistance, the junction capacitance and the anode and cathode parasitic capacitances.

depleted region that enhances the NIR sensitivity [46], but worsens the timing performance. Isolated SPADs are typically designed by diffusing a controlled n^+ enrichment in the center of the junction, beneath a highly doped shallow p^+ boron implantation in an n-doped well (**Figure 2D**). In the central region, the breakdown voltage is reduced, thus it acts as the active area, compared to the edge abrupt p^+n junction that presents a lower electric field. Instead of the enrichment, a doughnut-shaped

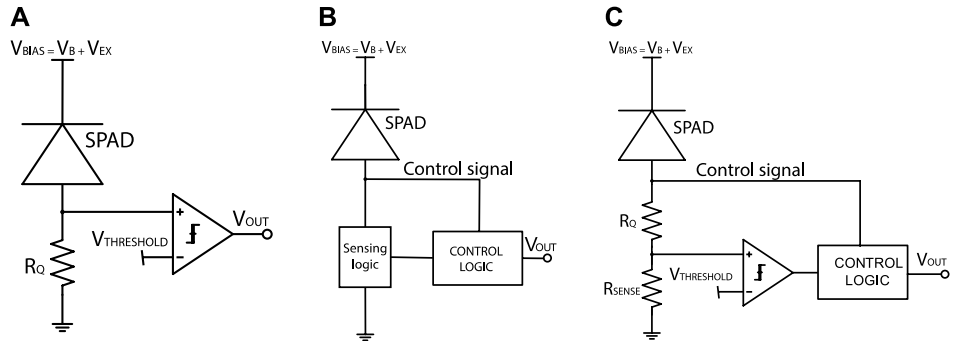

FIGURE 4 | Quenching circuits: example of passive quenching circuit **(A)**, block representation of an active quenching circuit **(B)** and of a Variable Load Quenching Circuit **(C)**.

p^- diffusion covering just the edge of the p^+ implantation can be used as a "guard-ring" to prevent edge breakdown. The depletion region can be about 0.3–1 μm thick across the active area, depending on the thickness and doping concentration of the n-well. The anode metal layer is laid out not only to contact the top p^+ implantation, but also to act as a pin-hole, thus exposing only the active area to the incident light, while shielding all the surrounding regions. The use of isolation techniques helps in protecting the circuit from the cathode high voltage also limiting the electrical crosstalk.

Besides the differences in technology, there are two approaches to illuminate the SPADs: Front-Side Illumination (FSI) and Back-Side Illumination (BSI). An insight is provided in Part II of this paper.

2.3 SPAD Modeling

A consistent model, able to predict the device behavior in all conditions, is fundamental in a solid workflow for designing the frontend circuit. A starting point for the SPAD model structure is the one proposed in [47] which represents a good approximation of the SPAD main operation principles. As illustrated in **Figure 3**, its schematic includes two parallel branches: the first one composed of the series of the device resistance (R_D), the avalanche switch, and the V_B voltage generator, while the second one composed of the junction capacitance (C_J). R_D is the diode internal resistance given by the sum of the space-charge layer resistance (R_{SCL}) and the ohmic resistance of neutral regions crossed by the avalanche current (R_{SERIES}) [13]. Its value depends on the device structure varying from a few hundred ohms up to some kΩ: the smaller the active area and the wider the undepleted silicon, the higher the resistance gets. The switch emulates the avalanche, getting closed when an avalanche occurs and opened when the avalanche is quenched. C_J is the junction capacitance, which is the capacitance of the depleted region, which varies with the SPAD bias voltage and the selected SPAD geometry, with typical values ranging from fF to pF. In addition, there are two stray capacitances, C_{ANODE} and $C_{CATHODE}$ (connected respectively to anode and cathode sides), which take into account parasitisms of the SPAD cross-section. The values of every single parameter of the SPAD model are usually estimated through TCAD simulations or measured on fabricated devices. Even more sophisticated models can be found in the literature, based on Verilog-A language, in which a mimic of statistics and noise is introduced [48–51].

3 SPAD FRONTENDS

3.1 Passive Quenching Circuits

The Passive Quenching Circuit (PQC) consists in a simple resistor (R_Q) connected either to the SPAD cathode or anode and often followed by a comparator to provide a digital output (**Figure 4A**). Basically, after triggering an avalanche, a huge current starts flowing through the resistor, which creates the voltage drop equal to V_{EX} required to bring the SPAD at a bias equal to V_B, thus interrupting the avalanche current [13, 52, 53]. It is possible to distinguish two different phases in the PQC operation: quenching and reset transitions. These two phases raise a trade-off on the optimum value of the quenching resistor (R_Q), as it will be clarified in the following discussion. During the quenching phase, the depleted capacitance (C_J) is discharged, undergoing a voltage drop equal to V_{EX}, on the other hand the anode or cathode parasitic capacitance is charged with the same amount. A high value of the resistance is suitable for reducing the quenching time after the event detection, promptly producing the appropriate voltage pulse. The avalanche current flowing in the junction (I_D) is characterized by an exponential decrease in which the reached peak value is $I_{D_{peak}} = \frac{V_{EX}}{R_D}$, while the steady state value and the time constant are given by the following equations:

$$I_{D_{steady\ state}} = \frac{V_{EX}}{R_D + R_Q} \cong \frac{V_{EX}}{R_Q}$$

$$\tau_Q = \left(C_j + C_{stray}\right)\frac{R_D R_Q}{R_D + R_Q} \approx \left(C_j + C_{stray}\right)R_D$$

Typically, R_Q is some order of magnitude higher than R_D, justifying the approximation done in both expressions.

Considering the avalanche physics, when the voltage across the diode is approaching V_B, the impact ionization probability decreases, and consequently also the number of carriers in the

depleted region decreases. Being a statistical process, to have a negligible probability of electron-hole pairs creation in the high-field region, the current value should drop below a threshold value, namely $I_{latching}$, usually in the order of 100 μA [13], thus R_Q is sized in order to assure an $I_{D_{steady\ state}}$ lower than $I_{latching}$. If $I_{D_{stady\ state}} << I_{latching}$, the quenching has a sharp and quick slope, guaranteeing a safe operation of the device. Thus, focusing on the quenching phase, the best option is to use a very high value for R_Q so that the avalanche is quenched immediately, the power consumption is reduced, and the output pulse rising edge is fast enough to limit the timing dispersion. However, after quenching, the initial bias of C_j must be restored, also discharging the parasitic capacitance at the anode or cathode side (reset phase). This process follows an exponential decay of the current dependent on R_Q, characterized by a time constant equal to τ_r:

$$\tau_r = R_Q \cdot \left(C_j + C_{stray}\right)$$

Thus, a high value of R_Q results in a long reset phase, with a related limitation of the maximum count rate. To optimize both the quenching and reset phase, the typical values of R_Q range from tens of kΩ to hundreds of kΩ.

An intrinsic drawback of the PQC is the non-controlled hold-off time of the SPAD, in fact during the reset phase another photon can trigger a new event, with different probability depending on the excess voltage across the SPAD, which increases during the reset. These pulses keep the output of the comparator always high, thus causing significant count losses. In integrated solutions, the quenching resistor can be implemented for instance with poly-resistors, or, in order to reduce the area consumption, with transistors working in their ohmic region, even though they introduce some limitations in terms of maximum V_{EX}.

3.2 Active Quenching Circuits

To overcome PQC limitations, the Active Quenching Circuit (AQC) has been proposed, the first one is described in [31]. The avalanche sensing, the quenching and the recharge phases rely on active components (**Figure 4B**), not suffering from a time-dependent excess voltage, and introducing a well-defined SPAD deadtime. The main disadvantage of AQCs is that the avalanche may be detected with a non-negligible delay. The sources of this delay come from the SPAD time constants and the active circuit bandwidth and gain limitations. If the introduced delay is too long, the current will flow for a consistent amount of time at its peak value, with a consequent increase of the current flowing across the junction which negatively impacts SPAD figures of merit (**Section 4**) [54]. In addition, the avalanches triggered during the reset phase are not detected until this phase is concluded (the higher the stray capacitance, the longer the rest time), increasing the power consumption. Initially, AQCs were designed with discrete components, as in [55], then also integrated configurations have been introduced [54, 56].

3.3 Variable Load Quenching Circuits

A mixed approach for the quenching circuit, called Variable Load Quenching Circuit (VLQC), has been proposed [57] to combine both advantages of PQCs and AQCs, exploiting a passive-active quenching and an active reset solution (**Figure 4C**). During the first phase of the avalanche a passive load starts to quench the SPAD, after a while an active feedback is activated and helps the quenching increasing the resistive load. This kind of quenching solution allows the introduction of an additional current which helps in charging and discharging the moving nodes during the quenching phase. This additional current is coming from the active reaction of the circuit after the electronics has sensed the avalanche, i.e., the threshold of the active feedback is overcome. Thus, this double mechanism helps in solving the quenching resistance value trade-off, without introducing a substantial parasitic capacitance, resulting in a well-controlled recharge time even with a high value quenching resistance. Another advantage is the absence of the delay typical of AQCs, indeed in VLQC the passive quenching starts working immediately. On the other hand, VLQCs require a lot of the area of the pixel reducing the active area. The trend is now to find ways to reduce the VLQC area either by minimizing the number of transistors, as in [58, 59], or by exploiting 3D-stacking solutions [17, 60].

3.4 Gated Frontends

One more quenching solution technique is called gated frontend, where the action of the circuitry is to enable or disable very quickly the detector. In this operation, a gate-window in which the SPAD can detect photons is defined. This feature is typically used to time-filtering the useful signal from noise or background. However, these advantages are at the expense of a larger circuit area and higher power consumption to charge and discharge the SPAD capacitances at each gate cycle. Much more details about the gated operation are available in [55, 61–63].

4 SPAD FIGURES OF MERIT

The digital nature of SPADs operation overcomes the problem of excess noise and read-out noise typical of APD devices. However, SPADs have other non-ideal behaviors that must be carefully characterized: other noise sources (namely, thermal generation, band-to-band tunneling, and afterpulsing), a limited light sensitivity which varies with the light wavelength, and a timing response which varies with absorption position.

4.1 Noise Sources

Commonly, thermal generation and band-to-band tunneling effects are characterized together as Dark Count Rate (DCR), defined as the mean value of the output pulse rate when no light interacts with the sensor. Note that the DCR value has a Poisson statistical distribution and cannot be easily subtracted from the measured detection rate since its statistic variation remains.

DCR strongly depends on temperature, usually becoming more than double when the temperature increases by 10°C around room temperature [64] (as in the example shown in **Figure 5A**), since at this temperature thermal generation is the dominant noise source. According to the Schockley-Read-Hall theory, electron-hole pairs are generated in sequence through generation–recombination centers that are local levels at about

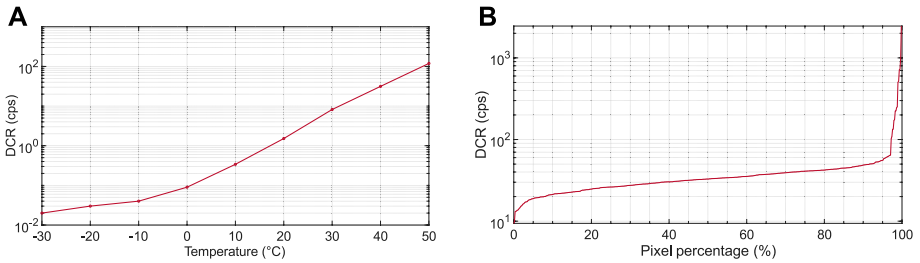

FIGURE 5 | Example of variation in DCR for different temperatures for a single SPAD **(A)**, DCR distribution in a SPAD array **(B)**. In this case, hot-pixels are pixels with a DCR higher than 32 cps, corresponding to roughly 3% of the pixels.

mid-gap. The presence of traps, whose number depends on the implantation process, increases the probability of thermal generation [10]. Thus, the reduction of ion implantation-induced defects by additional annealing is essential for achieving low DCR [65].

The contribution to DCR due to the Poole–Frenkel effect and trap-assisted tunneling does not increase significantly with temperature but instead increases with excess bias. This contribution is usually the dominant one in SPAD architectures with high-doping junctions (i.e., a low V_B) [10].

In order to measure DCR, the device is kept in dark and the number of avalanches per second is counted. For SPAD arrays characterization, it is common to report the cumulative distribution function of DCR, as in the example shown in (**Figure 5B**). This plot depicts the statistics of the DCR among different pixels, in particular the average DCR value and the percentage of noisy SPADs. Noisy pixels, called hot-pixels, are usually defined as the pixels with a DCR higher than twice the median value. Usually, DCR is reported normalized by the active area.

DCR is not correlated with the photon-detection rate, whereas afterpulsing is. During an avalanche, deep level traps present in the detector can capture carriers and release them after a well-defined time (namely the trap release lifetime) [66]. If a carrier is released when the SPAD is fully reverse-biased, a secondary avalanche (afterpulse) is generated. The lifetime can vary from a few nanoseconds to several microseconds and decreases at higher temperatures [67, 68]. Consequently, conversely to DCR, a reduction of temperature has an adverse effect on afterpulsing since it increases the lifetime [10].

The afterpulsing probability is defined as the ratio between the number of afterpulsing events and the total number of events. In order to reduce afterpulsing, after each avalanche, SPADs are kept off for a time window of few nanoseconds (hold-off time, T_{ho}), so that the majority of the trapped carriers are released before rearming the SPAD. However, a long hold-off time lowers the maximum count rate to $\frac{1}{T_{ho}}$ or to $\frac{1}{e\tau_r}$, in case of AQC or PQC respectively.

The probability of having an afterpulse event depends on the number of carriers that flow during each avalanche. Thus, reducing the avalanche current (i.e., the charge per pulse) is fundamental to decrease the afterpulsing probability. A careful design of the SPAD layout and its frontend circuit can reduce the afterpulsing probability, in fact minimizing the parasitic capacitance associated with the SPAD terminals reduces the avalanche charge. Moreover, the number of deep level traps is lower in high-quality processes, which thus presents a lower afterpulsing probability.

Afterpulsing can be characterized through Time-Correlated Carrier Counting measurements [65, 69]: a histogram of inter-arrival times between two consecutive avalanche pulses is collected. The device must be kept in the dark or under constant illumination so that the event rate is low enough not to limit the maximum inter-arrival time. If no afterpulsing contribution is present, the inter-time trend follows a theoretical exponential distribution (red plot in **Figure 6A**), which can be subtracted from the measured one (blue plot in **Figure 6A**). The remaining events are divided by the total counts for computing the afterpulsing probability. The characterization should be repeated at different hold-off times.

4.2 Photon Detection Probability

Photon Detection Probability (PDP) is defined as the ratio between the number of detected photons and the number of photons impinging on the active area, thus it characterizes the SPAD light sensitivity. PDP depends on two main parameters: absorption probability and triggering efficiency [70]. The former is the probability that a photon is absorbed within the depleted region and depends on the detector reflectivity, the depth of the junction and the thickness of the depletion region, while the latter is the probability that a photogenerated electron-hole pair triggers a self-sustaining avalanche process and depends on the electric field (it increases with V_{EX}). Although some architectures have an enhanced efficiency in the infrared region to suit specific applications, silicon SPADs have typically high sensitivity in the visible spectrum with a peak in the 300–600 nm range, while their PDP abruptly decreases in the infrared region, as in the examples in **Figure 6B**. Commonly, PDP is measured by illuminating the device with a light flux at a specific wavelength and the same flux is measured by an instrument with a known responsivity and the two results, after a proper calibration, are compared by normalizing for the areas of the detector. In this way, the result is independent of the geometrical characteristics of the detectors. Note that the light level should be low enough to work in the linear

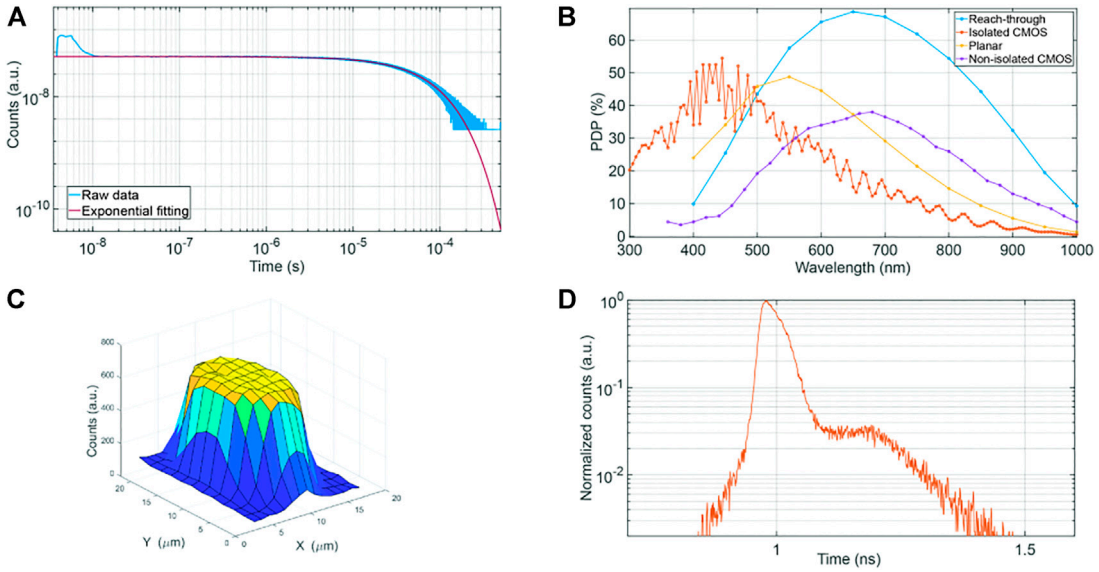

FIGURE 6 | Example of inter-arrival time histogram for measuring afterpulsing probability **(A)**, the acquired data are plotted in blue while the exponential decay is plotted in red. PDP of SPADs in different technologies **(B)**. In orange the PDP of a standard isolated CMOS SPAD [71], in yellow the one of a custom planar SPAD [37], in blue the one of a custom reach-trough by Excelitas [72], and in purple the one of a standard non-isolated CMOS SPAD [73]. The ringing present the standard isolated CMOS (orange plot) is due to the oxide layer which causes an interference pattern. Notice that the optimization of the superficial layers, for example by using an antireflection coating, is mandatory to maximize detection efficiency. Results of an active area uniformity test carried out by focusing a laser beam on a spot and scanning the SPAD **(C)**. Example of a SPAD IRF **(D)**.

region of the SPAD response, and the DCR should be subtracted from the measured number of events. The measurement is repeated at each wavelength extracting the complete curve (**Figure 6B**), which offers quantitative information on the SPAD capability of detecting single photons at each wavelength.

4.3 Active Area Uniformity

In order to ascertain SPADs active area uniformity and guard ring functionality, two measurements can be performed: Light Emission Test (LET) and laser beam scanning. During LET, the light emitted during the avalanches is observed with an infrared sensible camera with multi-second acquisition time (e.g., a CCD camera). The light emission is originated from the high field region and shows the uniformity of the field across the active area and possible problems like premature edge breakdown [74].

The extension of the active area can also be measured by focusing a laser beam on a spot smaller than the SPAD under test. The SPAD surface is then scanned recording the count rate per spot position. In this way, it is possible to measure the actual active area diameter and the variation in sensitivity across the device (**Figure 6C**).

4.4 Timing Jitter

A non-constant time delay between photon absorption and avalanche signal sensing causes a statistical temporal spread of the output pulse. The jitter in the arrival time detected for the single photon is commonly expressed by indicating the Full-Width at Half-Maximum (FWHM) of the SPAD Instrument Response Function (IRF). The IRF can be obtained by illuminating with a pulsed laser the SPAD and building a histogram with the time delays between a reference signal and the SPAD detections. An example of a SPAD IRF is shown in **Figure 6D**, with its two main components: the Gaussian peak and the exponential tail [75, 76]. Indeed, SPADs show different timing performance depending on the regions in which photons are absorbed. The impact ionization and diffusion of the electron-hole pairs in the depletion region translate into the peak, which is often fit with a Gaussian shape. On the other hand, the drift and diffusion of the minority carriers, generated by photons absorbed in the neutral regions, delay the avalanche triggering causing the exponential tail [76].

The shape of the IRF results distorted if the detected photon rate is too high, because of the pile-up distortion. To prevent this issue, for each laser pulse only one photon should be detected. A non-distorted IRF can be obtained by using a laser power low enough to trigger the SPAD in less than 5% of the pulses, so that, for the Poisson statistics, the probability to have two photons in the same pulse is completely negligible.

Being SPAD jitter strongly influenced by the behavior of the avalanche build-up and spreading phase, by lowering the frontend electronics sensing threshold, allowing to detect pulses when the avalanche is still at the beginning of the build-up phase, the timing jitter reduces, while it increases with detector size. Moreover, the jitter can be reduced by increasing excess biases or by carefully designing the electric field profile [75].

5 SINGLE SPAD PIXELS

Typically single SPAD pixel modules provide a digital output pulse every time a photon is detected and can be used for simple counting applications or be optimized targeting low timing jitter, gated or fast-gated operation and high-count rates. Indeed, single SPAD pixels are used in various fields such as single point scanning LiDAR [77], Non-Line of Sight (NLOS) imaging [78, 79], bioimaging and confocal microscopy [80], optical communication and Quantum Key Distribution [81], bucket detector in quantum Ghost Imaging [82], astronomic observation [83], and single-photon source characterization [84].

Single SPAD pixel modules are produced by many companies (e.g., MPD, Excelitas, Hamamatsu, ID Quantique, and PicoQuant) and are available on the market while scientific research is active to improve performance targeting specific applications.

High efficiency, especially in the NIR spectrum, is important when non-visible light must be used. Nevertheless, high PDP in the NIR is typically achieved with deep and thick junctions, which lead to impair the SPAD timing jitter. In [85] 60% PDP at 800 nm is achieved with a reach-trough SPAD by Excelitas that, combined with an integrated frontend circuit, performs only 235 ps timing jitter and an afterpulsing probability below 1.5% at 10 ns deadtime. Even lower jitters of 173 and 83 ps are obtained respectively with a BSI SPAD [86] and SPAD in custom technology connected to an integrated 180 nm CMOS frontend circuit [87] both performing 40% PDP at 800 nm.

Low timing jitter is important in many applications, such as LiDAR and even more in NLOS. The best timing jitter ever reported in literature is presented in [88], with only 7.8 ps jitter FWHM, including SPAD and frontend contributions, but at the expense of a very high DCR (2.8 kcps/μm^2) and extremely low PDP (8% peak). Low timing jitter of 27 ps FWHM, along with 60% peak PDP and 0.2 cps/μm^2 has been reported in [89].

The capability to fast enabling and disabling the SPAD (i.e., gating operation) is fundamental in NLOS and in many bioimaging techniques. Fast-gated SPAD pixels are reported in [90] (5 ns gate windows and 100 MHz gate frequency), and in [91] with State-of-Art performance in terms of gate window (500 ps) and gate frequency (160 MHz).

High dynamic range and high-count rate are required in LiDAR for background rejection, in quantum communication for achieving high-transmission rates and fluorescence imaging to collect high photon number without pile-up issues. Reducing SPAD deadtime negatively affects the afterpulsing probability, nevertheless low afterpulsing probability below 0.14% and 0.93 ns deadtime are reported in [92], allowing to reach a detection rate exceeding 1 Gcps. A SPAD module designed to surpass the pile-up limit in TCSPC is presented in [93] and its effectiveness is demonstrated in [94]. The module matches the SPAD deadtime with the laser period, providing a uniform probability to detect photons during the entire measurement FSR, thus allowing to obtain TCSPC histograms without distortion, even if the detection rate is higher than 5% (which typically is considered the limit for having negligible distortion).

When SPAD pixels are designed in order to be integrated in SPAD arrays, high fill-factor and small pitch are important parameters to allow the integration of many pixels in a small area. The exploitation of 3D-stacked technologies plays an important role in this route. In [95] the smallest pixel pitch (2.2 μm) ever presented in literature is reported. In the same work, also SPADs with 4 μm pitch are characterized, showing very good results such as 33.5% peak PDP, 2.5 cps median DCR and 88 ps timing jitter.

Expected future trends of SPAD pixels are reported in [96], suggesting that scaling pixel size for larger integrability in imagers will contribute to improving DCR and power consumption, but degrading other figures such as PDP and fill-factor.

6 CONCLUSION

This review shows the main characteristics, both in terms of technology and figures of merit, of SPADs, photodetectors that are acquiring more and more popularity for SPC and TCSPC applications. It also offers an overview of the advantages and drawbacks of different frontend circuits. This paper is followed by a second part which instead focuses on SPAD arrays, presenting different architectures and their exploitation.

AUTHOR CONTRIBUTIONS

IC, literature review, writing, review and editing of the full paper. DB, EC, AI, FM, AM., CN, SR, writing of a section of the paper. FV, paper organization, literature review and review of the full paper.

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