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A TCAD study on the effect of process parameters on silicon optical phase shifter performance

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On-chip integrated optical phase shifters are an important part of optical phase modulators. The performance of such modulators relies heavily on the phase shifter performance, which in turn depends on multiple process parameters. This paper reports the study of the effect of different process parameters on the performance of a silicon PN optical phase shifter obtained by process simulation using Silvaco® TCAD. The effect of dopant implantation dose, implantation energy, annealing temperature and time, wafer temperature, wafer tilt and rotation, and pre-amorphization on the phase and absorption of light is discussed. The 3-dB modulation bandwidth of a lumped phase shifter and the dependency of the performance metrics on different process parameters are presented. Monte Carlo numerical simulation shows that the free-carrier absorption has a much greater dependency on the process parameters than the phase shift. The study shows that ion channeling poses a limiting factor on the phase shifter performance, which can be improved by tilting the wafer or using a pre-amorphized substrate for implantation. The study shows that the 3-dB modulation bandwidth is highly dependent on the wafer tilt angle, rotation angle, and the lattice structure of the solid substrate. A bandwidth improvement of more than 5× is observed with 1.7× lower absorption for a pre-amorphized sample at −5 V compared to a crystalline sample with the same process flow.

KEYWORDS

phase shifter, photonics, process simulation, silicon, TCAD

1 Introduction

It is estimated that the photonic integrated circuit (PIC) industry will see a compound annual growth rate (CAGR) of 28.30% during 2020–2025 [1]. Compared to the traditional electronic integrated circuits (EICs), PICs are fast, have higher bandwidth, and are energy efficient. Silicon photonics is a vastly growing area with applications in medical [2], astronomy [3], communication [4], etc. The global silicon photonics market is expected to expand at a CAGR of 29.61% and is estimated to reach USD 4918.87 million by 2027. [5]. The rapid rate of increase in data traffic requires low-cost, high-bandwidth devices where silicon photonics provides a viable solution. Optical modulators modulate data that are sent *via* photons through a fiber. The silicon PN modulators are fast, and modulation occurs through the use of phase shifters using the free-carrier plasma dispersion (FCPD) effect [6]; [7]. The modulator characteristics are highly dependent on the phase shifter metrics, which are the phase shift, loss, and bandwidth. The two commonly used modulator structures, *viz.*, the Mach-Zehnder and ring/racetrack modulators have been widely investigated and huge amount of literatures are present [8]; [9,10]; [11]; [12]; [13,14]. Different driving configurations and architectures [15]; [16]; [17] have been investigated to realize

modulators with large modulation bandwidth, low energy-per-bit transmission, low bit-error-rate, and high extinction ratio.

Studies can be found in literature where different materials have been integrated in silicon platform to improve the device performance like electro-optic polymer [18], barium titanate [19], indium tin oxide [20] etc. However, such heterogenous integration techniques seldom resolves the trade-offs involved and results in design and fabrication complexity. Multiple studies can be found in literature where silicon optical phase shifter performance is optimized by adjusting the process parameters. A study of ion implantation condition on PN phase shifter performance can be found in [21] which took into account the effect of tilt angle and implantation energy. A U-shaped [22], and S-shaped [23] PN junction has been reported with enhanced performance by optimizing the implantation energy, dose, and tilt angle. The effect of P and N doping on the phase shift and absorption loss is reported in [24] along with the effect of the PN junction offset. However, all these studies focussed on a limited number of process parameters, and a thorough study, including the tradeoffs between phase shift, loss, and bandwidth, have not yet been reported so far to the best of the authors' knowledge.

The phase shifter performance depends on the fabrication process flow and can be tuned by tuning the process parameters accordingly. Multiple tradeoffs are involved, and the effect of different parameters needs to be taken into consideration. Changing the process parameter values changes the phase shift, loss, series resistance, and junction capacitance. Designing a phase shifter with higher phase shift and lower loss may result in lower modulation bandwidth despite having a smaller size. Therefore, it is important to study the degree of dependency of the performance metrics on different process parameters and to tune them accordingly. Virtual fabrication ensures fabrication-ready design by incorporating practical effects in the design steps. Process simulation is a virtual fabrication tool that takes the effect of different fabrication parameters into the device design. This ensures that the device performance upon fabrication is close to the simulated results. Process simulation allows the flexibility of tuning multiple parameters to enhance the device performance. Over the years, multiple models and tools have been developed to accurately predict dopant implantation, diffusion, annealing, damage accumulation, *etc.* [25]; [26]; [27]; [28]; [29]. These constitutes the technology computer-aided design (TCAD) simulation of different electronic and optoelectronic devices. Multiple studies have been done using TCAD tools to optimize and design different devices and technologies [30]; [31]; [32]; [33].

In this paper, TCAD simulation is done to study the effect of different process parameters like wafer temperature, implantation dose, implantation energy, wafer tilt, wafer rotation, annealing temperature and time, and pre-amorphization on a silicon optical PN phase shifter performance. Process simulation, as well as device simulation, is carried out and the effect of each parameter on the phase shift, free-carrier absorption (FCA), and the 3-dB modulation bandwidth is presented and discussed. A reference PN phase shifter is designed, and the effect of different parameters on the performance is quantified by comparing with the reference phase shifter. The PN phase shifter process steps, structure, and metrics are given in Section 2. Section 3 presents the process parameter study, and Section 4 gives a comparison and discussion of the effect of different process parameters on the phase shifter performance. Section 5 concludes the paper. A supplementary file is provided with this manuscript, which gives the effect of different process parameters on the phase shifter resistance and capacitance. The study presented in this manuscript focuses on how different parameters affect the optical PN phase shifter performance at the process level and identify the limiting factors to realize an efficient phase shifter by tuning the process parameters accordingly. Designing and optimizing the modulator performance that includes a different set of performance metrics is beyond the scope of this study.

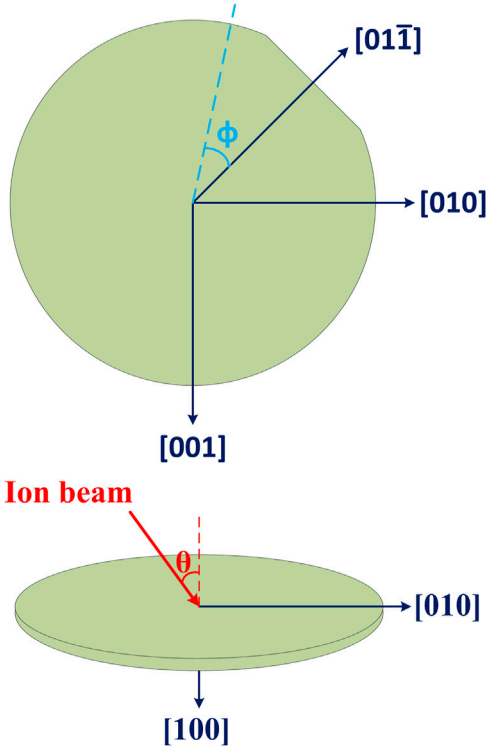

FIGURE 1
(A) Top-view and **(B)** side-view of SOI wafer depicting orientation and different crystallographic axes used in this paper.

2 Phase shifter simulation

A 220 nm silicon-on-insulator (SOI) wafer with 2 μm buried oxide (BOX) and 500 μm bottom silicon is used in this study. The SOI wafer orientation used in this paper is shown in Figure 1 with the different crystallographic directions. A <100> intrinsic crystal is used with wafer flat along [01$\bar{1}$] direction as shown in Figure 1A. The wafer rotation angle is denoted by ϕ, which is measured counter-clockwise from the wafer flat direction. The [100] direction is into the paper in Figure 1A. Figure 1B shows the 3D side view with the ion beam direction tilted at an angle θ with the wafer normal. It should be kept in mind that Figure 1B is descriptive only, and the ion beam is actually vertical. θ is defined as the wafer tilt angle.

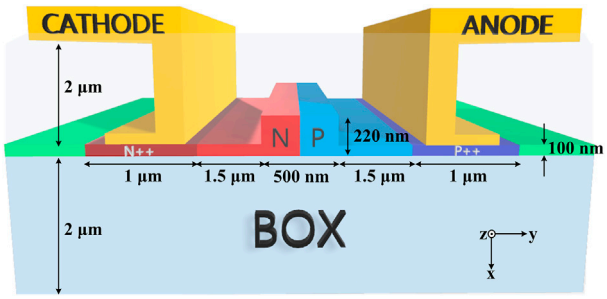

FIGURE 2
3D front view of the silicon phase shifter (not to scale).

When dopants are implanted, the collision between the dopant atoms and host (silicon) atoms leads to lattice damage [28]. Dopants that rest in interstitial sites are inactive and need to substitute the bonded silicon atom sites to be electrically active and contribute to electrical conduction. To recrystallize and activate the dopants, annealing is done whereby the wafer is subjected to high temperature for a short duration of time [34]. The annealing step provides energy to the dopant atoms/ions and leads to the broadening of the as-implanted profile due to diffusion. In this study, Monte Carlo analysis is used with the ion implantation being modeled by the binary collision approximation (BCA) [35]; [36]. During annealing, different regions having different dopant and defect concentrations recrystallize leading to dopant-interstitial and dopant-vacancy pair creation. The analysis of defect cluster formation is important for devices used in high-speed applications [28]; [37].

The effect of different parameters on phase shifter performance is quantified by comparing it with a reference phase shifter. The wafer orientation for the reference phase shifter is same as shown in Figure 1 with $\theta = 0$ and $\phi = 0$. The PN junction is formed by single implantation of boron and phosphorus with a dose of $2 \times 10^{13}\,\mathrm{cm}^{-3}$ each, which is below the amorphization threshold [26]. The implantation energy is selected to be 17 keV and 25 keV for boron and phosphorus, respectively. The wafer is kept at room temperature (20 °C), and the beam divergence is 1°. To form the rib structure, a 120 nm anisotropic etch is performed, keeping the waveguide width 500 nm. To form the anode and cathode, highly doped P++ and N++ regions are formed to ensure ohmic contacts. The P++ and N++ regions are formed with an implantation dose of $1 \times 10^{15}\,\mathrm{cm}^{-2}$ using boron and phosphorus with the energy of 3 keV and 10 keV, respectively. Each of the implantation steps is followed by rapid thermal annealing (RTA) at 1,100 °C for 10 s in a nitrogen ambient. The top cladding is formed by depositing 2 μm silicon dioxide. Vias are created over the P++ and N++ regions, followed by the deposition of aluminum to form the anode and cathode, respectively. The PN phase shifter structure is shown in Figure 2.

The PN phase shifter is operated in reverse bias with carrier depletion leading to a change in the refractive index. The change in the carrier concentration changes the refractive index and the FCA, which is given by Soref for 1,550 nm wavelength as [6]; [38].

$$\Delta n(x,y,V) = -\left[8.8 \times 10^{-22}\Delta N_e(x,y,V) + 8.5 \times 10^{-18}\left(\Delta N_h(x,y,V)\right)^{0.8}\right] \tag{1a}$$

$$\Delta\alpha(x,y,V) = 8.5 \times 10^{-18}\Delta N_e(x,y,V) + 6.0 \times 10^{-18}\Delta N_h(x,y,V) \tag{1b}$$

Where Δn and $\Delta\alpha$ are the changes in the refractive index and FCA coefficient, respectively. ΔN_e (ΔN_h) is the change in the electron (hole) concentration with applied reverse bias voltage.

The change in the mode effective index (Δn_{eff}) is given as [21]

$$\Delta n_{eff}(V) = \frac{\int_x\int_y \Delta n(x,y,V)|E(x,y)|^2\,dx\,dy}{\int_x\int_y |E(x,y)|^2\,dx\,dy} \tag{2}$$

where E is the mode electric field distribution.

The phase shift ($\Delta\varphi$) and FCA (α) can be calculated as

$$\Delta\varphi(V) = \frac{2\pi\Delta n_{eff}(V)L}{\lambda_0} \tag{3a}$$

$$\alpha(V) = \int_x\int_y \left[\alpha(x,y,0) - \Delta\alpha(x,y,V)\right]|E(x,y)|^2\,dx\,dy \tag{3b}$$

Where L is the phase shifter length and λ_0 is the free-space wavelength of light. The phase shifter is also characterized by the modulation efficiency, which is the product of voltage and phase shifter length required to obtain π phase shift, and is calculated as

$$V_\pi L_\pi(V) = |V| \times \frac{\pi}{\Delta\varphi(V)} \tag{4}$$

A lower value of the modulation efficiency corresponds to a better phase shifter. The phase shifter simulation and different parameter study is done using Silvaco® TCAD. Silvaco® Athena has been used for process simulation and Silvaco® Atlas for the device simulation. The phase shifter performance is analyzed for the 1,550 nm wavelength of operation. The small-signal analysis is done by extracting the admittance matrix at 50 GHz frequency. The frequency normalized impedance is calculated, and the 3-dB bandwidth is determined for a 50 Ω source and termination impedance when the phase shifter is driven as a lumped element [39]. The 3 dB bandwidth (f) is determined as

$$f = \frac{1}{2\pi RC_d} \tag{5}$$

where C_d is the PN depletion capacitance and R is the equivalent resistance by taking into account the source, termination, and the series PN resistance. A phase shifter with lower junction depletion capacitance and series resistance leads to higher modulation bandwidth. The reference phase shifter has a phase shift of 42° and FCA of 1.54 dB for a 1 mm long phase shifter at -5 V. The phase shifter modulation efficiency is 2.14 V cm with a 3-dB bandwidth of 7.15 GHz at -5 V.

3 Parameter study

This section presents the effect of different process parameters on the phase shifter performance, namely, phase

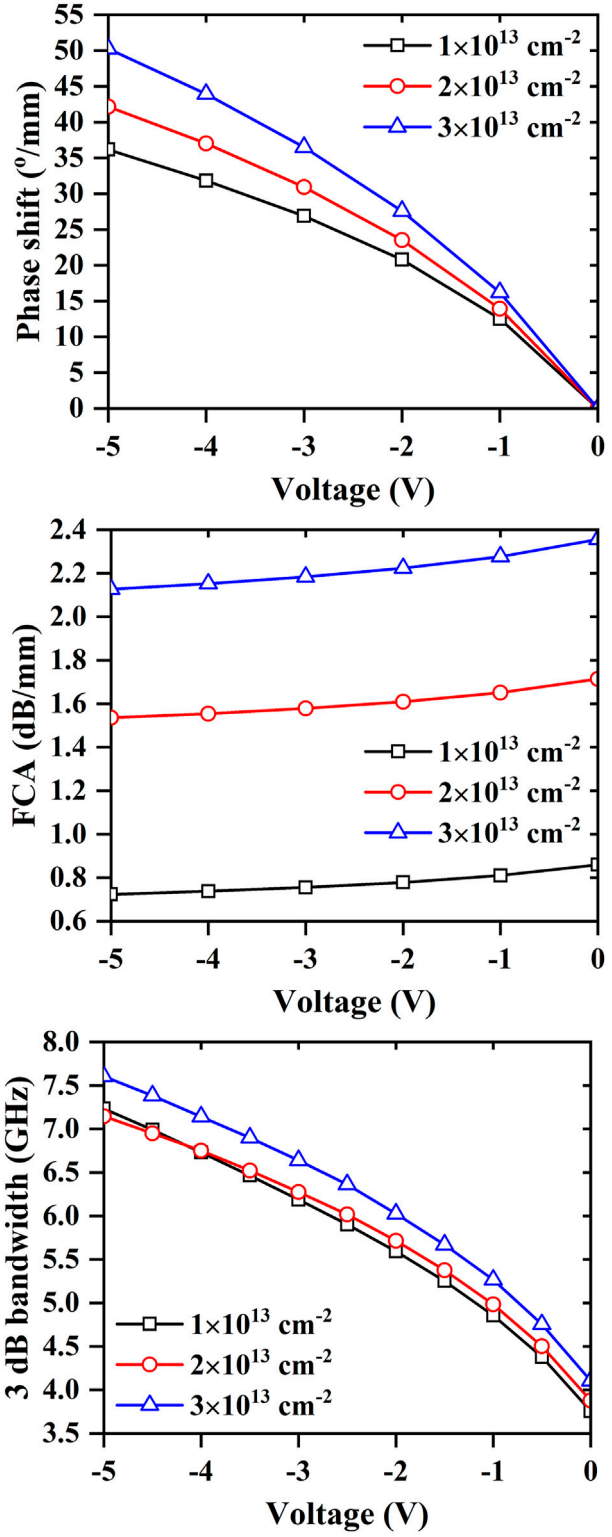

FIGURE 3
(A) Phase shift per unit length, **(B)** free-carrier absorption per unit length, and **(C)** 3-dB bandwidth for different implantation doses. The boron and phosphorus implantation dose is equal for each sample.

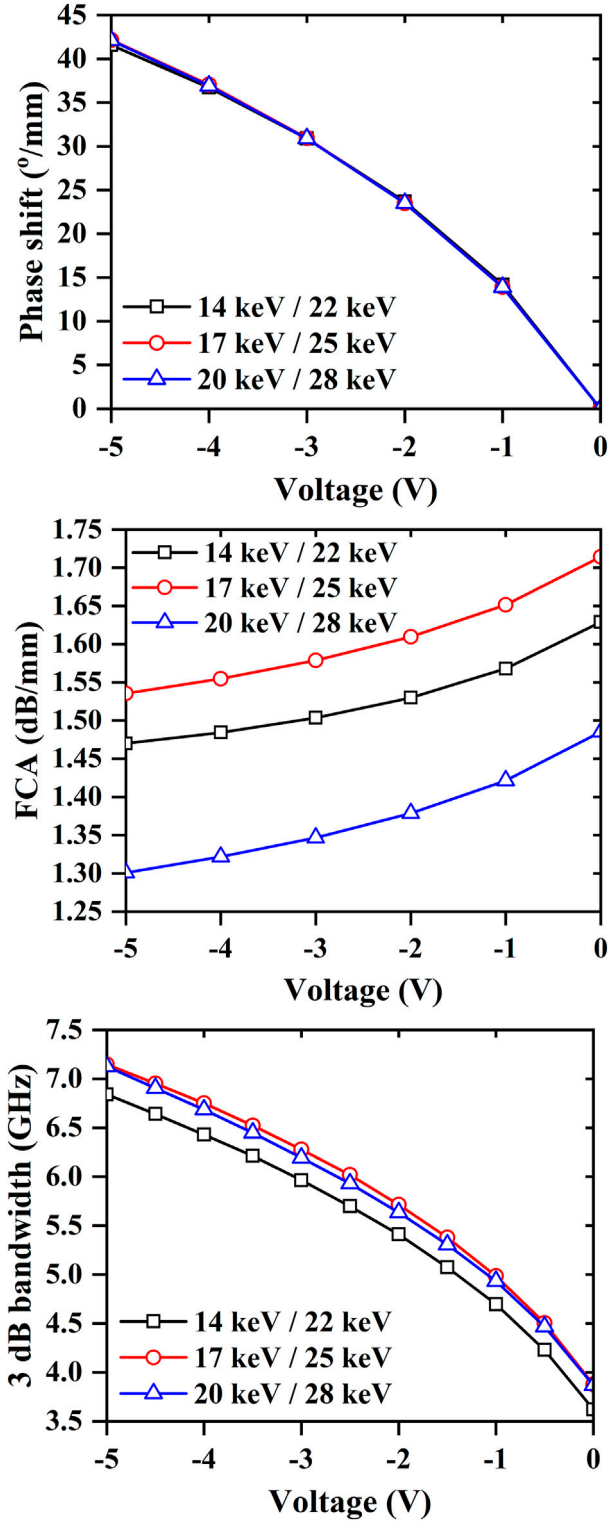

FIGURE 4
(A) Phase shift per unit length, **(B)** free-carrier absorption per unit length, and **(C)** 3-dB bandwidth for different boron/phosphorus implantation energies.

shift, absorption, and the 3 dB bandwidth as obtained using Silvaco® TCAD. The process parameters include the implantation dose, implantation energy, annealing temperature and time, wafer temperature, wafer tilt, wafer rotation, and substrate pre-amorphization. Performance comparison with different process parameters has been made

with the reference phase shifter to analyze and quantify the performance dependency on different parameters. In each of the parameter studies, only one parameter is changed, keeping all other parameters same as that of the reference phase shifter unless otherwise specified. The phase, absorption, and bandwidth for different parameter variations are shown in this paper. The phase shifter resistivity and capacitance curves are given in the supplementary file of this paper.

3.1 Implantation dose

Changing the implantation dose, changes the waveguide dopant concentration. The implantation profile is a Gaussian-like shape that broadens upon annealing. Same implantation doses of boron and phosphorus have been used to form the PN junction. The effect of three different implantation doses are evaluated, keeping the boron and phosphorus dose same in each case. The phase shift and FCA per unit length with three different implantation doses, *viz.*, 1×10^{13} cm^{-2}, 2×10^{13} cm^{-2} (reference), and 3×10^{13} cm^{-2} are shown in Figures 3A, B respectively. Increasing the dose increases the electron and hole carrier concentration, thereby increasing both the phase shift and absorption loss. Comparison between an implantation dose of 1×10^{13} cm^{-2} and 3×10^{13} cm^{-2} shows that for 3× increase in dose, the phase shift and absorption increases by 1.39× and 2.96× respectively at -5 V. The phase shifter resistance and capacitance is given in the Supplementary Figure S1 respectively. The 3-dB bandwidth for different implantation doses are shown in Figure 3C. The bandwidth change is negligible with the change in the implantation dose. The bandwidth increases to 7.6 GHz for a dose of 3×10^{13} cm^{-2}. The bandwidth improvement is only ~6.3% compared to the reference phase shifter at 5 V reverse bias.

3.2 Implantation energy

Changing the implantation energy changes the peak position of the implantation profile. The implantation energy of both boron and phosphorus is changed by ± 3 keV from that of the reference phase shifter. The phase shift and FCA loss per unit length for different implantation energies is shown in Figures 4A, B respectively. The figure legend shows the "boron energy/phosphorus energy". Three different samples with different boron/phosphorus energies, *viz.*, 14 keV/22 keV, 17 keV/25 keV (reference), and 20 keV/28 keV, have been simulated. Similar phase shifts are observed for all three samples. However, the absorption loss of the three samples is different, with the highest absorption occurring for the reference phase shifter. The lowest absorption is for the 20 keV/28 keV implantation energy and is 1.18× lower than the reference phase shifter. The absorption depends on the modal overlap of free electrons and holes. For the reference phase shifter, the carrier concentration at the mode maxima is larger than for the other two samples. Supplementary Figure S2 of the supplementary file shows the phase shifter resistivity and capacitance curves. The phase shifter bandwidth is shown in Figure 4C, from which it can be observed that the bandwidth decreases to 6.84 GHz for the lowest implantation energy.

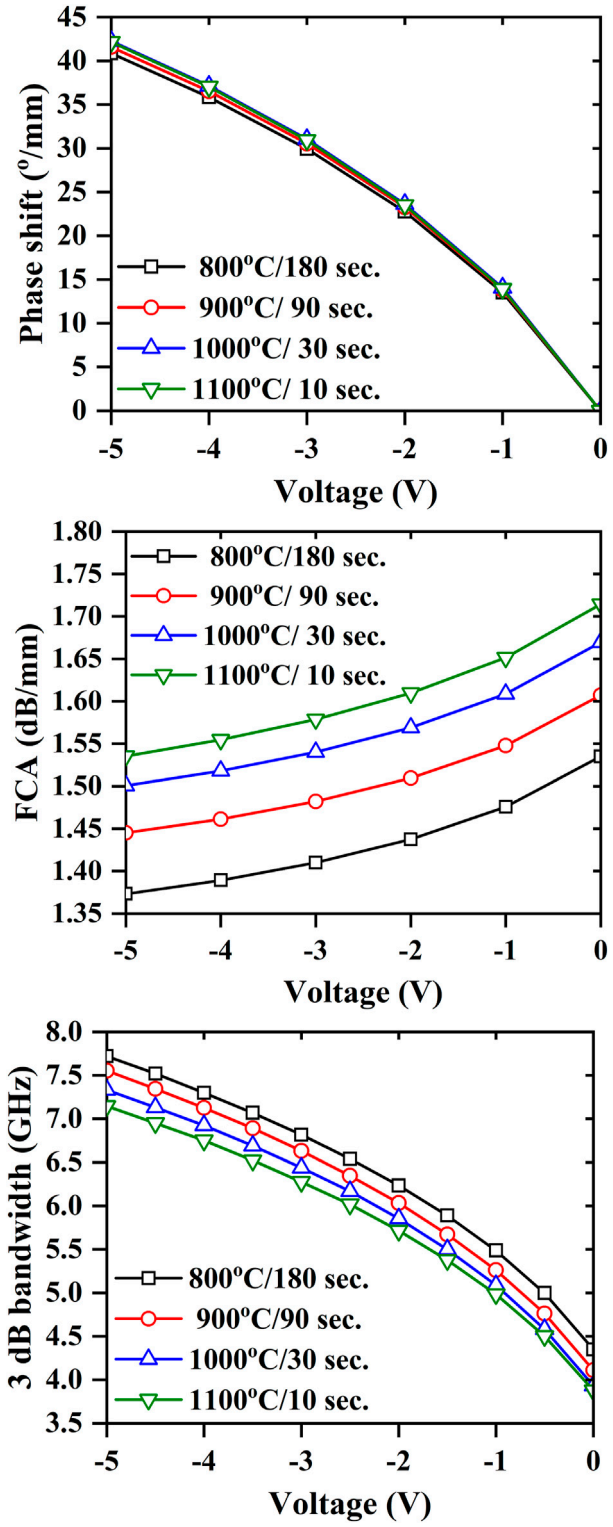

FIGURE 5
(A) Phase shift per unit length, **(B)** free-carrier absorption per unit length, and **(C)** 3-dB bandwidth for different annealing temperature/time.

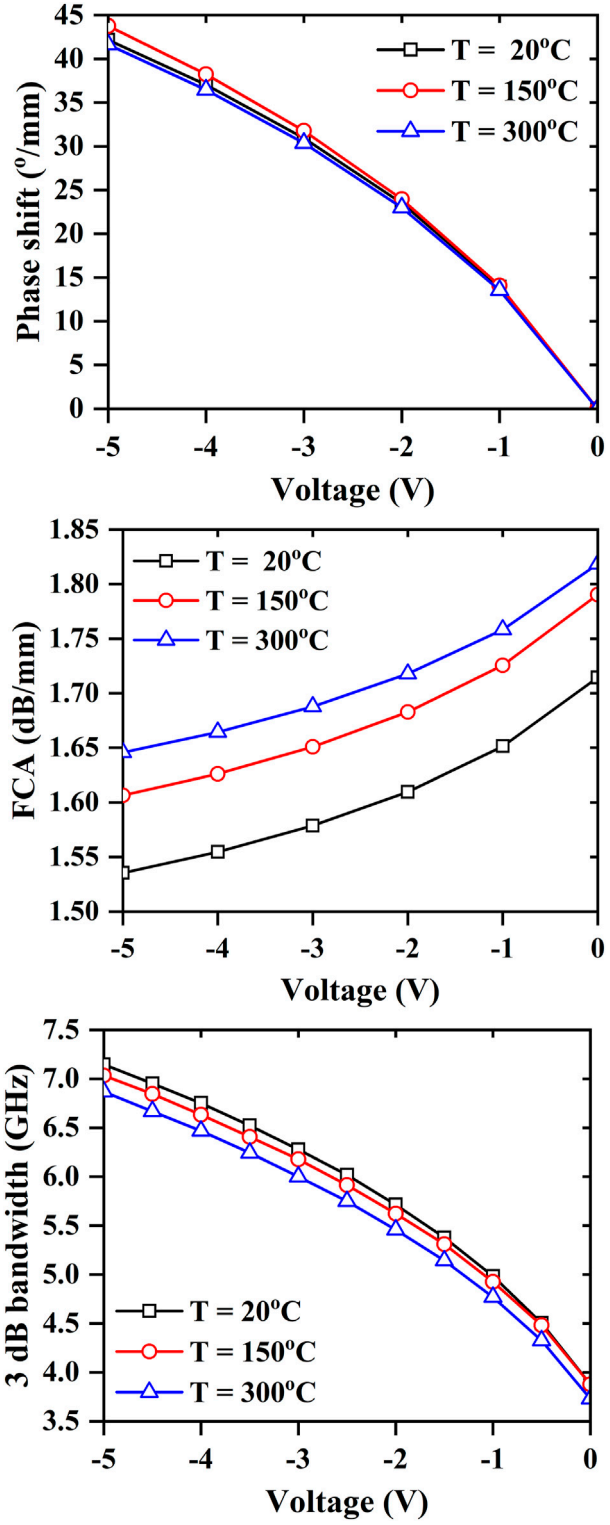

FIGURE 6
(A) Phase shift per unit length, **(B)** free-carrier absorption per unit length, and **(C)** 3-dB bandwidth for different wafer temperatures.

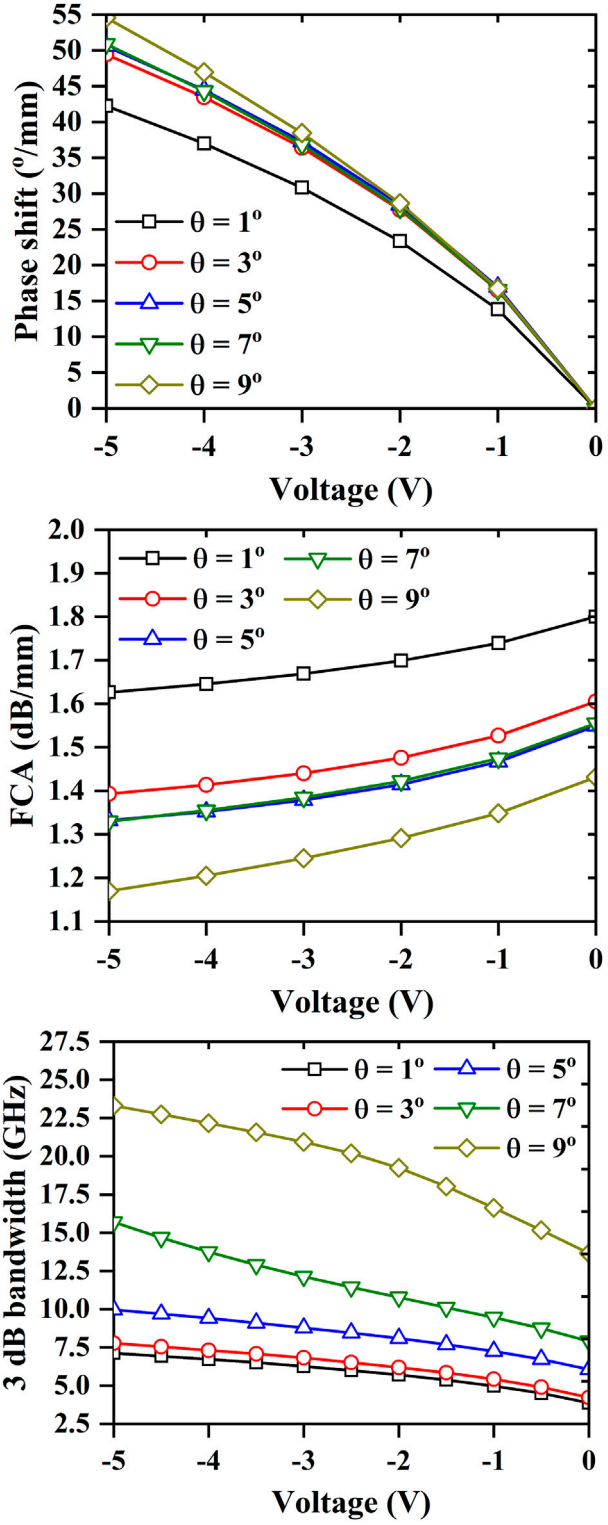

FIGURE 7
(A) Phase shift per unit length, **(B)** free-carrier absorption per unit length, and **(C)** 3-dB bandwidth for different wafer tilts.

3.3 Annealing temperature and time

As discussed previously, annealing is required for wafer recrystallization and dopant activation. Annealing at different temperatures for different times leads to different doping and damage concentration profile. Also, as-implanted profile broadening takes place during annealing by damage and dopant diffusion [40]. Four different annealing conditions have been

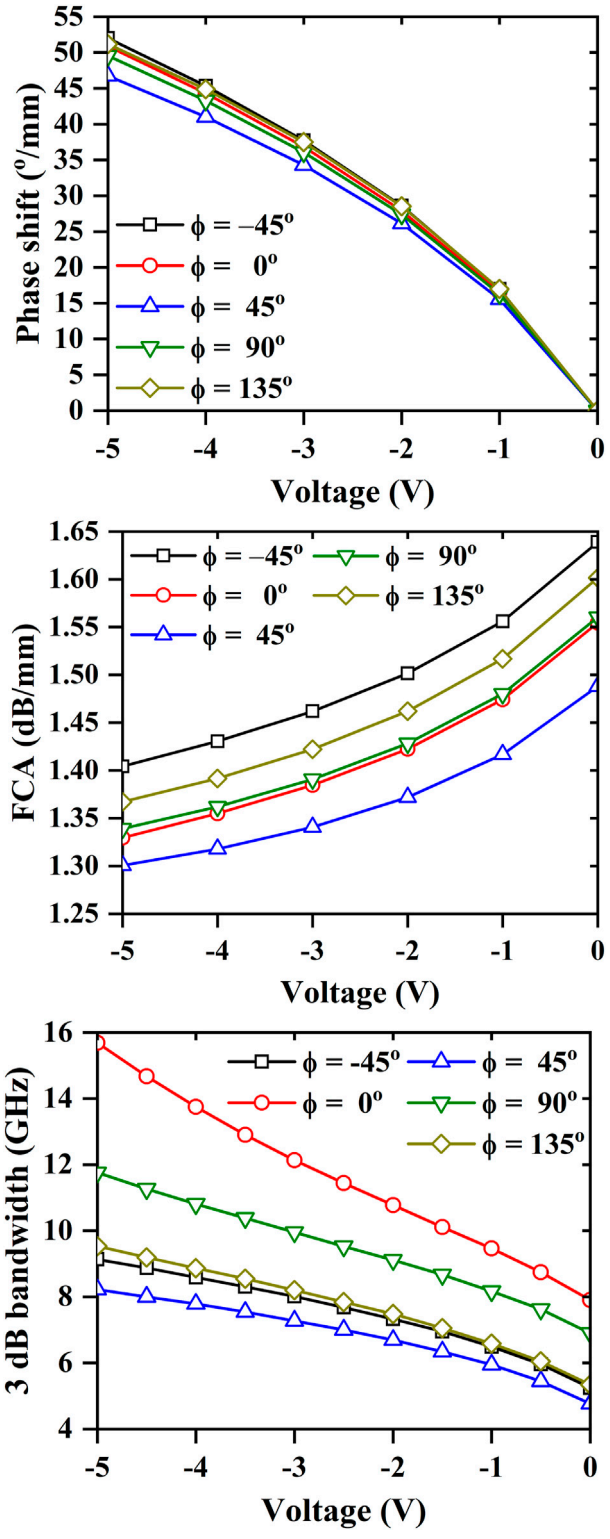

FIGURE 8
(A) Phase shift per unit length, **(B)** free-carrier absorption per unit length, and **(C)** 3-dB bandwidth for different wafer rotations at 7° tilt.

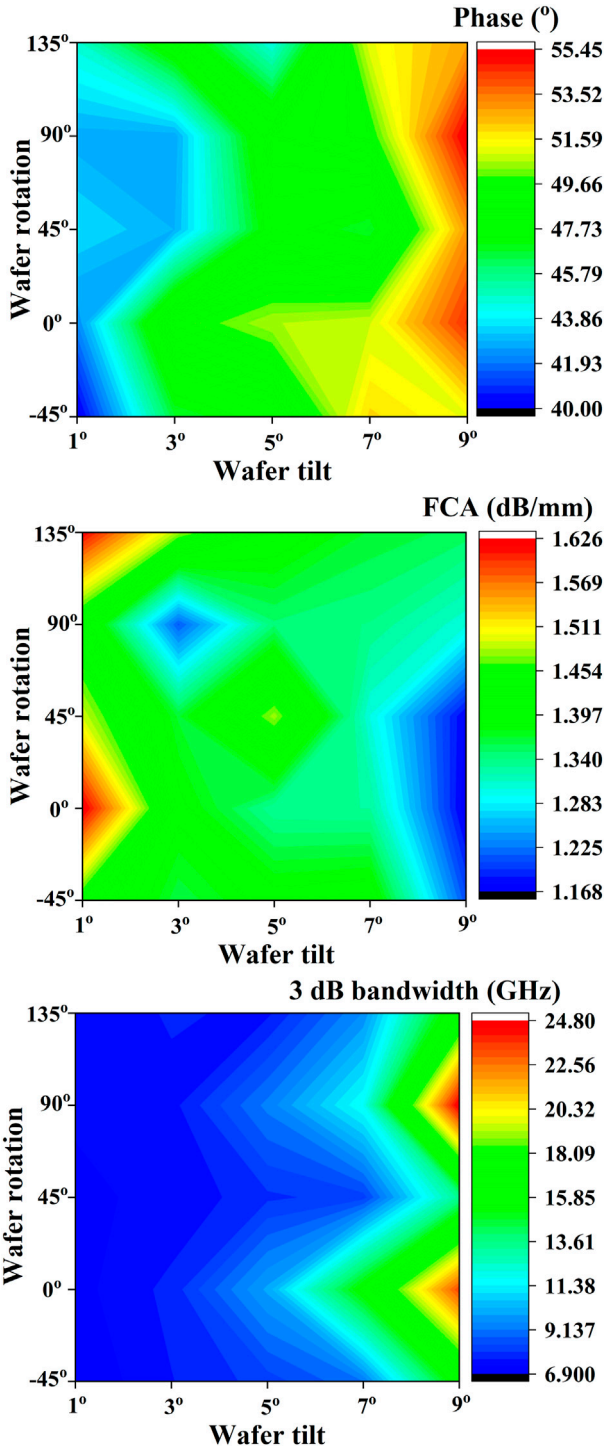

FIGURE 9
Image plot of **(A)** phase shift per unit length, **(B)** free-carrier absorption per unit length, and **(C)** 3-dB bandwidth at -5 V as a function of the wafer rotation and wafer tilt angles.

evaluated: 800 °C for 180 s, 900 °C for 90 s, 1,000 °C for 30 s, and 1,100 °C for 10 s (reference). The phase shift and FCA per unit length curve for the different annealing conditions are shown in Figures 5A, B respectively. The effect of different annealing temperature and time on the phase shift is negligible. However, compared to the reference phase shifter, lower temperature, longer duration annealing leads to 1.12× lower absorption loss. The phase shifter

resistivity and capacitance of all the samples are shown in Supplementary Figure S3 of the supplementary file. Figure 5C shows the 3-dB bandwidth of all four samples. It is observed that the bandwidth improves as the annealing temperature decreases and the duration increases. An improvement of ~8% has been observed for the sample annealed at 800 °C for 3 min compared to the reference sample.

3.4 Wafer temperature

Dopant implantation on a heated sample results in a broadened as-implanted doping profile due to dopant diffusion. The wafer temperature is varied from 20 °C (room temperature) to 150 °C and 300 °C. The phase shift and FCA loss per unit length are shown in Figures 6A, B respectively for different wafer temperatures. Increasing the wafer temperature increases the absorption loss with negligible change in the phase shift. An increase of 7.1% in absorption loss is observed at -5 V when the wafer temperature is changed from 20 °C (reference) to 300 °C. Supplementary Figure S4 in the supplementary file presents the phase shifter resistivity and capacitance curves for different wafer temperatures. The phase shifter bandwidth for the three samples are shown in Figure 6C. The bandwidth decreases with an increase in temperature. A 4% decrease in bandwidth at -5 V is observed for 300 °C heated wafer compared to the wafer at room temperature.

3.5 Wafer tilt

The lattice structure plays an important role in the channeling of dopant atoms or ions [41]. As dopants are implanted, the ions travel through the crystallographic planes. Different planes have different atomic density, due to which the degree of ion channeling is different in different directions. If a particular crystallographic axis provides larger ease of ion travel, the as-implanted profile is broadened with a lower concentration Gaussian peak. For an ion beam perpendicular to the <100> wafer surface, the ion channeling is more. As the wafer is tilted, ion channeling reduces, thereby leading to less profile broadening and higher peak concentration. The wafer tilt (θ) is varied from 1° to 9° in steps of 2°, and its effect on the phase shifter performance is evaluated. Large variation in phase shift as well as absorption loss per unit length can be seen in Figures 7A, B for different tilt angles. The phase shift is ~ 54.6°/mm for θ = 9° which is ~ 1.3× more compared to θ = 1°. The FCA per unit length is ~ 1.4× lower for 9° tilt compared to the 1° tilted wafer. The resistivity and capacitance curve of the phase shifter for different θ is shown in Supplementary Figure S5 of the supplementary file. The modulation bandwidth of the lumped phase shifter is shown in Figure 7C. Huge bandwidth improvement is observed as θ increases. With an equal change in θ, a non-linear increase in bandwidth can be observed. Compared to the reference phase shifter, a 3.26× increase in the 3-dB bandwidth for 9° tilted wafer can be observed at 5 V reverse bias.

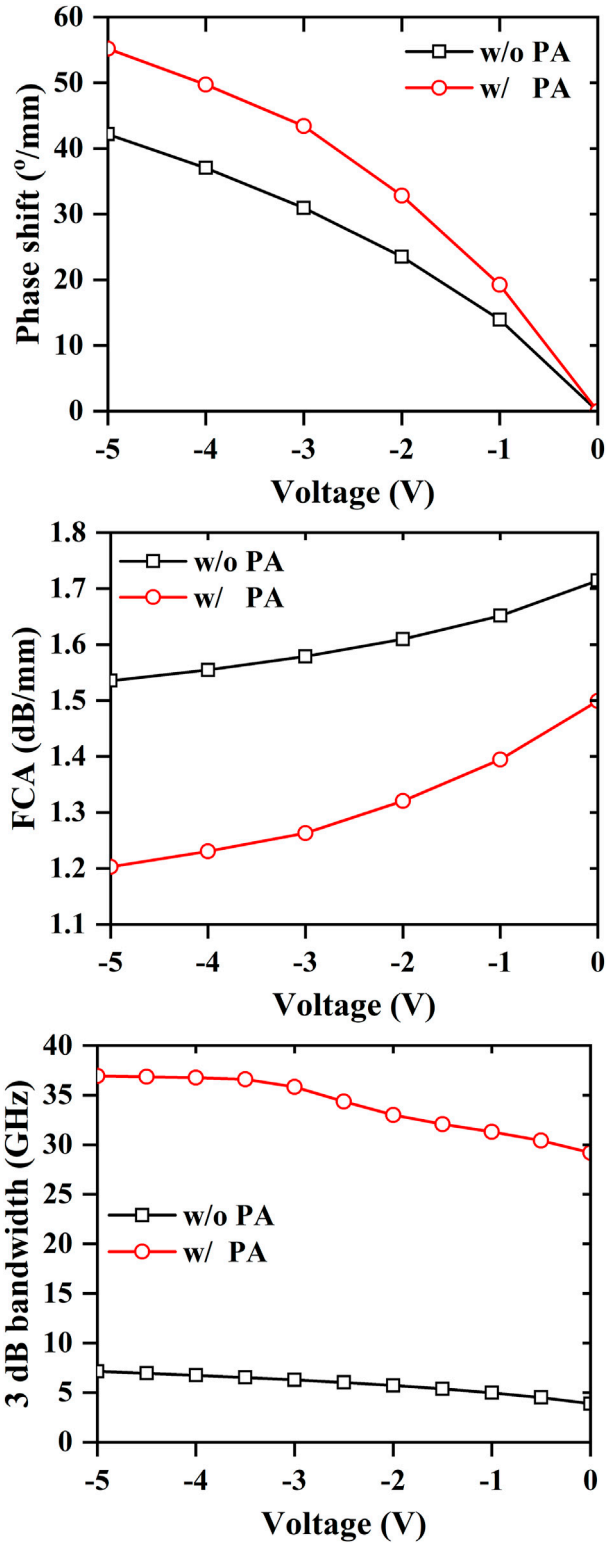

FIGURE 10
(A) Phase shift per unit length, **(B)** free-carrier absorption per unit length, and **(C)** 3-dB bandwidth for crystalline and pre-amorphized wafer (w/o PA: without pre-amorphization; w/PA: with pre-smorphization).

3.6 Wafer rotation

From the previous subsection, it can be observed that lower ion channeling leads to lower absorption and higher bandwidth. Here, the effect of wafer rotation on the phase shifter performance is evaluated for a 7° tilted wafer. The wafer is rotated 180° in steps of 45° starting from ϕ = -45°, for which the [01$\bar{1}$] direction shown in Figure 1A is along the *y*-axis of Figure 2. The phase shifter performance for different ϕ is shown in Figure 8. The maximum change in the phase shift and FCA occurs when ϕ = -45° and ϕ = 45°. Compared to ϕ = -45°, a 1.11× lower phase shift and 1.08× lower absorption per unit length is obtained for ϕ = 45° when the wafer flat is perpendicular to the *y*-axis of the phase shifter. Supplementary Figure S6 shows the resistivity and capacitance curves of the phase shifter for different rotation angles. The 3-dB modulation bandwidth is shown in Figure 8C from which it can be observed that maximum bandwidth of ~15.7 GHz at -5 V occurs when ϕ = 0°. For ϕ = 45°, the bandwidth decreases to ~8.2 GHz.

Wafer tilt and rotation during dopant implantation leads to a large variation in the bandwidth as seen from Figure 7C and Figure 8C. The image plot of the phase, absorption, and the 3 dB bandwidth for different wafer rotation and tilt angles at -5 V are shown in Figure 9A–C respectively. The lowest (highest) phase shift occurs for ϕ = -45° (ϕ = 90°) and θ = 1° (θ = 9°). The lowest (highest) FCA occurs for ϕ = 0° (ϕ = 45°) and θ = 9° (θ = 1°). The lowest (highest) 3 dB bandwidth occurs for ϕ = -45° (ϕ = 90°) and θ = 1° (θ = 9°). In all cases, the highest phase, lowest absorption, and largest 3 dB bandwidth occurs at 9° wafer tilt. The corresponding change between the highest and lowest values of the phase shift, FCA, and 3 dB bandwidth are ~ 1.39×, ~ 1.27×, and ~ 3.58×, respectively.

3.7 Pre-amorphization

Another effective way to stop ion channeling is to use a pre-amorphized wafer for implantation instead of tilting the wafer [42]. The substrate to be doped can be amorphized before dopant implantation by implanting silicon/germanium [43], carbon [44], or argon [41]. Thereafter, dopants are implanted into the amorphous host, followed by annealing. Comparison has been made between two phase shifters, one with a crystalline host (reference) and the other with an amorphous host. The phase shift and absorption loss per unit length is shown in Figures 10A, B respectively. The pre-amorphized sample has 1.31× higher phase shift and 1.28× lower FCA per unit length compared to the reference phase shifter. The PN phase shifter resistivity and capacitance of both samples are shown in Supplementary Figure S7 of the supplementary file. The modulation bandwidth is shown in Figure 10C for both samples, and it can be observed that the pre-amorphized sample has a 3-dB bandwidth of ~37 GHz at -5 V, which is 5.17× higher than that of the reference phase shifter.

4 Discussion

From the previous section, it can be observed that each of the parameters have different effects on the phase shift, loss, and bandwidth. The phase shift is less dependent on the implantation energy, annealing, wafer temperature, and wafer rotation angle. The free-carrier absorption is dependent on all the process parameters taken in this study. The bandwidth is highly dependent on wafer tilt angle, rotation angle, and whether the host is crystalline or amorphous. The performance comparison of different process parameters is given in Table 1 at 5 V reverse bias voltage and phase shifter length for π phase shift. Increasing the implantation dose results in better modulation efficiency but at the expense of higher absorption. The bandwidth dependency is negligible for the simulated doses. A higher implantation energy results in low loss with no impact on the modulation efficiency. However, the FCA loss is dependent on the modal overlap with the free-carriers, and different implantation energy results in different depth profiles and, as such, will also depend on the waveguide dimension. A high-temperature, short-duration anneal results in better modulation efficiency but with higher loss and lower bandwidth.

TABLE 1 Performance comparison of different process parameters at -5 V.

Name	Value	$V_\pi L_\pi$	FCA	Bandwidth
		(V.cm)	(dB)	(GHz)
Implantation	1×10^{13}	2.49	3.58	7.23
dose (cm^{-2})	#2×10^{13}	2.14	6.55	7.15
	3×10^{13}	1.79	7.63	7.60
Implantation	14/22	2.17	6.37	6.84
energy (keV)	#17/25	2.14	6.55	7.15
	20/28	2.14	5.55	7.13
Annealing	800 °C/180 s	2.21	6.04	7.72
temperature	900 °C/90 s	2.17	6.28	7.55
and time	1,000 °C/30 s	2.13	6.39	7.33
	#1100 °C/10 s	2.14	6.55	7.15
Wafer	#20	2.14	6.55	7.15
temperature (°C)	150	2.06	6.62	7.03
	300	2.16	7.13	6.87
Wafer tilt	#0°	2.14	6.55	7.15
	1°	2.13	6.94	7.13
	3°	1.82	5.06	7.77
	5°	1.78	4.73	9.97
	7°	1.77	4.71	15.69
	9°	1.65	3.86	23.31
Wafer rotation*	-45°	1.73	4.84	9.14
	0°	1.77	4.71	15.69
	45°	1.93	5.01	8.22
	90°	1.82	4.86	11.76
	135°	1.76	4.82	9.53
w/o PA#		2.14	6.55	7.15
w/PA		1.63	3.91	36.94

#reference phase shifter; *7° tilted wafer; PA: pre-amorphization.

Implantation at room temperature results in low loss and high bandwidth compared to when the wafer is heated. The wafer tilt angle results in a marked difference in the phase shifter performance metrics. A large θ results in better modulation efficiency, low loss, and higher bandwidth. This is due to reduced channeling effect. For a 7° tilted wafer, rotating the wafer changes the performance metrics due to different degrees of channeling along different crystallographic planes. For the simulated phase shifter, $\phi = 0°$ results in low loss and high bandwidth. A ~ 1.2× better modulation efficiency, ~ 1.4× lower FCA, and ~ 2.2× higher bandwidth is observed for a phase shifter with $\theta = 7°$, $\phi = 0°$ compared to a phase shifter with $\theta = 0°$, $\phi = 0°$ (reference). Implantation on a pre-amorphized substrate gives a ~ 1.3× better modulation efficiency, ~ 1.7× lower loss, and more than 5× higher bandwidth compared to implantation on a crystalline substrate (reference). The study shows that while the phase shifter performance metrics have different degrees of dependency on the process parameters, ion channeling is the main limiting factor. Tilting the wafer or amorphizing the substrate before implantation can greatly enhance the performance.

5 Conclusion

A process parameter study has been implemented in simulation using Silvaco® TCAD software to investigate the performance of a silicon optical PN phase shifter. The effect of the implantation dose, implantation energy, wafer temperature, annealing temperature and time, wafer tilt, wafer rotation, and pre-amorphization on the phase shift, absorption loss, and modulation bandwidth has been discussed. It has been observed that the phase shifter modulation bandwidth has a high degree of dependency on the wafer tilt, wafer rotation, and pre-amorphization compared to other process parameters. The ion channeling mechanism is found to be a limiting factor in the phase shifter performance and can be overcome by tilting or amorphizing the wafer. Compared to a reference phase shifter with 0° tilt and crystalline substrate, a 7° tilted crystalline wafer and a 0° tilted pre-amorphized wafer has 1.2× and 1.3× better modulation efficiency, 1.4× and 1.7× lower absorption, and 2.2× and 5.17× higher bandwidth at -5 V. Comparison of the 9° tilted sample and the pre-amorphized sample shows that both have the same modulation efficiency and free-carrier loss, but with 1.6× higher 3-dB bandwidth for the pre-amorphized sample at -5 V.

Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

Author contributions

DM and RS contributed to the conception, design, and analysis of the study. DM performed the simulations. All authors contributed to manuscript revision, read, and approved the submitted version.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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Supplementary material

The Supplementary Material for this article can be found online at: https://www.frontiersin.org/articles/10.3389/fphy.2023.1123885/full#supplementary-material

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