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Enhancing responsivity of silicon PIN photodiodes at 1064 nm via light trapping and geometry optimization: a simulation study

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Nd:YAG laser light detection at 1064 nm is widely used in applications requiring high-performance photodiodes to measure low light intensities. This study investigates the impact of light trapping and geometric variations on the responsivity of silicon-based PIN photodiodes at 1064 nm. Simulations using Ansys Lumerical FDTD and CHARGE reveal several key findings. Without diffuse reflectors, the responsivity of the photodiodes aligns with theoretical and literature values of approximately 0.4–0.45 A/W. When rear-side diffuse reflectors are used, larger photodiode dimensions result in higher responsivity, with a peak of 0.58 A/W for photodiodes with a 400 µm thickness. Our simulations suggest that combining light trapping with optimized geometries or side reflectors could surpass the current responsivity ceiling of ~0.57 A/W, offering a pathway to exceed this limit without sacrificing electrical performance. Also, light trapping reduces the required thickness of Si PIN photodiodes for achieving specific responsivity at 1064 nm. For instance, 100 µm thick photodiodes with diffuse reflectors exhibit a responsivity of approximately 0.31 A/W, compared to 0.28 A/W in 400 µm thick photodiodes without reflectors. However, the enhancement from light trapping diminishes as photodiode thickness increases. Optimal photodiode dimensions for balanced performance are suggested to be a thickness of 200–300 µm and an area of 0.6–2.5 mm^2. Experimental validation is recommended to assess texturing-related effects, such as increased dark current or recombination.

KEYWORDS

silicon PIN photodiode, responsivity, near-infrared light, black silicon, light trapping, numerical simulation

1 Introduction

The Nd:YAG laser light (1064 nm wavelength) is critical in various fields, including medicine [1], environmental monitoring [2], spectroscopy [3], and defense and security [4]. Consequently, photodetectors based on different semiconductor materials, such as InGaAsP/InAlAs [5], p-BP/n-$PdSe_2$ [6], InN/GaN [7], TiS_3 [8], or silicon [9] have been developed to detect 1064 nm light. The performance of a photodiode in detecting light within a specific wavelength range is primarily determined by its responsivity, defined as the ratio of the photodiode's output current to the incident optical power [10]. Thus, Silicon-based PIN photodiodes (PDs) are a preferred choice for such near-infrared detection due to their cost-effectiveness, scalability, and seamless integration with Complementary

Metal-Oxide-Semiconductor (CMOS) technology and silicon photonics [11]. However, the low absorption coefficient of silicon (~10 cm^{-1}) in the 1064 nm wavelength range poses a significant challenge for achieving high responsivity, which is essential for applications requiring high sensitivity to low-intensity light, such as environmental sensing or medical diagnostics [12, 13]. To measure low-intensity 1064 nm light using Si photodetectors, a common approach is to employ Si PIN PDs with a thicker substrate and depletion region, increasing the optical path length of the incoming light [12, 14]. However, silicon PIN PDs thicker than 500 μm are impractical due to degraded electrical performance, such as higher noise, slower rise times, and reduced bandwidth [14].

Several strategies have been demonstrated to improve the responsivity of Si PIN PDs at 1064 nm. First, Anti-Reflection Coatings (ARCs) are used to minimize the percentage of reflected light to below 1% (~30% reflection without ARC) [15]. Second, a rear-side specular reflector can be used to reflect light, thereby extending the optical path length without increasing the thickness of the detector [14]. Third, the optical path length can be maximized without increasing the physical path length, using rear-side texturing to create a diffuse reflector that increases the probability of light being scattered and reabsorbed within the detector, thereby enhancing light trapping [16, 17]. Fourth, the Si PIN photodiode's temperature can be increased using heat, which increases the silicon's absorption coefficient [18]. Fifth, the responsivity can be enhanced by optimizing the electrical parameters, such as increasing minority carrier lifetime and diffusion length and operating in full depletion mode (detector thickness Z ≈ depletion region width W) [11, 19]. Lastly, utilizing multiphysics simulation tools, like COMSOL and Ansys, can help in understanding and optimizing the photodiode's performance by modeling the effects of different designs and operational parameters on electrical and optical characteristics [13, 20].

While techniques like ARCs [15], specular reflectors [14], and texturing [16] could individually enhance responsivity, few studies systematically combine light trapping with geometric optimization (area and thickness) to maximize responsivity at 1064 nm while maintaining electrical performance within practical thickness limits (≤400 μm). This gap drives our study, which uses Ansys Lumerical FDTD and CHARGE to explore the synergistic effects of rear-side diffuse reflectors and dimensional variations, aiming to push responsivity beyond the current ceiling of ~0.57 A/W reported in the literature [16, 21]. To the best of our knowledge, the combined effects of light trapping and geometric parameters on responsivity at 1064 nm in this context have not been fully addressed in the literature. Thus, we use Ansys Lumerical FDTD and CHARGE to assess how rear-side texturing affects responsivity at 1064 nm across varying Si PIN photodiode dimensions. Therefore, we have incorporated ARCs, rear-side texturing, and full depletion mode in our simulated Si PIN PDs to figure out the maximum achievable responsivity of light detection at 1064 nm due to light trapping optimization. Simultaneously, our Si PIN PDs are designed with dimensional constraints to preserve favorable electrical characteristics, such as low noise, fast response times, and high bandwidth.

In this work, we have investigated how light trapping and geometric parameters of Si PIN PDs affect their responsivity, considering trade-offs in response time, bandwidth, and noise (e.g., dark current). Therefore, in section two, we briefly define the primary optical and electrical characteristics and the impacts of light trapping. Section three describes the setup for three structures of Si PIN PDs and specifies the parameters of the optoelectronic simulation. In section four, we present the findings and discuss the results.

2 Photodiode characteristics

This section outlines the optical and electrical characteristics of silicon PIN PDs critical to interpreting the simulation results at 1064 nm. These properties, such as responsivity, dark current, noise equivalent power (NEP), and rise time, define the performance trade-offs analyzed in this study. Section 2.3 also discusses the feasibility, impact, and fabrication methods of light trapping using specific micro- and nanostructures.

2.1 Optical characteristics

The responsivity is the main optical characteristic of a photodiode, and it describes its ability to convert incident optical power into electrical current and is the primary metric evaluated here. It is expressed as [15]:

$$R(\lambda) = \frac{\eta_e q}{hf} = \frac{\eta_e q}{h\left(\frac{c}{\lambda}\right)} = \frac{\eta_e q \lambda}{hc} = \eta_e \frac{\lambda[\mu m]}{1.24} \tag{1}$$

Where η_e is the external quantum efficiency, q is the electron charge, h is Planck's constant, and f is the frequency of the optical signal. $f = c/\lambda$ where c is the speed of light and λ is the wavelength of the incident light. For silicon at 1064 nm, the R(λ) for a photodiode depends heavily on η_e, as (q, λ, h, and c) are constants. Theoretically, with η_e = 100% (every photon absorbed produces a carrier), the maximum responsivity of a silicon PIN photodiode at 1064 nm would be: $R_{Max}(1.064) = 1 \times \frac{1.064}{1.24} = 0.858\,A/W$. However, in practice, η_e is never 100% at 1064 nm due to low absorption, reflection losses, and recombination. The external quantum efficiency is [22]:

$$\eta_e = \left(1 - R_f\right)\eta_i \tag{2}$$

Where R_f is the front reflection (~35% for bare silicon at 1064 nm, leading to η_e = 0.65 η_i [23], reducible to <1% with ARCs [15]) and η_i is the internal quantum efficiency. The η_i represents the carriers detected within the detector divided by photons entering the front surface. The η_i can be calculated using the following formula [10]:

$$\eta_i = \alpha \int_0^x P_D(x) e^{-\alpha x} dx \tag{3}$$

Where α is the absorption coefficient (α = 10 cm^{-1} at 1064 nm wavelength for silicon), $P_D(x)$ is the carrier detection probability, and x is the thickness of the depletion region. In the ideal case, $P_D(x)$ = 1. Thus, the formula can be simplified to [10]:

$$\eta_i = \alpha \int_0^x e^{-\alpha x} dx = 1 - e^{-\alpha x} \tag{4}$$

TABLE 1 Comparison of main features of the reported YAG photodiodes.

Detector	Active area (mm^2)	Responsivity (A/W) at 1060 nm	Dark current (nA)	Rise time (ns)	Noise equivalent power (pW/$\sqrt{Hz}$)
Si-PIN photodiodes without diffuse reflector					
Excelitas YAG-100AH [25]	5.6	0.44	11	12	0.08
OSI PIN-5-YAG [26]	5.1	0.4	10	18	0.012
Hamamatsu S3759 [27]	19.6	0.38	10	12.5	NA
Si-PIN rear side specular reflector 4TM10 [28]	19.6 (Area) and 525 μm (Thickness)	0.43	5	10	NA
Si-PIN photodiodes with diffuse reflector					
Si-PIN rear side diffuse reflector [14]	300 μm (Thickness)	0.46	10	NA	NA
Si-PIN rear side diffuse reflector [20]	3.1 (Area) and 200 μm (Thickness)	0.53	10	NA	NA
Si-PIN front side diffuse reflector [16]	13 (Area) and 300 μm (Thickness)	0.57	NA	NA	NA
Hamamatsu S15137 [17, 21]	19.6	0.57	10	12.5	NA

Thus, a thicker depletion region can substantially enhance the η_i of silicon PDs at 1064 nm. However, increasing the physical thickness beyond 500 μm is impractical due to degradation in essential characteristics like I_{dark}, *NEP*, and rise time τ_R [24]. Also, x can be increased directly to be almost equal to the photodiode thickness (Z ≈ x) by operating the photodiode in full depletion condition to achieve higher responsivity. In full depletion condition, the photodiode operates effectively as a photodetector. Thus, by substituting η_e from Equations 2–4 into Equation 1, the responsivity $R(\lambda)$ at 1064 nm can be estimated using the following formula:

$$R(\lambda) = \frac{1}{1.24} \times \lambda[\mu m] \times \left(1 - R_f\right) \times \left(1 - e^{-\alpha Z}\right) \quad (5)$$

From Equation 5, with ideal front reflection ($R_f \leq 0.01$) and physical thickness (Z = 0.5 mm), the responsivity of Si photodiode $R_A \approx 0.337$ A/W, which is much less than the reported responsivity (≥0.4 A/W) at 1064 nm for state of the art YAG PDs shown in Table 1. Therefore, it is necessary to use reflectors to increase the optical path length of the light within the Si PIN PDs. In full depletion condition, when a rear side specular reflector is used, the responsivity $R(\lambda)$ at 1064 nm can be estimated using the following formula [10]:

$$R(\lambda) = \frac{1}{1.24} \times \lambda[\mu m] \times \left(1 - R_f\right) \times \left(1 - e^{-\alpha Z}\right) \times \left(1 + R_r e^{-\alpha Z}\right) \quad (6)$$

However, based on Equation 6, the responsivity does not exceed 0.5 A/W (far below the theoretical maximum responsivity) of a fully depleted Si PIN photodiode with ($R_f \leq 0.01$) with an ideal rear side specular reflector ($R_r \approx 0.9$) and (Z = 0.5 mm).

2.2 Electrical characteristics

While high responsivity is critical for Si PIN PDs, other electrical characteristics are also essential for performance in low light intensity measurements, such as:

a. Low dark current I_{dark}: In wide depletion regions PDs, dark current is dominated by the recombination-generation current $I_{R\text{-}G}$, which is related to the product of area *A* and thickness *Z*, as shown in the equation [19, 29]:

$$I_{R-G} = \frac{qn_i}{2\tau_0} \times AZ \quad (7)$$

Where n_i is the silicon intrinsic concentration (10^{10} cm^{-3} at 300K), τ_0 is the carrier lifetime, *A* is the photodiode area, and *Z* is the photodiode thickness.

b. Low Noise Equivalent Power (NEP): The optical power needed to get a signal-to-noise ratio of 1. The NEP of a photodiode is defined as [30, 31]:

$$NEP = \frac{\sqrt{2q \times I_{dark}}}{R} \quad (8)$$

Where *q*, I_{dark}, and *R* are electron charge, dark current, and responsivity, respectively.

c. Short Rise time τ_R and high Bandwidth (BW) represent the photodiode response speed. Bandwidth has an inverse

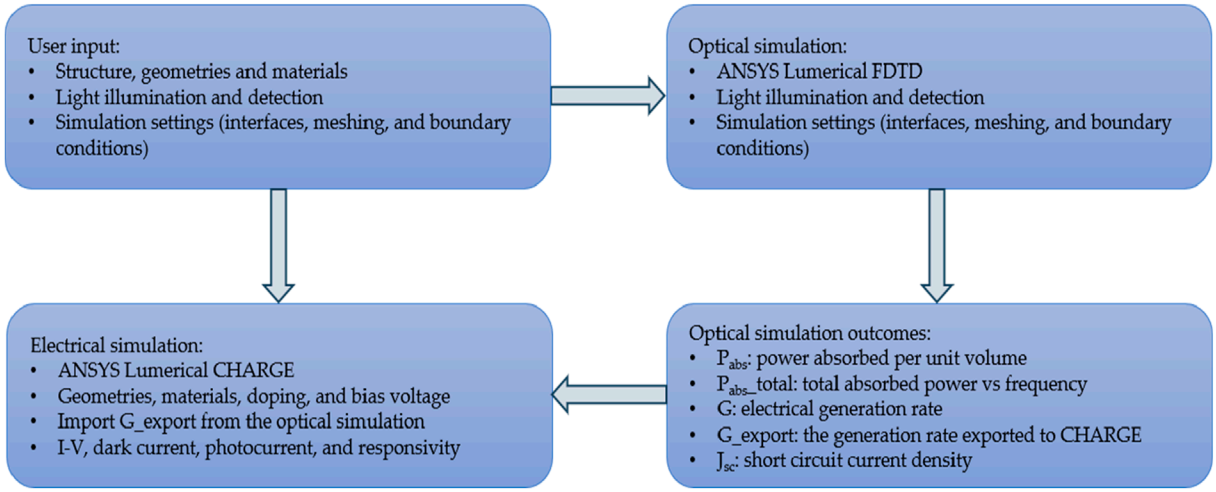

FIGURE 1
Simulation workflow for photodiodes using ANSYS Lumerical FDTD and CHARGE.

TABLE 2 Dimensions of the simulated Si PIN photodiodes.

Si PIN area (mm^2)	Si substrate thickness (μm)			
	100	200	300	400
0.16	PD100A	PD200A	PD300A	PD400A
0.64	PD100B	PD200B	PD300B	PD400B
2.56	PD100C	PD200C	PD300C	PD400C
10.24	PD100D	PD200D	PD300D	PD400D

relationship with the rise time according to the following equations [32–34]:

$$BW = \frac{0.35}{t_R} \tag{9}$$

$$t_R = \sqrt{{t_T}^2 + {t_C}^2} \tag{10}$$

Where BW, t_R, t_T, and t_C are bandwidth, rise time, transit time, and RC time constant, respectively. In full depletion condition:

$$t_T = \frac{Z^2}{905\, V_R} \tag{11}$$

$$t_C = 220\frac{\varepsilon_{Si} A}{Z} \tag{12}$$

$$\varepsilon_{Si} = 10^{-12} F/cm \rightarrow t_C = 2.2 \times 10^{-10} \times \frac{A}{Z}$$

Where V_R and ε_{Si} are reverse bias voltage and the absolute permittivity of silicon, respectively. Therefore, most characteristics of Si PIN PDs can be roughly estimated using Equations 7–12. These equations also highlight how geometries directly influence the characteristics of Si PIN PDs.

2.3 Feasibility and impact of light trapping

Light trapping techniques, such as surface texturing, significantly boost the responsivity of silicon PIN PDs up from the baseline range of ~0.45 A/W at 1064 nm, as shown in Table 1. However, texturing for light trapping may introduce electrical drawbacks, such as surface recombination, elevated noise, increased dark current, and longer response times, necessitating further investigations in fabricated devices [35]. Nevertheless, in the reported silicon PIN PDs, see Table 1, the responsivity at 1064 is improved significantly without degradation of the electrical characteristics [21]. On the other hand, inverted pyramid light-trapping structures, a nanoscale texture often used in black silicon (BSi), can be fabricated via lithography or metal-assisted chemical etching (MACE), with copper-assisted method [35], and Tang et al. highlight their adaptability through temperature-controlled sizing [36]. MACE is a scalable and cost-effective method, with variations like copper-assisted chemical etching being particularly effective for creating these structures [35].

3 Simulation methods

We studied the impacts of rear-side texturing on Si PIN PDs through a two-stage multiphysics simulation process, as explained in [37, 38]. Initially, we simulated the optical properties of the PDs using ANSYS Lumerical Finite-Difference Time Domain (FDTD). Next, we exported the results from ANSYS Lumerical FDTD into ANSYS Lumerical CHARGE to simulate the electrical properties. Figure 1 illustrates the simulation workflow for photodiode devices in this work.

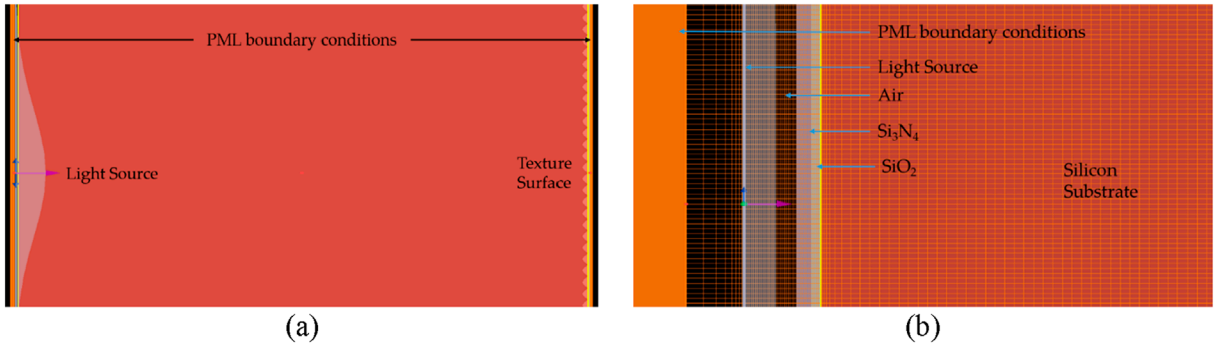

FIGURE 2
Cross-section of the simulated photodiodes: **(a)** front and rear side interfaces, and **(b)** components of the front side interface for all three structures.

3.1 Photodiode structures

Three distinct Si PIN photodiode configurations were simulated and evaluated:

a. Structure 1: No rear-side reflection ($R_r = 0$).
b. Structure 2: Specular rear-side reflection using a flat aluminum cathode ($R_r \approx 0.85$ or 85%).
c. Structure 3: Diffuse rear-side reflection using pyramidal structures (triangle in 2D with 53° angles between sides and base).

For all three structures, simulations were performed with varying areas and thicknesses, as outlined in Table 2. A total of 16 PDs with different geometries were simulated for each structure. The responsivity results from structures 1 and 2 serve to validate the accuracy of our simulation approach and compare them with those of structure 3. The responsivity values are analyzed to evaluate the impact of area, thickness, and light trapping via rear-side diffuse reflection. Each photodiode is labeled according to its geometric dimensions to ensure clarity, as outlined in Table 2.

3.2 Optical simulation

The key parameters of the optical simulation include boundary conditions, mesh configuration, and the position of the laser source. First, Perfectly Matched Layer (PML) boundary conditions are applied to absorb incident light with minimal reflection and to match the impedance with surrounding materials, thereby reducing reflections [39]. Second, Conformal Variant 0 is used as the mesh refinement method, leveraging Conformal Mesh Technology (CMT) for the aluminum to ensure better accuracy at the metal interfaces and the complex geometry of the pyramids [40]. Mesh sizes down to 5 nm at interfaces and up to 50 nm in the substrate ensure ±2% photocurrent accuracy [40], though finer meshes (<5 nm) could further reduce errors at a higher computational cost [41]. Third, the light source is positioned at the same height as the highest part of the PIN photodiode, with the anodes 400 nm above the silicon surface (270 nm above the upper layer of the ARC). The simulation setup is illustrated in Figure 2.

3.2.1 Front-side interface

All simulations of the PDs use normal incidence ($\theta = 0°$), a narrow wavelength band (1062 nm–1067 nm), and a Gaussian light source, as shown in Figure 2b. The optical power of the source is adjusted by multiplying the fixed light intensity by the variable areas of the PDs. Therefore, the optical power for PDs A, B, C, and D is 0.16 μW, 0.64 μW, 2.56 μW, and 10.24 μW, respectively. Additionally, the beam diameters correspond to 20% of the PDs width, with values of 80 μm, 160 μm, 320 μm, and 640 μm for PDs A, B, C, and D, respectively. Two layers of Anti-Reflection Coatings (ARCs) have been used in this work. The upper layer is Si_3N_4, and the lower layer is SiO_2, where the thickness is 80 nm and 50 nm, respectively [34]. This ARC assures little reflection of the incoming light at 1064 nm (≤0.1%), as shown in Figure 3a. Moreover, This ARC is tolerant to the variation of layer thicknesses during the fabrication process. Figure 3b demonstrates that the reflection is less than 3% if the total thickness of both layers ranges from (110 nm–150 nm).

3.2.2 Rear side interface

For Structure 1, which has no rear-side reflection ($R_r = 0$), an absorber boundary condition is applied to the rear side, the supposed position of the cathode, to prevent light reflection, as shown in Figure 4a. In Structure 2, where the rear-side reflection is $R_r = 0.85$, a flat aluminum cathode covers the entire rear side of the photodiode, with a thickness of 400 nm, as depicted in Figure 4b. For Structure 3, the PDs feature textured rear surfaces with aluminum pyramids (~0.66 μm height) on the flat aluminum cathode (0.4 μm thickness). These textures have been formed using aluminum pyramids (triangles in 2D with 53° angles between sides and base), as illustrated in Figure 4c. This pyramid structure was selected because it can be fabricated using black silicon methods, as mentioned in Section 2.3, and subsequent metallization techniques [42–44]. Specifically, inverted

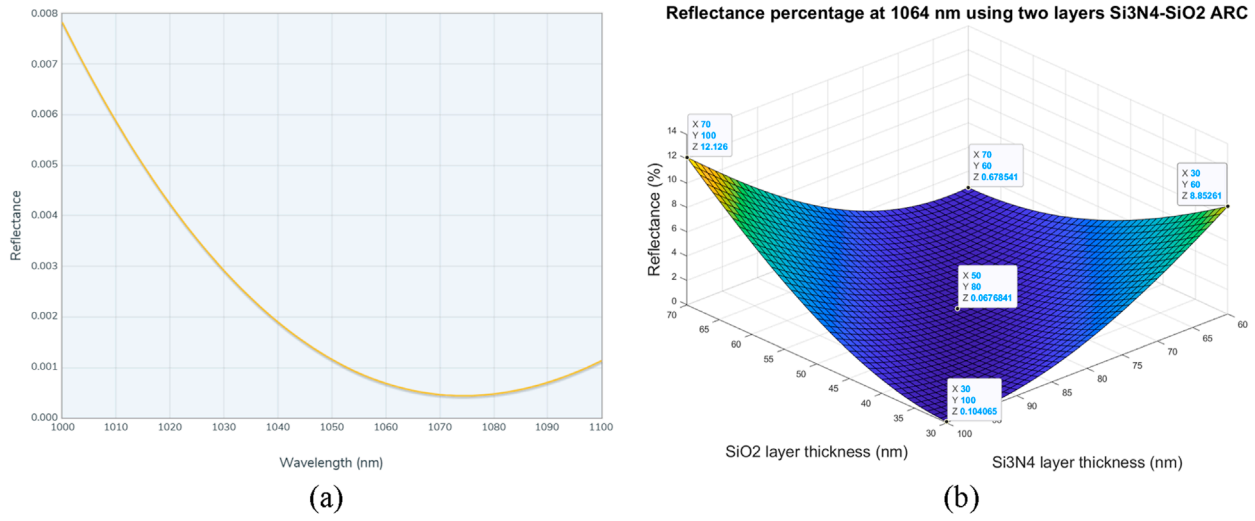

FIGURE 3
The reflectance percentage at 1064 nm using two layers **(a)** Si_3N_4-SiO_2 ARC, where Si_3N_4 is 80 nm, and SiO_2 is 50 nm, and **(b)** Si_3N_4-SiO_2 [Si_3N_4 80 nm ± 20 nm] and [SiO_2 50 nm ± 20 nm].

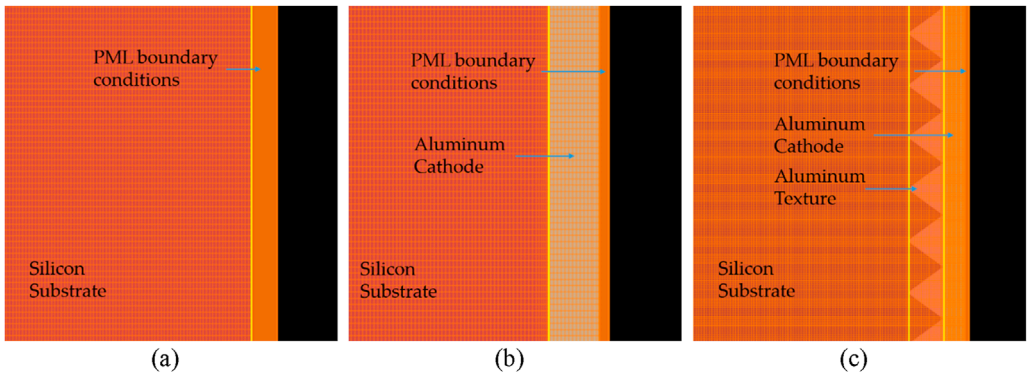

FIGURE 4
Cross-sectional views of the rear-side structures of the photodiodes: **(a)** no rear side reflection (Structure 1), **(b)** rear side specular reflection using flat surface of the aluminum cathode (Structure 2), and **(c)** rear side with texture aluminum pyramids layer as a diffuse reflector (Structure 3).

pyramid arrays can be created on the rear side of a silicon wafer through etching methods described in the literature [45], and the inverted pyramids can be filled with highly reflective metals, such as aluminum, via metallization. Figure 4 shows the cross-sectional views of the rear-side setups for all three photodiode configurations.

3.3 Electrical simulation

Before conducting the electrical simulation, certain parameters need to be established to optimize silicon PIN PDs for detecting Nd:YAG light and to align their electrical characteristics with those of the PDs listed in Table 1. The preliminary estimated results are displayed in Figure 5.

First, the doping concentration of the [n-type] intrinsic region N_B in a silicon PIN diode for 1064 nm detection should be kept low, around 10^{12}, to ensure full depletion mode at low reverse bias voltage, achieve high quantum efficiency and minimize dark current and recombination [13]. Figure 5a illustrates the relationship between the bias voltage required for full depletion and the N_B for the selected thicknesses in this study. Furthermore, Figure 5a also demonstrates that the N_B must be low enough to ensure full depletion and allow the depletion region to extend through the entire intrinsic region when a reverse bias is applied. Since we aim to unify all parameters for all PDs' structures, an intrinsic doping concentration of $N_B = 1.1 \times 10^{12}\ cm^{-3}$ was selected, tailored for PDs up to 0.4 mm thickness and 10.24 mm^2 area. For instance, at this N_B, the required reverse bias voltage to reach full depletion for PD400 (W = 0.4 mm

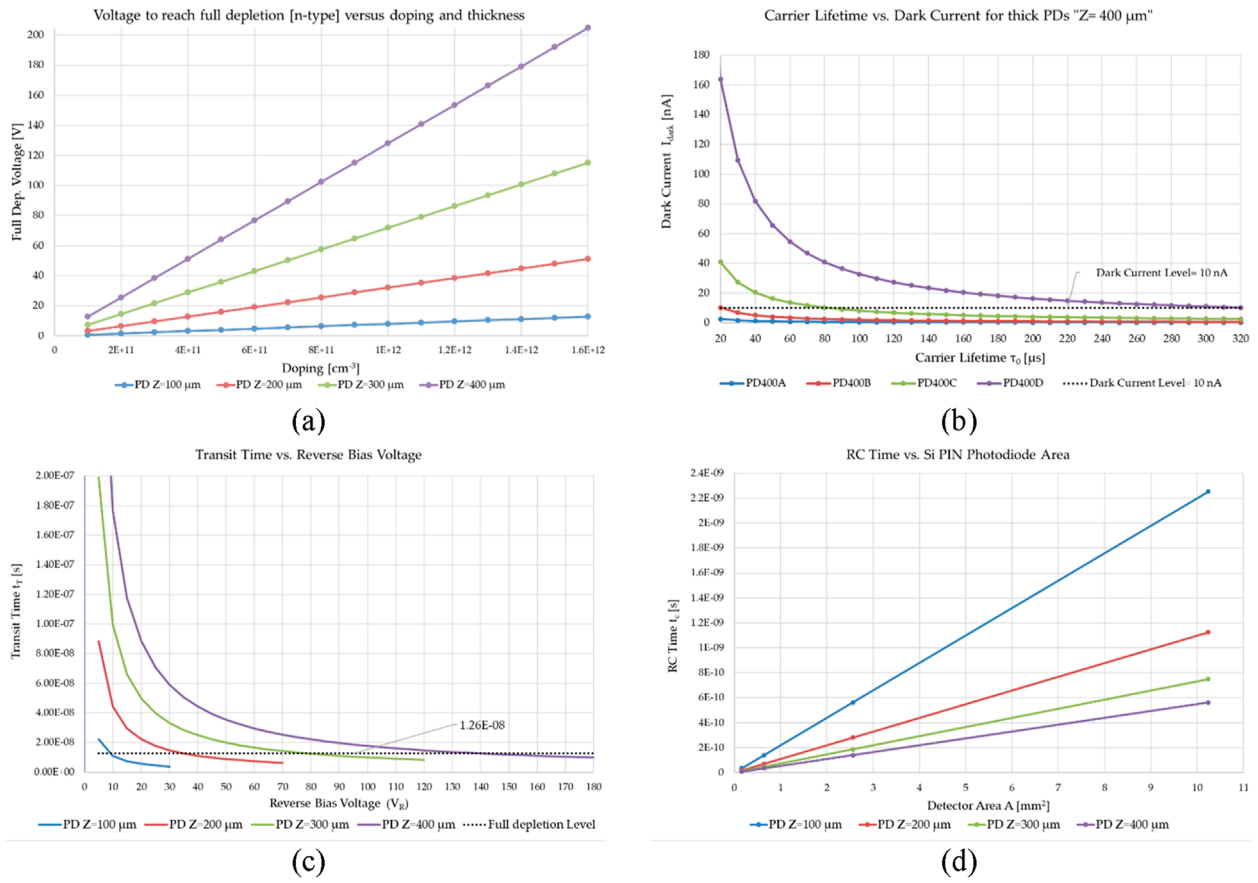

FIGURE 5
Parameters of the simulated photodiodes: **(a)** required bias voltage to operate in full depletion mode *versus* the doping levels of the intrinsic region N_B for Si PIN photodiodes with thicknesses ranging from 100 µm up to 400 µm, **(b)** dark current values for photodiodes vs carrier lifetime of the silicon substrate, **(c)** transit time vs reverse voltage, and **(d)** RC time vs photodiode area.

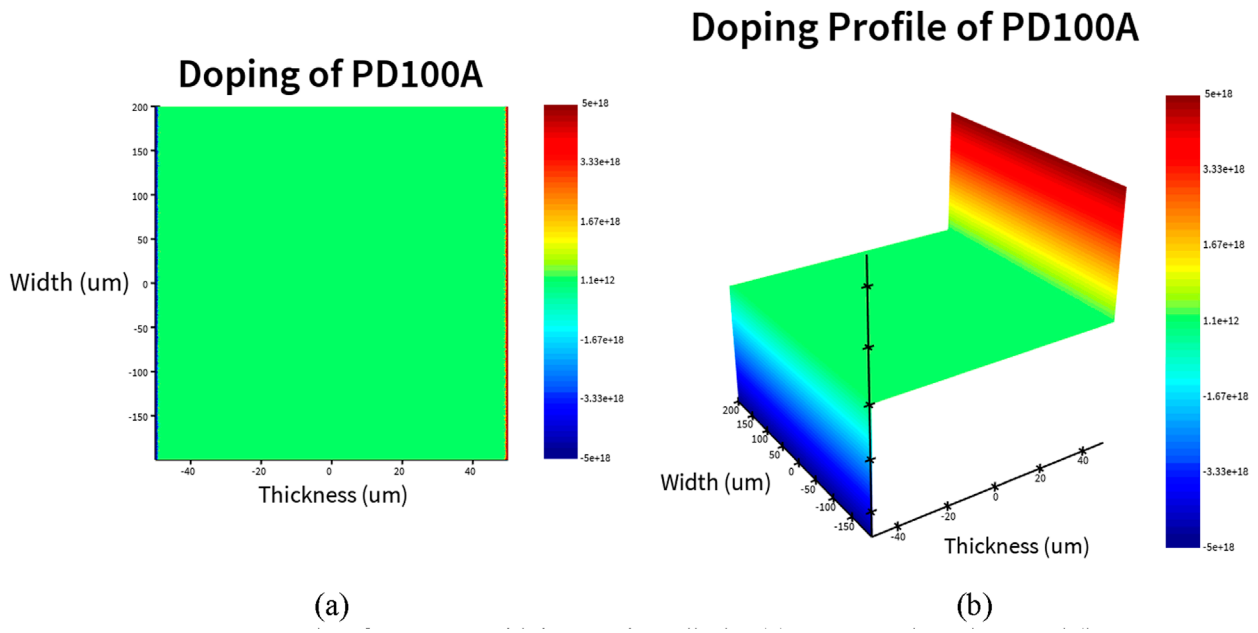

FIGURE 6
Doping distribution for 100 µm thickness photodiode: **(a)** cross-section view, and **(b)** angle view.

TABLE 3 Key simulation parameters for silicon PIN PDs at 1064 nm.

Parameter	Value	Selection criteria
Wavelength	1064 nm (1062–1067 nm)	A narrow band is used to match Nd:YAG laser applications and for precise results and faster computations
Incident Power (P_{in})	0.16–10.24 μW	Scaled to the areas of PDs (0.16–10.24 mm^2) for consistent intensity
Mesh Size (FDTD)	Down to 5 nm at interfaces	Balances accuracy and computation time; refined at interfaces
PML Layers	8	Minimizes boundary reflections (<1%) in FDTD.
ARC Thickness	Si_3N_4: 80 nm, SiO_2: 50 nm	Optimizes R_f < 0.01 at 1064 nm; tolerant to ±20 nm fabrication variance tolerance
Simulation Time (FDTD)	Up to 35 ps or meet Auto Shutoff Min (0.001 = 0.1%)	Simulation Time is the maximum duration of a simulation to be performed. However, all simulations are always satisfied early auto-shutoff criteria
Intrinsic Doping (N_B)	1.1×10^{12} cm^{-3}	Ensures full depletion at low bias voltage and thermal stability up to 60°C
p/n Doping	5×10^{18} cm^{-3}	High doping (0.5% thickness) ensures low resistivity and a strong electric field
Bias Voltage (V_R)	Up to 140V	Achieves full depletion with minimal voltage

thickness) is approximately 140V, which can be estimated using the equation [46]:

$$V_R = \frac{W^2 q N_B}{2\varepsilon_{Si}} - V_{bi} \tag{13}$$

Where W is the depletion width, the silicon permittivity ε_{Si} = 10^{-12} F/cm, and the built-in voltage V_{bi} = 0.7 V. Therefore, based on Equation 13, the chosen N_B allows Si PIN PDs to achieve full depletion mode at practical reverse bias voltage levels (≤140 V). Additionally, this N_B doping improves thermal stability at elevated temperatures (up to 60°C), which is essential for reliability in harsh environments, as increased N_B mitigates the effect of rising intrinsic carrier concentration n_i. The n_i represents the number of thermally generated electron-hole pairs in an undoped semiconductor and is described by Equation 14 [46]:

$$n_i = B \times T^{3/2} \times e^{-E_g/(2kT)} \tag{14}$$

Where, for silicon, B is the material constant ≈ $5.4 \times 10^{15} cm^{-3} K^{-3/2}$, E_g = 1.12 eV, k is Boltzmann's constant, and T is the temperature in Kelvin. At 60°C, n_i = 1.4× 10^{11} cm^{-3}, n_i « N_B, which ensures dopants, not thermal generation, dominate the depletion region's carrier concentration.

Second, the required carrier lifetime of silicon to achieve a dark current as low as the reported PDs in Table 1 (I_{Dark} ≤ 10 nA). As shown in Figure 5b, our analysis indicates that the required carrier lifetimes for photodiodes PD400A, PD400B, PD400C, and PD400D are greater than 5 μs, 20 μs, 80 μs, and 320 μs, respectively. Third, the impact of the operating reverse bias voltage and area of the PDs on the rise time to be t_R ≤ 13 ns. Thus, transit time (t_T), RC time constant (t_C), and rise time (t_R) have been calculated, and Figures 5c, d illustrate the variation of the components of the rise time (transit time and the RC time constant). As shown in Figure 5c, the transit time is the dominant factor contributing to the rise time. However, by increasing the reverse bias voltage, the transit time can be significantly reduced to below 10 ns, thereby achieving the desired rise time of t_R ≤ 13 ns.

Lastly, the Si PIN PDs, modeled electrically using ANSYS Lumerical CHARGE, shared the same structural design, with electrical parameters such as doping levels and applied bias voltage on the anodes incorporated into the simulation. The p-type and n-type doping regions were modeled using a Gaussian diffusion profile with a doping concentration of 5 × 10^{18} cm^{-3} doping level. The junction width was set to 0.5% of the PDs thickness for both the p-type and n-type regions, while the intrinsic [n-type] region occupied up to 99% of the PDs thickness, with a doping concentration of 1.1×10^{12} cm^{-3}. Figure 6 illustrates the doping distribution used in this study.

3.4 Simulation parameters

A sensitivity analysis was conducted by varying the thickness (100–400 μm) and area (0.16–10.24 mm^2) while keeping other

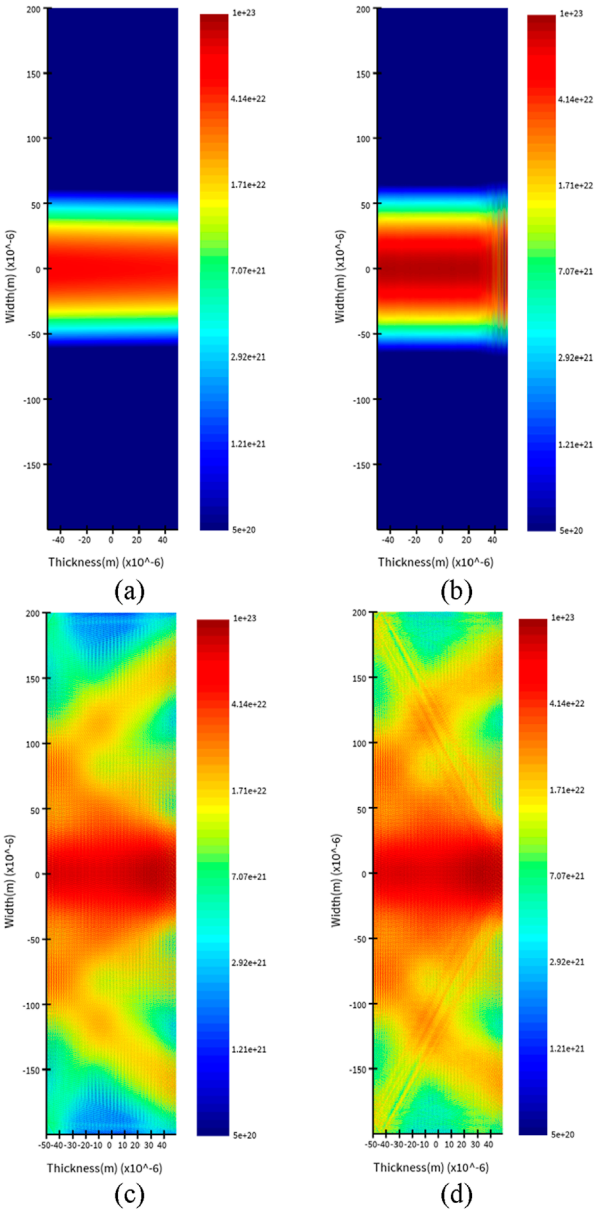

FIGURE 7
Optical simulation of the electrical generation rate (charge pairs/m^3/s) in PD100A with various structures: **(a)** Structure 1, **(b)** Structure 2, **(c)** Structure 3, and **(d)** Structure 3 with side reflection.

parameters constant, as summarized in Table 3. This approach demonstrates how changes in input variables (thickness or area) impact the output of the simulation (responsivity of the photodiodes).

4 Results and discussion

This section presents the responsivity *versus* dimensions for all three photodiode structures. The calculated responsivity values, estimated using Equations 5, 6, are compared with the simulated responsivity for each photodiode structure. Then, we analyze the light-trapping effects on responsivity and explore the optimal geometries for PDs with rear-side diffuse reflectors. Figure 7 illustrates how the optical path length in the PDs increases and how the light scatters due to the impacts of the rear-side diffuse reflectors on the incoming light and, subsequently, enhancing responsivity.

4.1 Responsivity comparison of the photodiodes

Figure 8 compares the simulated responsivity of all three photodiode structures with values calculated using Equations 5, 6. For Structure 1 (no rear-side reflection), Figure 8a shows that simulated responsivity aligns closely with calculations from Equation 5, regardless of area variations. This agreement validates the simulation methodology and indicates that responsivity in Structure 1 depends primarily on thickness, with the area having a negligible impact. In addition, Figure 8b presents the responsivity for PDs with rear-side specular reflectors (Structure 2). The differences between the calculated responsivity (using Equation 6) and the simulated responsivity are minimal (<5%), even with varying photodiode areas. This validates the simulation approach and shows that the responsivity of PDs with specular reflectors depends mainly on thickness, not area. On the other hand, Figure 8c depicts the responsivity for PDs with rear-side diffuse reflectors (Structure 3). In this structure, the differences between the calculated and simulated responsivity are more significant due to the increased optical path length, which is influenced by both the area and thickness of the PDs. The maximum responsivity reaches up to 0.58 A/W, aligning with reported responsivities at 1064 nm for several PDs, as shown in Table 1 [16, 21, 43].

4.2 Optimal geometries for photodiodes with rear-side diffuse reflectors

Each of the 16 Si PIN PDs has been simulated in all three structures, and the responsivity values are compared in Figure 9a. The percentages of responsivity enhancement for PDs with diffuse reflectors (Structure 3) *versus* PDs without rear-side reflection (Structure 1) and with specular reflectors (Structure 2) are presented in Figure 9b.

As seen in Figure 9a, the responsivity of PD200C, 200 µm thickness, with diffuse reflectors surpasses those of PDs with rear-side specular reflectors, 400 µm thickness (~0.45 A/W vs. ~0.43 A/W). Also, PD400D achieves the highest responsivity of 0.58 A/W at 1064 nm, slightly outperforming PD400C at 0.56 A/W and PD400B at 0.52 A/W. Put differently, expanding the area by 1600% (from ~0.64 mm^2 to ~ 10.24 mm^2) boosts responsivity by only ~10%, an improvement outweighed by the resulting decline in electrical performance, notably increased dark current and NEP. Thus, the ceiling of the maximum achievable responsivity of Si PIN PDs at 1064 nm is ~0.6 A/W as a result of using light trapping. On the other hand, Figure 9b shows that the enhancement in responsivity due to light trapping increases

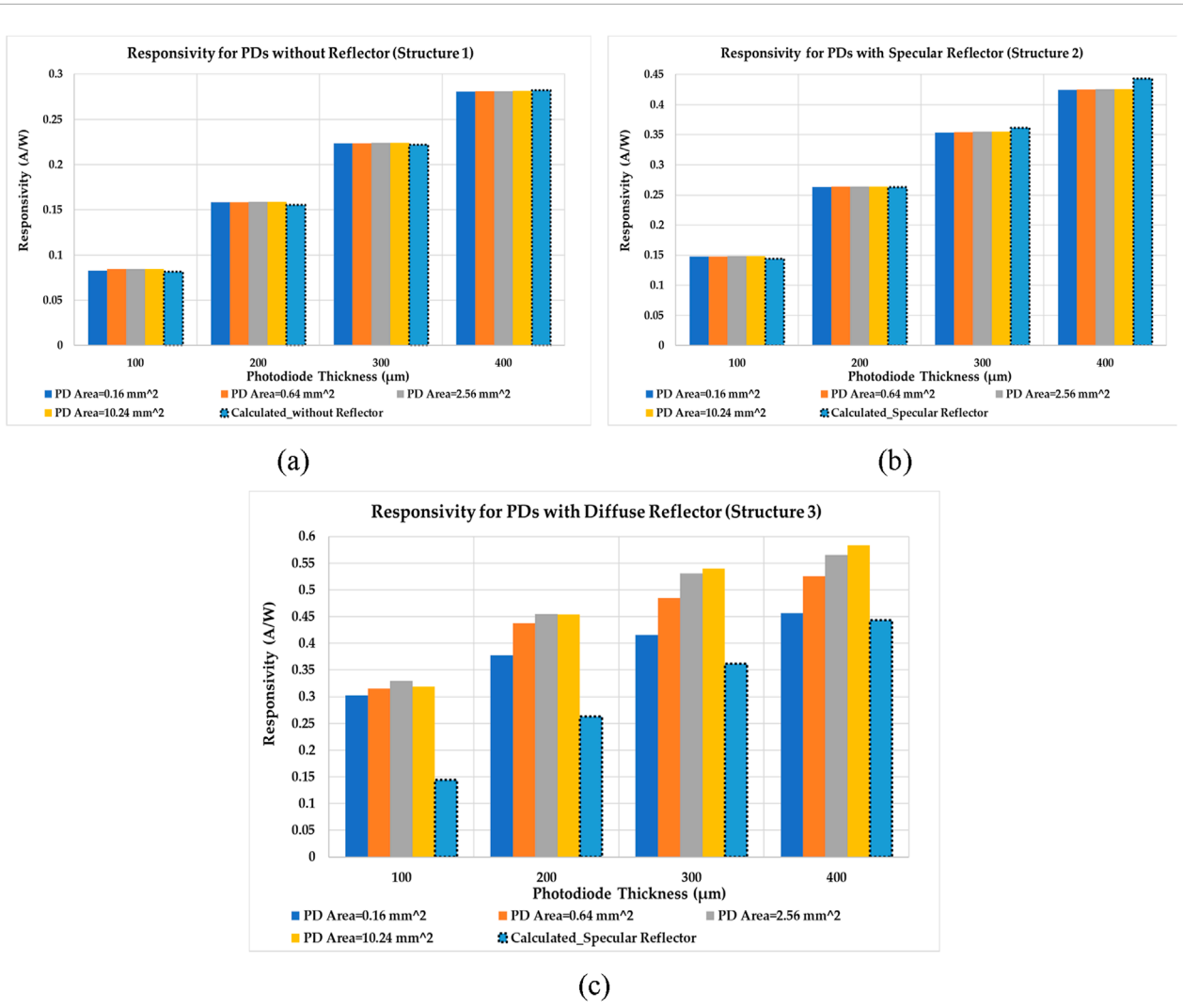

FIGURE 8
Simulated responsivity for: **(a)** PDs without rear-side reflector versus calculated responsivity using Equation 5, **(b)** PDs with specular reflector versus calculated responsivity using Equation 6, and **(c)** PDs with rear-side diffuse reflector versus calculated responsivity using Equation 6.

with larger areas but decreases with greater thickness. Thus, increasing the thickness enhances the responsivity, especially for larger PDs. However, the average responsivity enhancement diminishes to less than 10% when the thickness increases from 300 μm to 400 μm for PDs with diffuse reflectors, as shown in Figures 8c, 9b.

Overall, the dimensions of custom-made Si PIN PDs with light trapping should be chosen considering the optical and electrical characteristics trade-off to meet the desired responsivity without degrading the electrical characteristics. Also, the dimensions can be selected either to enhance responsivity while maintaining good electrical characteristics or to enhance electrical characteristics while maintaining good responsivity. For example, the photodiode PD300C, 300 μm thickness, and 2.56 mm^2 area achieved a responsivity up to 0.53 A/W, surpassing state-of-the-art Si PIN PDs reported in the literature.

Another explored approach to optimize the performance of Si PIN PDs is to use side reflectors to maximize the responsivity with much smaller thicknesses and areas, which are favorable for better electrical characteristics. The benefits of the side reflector are maximized for small area PDs where the percentage of responsivity enhancement is ~25% and 11% for 0.64 and 2.56 mm^2 PDs, respectively, as shown in Figure 10. In our case, we used 50 μm SiO_2 to reflect the light and maximize the optical path length without the necessity to enlarge the area of the PD elements. Filling the inter-element gaps in Si PIN PD elements in a photodetector array or quadrant with SiO_2 prevents electrical crosstalk between adjacent photodiode elements, and it causes scattering or reflection of the light due to refractive index mismatch with silicon.

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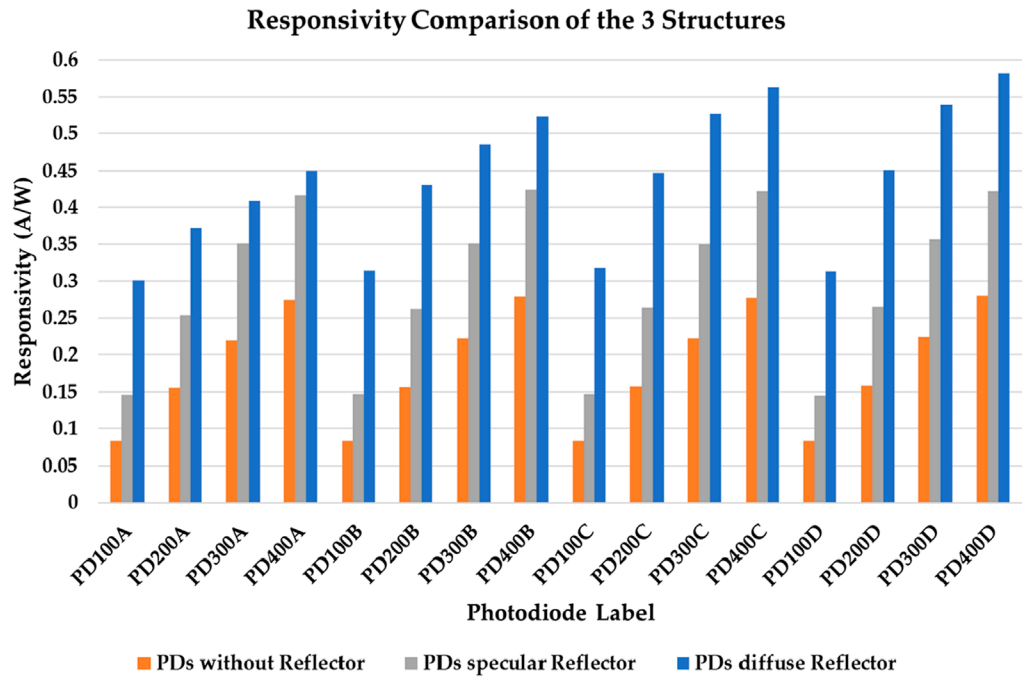
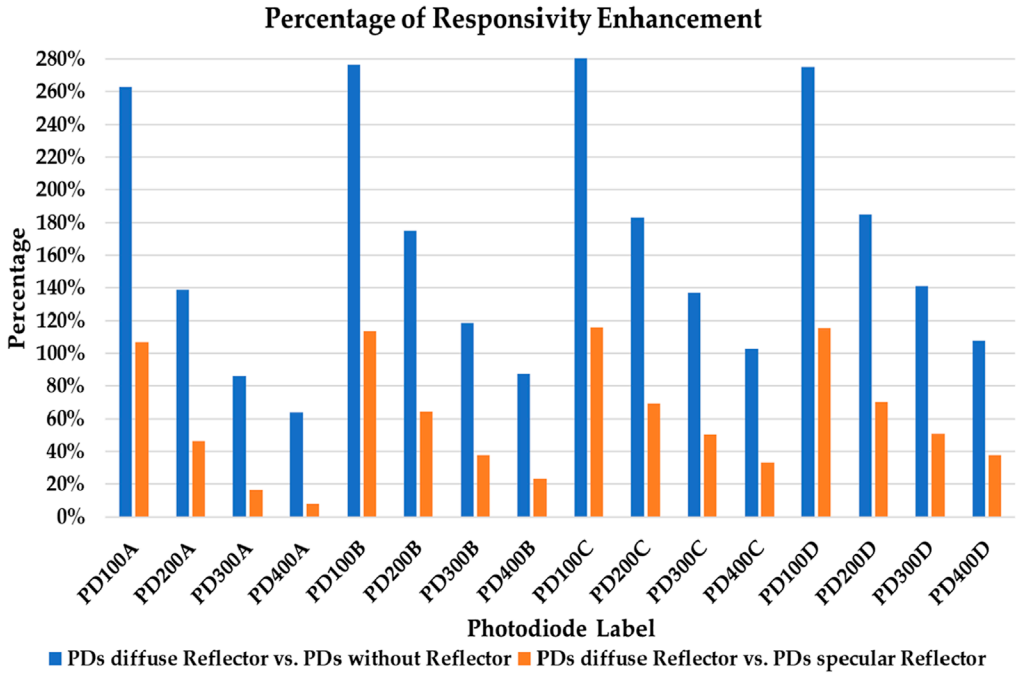


(a)



(b)

FIGURE 9
Comparison of PDs with diffuse reflector vs PDs with specular reflector and PDs without reflector **(a)** Responsivity values, **(b)** Percentage of responsivity enhancement.

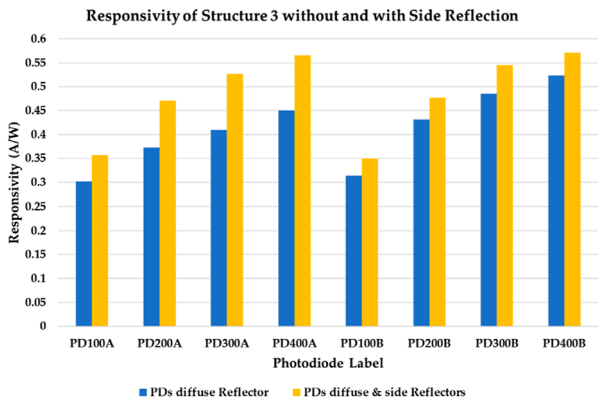


FIGURE 10
Responsivity comparison of Structure 3 PDs without and with side reflector.

5 Conclusion

In this work, we have investigated the impact of light trapping on the responsivity of silicon-based PIN PDs for light detection at 1064 nm. Thus, Ansys Lumerical FDTD and CHARGE have been utilized to simulate Si PIN PDs and obtain their optical and electrical characteristics *versus* varying dimensions. The following conclusions were obtained:

- When there are no diffuse reflectors, the optical characteristics, such as responsivity, of the simulated PIN PDs agree with the theoretical calculations and the reported values in the literature, as shown in Table 1.
- When there are diffuse reflectors, larger dimensions of the PDs lead to higher responsivity values, which agree with the reported results in Table 1. Results show that Si PIN PDs with rear-side diffuse reflectors significantly enhance responsivity, reaching up to 0.58 A/W for 400 μm thick PDs. However, additional methods should be investigated to be used alongside light trapping to enhance the responsivity up toward the maximum theoretical responsivity, 0.85 A/W, at 1064 nm.
- The light trapping increases responsivity values significantly in thin PIN PDs. For instance, thin PDs (100 μm thickness) with diffuse reflectors exhibit a higher responsivity (~0.31 A/W) compared to thicker PDs (400 μm) without rear-side reflectors (~0.28 A/W). However, the percentage of responsivity enhancement due to the light trapping decreases significantly in thicker PDs.
- There is a trade-off between the characteristics of optical and electrical properties. For instance, while PDs with the largest area and thickness showed the highest responsivity, they also exhibited the highest dark current and noise equivalent power, potentially limiting their utility in low-light or high-speed applications. Therefore, the optimal dimensions to realize high responsivity and low dark current (≤5 nA) are found to be 0.2–300 μm thickness and 0.6–2.5 mm^2 area to form quadrant or array photodetectors.
- Filling the gaps between Si PIN photodiode elements with SiO_2 can be used to optimize optical and electrical characteristics, such as achieving higher responsivity for smaller-size PD elements. Also, it provides electrical isolation, reducing electrical and optical crosstalk between adjacent elements.
- Simulations omit texturing side effects like high electric fields and interface defects, which could increase dark current (e.g., from 10 nA to 50 nA) and noise. Fabrication trials or advanced simulations (e.g., with defect modeling) are needed to quantify these impacts.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

FA: Conceptualization, Investigation, Methodology, Supervision, Validation, Writing–review and editing. NA: Conceptualization, Data curation, Formal Analysis, Methodology, Resources, Software, Validation, Writing–original draft. MA: Conceptualization, Data curation, Formal Analysis, Resources, Software, Validation, Writing–original draft, Writing–review and editing.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Generative AI statement

The author(s) declare that no Gen AI was used in the creation of this manuscript.

Publisher's note

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