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TimeSPOT developments on charged-particle silicon sensors for high intensity 4D-Tracking

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This paper provides a comprehensive overview of recent advances in silicon sensors designed for 4D tracking. These devices are of particular relevance for the next-generation of high intensity collider experiments, where meeting stringent requirements in both spatial and temporal resolution, along with unprecedented levels of radiation hardness, will be crucial. Among the various sensor technologies under development, 3D silicon sensors have demonstrated the potential to satisfy all key performance criteria. The paper discusses the development and fabrication processes of these sensors, emphasizing their capability to deliver exceptional timing resolution and radiation tolerance. Methods adopted for their characterization and results obtained from recent experimental campaigns are presented and critically analyzed. Furthermore, the pivotal role of readout electronics in enabling high-precision timing performance is underscored.

KEYWORDS

particle tracking detectors, solid-state detectors, timing detectors, high time resolution, high luminosity

1 Technical requirements in high-intensity 4D-tracking

The term 4D-tracking generally refers to a tracking technique involving the simultaneous measurement of a particle's position and time of passage across sensor-equipped tracking planes. As defined, this technique does not specify the required precision for time and spatial measurements, nor does it consider the environmental and experimental conditions under which the measurements must be performed.

Several collider experiments—currently in the design phase (e.g., LHCb Upgrade 2), at the proposal stage (e.g., neutrino tagging in short- and long-baseline experiments), or in conceptual development (e.g., FCC-hh)—require operation at unprecedented intensity levels ($Events/s/cm^2$). This imposes exceptionally stringent requirements on the tracking systems, particularly in their innermost regions, representing a substantial leap beyond the specifications of currently operating vertex detectors. Key performance targets include a spatial resolution better than 10 μm and a time resolution better than 50 ps per single pixel and per single-particle hit, considering the complete readout chain (sensor, amplifier, discriminator, and Time-to-Digital Converter). Additionally, system-level challenges such as ultra-low jitter reference distribution over large detector areas must be addressed. The trackers must also sustain extreme radiation levels, approaching fluences of 10^{17} 1-MeV n_{eq}/cm^2.

These requirements represent a paradigm shift compared to existing vertex detector designs and are particularly challenging given the strict system constraints, especially

regarding power density (1–2 W/cm^2). Such advancements should be regarded as the design and realization of a novel and powerful instrument for discovery in physics research, warranting a specific designation: the High Intensity 4-Dimensional Tracker (hereafter referred to as HI4DT).

The successful design of a HI4DT necessitates concurrent and coordinated progress in sensor development, microelectronics design, cooling systems, and precision mechanics. In this paper, we focus on developments in silicon sensors and associated electronics, summarizing recent results that demonstrate the feasibility of meeting these demanding requirements. These achievements represent a major step forward in paving the way for the realization of the HI4DT.

2 Materials and methods

2.1 3D silicon sensors

Sensors for the detection of charged particles and suitable for a HI4DT must primarily have very high intrinsic space-time resolution. As mentioned earlier, experimental requirements demand a spatial resolution better than 10 μm, as in the case of LHCb vertex detector for the Upgrade 2 of the experiment (scheduled to be operated from 2035) (LHCb Collaboration, 2024). A binary resolution of 10 μm requires a pixel size of approximately 35 μm $\approx 10\mu m \times \sqrt{12}$. Such a pixel dimension would be not suitable for various technological reasons on the sensor side, which will be clarified below. With present technologies, it would be very difficult to match also on the front-end electronics side, for limited space with respect to the functionalities to be integrated. The pixel size is therefore usually increased to around 50 μm, while the needed spatial resolution is obtained using clever clustering techniques and/or calculating the barycenter of charge deposits within the cluster. While complicating data processing stages, such techniques can lead to sub-binary space resolutions (Bassi et al., 2023).

Concerning time resolution, a longer argument is needed. High time resolution in particle sensors can be reached leveraging on the amplitude of the induced current signal and on the speed in Charge Collection Time (CCT) on the electrodes. Most importantly, a fundamental property of high resolution sensors is collection time uniformity, which results in narrower time-of-arrival distributions. Small CCT requires reducing inter-electrode (bias to junction) distance d, which turns to be also highly beneficial for radiation robustness, minimizing the probability of charge trapping in radiation-induced reticular defects. In traditional planar sensors, d gives also the amount of charge deposited by Minimum Ionizing Particles (MIPs) by dE/dx. For this reasons, in fast planar sensors (reduced d), a low-gain doped layer must be introduced to gather a sufficient amount of charge (LGADs) (Cartiglia et al., 2014). On the other hand, introduction of gain by doping makes the sensors more prone to radiation damage, due to radiation erosion of the gain layer itself, which lowers the gain and deteriorates the sensor timing performance. For this reason, present gain-based planar sensors hardly reach a radiation resistance of a few 10^{15} 1-MeV n_{eq}/cm^2 (Ferrero et al., 2019).

In summary, an ideal silicon sensor for high time resolution and high radiation resistance (above 10^{16} 1-MeV n_{eq}/cm^2) should have the following main properties:

1. Fast CCT, so possibly small d;
2. Maximum uniformity in CCT across the sensible volume;
3. Large amount of charge deposit;
4. Possibly, no gain by doping.

These important items are briefly quantified and analyzed below.

2.1.1 Charge amount, sensor thickness, no gain

The minimum amount of charge required for fast timing depends on the performance of the front-end electronics, which must also comply with system constraints. From a circuit design perspective, several solutions capable of achieving satisfactory timing performance can be envisioned (Lai and Cossu, 2020; Cossu and Lai, 2023). However, they all ultimately depend on three key parameters:

- The affordable power density, which determines the maximum bias current in the amplifying stage and, consequently, its Slew Rate;
- The capacitance of the pixel sensor, which impacts the Signal-to-Noise Ratio (SNR);
- The amplitude of the induced current signal (i.e., the total deposited charge over time).

Recent studies on front-end electronics for timing, can provide a clear picture on how these parameters affect the final time resolution. Such results are shown in Figure 1. A sensor capacitance in the typical range of 50–100 fF is considered, along with a power density of 1–2 W/cm^2. For a total target time resolution per pixel below 50 ps, it is safer to specify a combined sensor and front-end contribution better of 30 ps It can be seen that a time resolution of 30 ps rms is achieved with a charge amount not lower than 1.5-2 fC. Considering a dE/dx of about 80 electron-hole pairs per μm, this corresponds to a minimum thickness in the range of 150–200 μm. Planar sensors having such thickness would have CCTs of several ns. In the following subsection we will show that such CCT cannot give resolutions better than several hundreds of ps.

A simple and clever idea consists in decoupling the sensor thickness z from the electrode distance d (Parker et al., 1997), by building vertical (or 3-Dimensional) electrodes, thus inventing the so-called 3D silicon sensors. In this case, bias and junction electrodes are digged into silicon by the DRIE (Deep Reactive Ion Etching) technique (Laermer et al., 2015; Forcolin et al., 2020). This well-known idea opens the great advantage to allow "playing" with the electrode shape and the pixel cell geometry, so to optimize the pixel timing performance by design of its geometry. This is explained in the following sub-section.

2.1.2 CCT: fast and maximally uniform

3D silicon sensors can have considerably reduced inter-electrode distance d. For a given pixel geometry, the limiting factors in d are the fabrication process resolution and the pixel capacitance. Present fabrication techniques would allow $d \approx 10$ μm. However, a larger size

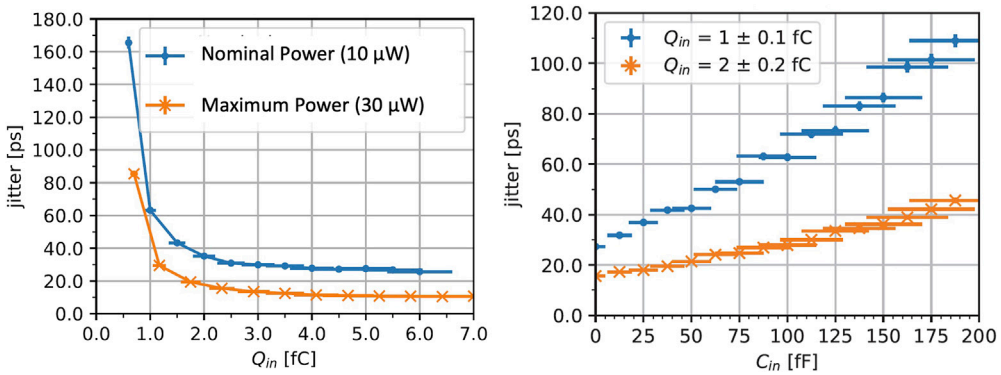

FIGURE 1
Relationship between electronic jitter vs. total collected charge Q_{in} (left) and vs. sensor capacitance C_{in} (right). Both plots are results from measurements on the Ignite-0 test prototype (The IGNITE Collaboration, 2024). A power consumption on front-end of 10 μW corresponds approximately to a power density of 1.5 W/cm^2. The left plot is taken at C_{in} = 100 fF. For a satisfactory jitter at nominal power a $Q_{in} \gtrsim 2\,fC$ is needed.

is typically used (20–30 μm) in order to limit pixel capacitance, which has a direct impact on time resolution, especially when strong power density constraints are imposed by the system.

Pixel geometry and electrode shape have paramount importance in deciding the final timing performance of the designed 3D pixels. As it is well known (Ramo, 1939; Schockley, 1938), the contribution to the induced current signal i of a charge carrier drifting towards the readout electrode is given, in each point of its path, by the dot product:

$$i = q\overrightarrow{E_w} \cdot \overrightarrow{v_d}$$

where q is the carrier charge, $\overrightarrow{E_w}$ the weighting field, and $\overrightarrow{v_d}$ the drift velocity $\overrightarrow{v_d}$ of the carrier. Carrier drift velocity is a known function of the electric field, from the low field regime, where its mobility is defined, up to full saturation regime at high electric field ($E > 10^5\,V/cm$ in silicon) (Sze et al., 2021). When sharp timing distribution are required, it is important not only to have fast signals (short CCT), but especially to ensure a uniform electric field across the full pixel volume and operate towards the velocity saturation regime as much as possible.

By leveraging the design flexibility of 3D silicon pixels, extensive and accurate studies can be carried out optimizing pixel timing performance for a given system-required pixel size, as for example, in (Lampis, 2023) and (Loi et al., 2025). Due to this specific feature, 3D sensors can also be referred to as geometric sensors.

2.1.3 Timing resolution vs. detection efficiency

In assessing the timing performance of pixel sensors, it is crucial to correlate timing measurements with a precise characterization of detection efficiency. The interdependence of these two characteristics must be complemented by ensuring maximal response uniformity across the entire detection volume. Due to their geometric feature, such property is of particular relevance in 3D sensors, where bias and junction electrodes can give different shape to the pixel volume and electric field.

The specific geometry adopted in the sensor design can lead to variations in the electric field intensity across different regions of a pixel, resulting in differences in the total charge collection time (CCT). In some cases, significant variations in response can occur within the same pixel. Depending on the characteristics of the front-end electronics, regions with low electric field may exhibit delayed signal formation or even fail to generate a detectable response, particularly if the field approaches a local zero or if the electronics are sensitive predominantly to the fast component of the induced signal. Consequently, if only the fast component of the signal or the fastest regions of the pixel are considered, the measured time resolution may be biased toward such contributions, neglecting the tails in the Time-of-Arrival distribution. This effectively corresponds to disregarding a substantial portion of the pixel volume and leads to a mischaracterization of the true detection performance.

This phenomenon can be effectively illustrated by comparing two extreme cases: the hexagonal columnar geometry and the squared trench geometry, the latter being the geometry adopted for the TimeSPOT sensors, as illustrated in Figure 2. It can be observed that, although the hexagonal geometry has a much faster region all around the central readout electrode, its time distribution has a much wider dispersion, due to the weak-field region in correspondence to its periphery. Although in average slower, the final rms resolution is strongly in favor of the trench geometry, being it more uniform across the full detection volume.

Extensive studies of this kind have clearly indicated the trench geometry as the best one for timing, and encouraged for a fabrication and test campaign using such technology: the 3D-trench TimeSPOT sensors.

2.2 The TimeSPOT 3D-trench sensors

As an output of the studies just described, the optimal geometry chosen for fast timing applications has been the 3D-trench, which is shown in Figure 3. As of today, three batches of TimeSPOT 3D-trench sensors, with pixel size and shape described in the same Figure 3, have been produced by the Fondazione Bruno Kessler (FBK, Trento) on 6 wafers. They correspond to a clear evolution in production technology. The DRIE process is particularly stressful for the processed wafers, especially when several contiguous trenches must be fabricated. First wafers were fragile and tended to easily

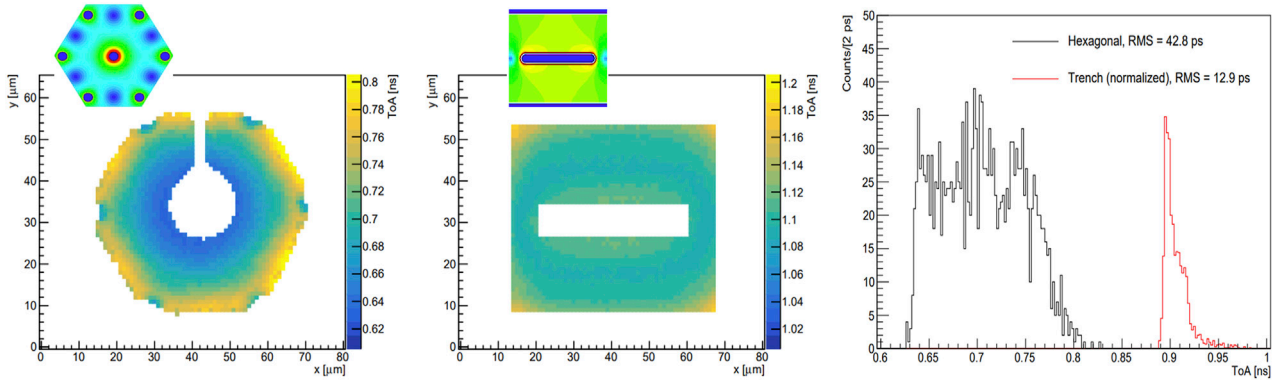

FIGURE 2
Comparison of timing performance between different geometries of 3D sensors (Loi, 2020). Left: Time-of-Arrival map of a columnar hexagonal geometry, obtained by TCT technique (IR laser). Center: Same measurement on a trench square geometry. White areas in the maps are not accessible by this technique, being covered by metal structures. The insets are the corresponding electric field maps, where blue dots are weak field areas. Right: Time of Arrival distributions for the same geometries.

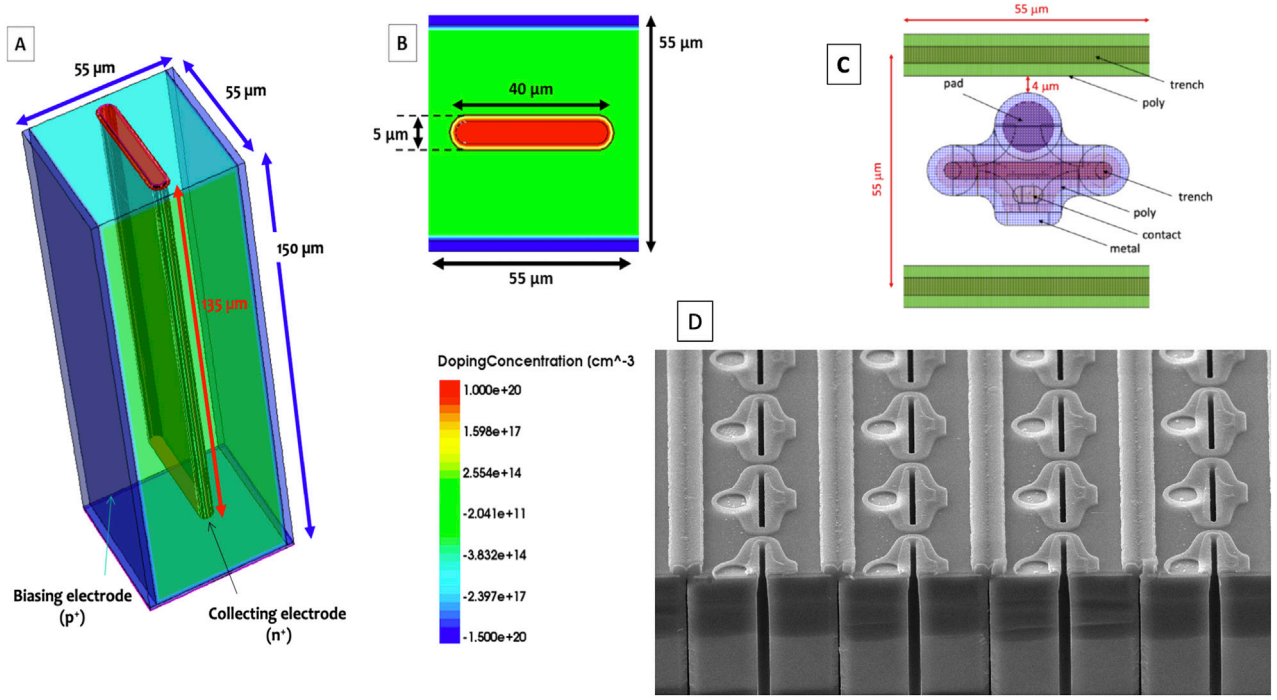

FIGURE 3
Different views of the TimeSPOT 3D-trench pixel (Lampis, 2023). **(A)** Geometry and sizes of the detection volume. **(B)** Doping concentrations. **(C)** Pixel layout. **(D)** SEM picture of a pixel array (courtesy FBK).

break during production. This suggested the practice to start producing a very low density of reticules: 11 per wafer (2019), which turned to be 18 in 2021, reaching then a full coverage of the wafer surface in the 2024 AIDAInnova batch, after dedicated improvements in the production process (Boscardin, 2025).

The wafers integrated a manifold of different small test-structures and medium-size pixel matrices. Test structures feature single, double, four pixels, and multi-pixels, organized in strips of tens of pixels short-circuited together for being read-out on single-channel amplifiers (see Section 2.3). Dedicated test structures allow an accurate characterization of pixels and have been used to gain a deep knowledge of the sensor behavior concerning time resolution and efficiency. In this respect, the direct comparison between simulation models and experimental results helped to gain great confidence and control about the sensor behavior and performance (Loi et al., 2021; Brundu et al., 2022; Brundu et al., 2021).

The wafers include also pixel matrices of different sizes: 256 × 256 pixels and 32 × 32 pixels (2019 batch); 32 × 32 pixels

(2021 batch); 32 × 32, 64 × 64 and 128 × 128 pixels (2024, AIDAInnova batch). Matrices have been produced to test the production yield on large structures and develop suitable sensors for matrix readout, using dedicated ASICs with embedded high-resolution timing facilities under development (Cadeddu et al., 2023), (The IGNITE Collaboration, 2025).

2.3 TimeSPOT sensors and front-end electronics

The time resolution of the TimeSPOT sensors has already been proven to be better than 10 ps (see Section 2.4). This performance, however, is strongly dependent on the characteristics and performance of the electronic front-end stage used (Cossu et al., 2023). The interplay between sensor timing performance and electronic front-end has been studied in detail in Lai and Cossu (2020), Riegler and Rinella (2017), and Riegler (2025). In this paper a summarized report of such studies is given.

As previously noted, the charge collection time (CCT) can serve as a reliable indicator of the sensor's intrinsic timing resolution. However, the extent to which this intrinsic performance can be achieved in practice is strongly dependent on the characteristics of the readout electronics. In this context, the conventional approach of summing the timing uncertainties of the sensor and front-end amplifier in quadrature, treating them as statistically independent, provides only an approximate description. In reality, the final timing resolution is strongly correlated with the operation of the front-end electronics.

In conventional tracking detectors, optimized for spatial resolution, charge collection efficiency is the primary concern. These systems typically employ relatively slow front-end amplifiers operating in charge-sensitive (integrating) mode (Charge Sensitive Amplifier–CSA). It can be shown that (Lai and Cossu (2020), Riegler and Rinella (2017) and Section 2.3.1), with a CSA, the best achievable time resolution corresponds to half the standard deviation of the CCT distribution.

While CSAs integrate the total charge made available in the detection process, in order to maximally exploit the sensor capabilities in terms of speed, a different approach is more convenient. This is possible using a Trans-Impedance-Amplifying (TIA) mode, where the amplifier capacitive feedback is minimized and the focus is moved to the fast current rise at the start of the inductive process on the collecting electrode. It has been demonstrated (Lai and Cossu, 2020; Cossu and Lai, 2023) that in TIA mode, the output time resolution can be lowered up to a smaller fraction of the standard deviation of the CCT distribution (Figure 4). However, in this case other features become critical (Cossu and Lai, 2023):

- The intrinsic bandwidth of the transistor technology used.
- The noise rejection capability of the front-end circuit. As shown in Figure 4, the possibility to lower the electronics jitter σ_t to a smaller fraction of the CCT standard deviation σ_{tc} is possible only if the discrimination threshold can be sufficiently lowered. This is only possible in a low-noise design.
- An adequate power budget available, to ensure a high slew rate of the output signal against a relatively high sensor capacitance.

The TIA approach is therefore especially effective using intrinsically wide-band technologies, as Heterogeneous Bipolar Si-Ge Transistors (Si-Ge HBTs), having transition frequency of about 85 GHz. TimeSPOT has developed dedicated fast, discrete-component TIA front-ends for the characterization of the timing performance of its 3D-trench sensors (Cossu and Lai, 2023) both in laboratory and in test-beam campaigns. Such front-end electronics features a signal-to-noise ratio SNR ≈ 20 and an electronic jitter below 7 ps at 2 fC input charge. The amplifier rise time is shorter than 100 ps. The power consumption is about 70 mW/channel. The TimeSPOT board directly houses and biases the sensors under test, which are wire-bonded to the amplifier input pads.

Si-Ge HBTs are also being used in integrated pixel systems (Milanesio et al., 2024). However, the design of a HI4DT apparatus is extremely complex, imposing hard system constraints, which necessarily become decisive in establishing the performance limit of the whole readout chain and in deciding specific technological choices. This issues are addressed in the next subsection.

2.3.1 TimeSPOT electronics and 4D-tracking systems

Integrated electronics for HI4DT have very demanding performance requirements, especially because they must be satisfied within very strict system constraints. Each readout channel, or electronics pixel, should integrate an amplifier and a fast discriminator. To sustain typical hit rates per pixel above 100 kHz, a Time-to-Digital-Converter (TDC) circuit with due precision (≈10 ps) and limited conversion time (≈1 μs) should also be integrated per single channel or shared among a small group of channels (2–8 typically).

Among the several system constraints, the most significant is the limited power budget allowed per electronics pixel. This is technically motivated by the present maximum technical capability to dissipate the power produced in a highly-integrated system, that is around 2 W/cm^2 (LHCb, 2021). Compared to fast-TIA solutions used in the characterization of a small number of channels (Analog Front End–AFE–rise time around 100 ps), a reduced-bandwidth approach appears mandatory, allowing less current consumption, accepting a larger amount of signal integration, and a much longer rise time (Charge-Sensitive-Amplifier, AFE rise time of 5–10 ns). While it entails a slight performance degradation compared to the intrinsic timing capability of 3D-trench sensors, a Charge-Sensitive Amplifier (CSA) can still achieve a target resolution below 30 ps. This is demonstrated in detail in Lai and Cossu (2020) and is concisely illustrated in Figure 4. The plots show the estimated relationship between the intrinsic sensor timing performance, expressed by the average (t_c) and standard deviation (σ_{tc}) of its CCT distribution (left) and the final AFE time resolution σ_t. This relationship can be expressed as a fraction of the sensor σ_{tc}, and depends on both the integration time of the AFE τ and the discriminator threshold applied. The values of $\tau > 3\,ns$ correspond to the CSA approach. As said above, and shown in Figure 4, the ideal σ_t obtainable by a CSA is $0.5\sigma_{tc}$, which in the case of our sensor (3D-trench) is about

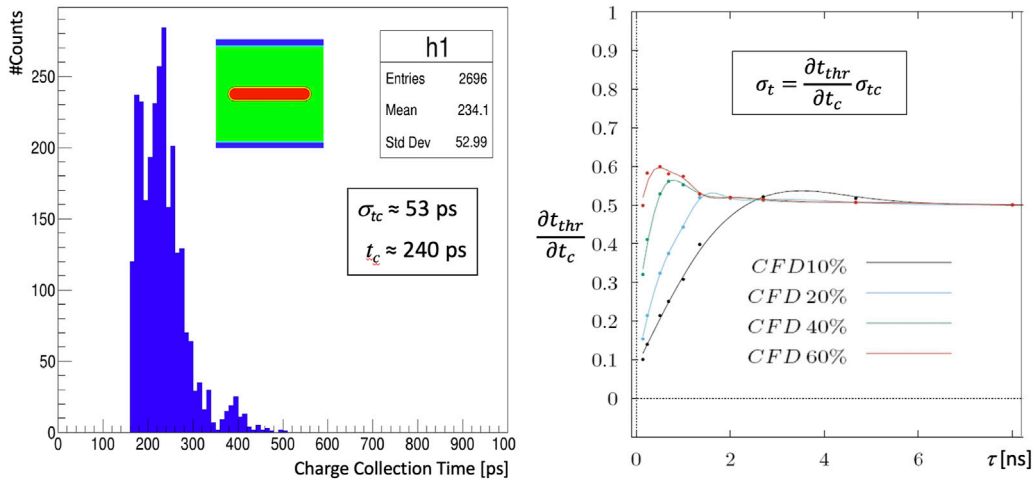

FIGURE 4
Relationship between sensor timing performance σ_{tc} (standard deviation of collection time distribution) and final Analog Front End (AFE) time resolution σ_t. Left: Simulated CCT distribution of a TimeSPOT sensor. Right: Propagation coefficient σ_t/σ_{tc} (defined in Lai and Cossu (2020)) for different AFE integration times τ and different discriminator thresholds.

26 ps. Further improvement of the final σ_t could require an increase in power consumption, to get $\tau < 3\,ns$.

If 3D-trench silicon sensors are used, capable of an intrinsic $\sigma_t \approx$ 10 ps, the native sensor contribution to time measurement uncertainty tends to be negligible: the largely dominant limitation to system performance is represented by the electronics stage, which now becomes the main technical challenge concerning the final performance of our tracking device.

Developments on integrated electronics for 4D-tracking have started in the last couple of years. The particle physics community is decidedly oriented towards the choice of the CMOS 28-nm technology node for the next decade of developments in the field (Lai, 2022). This choice is mainly due to the need to adopt a technology with superior integration capability and higher resistance to radiation doses, compared to the previously used node (CMOS 65 nm) (CDS, 2020), which is manifestly unsuitable to integrate also timing capabilities at the pixel level. Characterization studies on CMOS 28-nm technology have shown resistance to doses greater than 1 Grad, whenever suitable design precautions are adopted (De Matteis, 2020).

The TimeSPOT project has carried out the first development ever of a CMOS 28-nm pixel readout ASIC for a HI4DT. This is a small-size prototype ASIC, named Timespot1, featuring a 32×32 pixel matrix, a 55 μm pitch and about 3 mm^2 of sensitive area (Cadeddu et al., 2023; Lai, 2022). Although still a preliminary implementation, the *Timespot1* have demonstrated the technical possibility to limit the time jitter at the AFE level below $\sigma_t \approx 30$ ps within the power budget of ≈ 20 μW per channel. Furthermore, the Timespot1 ASIC development has clearly emphasized the hard technical challenge represented by the implementation of a large area ASIC (≈ 2 cm^2), capable to ensure a time resolution better than 50 ps in each pixel with the required low power budget. The Timespot1 shows an unacceptable dispersion in the timing performance values across its 1,024 pixels (Figure 5). This clearly demonstrates the need of superior accuracy in the distributions of the clock and power lines, which must be kept under strict control even at the level of small areas.

The challenge for a large area timing ASIC for HI4DT is therefore still open. The ASIC developments initiated in the TimeSPOT project are being further pursued and refined within the INFN IGNITE project (The IGNITE Collaboration, 2025). A parallel CERN project, named LA-Picopix is also ongoing (Lopart, 2024). They have both the same target, which is being pursued with two alternative design approaches. Results are expected to arrive in the next couple of years.

2.4 Main results on 3D-trench sensors

The results obtained on TimeSPOT 3D sensor batches have been extensively and deeply described in several papers and conference talks (Brundu et al., 2021; Anderlini et al., 2020; Borgato et al., 2023; Borgato et al., 2024; Addison et al., 2024; Lai and Lampis, 2025). The reader is therefore invited to refer to those publications for any specific detail. However, it can be useful to summarize them here, emphasizing some features of particular relevance.

2.4.1 3D-trench sensors before irradiation

Before irradiation 3D-trench TimeSPOT pixels show a typical leakage current $I_{leak} < 10$ pA per pixel (55×55 μm^2) at room temperature, up to 100 V reverse bias. The breakdown voltage is typically above 150 V reverse bias (Forcolin et al., 2020).

Being the ohmic and junction electrodes not sensitive to MIPs, 3D-trench sensors have a geometrical inefficiency in detection of around 20% at 0° tilt angle α_{tilt}, corresponding to a perpendicular impinging direction with respect to the sensor surface. Such inefficiency is gradually recovered while the tilting angle is increased and is taken below 1% at $\alpha_{tilt} \approx 20°$ (Figure 7).

Typical time of arrival (ToA) distributions are obtained with a fast TIA front-end, and using a time reference with resolution

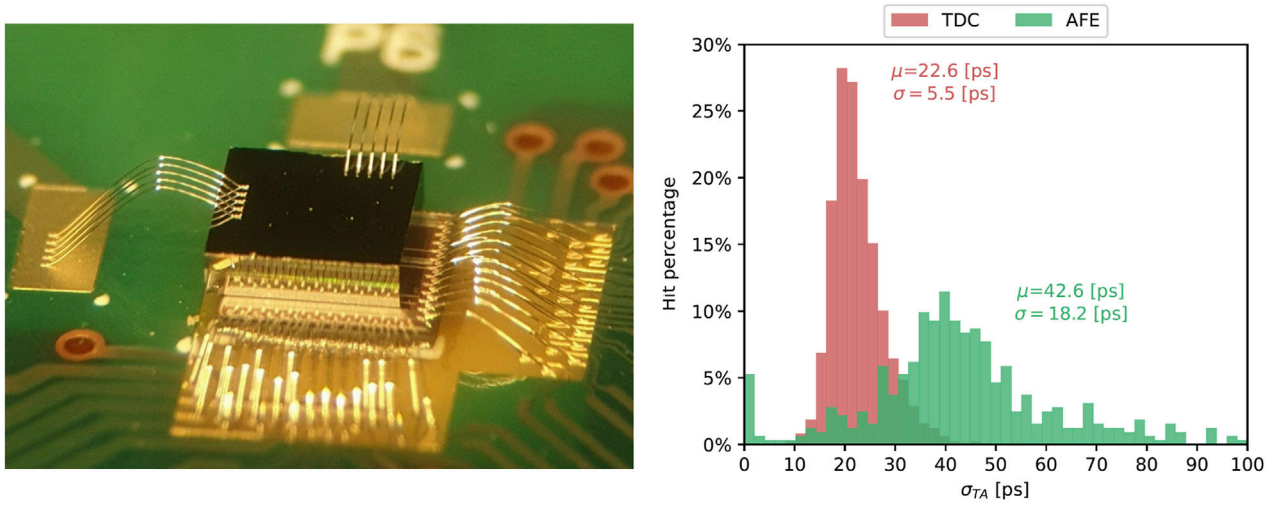

FIGURE 5
Left: The Timespot1 ASIC hybridized to a 32 × 32 3D-trench pixel matrix (placed on top). Right: Distribution of time resolutions σ_{TA}, acquired on test-bench, for the time arrival measured at the output of the Analog Front End and on the TDC only. The jitter performance on the AFE, although satisfactory in average, ranges on from 10 ps to 100 ps.

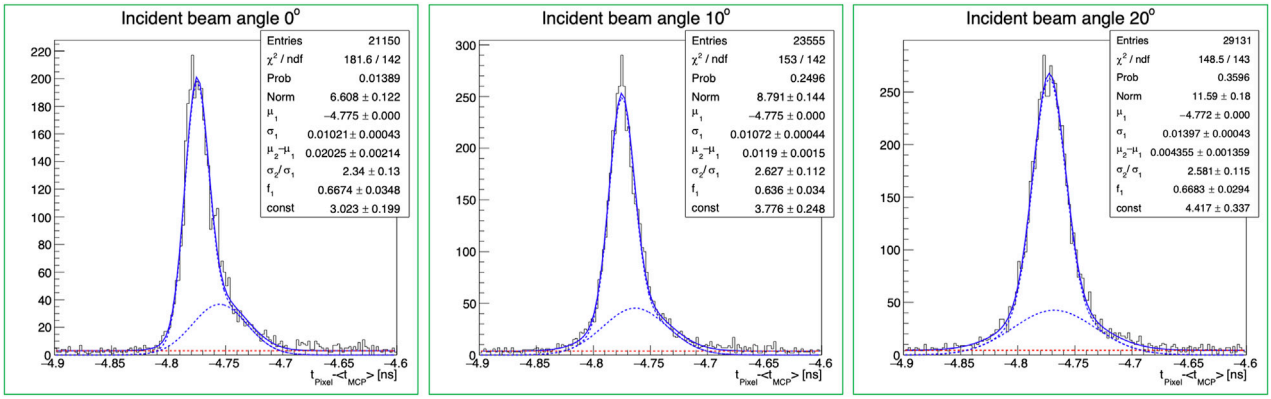

FIGURE 6
Time of arrival distributions at 50 V reverse bias and three different α_{tilt}. At $\alpha_{tilt} = 20^{\circ}$ the distribution is symmetric. An $\alpha_{tilt} \approx 20^{\circ}$ is the optimal operating condition of a 3D-trench sensor.

around 5 ps rms, based on MCP-PMT[1] devices. ToA distributions are slightly asymmetrical, presenting a small shoulder towards slower ToAs (see Figure 6). The measured time distributions can be perfectly fitted with two Gaussian curves, a bulk (fast) Gaussian and a correction (slow) Gaussian. A physical interpretation of such two-Gaussian behavior can also be given, assigning the slow Gaussian to entries of the restricted area of low-field contributions inside the pixel volume (refer also to the ToA map in Figure 2.Center). Such interpretation is confirmed by observing the shape of the time distributions for increasing tilt angles (Figure 6), which gradually become more symmetric with a possible single-Gaussian fit at large angles. Indeed, in a pixel operated at tilt angle above 15°, the timing contributions from the fastest and the slowest pixel regions are mixed, giving a more uniform response. TimeSPOT time resolutions are in any case quoted as an effective standard deviations σ_t^{eff}, which is a suitable weighted average of the two gaussian curves used in the distribution fit (Borgato et al., 2023):

$$\left(\sigma_t^{\text{eff}}\right)^2 = f_1\left(\sigma_1^2 + \mu_1^2\right) + \left(1 - f_1\right) \cdot \left(\sigma_2^2 + \mu_2^2\right) - \mu^2,$$

where f_1 is the fraction of the core Gaussian and μ is defined as $\mu = f_1\mu_1 + (1 - f_1) \cdot \mu_2$.

All the results published to date about tests on few-pixel structures have been obtained with a fast-TIA front-end (Cossu and Lai, 2023). Such tests are aimed at characterizing the performance limit of the sensor in time resolution. Time distributions have been constructed by acquiring the

1 Micro Channel Plate - Photon Multiplier Tube

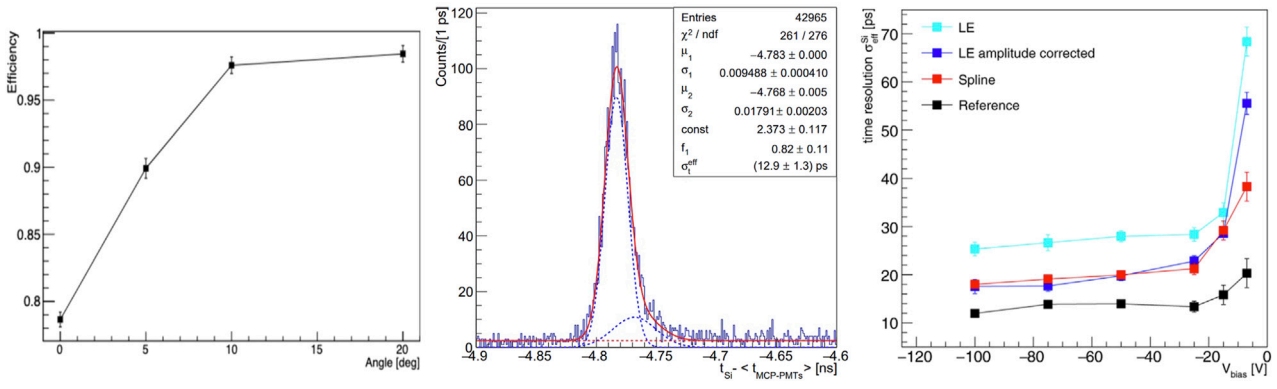

FIGURE 7
Performance of pre-irradiated TimeSPOT 3D-trench sensors. Left: Detection efficiency ε at different α_{tilt}. At $\alpha_{tilt} = 20^{\circ}$ $\varepsilon = (99.1 \pm 0.6)\%$. Center: Time distribution, showing $\sigma_t^{eff} = (12.9 \pm 1.3)$ps at 100 V reverse bias. Right: Time resolution σ_t^{eff} at different reverse bias voltages and using different analysis techniques (Borgato et al., 2023).

front-end output waveforms on a 8 GHz analog bandwidth 20 GSa/s 4 channels digital oscilloscope, and performing numerical waveform analysis. Analysis results have been quoted after four different alternative techniques (Figure 7): LE (Leading edge), i.e., fixed numerical threshold on the TIA signal, with no amplitude (time walk) correction; LE with amplitude correction; Numerical CFD (Constant Fraction Discriminator); ARC (Amplitude-Rise time Compensation) technique, that is a CFD technique with additional correction for the signal slope (Cho and Chase, 1972). The latter type of analysis has been also called Reference analysis, because it gives the most precise result.

Typical characteristics observed in time resolution measurements include the following: all techniques reach their peak performance at reverse bias voltages above 20 V, beyond which only minor improvements of 1–2 ps are observed (Figure 7). This indicates a broad operational plateau for sensor timing performance, extending from 20 V up to 150 V reverse bias.

With fast readout electronics, time resolutions well below 30 ps are achieved even using a simple LE discrimination technique, without the need for additional corrections or analysis. Applying amplitude corrections (CFD) improves the resolution to below 20 ps. Further refinement techniques (ARC) sharpen the resolution to approximately 10 ps.

Considering that the measured electronic jitter for a MIP energy deposit is around 7 ps, it is reasonable to estimate the intrinsic time resolution of the sensor alone to be better than 8 ps.

2.4.2 3D-trench sensors after irradiation

Test structures from the two TimeSPOT batches underwent three irradiation campaigns. All were performed with neutrons at JSI (Ljubljana) at the Triga Mark II Reactor facility. They correspond to the following fluences (Φ) in units of $1\,MeV\,n_{eq}/cm^2$:

1. $\Phi = 1 \cdot 10^{16}$ and $\Phi = 2.5 \cdot 10^{16}$;
2. $\Phi = 5 \cdot 10^{16}$ and $\Phi = 1 \cdot 10^{17}$;
3. $\Phi = 5 \cdot 10^{17}$ and $\Phi = 1 \cdot 10^{18}$.

The natural increase in leakage current caused by radiation is kept under control by operating the samples at temperatures below −20°C. Irradiated samples have been first tested with a red laser inside a climatic chamber, and then exposed to a 180 GeV/c π^+ beam at the CERN SPS (H8 beam line) being operated inside boxes cooled with dry ice. Details about the experimental setup can be found in Borgato et al. (2024).

The first step in testing irradiated samples involves compensating for the drop in Charge Collection Efficiency (CCE) due to charge trapping by increasing the bias voltage. A practical approach is to record amplitude spectra and use the Most Probable Value (MPV) from a non-irradiated sample as a reference. Full CCE recovery is considered achieved when the reference MPV is reached. A similar method can be applied to time resolution measurements, where the goal is to recover the pre-irradiation time resolution by increasing the reverse bias voltage. Results are illustrated in Figure 8.

Table 1 summarizes the results presented Borgato et al. (2024), Addison et al. (2024), and Lai and Lampis (2025). Tests at the two highest fluences were initiated in a climatic chamber but have not yet been completed. In fact, increasing the reverse bias voltage beyond 400 V was not tolerated by the front-end board, necessitating a specific redesign that is currently in progress. This also prevented the completion of meaningful timing tests, as full depletion of the detection volume could not be achieved. However, results obtained up to $\Phi = 10^{17}\,1\,MeV\,n_{eq}/cm^2$ already demonstrate that 3D silicon sensors are fully operational at extreme fluences, even beyond the requirements of HI4DT experiments of the next-generation, while still keeping outstanding performance in time resolution and efficiency.

3 Discussion

In this work it was shown a summary of the most relevant results obtained in the TimeSPOT project and in its immediate follow-ups. The TimeSPOT sensors and electronics have open a clear path

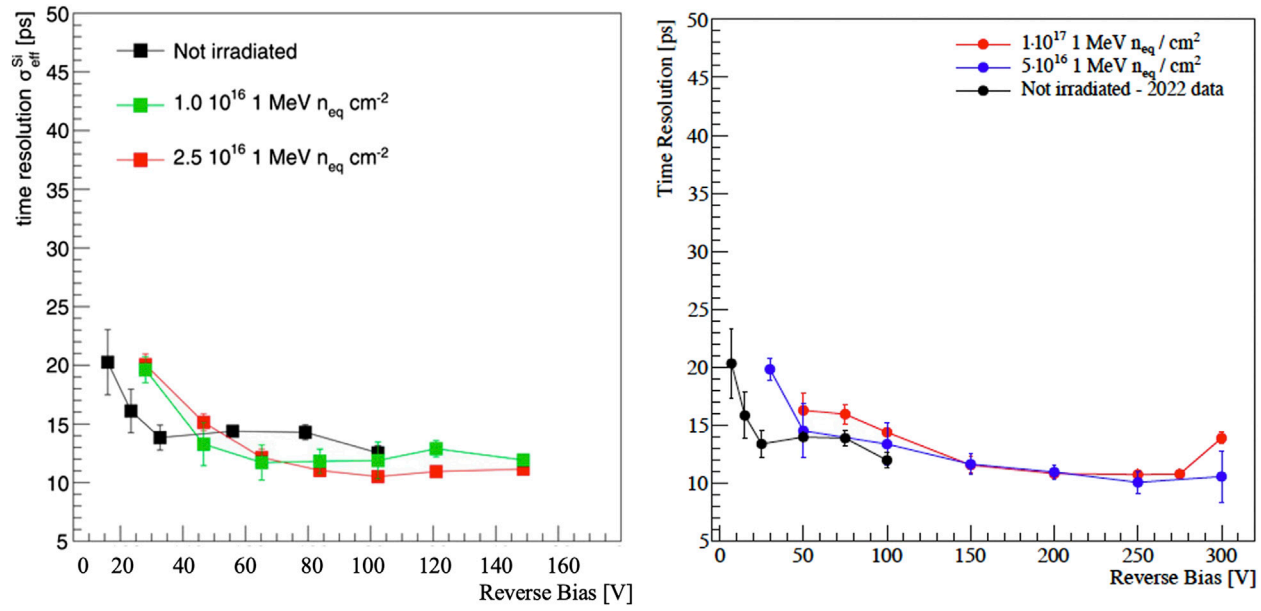

FIGURE 8
Performance of irradiated TimeSPOT 3D-trench sensors. Time resolution σ_t^{eff} at different reverse bias voltages and using different analysis techniques for four different fluences (Borgato et al., 2024; Addison et al., 2024).

TABLE 1 Operational reverse bias voltages vs. fluences. Fluences are given in units of $[10^{16}\ n_{eq}/cm^2]$.

Fluences	Reverse bias [V] for nominal CCE	Reverse bias [V] for T. res <20 ps	Notes
0	20	20	
1	60	40	
2.5	–	50	CCE not tested
5	220	100	
10	270	150	
50	70% at 400	NA	Preliminary
100	30% at 400	NA	Preliminary

towards the feasibility of High Intensity 4D Tracking, in the sense that have been specified above in the paper. Reaching the target timing performance below 50 ps per hit at the expected fluences of future experiments at colliders was not foregone before the TimeSPOT results. It can be said that the TimeSPOT technology has enabled this discovery path in fundamental research.

Such path has been enabled but is not yet concluded. Further developments are needed on 3D silicon sensor to improve production process and yield. On the other hand, integrated electronics still presents many issues to be solved about high resolution obtainable on large areas, while respecting very severe system constraints.

While also other research groups are attacking these problems, the TimeSPOT mission is evolving in the IGNITE project, which aims to solve the HI4DT challenge on the timing electronics side.

Author contributions

AL: Funding acquisition, Methodology, Writing – original draft, Investigation, Visualization, Validation, Conceptualization, Resources, Supervision, Project administration, Writing – review and editing.

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Conflict of interest

The author declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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