MULTILEVEL CONVERTERS: CONTROL TECHNIQUES FOR RENEWABLE ENERGY RESOURCES

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MULTILEVEL CONVERTERS: CONTROL TECHNIQUES FOR RENEWABLE ENERGY RESOURCES

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Analysis and Implementation of High-Performance DC-DC Step-Up Converter for Multilevel Boost Structure

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The conventional DC-DC converters such as SEPIC, boost converter, etc. produces large voltage ripples in multilevel converter systems. For that reason, in this paper, a new DC-DC converter topology is proposed, and the performance is analyzed. Since the proposed converter delivers high conversion efficiency, it can be selected for multilevel boost DC-DC converters. The adverse effects such as inductor resistance and inductor size of the conventional converters are overcome by the proposed converter. The output voltage ripples are reduced in the proposed converter, i.e., the spikes in the converter output voltage are almost zero. The theoretical analysis is presented in this paper, which speaks about the advantage of the proposed converter. The converter operation is analyzed and discussed in continuous conduction mode (CCM). The voltage gain of the proposed converter is higher than the conventional boost converter. To validate the performance of the proposed converter, an experimental prototype is fabricated and tested in the laboratory. The performance of the converter is compared with the conventional boost and SEPIC converter. The experimental result confirms the theoretical analysis. The proposed converter can be extended by connecting more number of voltage multiplier (VM) cells to get the desired multilevel output voltage.

Keywords: boost, CCM, multilevel boost, voltage gain, voltage multiplier, voltage ripple

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INTRODUCTION

The conventional boost dc-dc converter has several issues such as power loss, the voltage drop across various devices, and the effects due to the inductor resistance when it tries to achieve the required voltage gain. The quality of operation and the conversion efficiency is affected by the high duty cycle of the semiconductor switch (Premkumar et al., 2018a; Premkumar and Sumithira, 2019a). These problems are solved by introducing the new converters such as Zeta, SEPIC, and Cuk converters (Banaei and Bonab, 2016). The various converters are reported in Amir et al. (2019), and these converters are differentiated based on the switching methods (switching between the capacitor and inductor), and boosting techniques such as voltage multiplier (VM), voltage doubler, cascade connections, etc (Chen et al., 2018; Pop-Calimanu et al., 2019). Each of the converters has its drawbacks, and these drawbacks motivate the researchers to work on the new converters for the multilevel boost structure. For instance, the multilevel converters with conventional boost, Cuk, and SEPIC have output voltage ripples (Babaei et al., 2013; Selwan et al., 2015; Premkumar et al., 2018b).

The conventional buck-boost and boost converters are frequently preferred in solar photovoltaic systems, and fuel-based energy systems (Divakar et al., 2008; Kaouane et al., 2015; Premkumar et al., 2018b; Rosas-Caro et al., 2018a,b; Premkumar and Sumithira, 2019b). The authors in Kaouane et al. (2015) and Premkumar and Sumithira (2019b) reported converters with two MOSFET switches and hybrid boost, respectively, for solar photovoltaic (PV) systems to improve the output voltage gain along with the proper tracking technique. The quadratic buck-boost converter was reported by Rosas-Caro et al. (2018b) with the conversion output voltage and continuous input current with positive polarity.

The authors in Divakar et al. (2008) reported soft switching techniques such as zero voltage switching and zero-current switching to decrease the switching losses in the traditional boost converter. The authors in Hegazy et al. (2012) and Rosas-Caro et al. (2018a) reported the converters with the interleaved structure to achieve the required output voltage with the continuous input current. However, the interleaved structure is complicated when compared to the conventional boost converter. Besides, the author in Zeng et al. (2019) reported that the interleaved structure also helps to increase the conversion efficiency, and reduce the output voltage ripple. When the conventional interleave based boost or buck-boost converters are chosen for multi-level boost converters, it introduces a heavy spike in inductor current and the output voltage. The same can be observed from the experimental waveforms of the literature reported in Rosas-Caro et al. (2018a) and Hegazy et al. (2012).

The SEPIC converter is one of the conventional dc-dc converter derived from the traditional boost converter. Related to conventional boost converter and Cuk converter, the SEPIC converter has few ripples in the output current since the second inductor in the SEPIC converter smooths the current spikes. The SEPIC converter can be preferred in different applications such as PV system, fuel cell-based systems, and also multi-port converters (Saravanan and Babu, 2015; Buticchi et al., 2019). As a result, the SEPIC converter can be used for most of the renewable energy systems. Though the SEPIC converter voltage gain is less, and it can be used for step-up applications (Kircioglu et al., 2016; Shamshuddin et al., 2017; Premkumar et al., 2018c; Natarajan et al., 2019; Yousri et al., 2019). The voltage gain of the SEPIC converter is less than the conventional boost converter per duty ratio. The voltage gain of the SEPIC converter and boost converter is equal to D/(1-D), and 1/(1-D), respectively (Park et al., 2010; Ansari and Moghani, 2019). If the structure of the SEPIC converter is slightly modified, it may step-up voltage than the conventional boost converter. Therefore, in this paper, a modified structure for the SEPIC converter with high-quality output is discussed and examined.

A new structure is proposed for the SEPIC converter is proposed in this paper, and the converter is based on the traditional SEPIC converter. The major highlight of the proposed SEPIC converter is not having an extra parasitic element compared to the traditional SEPIC converter. A new structure is derived in a way such that a reduction in output voltage ripple and an increase in conversion efficiency. Moreover, the voltage gain is equal as the traditional boost dc-dc converter and higher than the conventional SEPIC converter with less effect of the inductor resistance. Another notable highlight of the proposed converter is its spike-free voltage and current waveforms. The efficiency of the converter is >95% when the duty ratio of the switch is <60%, >92% when the duty cycle of the switch is between 60 and 80%, and this advantage makes the converter a decent choice for the multi-level boost structure powered by the PV modules and fuel cells. The converter can also be extended to achieve high voltage gain by using elements such as inductors, diodes, and capacitors. The structure of the paper is as follows. Section Operation of the Proposed SEPIC Converter for Multi-Level Structure presents the operation of the proposed converter. The steady-state analysis under continues conduction mode (CCM) is performed in section Steady-State Analysis and Converter Comparison. The experimental results and further discussion are given in section Results and Further Discussions. The paper is concluded in section Conclusion.

OPERATION OF THE PROPOSED SEPIC CONVERTER FOR MULTI-LEVEL STRUCTURE

The converter proposed in this paper has high-quality output and high gain by making a small modification in the conventional SEPIC converter, as shown in **Figure 1**. In the proposed converter, the charging capacitor is changed its position, and the gain equation is altered accordingly. The proposed converter comprises one MOSFET switch, two capacitors such as the coupling capacitor (C_s), and the output capacitor (C_{out}), two inductors, namely L_1 and L_2, and one diode. For simplified analysis, the converter operation in CCM is divided into two modes of operation. Theoretical waveform is depicted in **Figure 2**.

The following are the assumptions made to streamline the converter examination.

- The various apparatuses of the converter are ideal. The forward drops of the switch and diode, on-state resistance

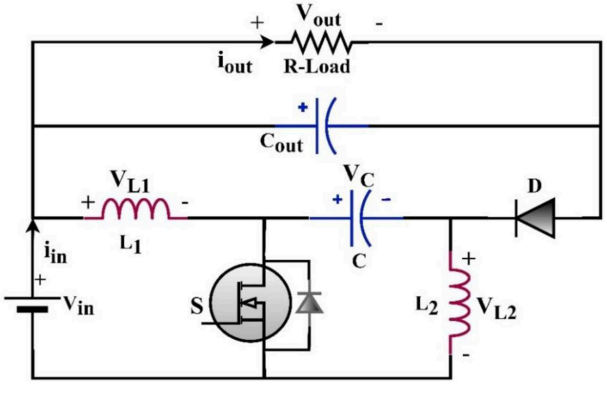

FIGURE 1 | Schematic of the proposed converter.

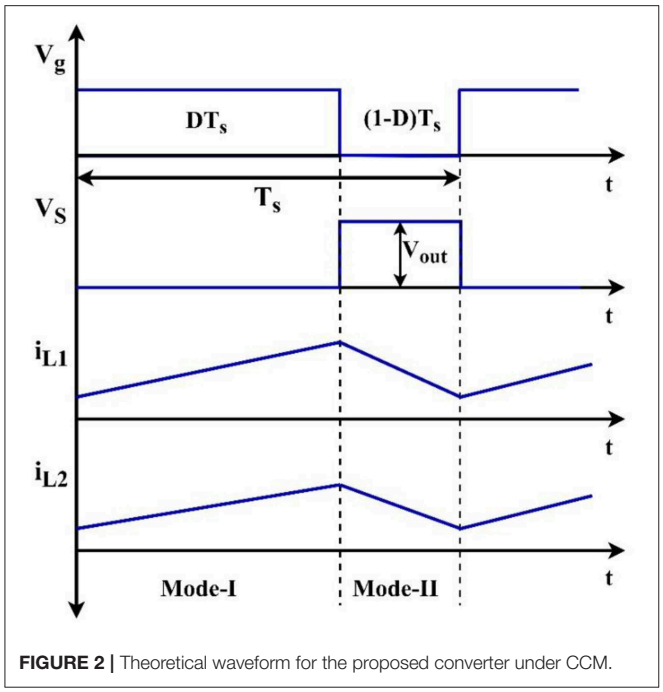

FIGURE 2 | Theoretical waveform for the proposed converter under CCM.

(R_{ds-ON}) of the MOSFET switch, the equivalent series resistance of the inductors, and capacitor are ignored.

- The capacitance values of the capacitors C_s and C_{out} are considered as high. Thus, the capacitor voltage is supposed to be constant during one switching cycle.

Mode-I

The current flow is depicted in **Figure 3A**. The analysis of the proposed converter is made by assuming the ideal components, and the converter is operated at CCM.

During this mode, the MOSFET switch is turned on by applying the pulse-width-modulated (PWM) signal to the gate terminal of the switch. When the switch is turned on, the current starts to flows the components such as C, L_1, and L_2. In **Figure 3**, the inductor currents are represented as i_{L1}, and i_{L2}, and the voltage across the coupling capacitor is represented by V_c. During mode-I, the diode is turned off due to the reverse voltage. There are three loops for energizing the storage components. The voltage across the inductor-1 (V_{L1}) is equal to the input source voltage (V_{in}) which rises the current in L_1. The source voltage also delivers the energy to the L_2 and the coupling capacitor (C) through the load. It is observed that the second and third loop is formed by the source voltage, C, and L_2. The voltage across the diode is equal to the voltage across the capacitor. The voltage across the inductor L_1 is presented in Equation (1), and other expressions are written as follows.

$$V_{L_1} = V_{in} = L_1 \frac{di_{L_1}}{dt} \tag{1}$$

$$V_c + V_{in} = L_2 \frac{di_{L_2}}{dt} + V_d + V_{out} \tag{2}$$

$$i_C = C \frac{dV_C}{dt} = i_{L_2} \tag{3}$$

$$i_{C_{out}} = C_{out} \frac{dV_{C_{out}}}{dt} = \frac{V_{out}}{R} - i_{L_2} \tag{4}$$

Mode-II

The current flow during this mode is depicted in **Figure 3B**. During this mode, the MOSFET switch is turned off. Due to this, there are two loops in the converter operation. The coupling capacitor is energized through the inductors L_1 and L_2. Both the inductors start to release the energy during this mode. The inductor L_2 also discharges, and the output capacitor delivers the load current. The voltage stress of the MOSFET switch is equal to the difference between the voltage across the inductor L_1, and the source voltage. Various output equations during mode-II are presented as follows.

$$V_{in} = L_1 \frac{di_{L_1}}{dt} + V_c + L_2 \frac{di_{L_2}}{dt} \tag{5}$$

$$L_2 \frac{di_{L_2}}{dt} = V_{in} - V_{out} \tag{6}$$

$$i_C = C \frac{dV_C}{dt} = i_{L_1} \tag{7}$$

$$i_{C_{out}} = C_{out} \frac{dV_{C_{out}}}{dt} = \frac{V_{out}}{R} - i_{L_2} \tag{8}$$

STEADY-STATE ANALYSIS AND CONVERTER COMPARISON

The steady-state analysis of the proposed converter is presented under the CCM operation. The voltage conversion of the proposed converter is the most significant parameter, and the same can be obtained from the above-two operating modes of the converter. The energy balance in the proposed converter is achieved by the charging and discharging cycle of the inductors L_1 and L_2. The average voltage of the inductors over one switching cycle is zero. The average voltage of the inductor is derived from the above-said equations. The average voltage equation is presented in Equations (9, 10).

$$DV_{in} + (1-D)(V_{in} - V_C) = 0 \tag{9}$$

$$D(V_{in} + V_C + V_{out}) + (1-D)(V_{in} - V_{out}) = 0 \tag{10}$$

From Equations (9, 10), the voltage across the capacitor, and the voltage gain of the converter being stated in Equations (11, 12).

$$V_C = \frac{1}{1-D} V_{in} \tag{11}$$

$$M = \frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{12}$$

As seen in Equation (12), the voltage gain of the proposed converter is similar to the traditional boost converter. Therefore, the proposed converter can be compared with conventional SEPIC and Cuk converters. The converters can be analyzed based on the current stress and voltage stress on the MOSFET switch under DCM and CCM operation, voltage gain, and the minimum inductance requirements. **Table 1** shows the essential parameters of the converter and the other conventional converters.

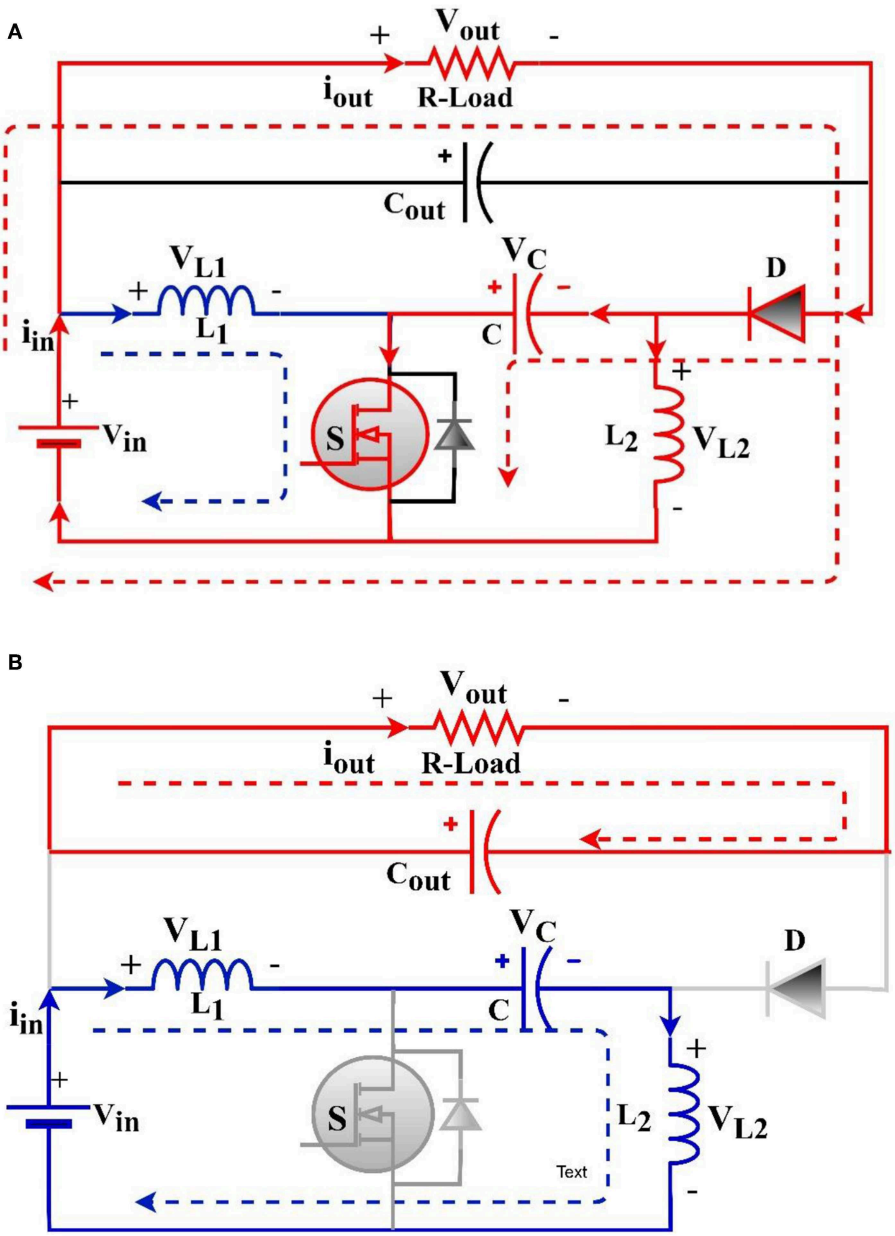

FIGURE 3 | Modes of operation; **(A)** Mode-I; **(B)** Mode-II.

The voltage stress on the MOSFET switch and the diode is obtained based on the modes of operation. The voltage stress on the diode is presented in Equation (13).

$$V_d = -V_C = -\frac{1}{1-D}V_{in} \tag{13}$$

During mode-II, the MOSFET switch is turned off. Thus, the voltage stress on the MOSFET switch is presented in Equation (14).

$$V_s = V_{in} - V_{L_1} = V_C = \frac{1}{1-D}V_{in} \tag{14}$$

The energy balance is obtained between the input and the output by the inductor elements. Based on the volt-second balance equation, the current through the inductors i_{L1} and i_{L2} are calculated as follows, and further, the current stress on the MOSFET switch is obtained.

$$V_{in}(i_{L_1} - i_{L_2}) = V_{out}I_{out} \tag{15}$$

From Equation (15), the current through the inductors are obtained as follows.

$$i_{L_1} = \frac{D}{1-D}i_{out} \tag{16}$$

$$i_{L_2} = i_{out} = \frac{V_{out}}{R} \tag{17}$$

Based on the above-said equations, the current stress on the diode and the MOSFET switch is obtained as follows.

$$i_d = i_{out} = \frac{V_{out}}{R} \tag{18}$$

$$i_s = \frac{D}{1-D} i_{out} \tag{19}$$

The inductor current oscillates between the minimum and maximum value depends on the inductance, and it is considered as the essential element in the converter design. Thus, the current ripple of the inductor and its respective inductance is calculated by considering the operating stages of the converter. The peak-peak ripple current over one switching period is calculated as follows.

$$\Delta i_{L_1} = \frac{DT_s}{L_1} V_{in} \tag{20}$$

$$\Delta i_{L_2} = \frac{DT_s}{L_2} V_{in} \tag{21}$$

The values of the inductances decide the boundary between DCM and CCM operation of the proposed converter. By assuming the minimum inductor current ($I_{L,min}$) is zero,

TABLE 1 | Assessment of the proposed modified SEPIC converter with the traditional converters.

Parameters	SEPIC converter	Cuk converter	Boost converter	Proposed modified SEPIC converter
M	$\frac{D}{1-D}$	$-\frac{D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
$L_{1,min}$	$\frac{(1-D)^2R}{2F_sD}$	$\frac{(1-D)^2R}{2F_sD}$	$\frac{D(1-D)^2R}{2F_s}$	$\frac{(1-D)^2R}{2F_s}$
$L_{2,min}$	$\frac{(1-D)R}{2F_s}$	$\frac{(1-D)R}{2F_s}$	-	$\frac{D(1-D)R}{2F_s}$
$\frac{\Delta V_{out}}{V_{out}}$	$\frac{D}{RC_{out}F_s}$	$\frac{(1-D)}{8L_2C_{out}F_s^2}$	$\frac{D}{RC_{out}F_s}$	$\frac{D(1-D)}{RC_{out}F_s}$

TABLE 2 | Specifications of the proposed SEPIC converter and other converters.

Parameters	Values		
	SEPIC converter	Cuk converter	Proposed converter
Input voltage, V_{in}	20 V	20 V	20 V
Inductors, L_1, L_2	1.4 mH	1.4 mH	1.4 mH
Coupling capacitor, C	10 μF	10 μF	10 μF
Output capacitor, C_{out}	220 μF	220 μF	220 μF
Load resistance, R	85 Ω	85 Ω	85 Ω
Switching frequency, F_s	20 kHz	20 kHz	20 kHz

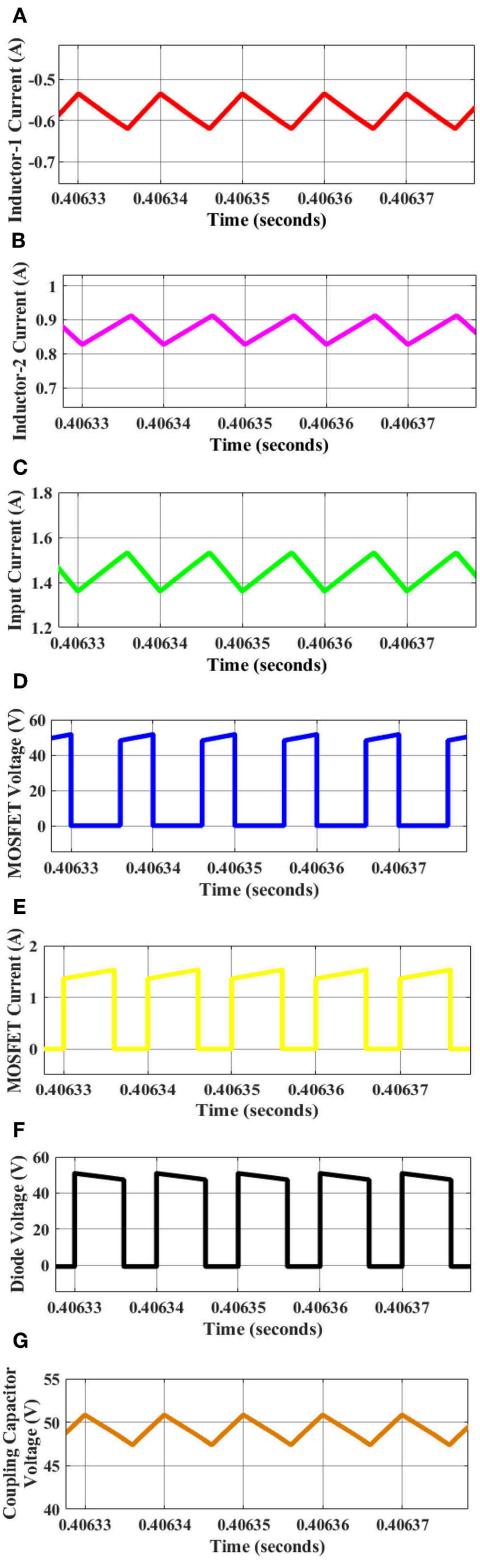

FIGURE 4 | Various simulation waveforms of the proposed converter; **(A)** Inductor current, i_{L1}, **(B)** Inductor current, i_{L2}, **(C)** Input current, I_{in}, **(D)** Voltage stress of the MOSFET, **(E)** Current stress of the MOSFET, **(F)** Voltage stress of the diode, **(G)** Voltage across coupling capacitor.

the minimum inductance of the inductors is calculated as follows.

$$I_{L,\min} = I_L - \frac{\Delta I_L}{2} \tag{22}$$

$$L_{1,\min} = \frac{(1-D)^2 R}{2F_s} \tag{23}$$

$$L_{2,\min} = \frac{D(1-D)R}{2F_s} \tag{24}$$

Where ΔI_L is the current ripples of both the inductors, and it is given by $(DT_s/L)V_s$. The peak-peak output voltage ripples of the proposed converter can be obtained by the differential equations. Since the proposed converter has two capacitors, the output voltage can be written as follows.

$$\frac{\Delta V_C}{V_c} = \frac{RC}{D} F_s \tag{25}$$

$$\Delta V_{C_{out}} = \Delta V_{out} \tag{26}$$

$$\frac{\Delta V_{out}}{V_{out}} = \frac{D(1-D)}{RC_{out}F_s} \tag{27}$$

RESULTS AND FURTHER DISCUSSIONS

The proposed converter, and the traditional converters such as SEPIC converter, and Cuk converters are simulated using MATLAB/Simulink software. To check the effectiveness of the proposed modified SEPIC converter, an experimental prototype is made, and the same is tested in the laboratory. The storage elements such as L_1, L_2, C, and C_{out} are selected as per the previous discussions. The inductors are chosen based on Equations (23, 24) by considering the CCM operation of the converter. Various parameters of the proposed modified SEPIC converter for both the simulation and experimental study are presented in **Table 2**. The simulation parameters of the SEPIC converter and Cuk converter, also listed in **Table 2**.

Simulation Study

As per the values presented in **Table 2**, the converters are designed and simulated using MATLAB/Simulink software. To check the performance of the proposed converter, the traditional converters such as Cuk and SEPIC converter also simulated. For the simplified analysis, the output voltage of the Cuk converter is assumed as a positive voltage; however, the actual output voltage of the Cuk converter is negative. First, the proposed converter is simulated with the duty cycle (D) of 0.6, and the results were depicted in **Figure 4**.

As seen in **Figure 4**, the proposed converter is operated at CCM operation. As shown in **Figures 4A,B**, the inductor currents (i_{L1} and i_{L2}) is oscillating between −0.55 A to −0.62 A, and 0.83 A to 0.91 A, respectively. This result proves that the proposed converter is operated under CCM operation. Another significant advantage of the proposed converter is continuous (constant) input current, and the same can be observed in **Figure 4C**. The input current is oscillating between 1.38 A and 1.52 A. Thus, the input ripple current of the proposed converter is observed as 0.14 A, which is less than the conventional SEPIC converter, and Cuk converter. **Figures 4D,E** shows the voltage and current stress of the MOSFET, respectively. The maximum voltage stress of the MOSFET switch is observed as 49.5 V, and the current stress is found as 1.5 A. **Figure 4F** depicts the voltage stress of the diode, and it is equal to the voltage across the coupling capacitor. **Figure 4G** illustrates the voltage across the capacitor, and the average voltage is observed as 49 V. Therefore, the diode voltage stress is equal to 49 V as shown in **Figure 4F**. As per the previous discussion, the proposed converter, and

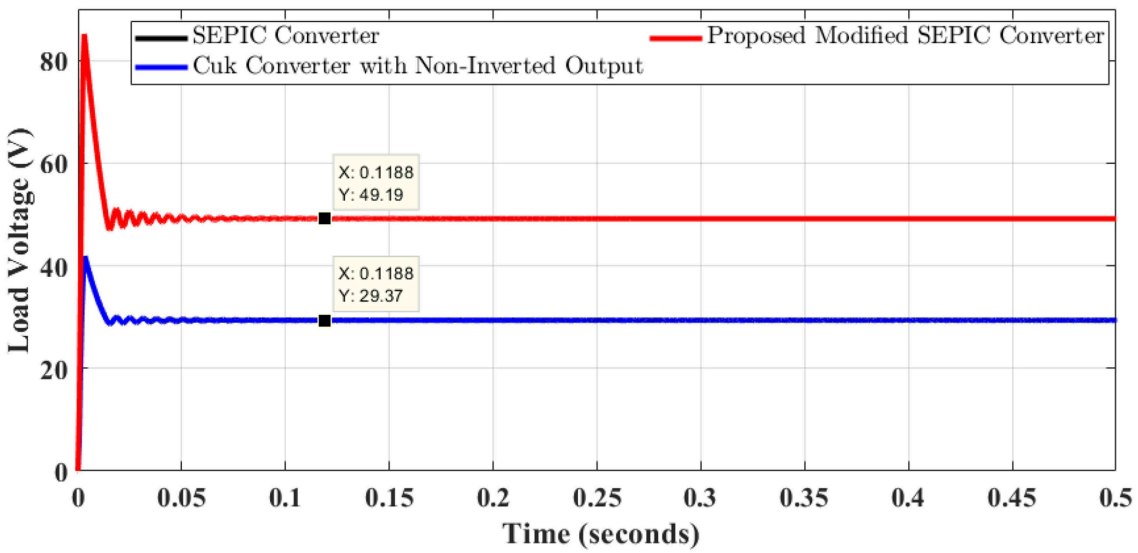

FIGURE 5 | Load output voltage waveform of all the converters at D = 0.6.

other traditional converters such as SEPIC converter, and Cuk converter also simulated for the duty cycle at 0.6. The load output voltage waveform of all the converters are depicted in **Figure 5**.

The load resistance of all the converter is kept constant at 85 Ω, and the output voltage of the SEPIC converter and Cuk converter is observed as 29.37 V (Cuk converter output voltage is assumed as positive). Whereas, the output load voltage of the proposed modified SEPIC converter is 49.19 V, which is 0.7 times higher than the conventional SEPIC converter. It is also observed that the settling time of all the converters is almost similar. It is concluded that the converter proposed in this paper is having more voltage gain than the traditional SEPIC converter with the same number of components. This high voltage gain is possible only by changing the connections of the conventional SEPIC converter, but not by increasing/decreasing the storage elements or switching devices. The proposed converter is also simulated for different duty cycles, such as 0.4, 0.5, 0.6, and 0.7. The converter switch duty is changed after 0.5 s, duration each. The output load voltage waveform is shown in **Figure 6**.

At the start, all the converters are operated with D=0.4, the output voltage of the SEPIC, Cuk, and proposed converter was observed as 13.57 V, 13.57 V, and 32.51 V, respectively. At t = 0.5 s, the duty cycle is changed to D = 0.5, and the output voltage is witnessed as 19.18 V, 19.18 V, and 39.17 V, respectively. At t = 1 s, the duty cycle is changed to D = 0.6, and the output voltage is observed as 29.38 V, 29.38 V, and 49.16 V, respectively. At t = 1.5 s, the duty cycle is changed to D = 0.7, and the output voltage is observed as 46.35 V, 46.35 V, and 65.72 V, respectively. It is observed and concluded that the duty up to D = 0.5, the SEPIC converter, and the Cuk converter acts as a buck converter, and after D = 0.5, the traditional converters act as a boost converter. Whereas, the proposed converter acts as the boost converter

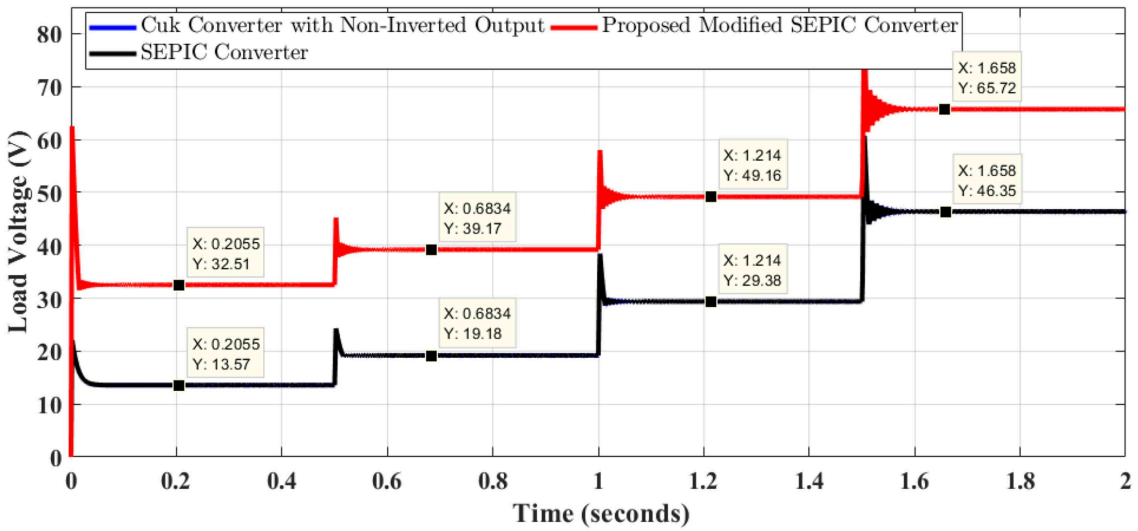

FIGURE 6 | Load output voltage waveform of all the converters at a various duty cycle.

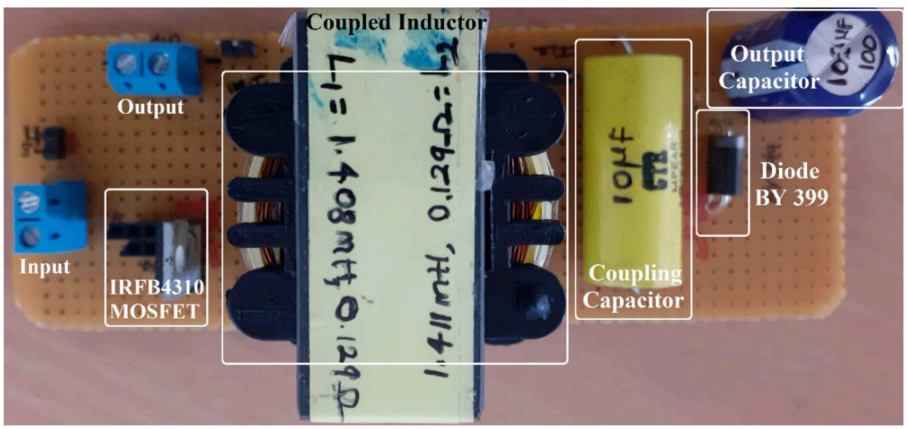

FIGURE 7 | Experimental prototype of the proposed converter.

irrespective of the duty cycle as similar to a conventional boost converter with constant input current capability.

Experimental Study

The experimental prototype of the converter is developed and verified in the laboratory environment as per the parameters are shown in **Table 2**. The experimental prototype is shown in **Figure 7**. Two inductors of the converter are selected as coupled inductors with EE33 ferrite core. Two strings of twisted copper wire (21 SWG) are wounded on the ferrite core to design the required value of inductance, and twisted pair can minimize the skin effect and coil resistance. The polypropylene metalized film capacitor is selected for a coupling capacitor, which has low ESR ($\approx$ 12.2 mΩ). A low on-state resistance N-Channel MOSFET switch is required for the converter operation, so IRFB4310 MOSFET is selected, which has 5.6 mΩ on-state resistance, and it can withstand up to 100 V, 140 A.

The converter requires a fast-acting diode to direct the current. Therefore, BY399 fast recovery diode is selected which has less forward voltage drop (<1.1 V) with less reverse recovery time (<500 ns). The PWM pulse is generated using the MSP430FR2355 Texas Instrument development board. A 20 kHz

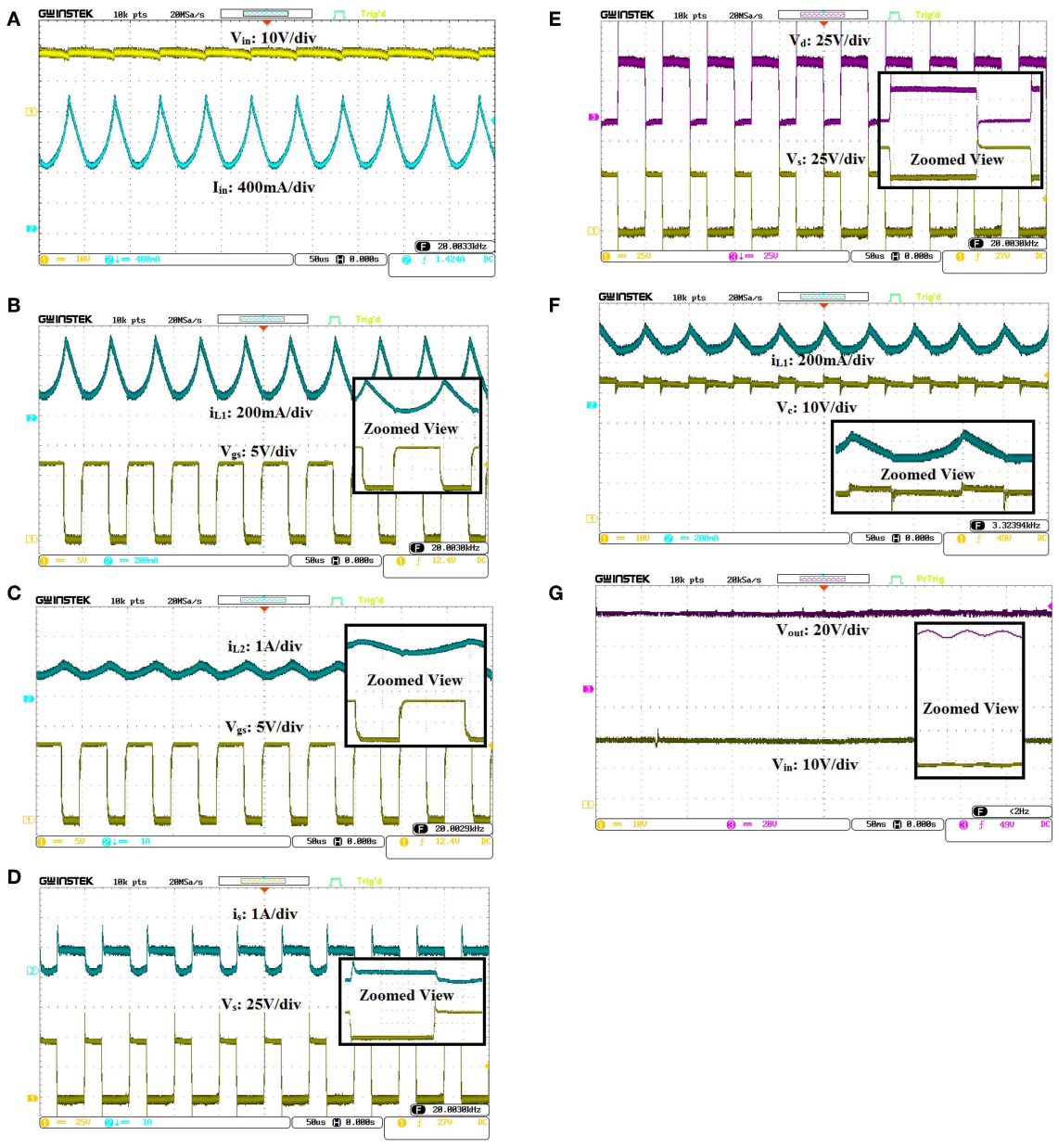

FIGURE 8 | Experimental waveforms of the converter for 60% duty cycle. **(A)** Input voltage, V_{in} and input current, I_{in}; **(B)** inductor current, i_{L1} and gate-source voltage, V_{gs}; **(C)** inductor current, i_{L2} and gate-source voltage, V_{gs}; **(D)** MOSFET current stress, is and MOSFET voltage stress, V_s; **(E)** MOSFET voltage stress, V_s and diode voltage stress, V_d; **(F)** Inductor current, i_{L1} and voltage across the capacitor, V_c, **(G)** Input voltage, V_i and output voltage, V_{out}.

PWM pulse with a 60% duty cycle is given to the MOSFET driver through the optoisolator. The MOSFET switch is driven with 4N25 optoisolator and IR2113 MOSFET driver. The proposed converter prototype is made for 50 W. The proposed converter rating can be extended using multiplier cell circuits if necessary. The adoption of the multiplier circuit is not discussed in this paper. The experimental waveforms are depicted in **Figure 8**.

Constant input current is one of the key objectives of this paper, and the same can be seen in **Figure 8A**. The input current at full load is 1.424 A (average). The input current oscillates between 0.9 A and 1.72 A, and it never reaches zero. The inductor currents such as i_{L1} and i_{L2} are depicted in **Figures 8B,C**, respectively. It is observed from **Figures 8B,C**, the converter is operated under CCM operation. The peak-peak inductor ripple current as per Equations 20, 21 is selected as 0.43 A. From **Figure 8B**, the ripple current (Δi_{L_1}) is observed as 0.45 A (oscillation between 0.56 A−0.11 A), and from **Figure 8C**, the ripple current (Δi_{L_2}) is observed as 0.44 A (oscillation between 0.71 A−1.15 A). This result displays good agreement between the theoretical analysis and the experimental setup. The MOSFET voltage stress and diode can be observed in **Figures 8D,E**, respectively. As per Equations 13, 14, the maximum voltage

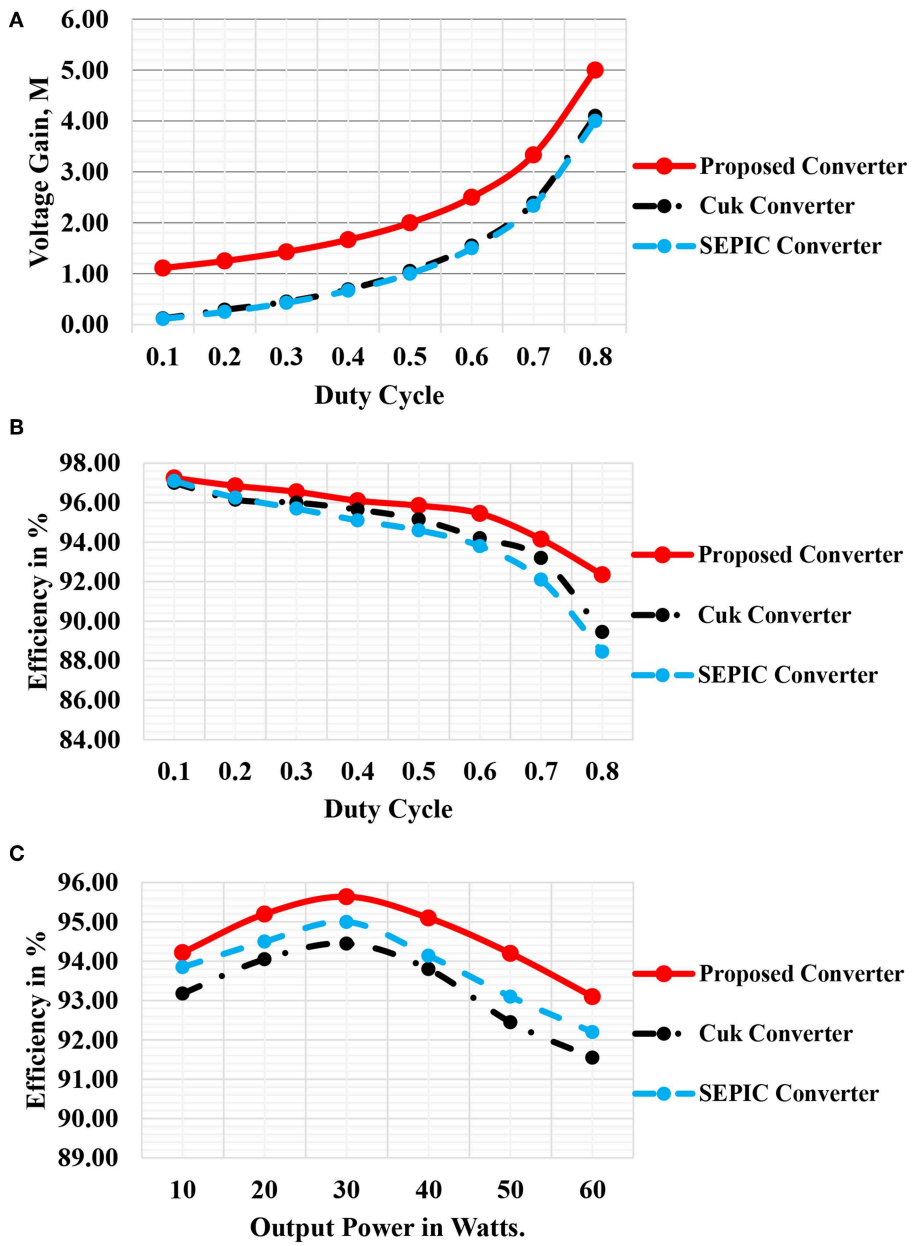

FIGURE 9 | Performance assessment of the proposed converter; **(A)** Voltage gain for several duty cycles, **(B)** Efficiency at various duty ratio, **(C)** Efficiency at different loading conditions.

stress of the MOSFET switch and the diode is equal to $\pm V_{out}$. Therefore, the voltage stress of the MOSFET and diode should be equal to 50 V when the duty cycle of the switch is 0.6. The same can be observed clearly in the waveforms as shown in **Figures 8D,E**. As per Equation 19, the current stress of the MOSFET switch is equal to 0.88 A. From **Figure 8D**, the current stress is observed as 0.84 A. As per Equation 11, the voltage across the coupling capacitor is equal to the output voltage of the converter which is equal to 50 V. The coupling capacitor voltage observed in **Figure 8F** is equal to 49 V. **Figure 8G** depicts the output voltage and the input voltage waveform. As per Equation 12, the output voltage of the converter for the duty cycle, D = 0.6, is equal to 50 V. The converter achieves 49 V experimentally, and this result displays good agreement between the theoretical analysis and the experimental setup. The difference in voltage ($\approx$ 1 V) can be ignored due to the voltage drop in other components. The proposed converter is compared with the other traditional converters in terms of voltage gain and efficiency. **Figure 9** shows the performance comparison of the proposed converter.

From the above discussions and the performance comparison presented in **Figure 9**, it is concluded that the proposed converter is superior in all aspects such as constant input current, high voltage gain, and high conversion efficiency without adding any extra components with the conventional SEPIC converter. The proposed converter is best suited for multi-level boost structure in solar photovoltaic systems or fuel-cell based energy systems instead of the traditional SEPIC converters. Finally, it is concluded that the proposed SEPIC converter can deliver the conversion efficiency at full load condition is equal to 94.2, and 95.64% maximum conversion efficiency.

CONCLUSION

The converter discussed in this paper improves the voltage conversion ratio than the other traditional dc-dc converters. The proposed SEPIC converter is analyzed in CCM operation, simulated, implemented, and compared with the traditional SEPIC, and Cuk converters. The analysis of various features such as inductor ripple current, voltage conversion, switch and diode voltage stress, and the converter efficiency is made for the proposed converter. The proposed converter is designed based on the theoretical discussions. The results obtained from the simulation, and experimentation is on par with the theoretical discussions. The conversion efficiency of the proposed converter is more than 92% for various duty cycle, and the maximum efficiency is equal to 95.64% at 30 W. This high conversion efficiency makes the proposed converter best suitable for the multilevel boost structure. The converter voltage gain can be further extended by adding the voltage multiplier circuits, and the same will be discussed and developed in future communications. The significant contribution in this paper is that the conventional SEPIC converter is extended without adding any additional equipment, and it behaves like a traditional boost converter with added features as following. (i) high voltage gain, (ii) high conversion efficiency, (iii) continuous input current, and (iv) less output voltage ripple.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation, to any qualified researcher.

AUTHOR CONTRIBUTIONS

Research simulation, experimentation, analysis, revision, and overall layout formation were carried out by MP. Literature review, mathematical analysis, simulation, and proof-read was done by RS. Redesigning the hardware components, experimental testing, revised article, and final proof-read by CK.

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An Improved Response of Multi Level Inverter Based PR Controlled SMPS

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This paper mainly focuses on identifying an optimum controller for Multi Level Inverter Based Switched Mode Power Supply (MLIBSMPS) for constant voltage applications. Generally, there is a greater demand of constant voltage for the sensitive loads. A closed loop control is introduced in the circuit in order to obtain constant voltage quickly if there are any disturbances occur at the input side. In this paper, closed loop Proportional Integral (PI) as well as Proportional Resonant (PR) controlled MLI based SMPS systems are simulated and the comparison of their performance is done. It is seen that an acceptable performance is achieved using PR controlled MLI based SMPS than PI Controlled MLI based SMPS. It also proves that PR Controlled SMPS with 7 level inverters has reduced steady state error and improved time domain response as compared to PI Controlled SMPS.

Keywords: multi level inverter based switched mode power supply (MLIBSMPS), proportional integral controller (PIC), dynamic response, proportional resonant controller (PRC), steady state error

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INTRODUCTION

Switching converters are in greater demand after the evolution of semiconductor technology. Nowadays, Switched Mode Power Supply (SMPS) with greater efficiency can be designed easily with lesser weight and cost effective. SMPS has also become increasingly popular due to its greater efficiency in distributing power to electronic device (Guo et al., 2010). In SMPS, fly back topology is mostly preferred due of its simple design, low cost, and greater efficiency compared to other topologies (Halder, 2014a). This fly back converter is used in applications where the load requires to be separated from mains supply. In addition to the good input/output isolation, the fly back converter uses lesser magnetic and semiconductor components that makes it a perfect converter for low- cost power supply applications (Halder, 2014b; Deepa et al., 2015). This converter steps up as well as steps down the input voltage retaining the similar polarity and ground reference for the input as well as output. MOSFET is used as a switching device whose turn-on and turn-off time is less when compared with other switching devices (Law et al., 2017). Switching devices with higher power handling capacity and switching speeds are readily available in the market. In this paper, fly back converter is cascaded which involves connecting multiple converters in parallel thus operating these converters at a phase shift of $360^{\circ}/n$ (n = number of converter modules). Due to cascading, the effective switching frequency can be increased "n" times which in turn high frequency harmonic components can be filtered easily. This cascaded fly back converter reduces the current ripple at both the input as well as output side. The main advantages of cascading are the reduction of cost and size of power filtering components and improved dynamic load performance (Sahu et al., 2016). A 7 level Multi Level Inverter (MLI) is used which is appropriate for high- power and medium voltage operation. In addition to greater power quality, MLI has better electromagnetic interference and lesser switching losses (Dogra and Pal, 2014). This multilevel inverter generates stepped voltage

output with the help of numerous dc voltage sources produced by the fly back converter. Practically, it is impossible to expect the load and input voltage to remain constant. Variations in load and input voltages will affect the output voltage which is not desirable (Chandran and Jothi, 2013). To overcome the above drawback, a closed-loop configuration is used wherein a part of the output is fed back to the switch which suitably corrects the duty ratio to maintain the output voltage constant (Sasikala and Krishnakumar, 2019). The PI and PR controllers are used in the feedback path to change the converter duty cycle which in turn the output voltage is regulated (Alzate and Posada, 2017). This works also evaluates the dynamic response and transient behavior of the systems.

BRIEF LITERATURE SURVEY

Isolated Switched-Mode Power Supply was presented by Reshma et al. A new idea in the design of switched mode energy conversion is given on the account of its intense simplicity, flexibility and performance. It has the capacity to replace a few conventional electric power processing techniques presently in use (Reshma et al., 2016). Multilevel power conversion system was presented by Babaei (2008). It emphasizes the use of multilevel inverters with less number of switches. Various topologies are discussed for utility and drive applications. Based on switching frequency and voltage sustaining capability, the selection of power devices has been investigated (Ebrahimi et al., 2012). Alishah et al. (2015) introduces the multilevel converters for the utility of renewable energy systems. Benefits of multilevel inverters such as improved power quality, simple design, and little switching stress along with the suitability for medium to high power applications are discussed.

MLI is used for power conversion and the reduction of load harmonics. As there is a greater demand in industry, conventional two level- inverter can be replaced with MLI. MLI has gained attention as it has low electromagnetic interference, high efficiency, and low switching frequency applications (Anjali et al., 2018).

A new topology with fewer bidirectional switches and power diodes count is compared against the other topology (Ludois et al., 2010). This paper presents a novel topology for the symmetrical multilevel inverter using a multi-output fly back converter but the bidirectional switches and gate driver circuits' count is very high (Noman et al., 2016; Sangeetha et al., 2016). This topology uses a single DC source which can be from renewable energy sources or energy storage devices (Ajami et al., 2014). The DC input is given to the multiple output fly back converter. The fly back converter's output is fed to the multilevel inverter to produce a seven level output. This structure needs a few switch counts in contrast with the conventional type of MLI (Xiao et al., 2015; Shankar et al., 2017; Lodh et al., 2018).

The modern controller usage in closed loop SMPS is totally fascinating. Various controllers like adaptive controllers, Sliding Mode controllers and Lyapunov based techniques are used for controlling the voltage in typical DC-DC converters (Salimi et al., 2015). In any case, switching power supplies (fly back and push-pull converter) haven't been researched unequivocally utilizing non-linear control draws near.

Likewise in mechanical switch mode power supplies, the change in load and line can be noticed under different operational conditions which lead to instability of the ordinary closed loop controller. Contrasted with other modern controllers, fly back control supply is utilized broadly in applications where low as well as medium power is sufficient (Kalirasu, 2017).

RESEARCH GAP

The above papers do not report the use of MLI for Switched Mode Power Supply (SMPS) and also the comparison of Proportional Integral (PI) and Proportional Resonant (PR) controlled SMPS is not dealt with. This work proposes MLI for SMPS and also compares the dynamic behavior of Proportional Integral (PI) and Proportional Resonant (PR) controlled SMPS.

BASIC EQUATIONS

The Basic equation for calculating the output of the fly back converter is given by,

$$V_0 = \{D*(N2/N1)*Vi\}/(1 - D) \quad (1)$$

where
Vi = Input Voltage
V_0 = Output Voltage
D = duty cycle
N2/N1 = transformer turns ratio
The Number of turns in the transformer is given as

$$N1 = V1/k*q*f \quad (2)$$

$$N2 = V2/k*q*f \quad (3)$$

where k = 4.4
q = maximum flux in the core
f = frequency in Hz
V_1 and V_2 are the RMF values of induced EMF in the primary and secondary winding, respectively.

The peak primary current (i_p) is dependent on the input voltage Vi, the primary inductance L_p and the on time of the switch,

$$i_p = (Vi*t_{on})/L_p \quad (4)$$

The average power delivered to the load,

$$P_{av} = (Lp*i_p^2)/2T$$

where
L_p = primary inductance if the transformer
T = switching period
Efficiency of the converter

$$e = V_2I_2/V_1I_1 \quad (5)$$

The PI controller is used in industrial application as it is simple and easy to design and effective. This controller removes all the unwanted oscillations and steady state error. The transfer-function of a PI controller takes the form of

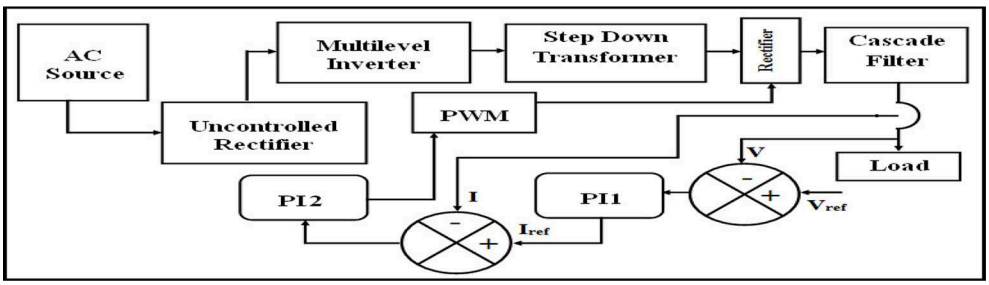

FIGURE 1 | MLIBSMPS block diagram with PI controller in two loop mode.

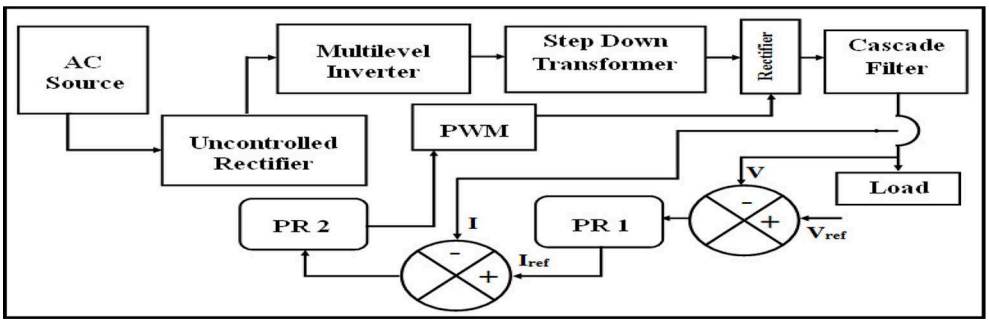

FIGURE 2 | MLIBSMPS block diagram with PR controller in two loop mode.

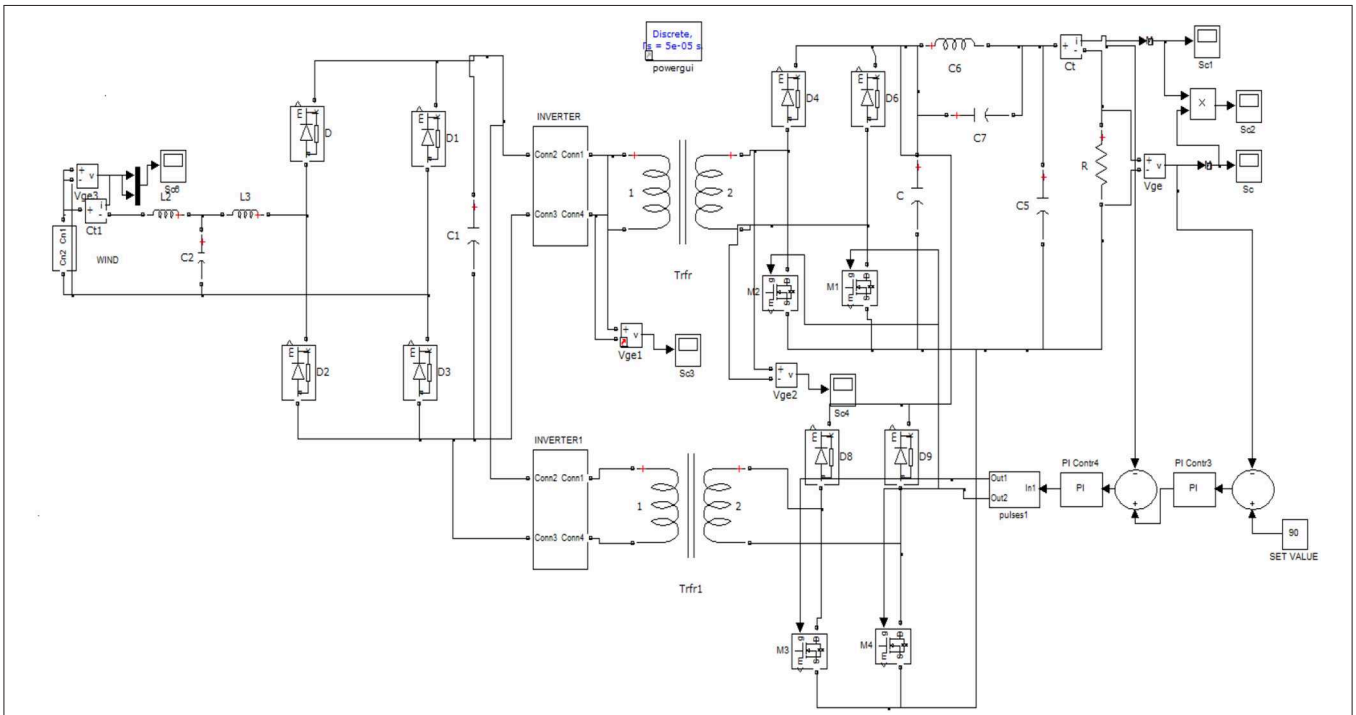

FIGURE 3 | Simulation diagram of MLIBSMPS with PI controller in two loop mode.

$$C_{PI}(s) = K_1 + K_2/s \quad (6)$$

$$C_{PR}(s) = K_1 + K_2 w/(s^2 + w^2) \quad (7)$$

where

K_1 = proportional constant

K_2 = Integral constant

The model of PR was established from fractional-differentiation. The PR controller introduces an infinite gain at a particular resonant frequency to remove steady state error at that particular frequency. The PR response is better than that of the PI controlled system. The transfer-function of a PR controller takes the form of

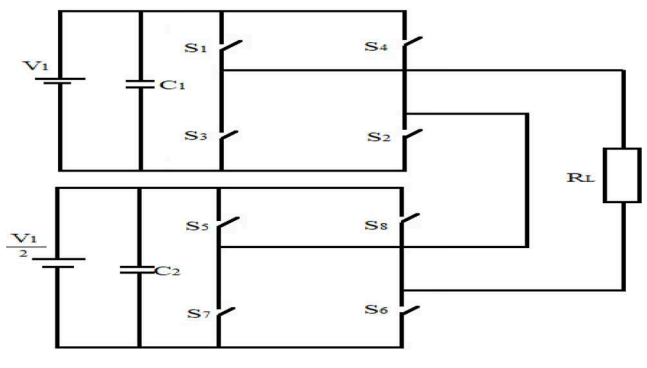

FIGURE 4 | Circuit diagram of 7-level inverter.

SYSTEM DESCRIPTION

The fly back SMPS consists of a diode bridge rectifier with a capacitor filter, high frequency switching device, a fly back transformer followed by the output rectifier and filter. In **Figure 1**, proposed closed loop MLIBSMPS system is shown where a multilevel inverter is introduced between the rectifier and the fly back converter. The fly back converter is also cascaded to reduce the current ripple at both the input as well as output side. At the output side a cascade filter is introduced which reduces the output current ripple. The fly back SMPS is operated in both voltage control mode (outer loop) as well as current control mode (inner loop). In **Figure 1**, PI controllers are used for both Voltage control mode as well as current control mode. In **Figure 2**, PI controllers are replaced with PR controllers and the output voltage, current, and power is measured. Here, the dynamic performance of the both the controllers is compared. In both modes, the output voltage is evaluated with reference yield voltage to provide the error signal. The obtained current signal is again related with reference current to get PWM signal for fly back converter. This error signal is coursed by the PI as well as PR to sustain the output voltage constant and diminish the steady state errors. The main ease of these two control modes are simple design, easy control and good voltage regulation.

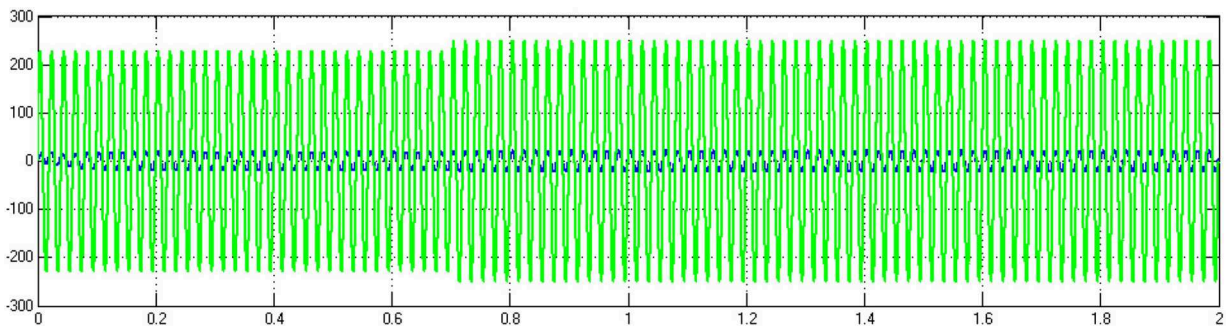

FIGURE 5 | Input voltage of MLIBSMPS.

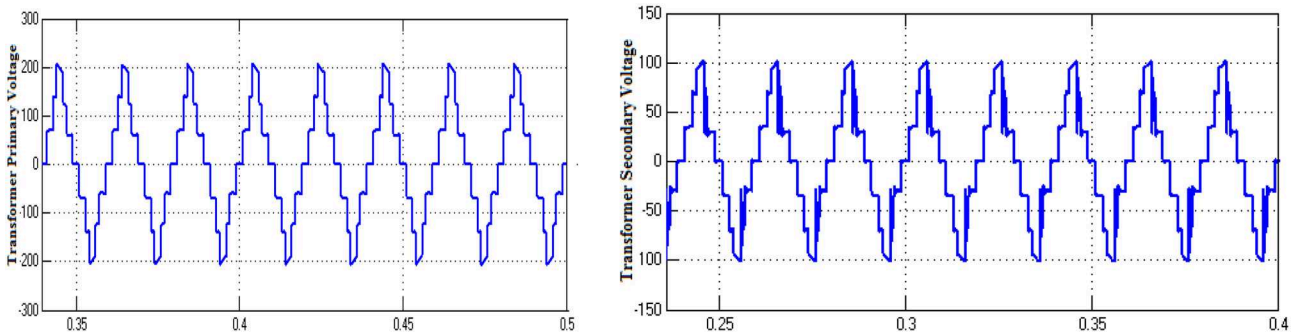

FIGURE 6 | Transformer primary and secondary voltage of MLIBSMPS with PIC.

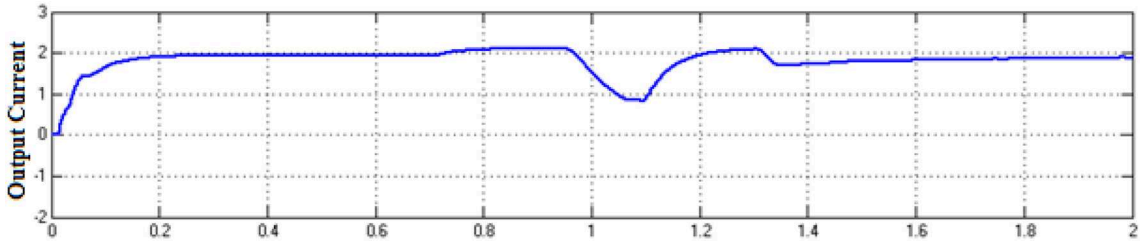

FIGURE 7 | Output voltage of MLIBSMPS with PIC.

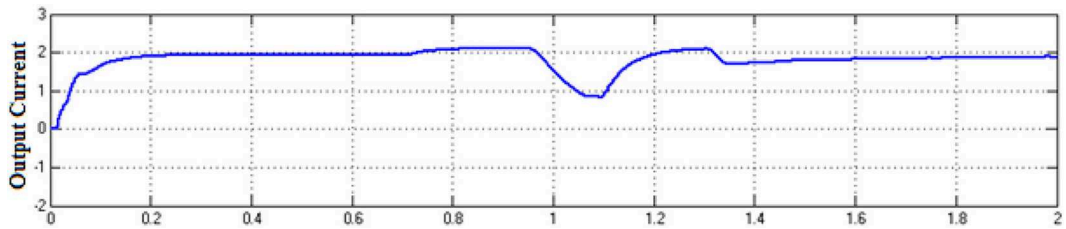

FIGURE 8 | Output current of MLIBSMPS with PIC.

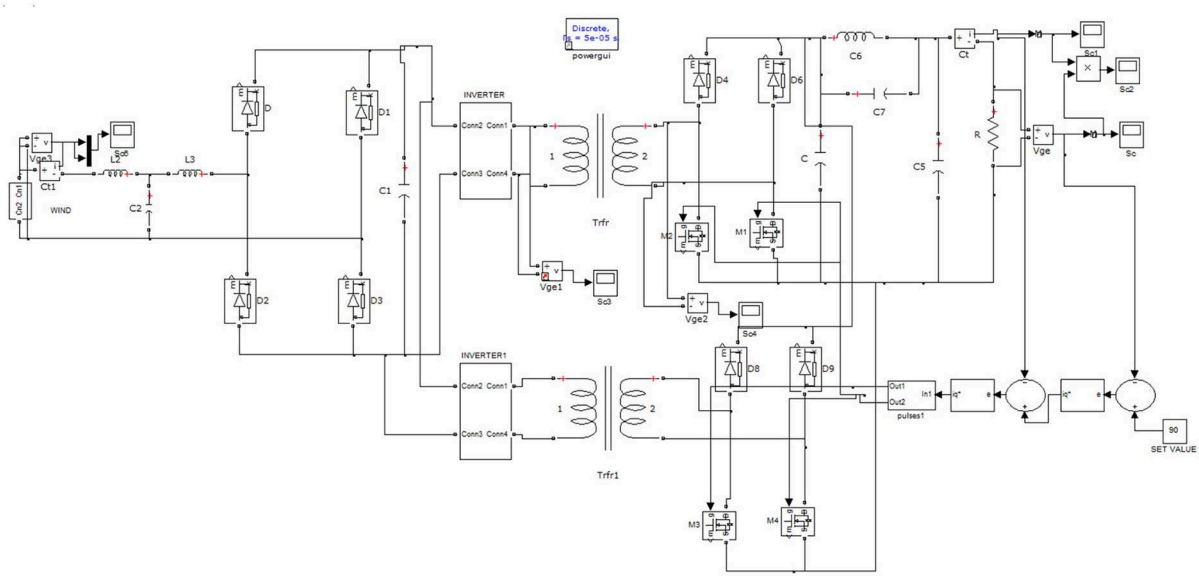

FIGURE 9 | Simulation diagram of MLIBSMPS with PR controller in two loop mode.

SIMULATION RESULTS

The results of MLIBSMPS with PI and PR controller in closed loop configurations are discussed simultaneously with the simulation diagram and along with their results.

MLIBSMPS With PI Controller in Closed Loop Configuration

The simulation diagram of MLIBSMPS circuit with PI Controller (PIC) in two loop mode is shown in **Figure 3** and the circuit diagram of 7-level inverter is given in **Figure 4**. A sine wave input of 250 V is given to the two loop PI controller and a disturbance is created at 0.7 s at the input side which is shown in **Figure 5**. The voltage across rectifier is obtained as 210 V. Transformer primary and secondary voltage of MLIBSMPS are obtained as 200 and 100 V, respectively, in **Figure 6**. Voltage across R-load with two loop PIC is shown as 90 V in **Figure 7**. It is observed that the output voltage reaches its peak at 1.30 s and settles at 1.38 s. Current through R-load with two loop PIC is shown 1.9 A in **Figure 8**. It is observed that the output current reaches its peak at 1.29 s and settles at 1.39 s.

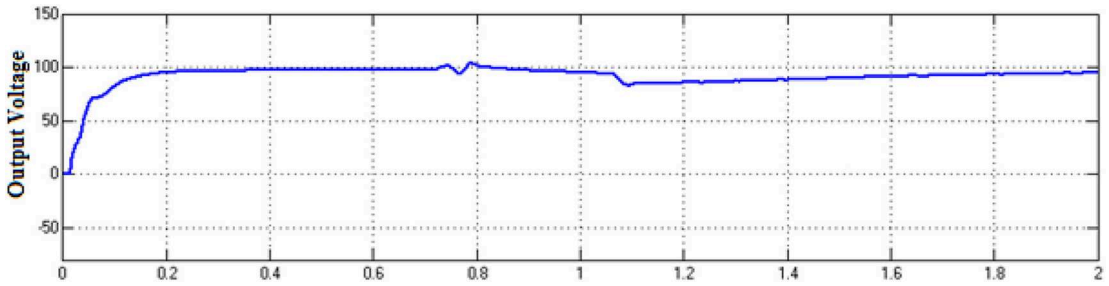

FIGURE 10 | Output voltage of MLIBSMPS with PRC.

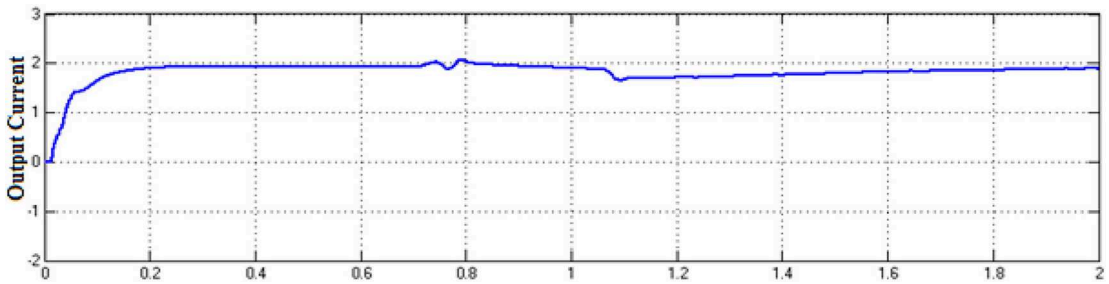

FIGURE 11 | Output current of MLIBSMPS with PRC.

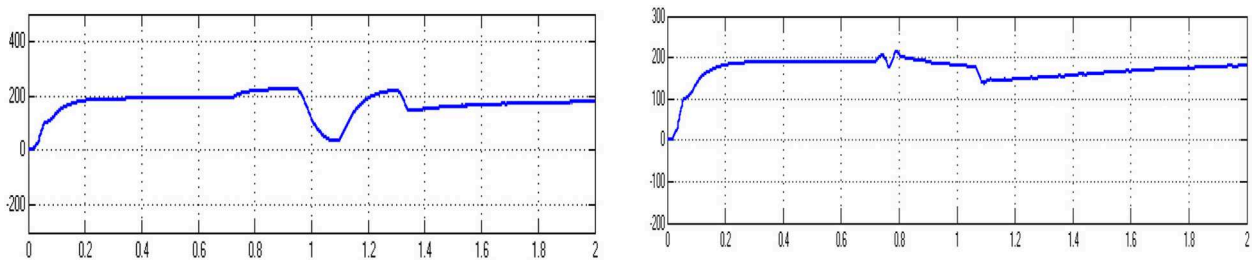

FIGURE 12 | Output power of MLIBSMPS with PIC and Output power of MLIBSMPS with PRC.

TABLE 1 | Summary of time domain parameters (Voltage) with PIC and PRC.

Controller	T_r (s)	T_p (s)	T_s (s)	E_{ss} (V)
PI-PI	0.76	1.30	1.38	1.3
PR-PR	0.74	0.84	1.14	0.8

TABLE 2 | Summary of time domain parameters (Current) with PIC and PRC.

Controller	T_r (s)	T_p (s)	T_s (s)	E_{ss} (V)
PI-PI	0.77	1.29	1.39	0.7
PR-PR	0.75	0.82	1.13	0.4

TABLE 3 | PI and PR controller parameters.

Controller	Kp	Ki	Kr
PIC	0.18	0.9	–
PRC	0.3	–	0.9

MLIBSMPS With PR Controller in Closed Loop Configuration

The simulation diagram of MLIBSMPS circuit with PR Controller (PRC) in two loop mode is given in **Figure 9**. A sine wave input of 250 V is given to the two loop PR controller and a disturbance is created at 0.7 s at the input side. The voltage across rectifier is obtained as 210 V. Transformer primary and secondary voltage of MLIBSMPS are obtained as 200 and 100 V, respectively, which are similar to the one shown in **Figure 6**. Voltage across R-load with two loop PRC is shown as 90 V in **Figure 10**. It is observed that the output voltage reaches its peak at 0.84 s and settles at 1.14 s. Current through R-load with two loop PRC is shown 1.9 A in **Figure 11**. It is observed that the output current reaches its peak at 0.82 s and settles at 1.13 s. The output power with two loop PIC and PRC is shown in **Figure 12** and its value is 200 W.

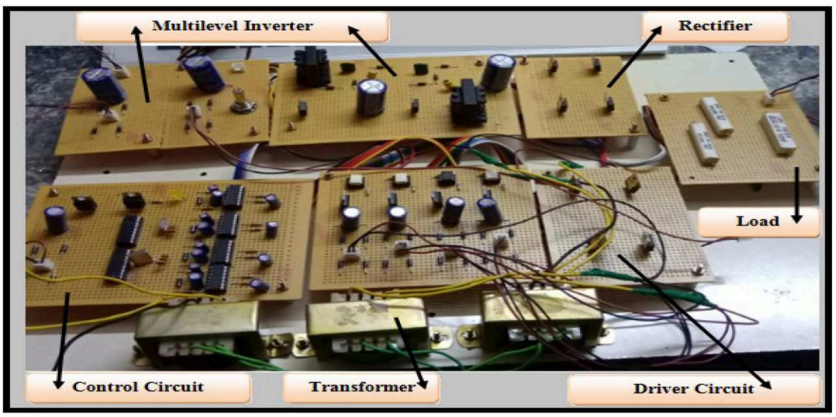

FIGURE 13 | Hardware structure of CFSMPS.

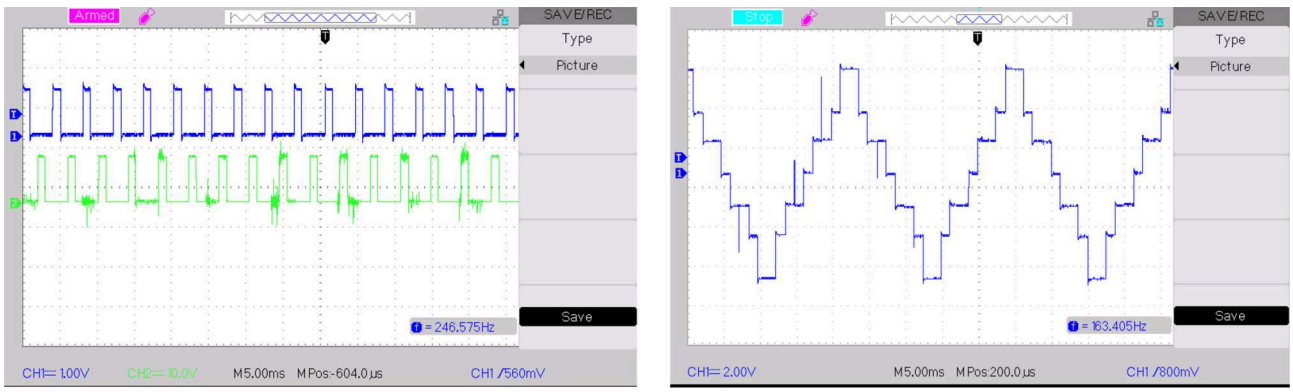

FIGURE 14 | Switching pulses for M1 and M2 of CFSMPS and Output voltage of 7 level inverter.

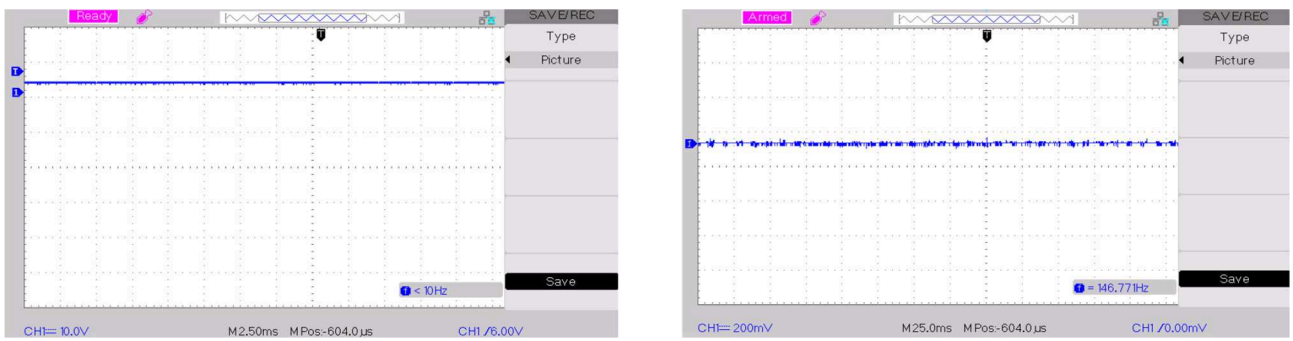

FIGURE 15 | Output voltage and Output current of CFSMPS.

The evaluation of time domain parameters (Voltage) with PI and PR controller is given in **Table 1**. It is observed that with PR controller, there is a reduction of rise-time from 0.76 to 0.74 s, the peak time from 1.30 to 0.84 s, the settling-time from 1.38 to 1.14 s and the steady state error from 1.3 to 0.8 V.

The evaluation of time domain parameters (Current) with PI and PR controller is given in **Table 1**. It is observed that with PR controller, there is a reduction of rise- time from 0.77 to 0.75 s, the peak time from 1.29 to 0.82 s, the settling-time from 1.39 to 1.13 s and the steady state error from 0.7 to 0.4 V.

It is observed from **Tables 1, 2** that the obtained time domain parameter values in PR controllers are reduced when compared to PI Controllers. Hence, it is proved that the dynamic response of the system is improved in PR Controllers than

TABLE 4 | List of components used for hardware of CFSMPS.

Name	Rating
C	1000E-03, 4.70E-05, 2.20E-03, 3.30E-11
Diode	1000 V, 3 A
L	10 uH
MOSFET (IR840)	600 V, 8 A
R	1 K, 100 K, 22 K
Regulator	7812, 7805
IC	IR2110
P.I.C controller	P.I.C16F84A

TABLE 5 | Simulation and hardware values of CFSMPS.

S. no	Simulation	Hardware
Vin	230 V	230 V
Vo	90 V	86 V
fs	1 KHz	1 KHz
Po	160 W	152 W

PI Controllers. The parameter used for PI and PR controllers is shown in **Table 3**. These values are used in the simulation of PIC and PRC.

EXPERIMENTAL RESULTS

To demonstrate the practical possibility of the proposed converter, hardware of Cascaded Flyback SMPS (CFSMPS) is fabricated and tested in the laboratory. The hardware of CFSMPS has rectifier, transformer, flyback converter, and control circuit modules. Hardware snapshot is given in **Figure 13**. The input voltage is given to the Cascaded Flyback SMPS. The Switching pulses for M1 and M2 of fly back converter and the output voltage of 7- level inverter are illustrated in **Figure 14**. Output voltage and current are shown in **Figure 15**. List of components used are given in **Table 4**. The magnitudes of input as well as output are in accordance with the expected results. It is interesting to note that the input current ripple is very low due to cascading techniques. Comparison of Simulation and hardware values of CFSMPS are given in **Table 5**.

CONCLUSION

Simulation studies were done for Proportional Integral (PI) and Proportional Resonant (PR) controlled closed loop MLIBSMPS. These studies were done using the Simulink-based models. By using controllers, good voltage regulation can be achieved hence efficiency can also be improved. The outcomes signify that the Proportional resonant (PR) controlled closed loop MLIBSMPS gave an improved response as evaluated to the PI controlled closed loop MLIBSMPS. The advantages of the proposed system are very fast settling time and low steady state error. The improvement in dynamic response is because of the use of PR controller. The hardware results match with simulation results. The contribution of the present work is to use MLI for SMPS and PRC to regulate load voltage.

DATA AVAILABILITY STATEMENT

All datasets generated for this study are included in the article/supplementary material.

AUTHOR CONTRIBUTIONS

All authors listed have made a substantial, direct and intellectual contribution to the work, and approved it for publication.

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frontiers in Energy Research

ORIGINAL RESEARCH
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Analysis of Switching Sequence Operation for Reduced Switch Multilevel Inverter With Various Pulse Width Modulation Methods

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Pulse width modulation (PWM) methods are used to control the switching sequence operations of conventional multilevel inverters (MLIs) and reduced switch multilevel inverters (RSMLIs). Many researchers proposed various RSMLIs with their switching sequence operation and PWM control techniques. However, the switching operations of RSMLIs are not similar to conventional MLIs, which are a major problem of switch control. Logical equations are proposed for the operation of RSMLIs with the multi-carrier PWM methods like alternative phase opposition disposition (APOD), phase opposition disposition (POD), and phase disposition (PD). To operate the individual switch in symmetrical and asymmetrical RSMLI, logical operators are used to produce required pulse sequence from the sequence of PWM method and their analysis is not present in previous works. The proposed methodology can be applied to PV systems for efficient operation. The proposed methodology and binary representation of PWM method are analyzed on various RSMLIs for seven-level output voltage to operate each individual switch. Control of individual switching sequence and the operation of RSMLIs are simulated using MATLAB/Simulink. THD comparison is presented for RSMLI, DCL MLI, and SCSD MLI with various PWM methods.

Keywords: pulse width modulation, multilevel inverter, reduced switch multilevel inverter, switching sequence, logic gates, total harmonic distortion

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INTRODUCTION

Reducing the switch count for the design of multilevel inverters (MLIs) has an area of research in MLIs and focused to the study on reduced switch multilevel inverters (RSMLIs) (Vemuganti et al., 2018). Single DC voltage source is used to neutral point clamped MLI, active neutral point clamped MLI, flying capacitor MLI, and modular cascaded MLI. Multiple DC voltage sources are used for cascaded H bridge MLI, diode clamped MLI, and hybrid MLIs. Based on the multiple DC sources voltage ratio, MLIs are classified as symmetrical and asymmetrical (Ali and Kannan, 2015; Prabaharan and Palanisamy, 2017). RSMLIs are also designed by symmetric and asymmetric voltage sources with and without H bridge circuits. Mode of operation for RSMLI is the complex task and is presented as switching sequence table (Kumar and Kumar, 2019a). RSMLIs are proposed to achieve cost minimization, optimal voltage stress, reduced power losses, switching frequency operations, and less harmonic distortions. Operation of these conventional MLIs is performed with the support of gating signals (pulses) to the power switches of the respective inverter design (Chen et al., 2019).

Various modulation methods are used to operate the switches of symmetrical and asymmetrical RSMLIs. Among these, sinusoidal pulse width modulation (PWM), space vector PWM methods, and selective harmonic elimination PWM are most suitable to achieve good efficiency, less switching losses, and less harmonic distortion values (Sudhakar Babu et al., 2015; Kumar and Kumar, 2018). Generation of gating signals is achieved by various pulse modulation techniques with fundamental switching frequency and high switching frequency. There are one or two gating signals per cycle for the switching operation with low switching frequency (50–100 Hz), whereas high switching frequency (2–20 kHz) has multiple gating signals per cycle (Dong et al., 2016; Orfi Yegane and Sarvi, 2018). Multiple high switching frequency is suitable for the operation of RSMLIs with SPWM technique; this will result in the multi-carrier SPWM technique. With respect to the parameter variation of modulation signal, unipolar PWM, level-shifted PWM, and phase-shifted PWM schemes are implemented in the SPWM technique. Similarly, alternative phase opposition disposition (APOD), phase opposition disposition (POD), and phase disposition (PD) are presented with the parameter variation of carrier signal (Carrara et al., 1992; Holtz, 1992; Colak et al., 2011; Vemuganti et al., 2018).

Sequences of switching operation of various RSMLIs are presented in many research works with one of the modulation methods. However, obtaining the required pulse sequence for individual switch in RSMLI is a critical part of the presented works. Obtained pulse sequence from the traditional modulation method is not exactly matching with the required pulse sequence of RSMLI switching operation. Analyzing the proper logical operator for the generation of required pulse sequence is the complex task for the RSMLI operation. Using the logical operations, the working module of various RSMLIs are not properly explained by the researchers in their research works (Krishna and Vadhera, 2013; Umashankar et al., 2013; Gnana Prakash et al., 2014; Uthirasamy et al., 2015). By observing the limitations of the abovementioned works, in this article, the authors proposed the switching operation of RSMLI with the required generation of pulse sequence with unique methodology. In addition, detailed analysis and comparative analysis are also presented to show the superiority of the proposed technique. For better understanding pulse sequence generated by the proposed methodology, other PWM techniques are presented in tabular form.

Wide research studies on various renewable energy sources like photovoltaic and wind energy generation system are presented with various improved parameters. Power electronic converters are used for the integration of various renewable energy sources called hybrid structures. Control aspects of the various power converters are performed to obtain the required system parameters like improved efficiency for PV system and demand side with economical conditions (Dorahaki, 2015; Narendiran and Sahoo, 2017; Dorahaki et al., 2019). Efficiency and economical conditions motivate the authors to propose the control of reduced switch count MLI with simulation analysis. Various controlled methodologies are used for the control of RSMLIs, which are complex. A simple methodology is proposed in the present work with basic logic operators for the pulse sequence operation. A comparative study of various reduced switch count MLIs is presented with switch count (S), diodes (D), capacitors (C), output voltage level, PWM techniques, and methodology applied for the switching operation and is given in **Table 1**.

The organization of the article is as follows: Various RSMLIs of seven-level output voltage is presented in section Reduced Switch Multilevel Inverter (Seven Level). Selection of multi-carriers and various carrier based modulation techniques are given in section Carrier-Based Modulation Technique. Implementation of proposed methodology is discussed in section Implementation of Proposed Methodology. THD values with respect to various modulation index values and results of RSMLIs are presented in section Results and THD Comparison. The proposed methodology for the switching sequence operation of RSMLIs concludes in the final section.

REDUCED SWITCH MULTILEVEL INVERTER (SEVEN LEVEL)

Multistep output voltage of the traditional inverter is obtained with the proper arrangement of power semiconductor switches. Power semiconductor switches in the design of the traditional MLIs are directly operated and controlled with the pulse sequence obtained from multi-carrier PWM methods. These MLIs do not require any intermediate circuit to convert the obtained sequence of pulse to the required pulse sequence. In traditional MLIs, usage of power semiconductor switches, number of DC sources, and linear and non-linear elements are given in **Table 2** (Kumar and Kumar, 2019a,b), where L is the level of MLI. Because of the greater number of electrical and electronic components, various parameters like power losses, total harmonic distortion (THD), efficiency, etc., are affecting the traditional MLI designs. To overcome these drawbacks from traditional MLIs, RSMLIs are introduced by many researchers. For the proposed analysis work on PWM, some of the recent RSMLIs are considered from the research work and compared with the performance parameters of the different systems. Intermediate switching circuitry is required for the operation of considered RSMLIs.

Umashankar et al. (2013) proposed a seven-level symmetric RSMLI design with five controllable semiconductor switches and 4 DC voltage sources (V_{DC}). This RSMLI is presented without H bridge and analyzed for the less THD values with resistive load. Chitra and Himavathi (2015) considered the proposed symmetric RSMLI by Umashankar et al. (2013) for the application of induction motor drive. Structure of the seven-level symmetric RSMLI is shown in **Figure 1A** and the switching sequence for the operation is given in **Table A1**.

Uthirasamy et al. (2015) proposed a DC link Cascaded (DCLMLI) seven-level asymmetric RSMLI with H bridge design. Eight controllable switches and 2 DC voltage sources (V_{DC1}, V_{DC2}) are used for the structure of the proposed module. THD result analysis with application to uninterrupted power supply system is done in their research work. Structure of asymmetric

TABLE 1 | Comparison of various reduced switch MLIs.

References	Output voltage level	Voltage sources	Number of switches/capacitors			PWM technique	Methodology
			S	D	C		
Chen et al. (2019)	5	1	6	2	2	Unipolar (PD)	K-Map
Viswanath et al. (2019)	7	3	7	3	0	–	Fuzzy logic
Prabaharan and Palanisamy (2016)	9	4	12	0	0	Unipolar (APOD, POD, PD)	Logic gates
Uthirasamy et al. (2015)	7	2	8	0	0	Bipolar (APOD)	Logic gates
Chitra and Himavathi (2015)	7	4	5	0	0	Bipolar (APOD, POD, PD)	Logic gates
Gautam et al. (2015)	9	2	7	4	2	Bipolar (POD)	Logic gates
Nagarajan and Saravanan (2014)	9	4	11	0	0	Unipolar (APOD, POD, IPD, PD)	–
Umashankar et al. (2013)	7	4	5	0	0	Bipolar (APOD, POD, PD)	Logic gates

TABLE 2 | Required number of components for traditional MLIs.

Type of MLI	No. of DC sources	No. of switches	No. of capacitors for DC- bus	Clamping capacitors	Clamping diodes
Diode clamped	1	2 × (L-1)	L-1	–	(L-1) × (L-2)
Flying capacitor	1	2 × (L-1)	L-1	(L-1) × ((L-2)/2)	–
Cascaded H-bridge	(L-1)/2	4 × ((L-1)/2)	–	–	–

RSMLI and the switching sequence are shown in **Figure 1B** and **Table A2**.

Viswanath et al. (2019) proposed a symmetric cascaded switched diode (SCSD) seven-level RSMLI with H bridge design. Seven controllable and three uncontrolled switches with three DC voltage sources (V_{DC}) are used for the design of proposed module. Combination of DC voltage source, controllable switch, and uncontrolled switch gives an elementary unit for the operation of the proposed RSMLI. Structural design and switching sequence table are shown in **Figure 1C** and **Table A3**. Switching sequence control of the proposed RSMLI is done with a fuzzy controller. THD analysis is presented in the results discussion for various levels.

In these proposed symmetric and asymmetric RSMLI, logical operators are used for individual switch for operating the switch with required switching sequence. Proper pulse conversion analysis is not presented based on carrier modulation techniques in their proposed research. Proper modulation techniques with analysis of logical operators are proposed in the present work.

CARRIER-BASED MODULATION TECHNIQUE

Various modulation techniques are reviewed for RSMLIs and conclusions with "per-carrier cycle" carrier-based PWM method (Hamman and van der Merwe, 1988; Carrara et al., 1992). Implementation of the carrier-based PWM technique exists in two methods. The direct digital technique has a pre-calculated inverter state, time length of each carrier, and modulation cycle employing space vector theory (Hava et al., 1999; Gopalakrishnan and Narayanan, 2014). The indirect technique works with carrier triangle intersection technique. Reference modulation wave with a low frequency is compared with high-frequency triangular carrier wave and the intersection results in the pulse switching sequence (Dong et al., 2016; Kumar and Kumar, 2018).

In the operation of MLIs, carrier triangular intersection technique is easy to implement with modulation wave comparison strategy. Bipolar sinusoidal wave, unipolar sinusoidal wave, and saw tooth wave are preferable for the modulation wave (Vemuganti et al., 2018). Single triangular carrier wave is suitable for two-level and three-level traditional MLIs. In case of five levels and more than five levels, multi-carrier triangular waves are used for the generation of levels (McGrath and Holmes, 2002). For the analysis of switching sequence in the considered RSMLIs, bipolar sinusoidal (SPWM) wave and unipolar sinusoidal (USPWM) is used as modulation signal. Based on position of multi-carrier waves, phase shift (PS) and level shift (LS) PWM techniques are proposed. Multi-carrier technique is used with three disposition carrier wave implemented as follows (Nagarajan and Saravanan, 2014; Prasad et al., 2017; Chen et al., 2019).

Alternative Phase Opposition Disposition

The arrangement of all triangular carrier waves alternatively in opposition with displacement of 180° to phase is called alternative phase opposition disposition (APOD). All carrier waves are compared with the low-frequency modulation bipolar sinusoidal wave or unipolar sinusoidal wave with preferred amplitude and frequency measured based on the level of MLI. Representation of APOD PWM technique is presented in **Figures B1**, **B2**.

Phase Opposition Disposition

Selection of all in-phase carrier waves considered for above zero reference value and all in-phase carrier waves but opposite with displacement of 180° to below zero reference value is called phase opposition disposition (POD). Only bipolar sinusoidal

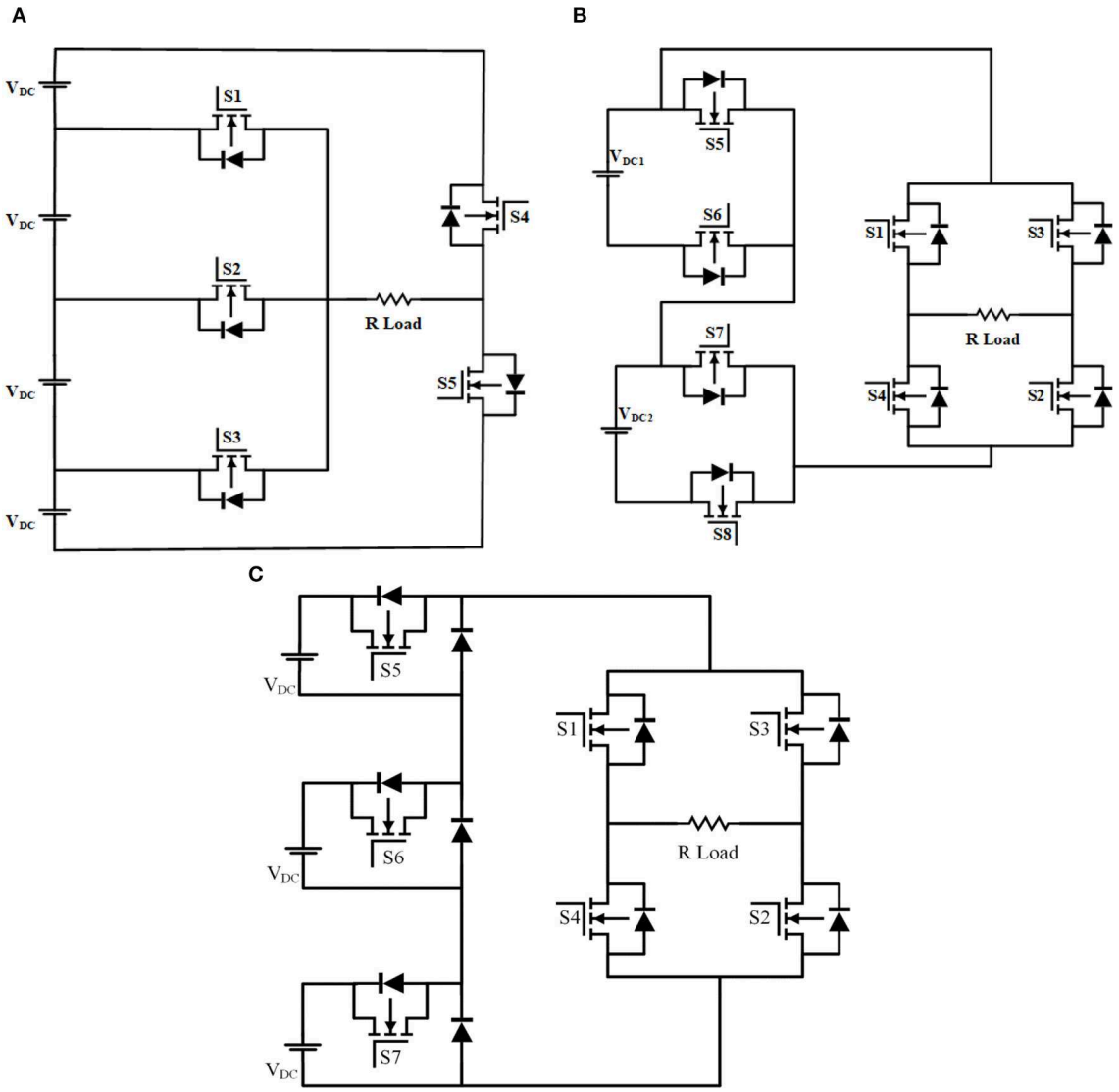

FIGURE 1 | Various seven-level MLIs. **(A)** Reduced switch MLI. **(B)** DC link MLI. **(C)** SCSD MLI.

modulation wave is possible in the POD PWM technique. The USPWM method is not possible for the POD PWM technique due to no below zero reference value in unipolar modulation wave. Representation of POD PWM technique is presented in **Figure B3**.

Phase Disposition

All the triangular carrier waves on above and below zero reference value are in-phase. This modulation technique is called phase disposition (PD). Bipolar and unipolar sinusoidal modulation wave is suitable for the operation of PD PWM technique. **Figures B4**, **B5** show representation of PD PWM technique.

Selection of number of multi-carrier waves for the operation of RSMLI in intersection technique is proposed with proper methodology and shown in **Figure 2**. Selection of number of carrier signals (C), amplitude of each carrier wave, amplitude of modulation wave (A_m) are to be defined based on the level of output voltage. With the proper analysis of the proposed algorithm, generation of gating signals are obtained with the comparison of amplitudes of modulation wave and carrier wave given in Equations (1) and (2).

$$\text{Amplitude of modulation wave, } |A_m| = \sum_{i=1}^{n-1} |C_i| \quad (1)$$

$$|A_m| \geq |C_i| \Rightarrow \begin{Bmatrix} P_1 \text{ to } P_{\frac{(n-1)}{2}}, & \text{If i} = 1 \text{ to} \frac{(n-1)}{2} \\ N_1 \text{ to } N_{\frac{(n-1)}{2}}, & \text{If i} = \frac{(n-1)}{2} + 1 \text{ to } (n-1) \end{Bmatrix} \quad (2)$$

In most of the bipolar PWM methods, $n-1$ carrier signals are used for the "n" level output voltage of RSMLI. $(n-1)/2$

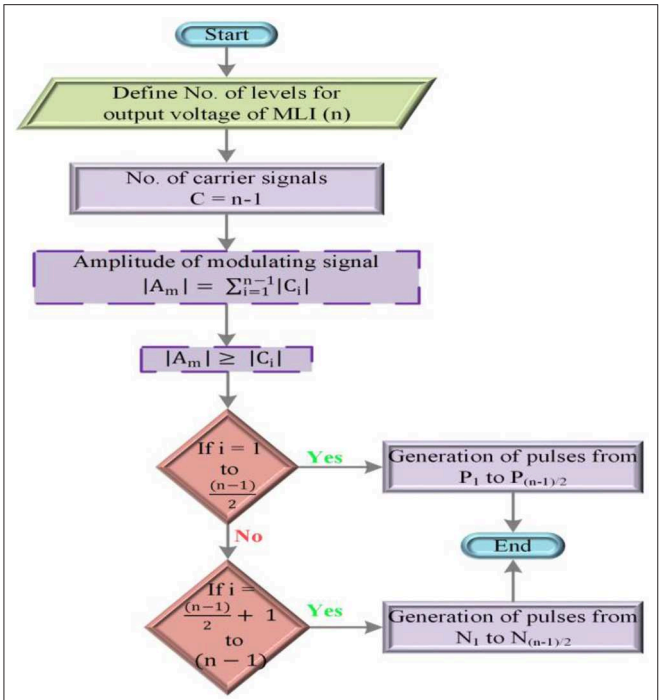

FIGURE 2 | Flowchart for calculation of number of carrier waves and generation of pulses.

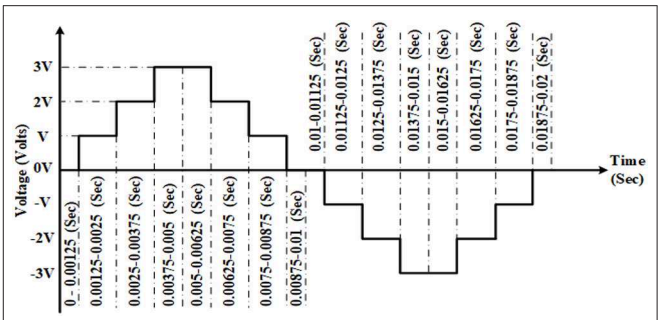

FIGURE 3 | Time distribution of one cycle for seven-level MLI.

carrier waves are used for the unipolar PWM methods (Huang et al., 2018). The switching sequence operation of seven-level symmetric RSMLI and asymmetric DCL MLI is performed by bipolar multi-carrier PWM method. SCSD MLI switching sequence operation is done with the unipolar multi-carrier PWM method. Calculation for number of divisions per cycle and time interval of each division is given in Equations (5) and (6). For seven-level output voltage of MLI, total time of one cycle is to be distributed for one cycle as shown in **Figure 3**.

$$\text{Frequency of the proposed system } (f_m) = 50\text{Hz} \quad (3)$$

$$\text{Total time period of one cycle } (t) = 1/f_m = 0.02\text{s} \quad (4)$$

$$\text{Number of divisions/cycle } (D_t) = (n^*2) + 2 \quad (5)$$

$$\text{Time interval of each } D_t(t_d) = [(n^*2) + 2]/t \quad (6)$$

To present the clear analysis of switching sequence operation for individual MLI, a binary representation switching sequence is presented in this research work. Binary representation of bipolar SPWM and unipolar SPWM methods is shown in **Tables B1**, **B2**.

IMPLEMENTATION OF PROPOSED METHODOLOGY

Switching sequences of individual switch in various RSMLI with the binary representation sequence of PWM method are compared to generate the required pulse sequence. Representation of switching sequence is in the form of "0's" and "1's", and it is easy to analyze the logical equations for the intermediate circuit. If a generated pulse sequence exactly matches any of the individual switching sequence of RSMLI, then the matched sequence is directly used for the operation of proper switch. If pulse sequence does not match any switching sequence, then an intermediate circuit is to be designed with the use of logic gates. Depending on the "ON" and "OFF" condition of a switch in one cycle, the use of logic gates is decided. If a switch is ON and OFF for more times per cycle, then a greater number of logic gates are used for the intermediate circuit. With the observation of irregular ON and OFF condition of a switch, some logical equations are analyzed and presented for individual switch, which do not have direct control from generated pulse sequence of the PWM method. A Karnaugh map is used for the analysis of logical equations (Vemuganti et al., 2018; Chen et al., 2019) for individual switch for five-level RSMLI. Application of K map is complex for the system with more than four variables. For seven-level RSMLI, a minimum of six pulse sequence variables are available.

To compare the sequence of each switch, the generated pulse sequence unique algorithm is proposed in this research work. All the considered RSMLI are of seven levels; six pulse sequences are obtained from the comparison and intersection methods of PWM. Initially, pulse sequences are defined in the comparison operation of the proposed methodology. Pulse sequences obtained from the carrier waves in PWM methods that are above the zero reference wave are considered as binary sequence of positive half cycle. Representation of the positive half cycle pulse sequence variables are P_1, P_2, and P_3. Pulse sequences from carrier waves that are below the zero reference wave are considered as negative half cycle binary sequence. N_1, N_2, and N_3 are the negative half cycle pulse sequence variables. Each switch sequence is divided into two halves, positive half switch sequence (S_P) and the negative half switch sequence (S_N). Each switch positive half sequence (S_p) is individually compared with single-variable pulse sequence of positive half pulse sequences (P_1, P_2, and P_3). Evaluating analysis of each variable along with its logical NOT operator variables is clearly presented in the flowchart representation as shown in **Figure 4A**. Similar to comparison of positive half switching sequence and pulse sequence, negative half cycle switching sequence (S_N) is compared individually with the single variable of negative half pulse sequences (N_1, N_2, and N_3) and logical NOT operator variables. Zero reference wave

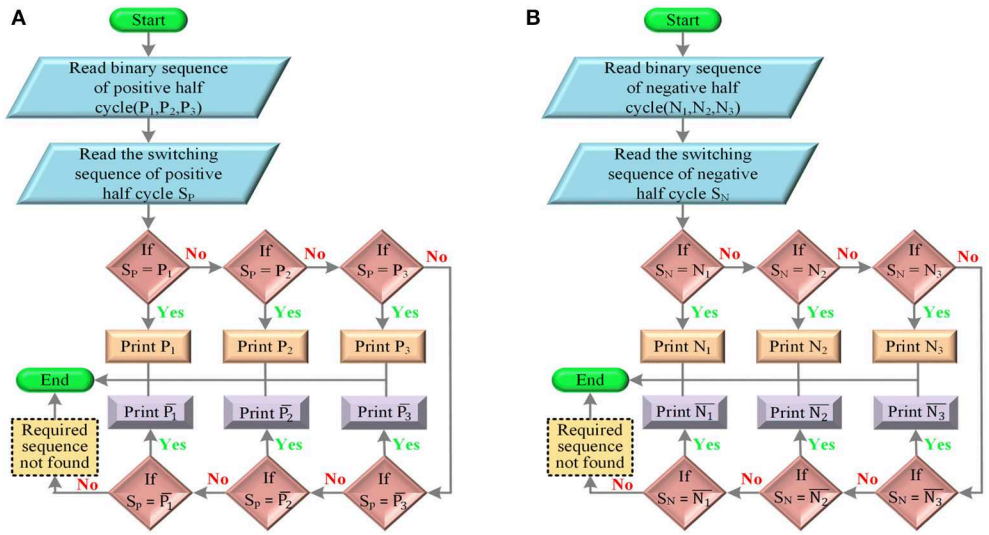

FIGURE 4 | Flowchart for selecting the single-variable pulse sequence. **(A)** Positive switching sequence. **(B)** Negative switching sequence.

variable is represented as PN_0. Flowchart representation of the proposed negative half cycle comparison is shown in **Figure 4B**. If the switching sequence does not match any of individual pulse sequences, then the logical combination of two variables is considered.

In combinational two-pulse sequence variable logical operator comparison of switching sequence, positive half switching sequence and negative half switching sequence are individually performed. Various logical operators like AND (•), OR (+), NOR ($\overline{+}$), NAND ($\overline{\bullet}$), EXOR ($\oplus$), and EXNOR ($\odot$) are used for the comparative analysis of two variables. Selection of required positive half pulse sequence with two variables for the positive switching sequence is shown in **Figure 5A**. Similarly, negative half cycle switching sequence comparison with two pulse variables is shown in **Figure 5B**. From the obtained pulse sequence of positive and negative half pulse variables, the final required switching sequence can be analyzed with the logical operator as shown in **Figure 6**. Resultants of each switch switching sequence ($S_\#$) of various RSMLI are presented as logical expression for the successful operation to generate seven-level output voltage where # is the switch number like S_1, S_2, S_3, etc., in various RSMLIs. Analysis of individual switch in RSMLI, DCL MLI, and SCSD MLI is performed for the logical expression of each switch. Random selections of switching sequence selection operation are presented in tabular analysis.

RESULTS AND THD COMPARISON

The proposed topology is analyzed for three different RSMLIs and the theoretical analysis of switching sequence logical equations is obtained. To verify the proposed theoretical analysis, MATLAB/Simulink is used for simulation process. Simulation parameters of the three MLIs are given in **Table 3**. Analysis of proposed methodology to the application of RSMLI, DCL MLI, and SCSD MLI is explained in the below subsections. THD comparison for the obtained output voltage and output current for resistive load of three MLIs with considered modulation techniques are presented.

To generate the modulation wave by the modulation technique, sinusoidal wave is selected for bipolar modulation technique as shown in **Figures B1**, **B3**, **B4**. Absolute sine wave is selected for unipolar modulation technique as shown in **Figures B2**, **B5** with an amplitude of 3 V and a frequency of 50 Hz. Multi-carrier waves are required for the operation of the multi-carrier PWM method as shown in **Figures B1**–**B5**. Each carrier wave of multi-carrier PWM is generated with a repeating sequence of the simulink library. Time value parameters of the repeating sequence for carrier waves P_1, P_2, P_3, N_1, N_2, and N_3 are given as [0 0.5/18,000 1/18,000], where 18,000 is the selected switching frequency of the proposed methodology. With respect to the time values of carrier waves, the output amplitude values are selected as [0 1 0] for P_1, [2 1 2] for P_2, [2 3 2] for P_3, [0 −1 0] for N_1, [−2 −1 −2] for N_2, and [−2 −3 −2] for N_3 in the modulation technique of APOD bipolar PWM method as shown in **Figure B1**; [0 1 0] for P_1, [1 2 1] for P_2, [2 3 2] for P_3, [0 −1 0] for N_1, [−1 −2 −1] for N_2, and [−2 −3 −2] for N_3 in the modulation technique of bipolar POD PWM modulation as shown in **Figure B3**; [0 1 0] for P_1, [1 2 1] for P_2, [2 3 2] for P_3, [−1 0 −1] for N_1, [−2 −1 −2] for N_2, and [−3 −2 −3] for N_3 in bipolar PD PWM modulation technique as shown in **Figure B4**; [0 1 0] for P_1, [2 1 2] for P_2, and [2 3 2] for P_3 in unipolar APOD PWM modulation as shown in **Figure B2**; [0 1 0] for P_1, [1 2 1] for P_2, and [2 3 2] for P_3 in unipolar PD PWM modulation as shown in **Figure B5**. Greater than relational operator is used in between modulation and carrier wave to obtain required pulse waveforms to switch ON and OFF semiconductor devices in MLIs. Obtained pulse sequences

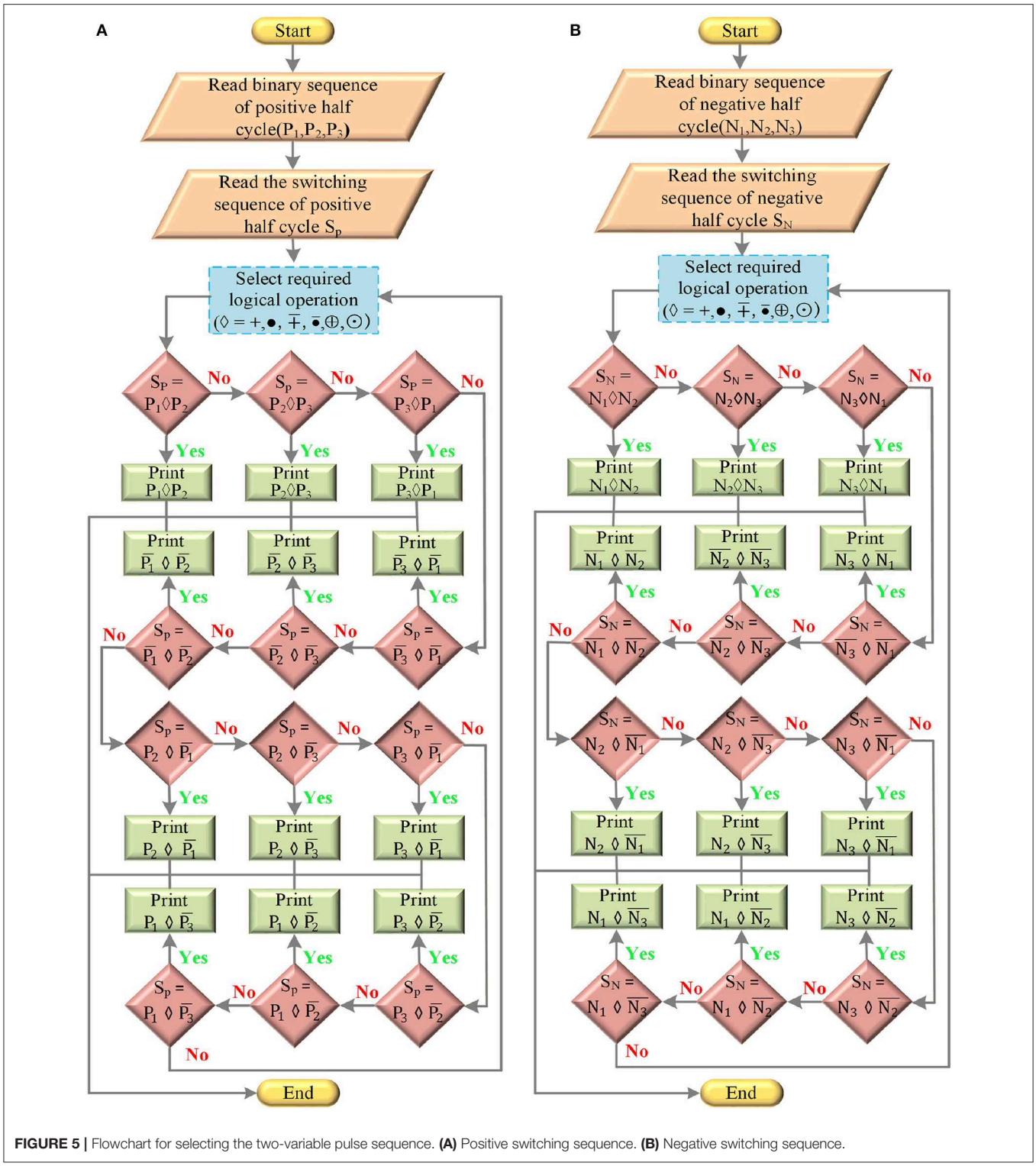

FIGURE 5 | Flowchart for selecting the two-variable pulse sequence. **(A)** Positive switching sequence. **(B)** Negative switching sequence.

are presented as binary representation in **Tables B1**, **B2**. With analysis of proposed methodology between binary representation of pulse sequence and the switching sequence of each switch, the required logical equation for switching sequence is presented in subsections.

Analysis of Proposed Methodology for RSMLI Switching Sequence Logical Equation

An MLI with less number of switches without H bridge is shown in **Figure 1A**. Five MOSFETs are used for the design and

simulation of the RSMLI. Among five switches, three switches are operated for the level generation of output voltage and two are used for the positive half cycle and negative half cycle of output voltage. Four symmetrical voltage sources (V_{DC}) are used for the seven-step MLI output voltage. Each voltage is fixed with a DC voltage of 72 V. Resistive load of 100 Ω is used for the observation of output voltage and current. To operate the switches in the required switching sequence as shown in **Table A1**, the proposed methodology is applied for the generated pulse sequence of PWM techniques. Focusing on the switching sequence of switch S_2, analysis of the proposed methodology is used to obtain logical equation to convert the generated pulse sequence into switching sequence for switch ON and OFF conditions.

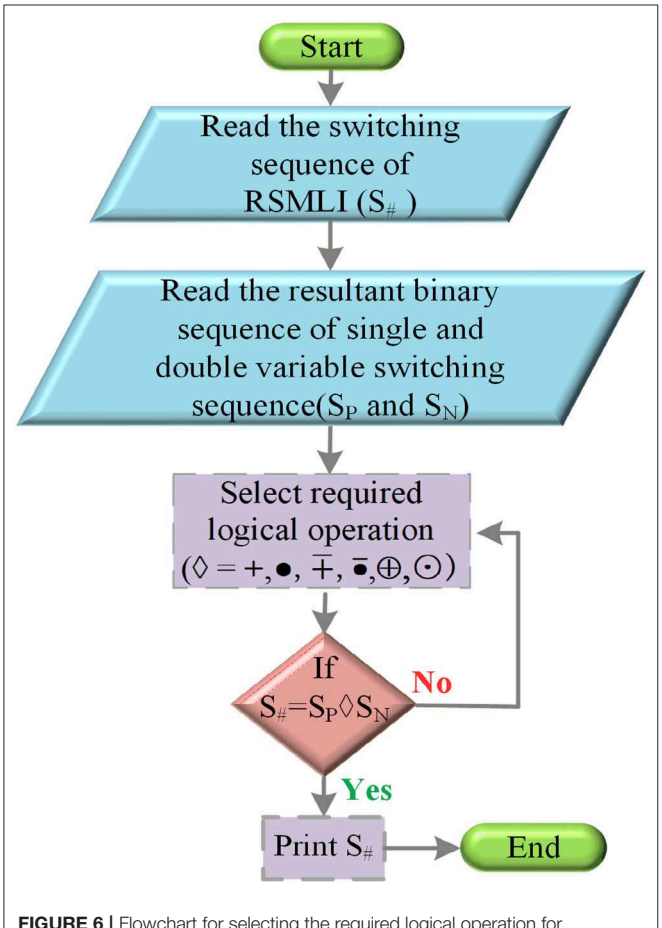

FIGURE 6 | Flowchart for selecting the required logical operation for switching sequence.

The switching sequence of switch S_2 is considered as two parts, one is positive half cycle S_p and the other is negative half cycle S_N. Bipolar PWM technique is used for the operation of switches in RSMLI. Binary representation of bipolar PWM technique shown in **Table B2** is considered for the logical comparative analysis of the proposed methodology. Initially, S_P sequence is compared with each binary representation sequence of P_1, P_2, P_3, $\overline{P_1}$, $\overline{P_2}$, and $\overline{P_3}$ as shown in **Figure 4A**. Similarly, S_N is compared with each binary representation sequence of N_1, N_2, N_3, $\overline{N_1}$, $\overline{N_2}$, and $\overline{N_3}$ as shown in **Figure 4B**. The pulse sequence matches any of the single-carrier wave pulse sequence; next, focus on the two carrier wave pulse sequence with the combination of logical operators. S_P is compared with the combination logical operations of two binary pulse sequence representations as shown in **Figure 5A**. Logical combination of $(\overline{P_1} \cdot P_2)$ matches with S_P. Similarly, S_N is compared with the logical combination of two binary pulse sequence representations as shown in **Figure 5B**. Logical combination of $(\overline{N_2} \cdot N_3)$ matches with S_N. Total switching sequence of switch S_2 is compared with the combination of logical operators of obtained S_P and S_N as shown in **Figure 6**. Total binary representation and logical comparison of each stage of switch S_2 is given in **Table C1**. Final logical equation required for the switch S_2 operation is obtained and given in Equation (7). With the similar application of proposed methodology, required final logical equations for the switch S_1, S_3 are presented in Equation (7). Switching sequence of switches S_4 and S_5 is operated with the pulse sequence of zero reference wave and is given in Equation (7). The resultant pulse sequence of RSMLI obtained with the analysis and the logical equations of each switch is shown in **Figure 7**.

$$\begin{aligned} S_1 &= P_1 + (\overline{N_1} \cdot N_2) \\ S_2 &= (\overline{P_1} \cdot P_2) + (\overline{N_2} \cdot N_3) \\ S_3 &= (\overline{P_2} \cdot P_3) + \overline{N_3} \\ S_4 &= \overline{PN_0} \\ S_5 &= PN_0 \end{aligned} \tag{7}$$

Analysis of Proposed Methodology for DCL MLI Switching Sequence Logical Equation

Asymmetric DC link MLI is simulated with eight MOSFETs as shown in **Figure 1B**. Four switches are used for the level

TABLE 3 | Parameters of various RSMLIs.

Type of inverter	Input and output parameters							
	Input voltage (V)	Modulating frequency (f_m) (Hz)	Carrier frequency (f_c) (Hz)	R Load (Ω)	Output voltage peak (V)	Output RMS voltage (V)	Output RMS current (A)	Output power (W)
Symmetric RSMLI	$V_{DC} = 72$	50	18,000	100	215.8	152.6	2.158	329.3
Asymmetric DCL MLI	$V_1 = 72$ $V_2 = 144$	50	18,000	100	195	137.9	1.95	268.9
SCSD MLI	$V_{DC} = 72$	50	18,000	100	193.2	136.6	1.932	263.9

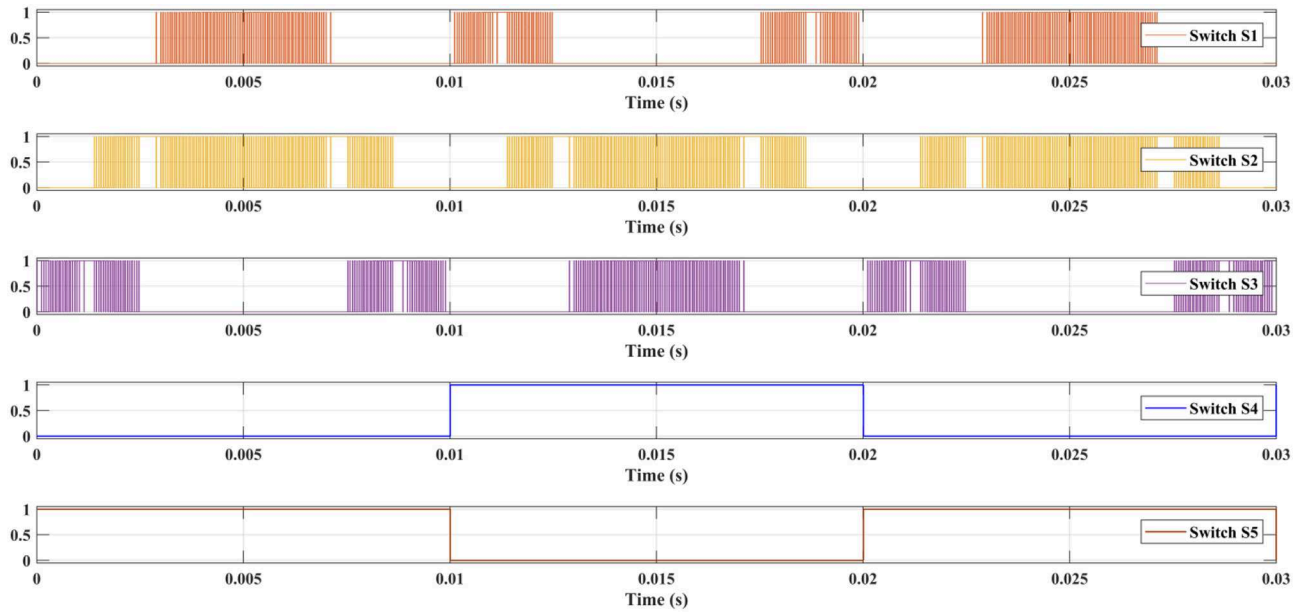

FIGURE 7 | Pulse sequence of RSMLI.

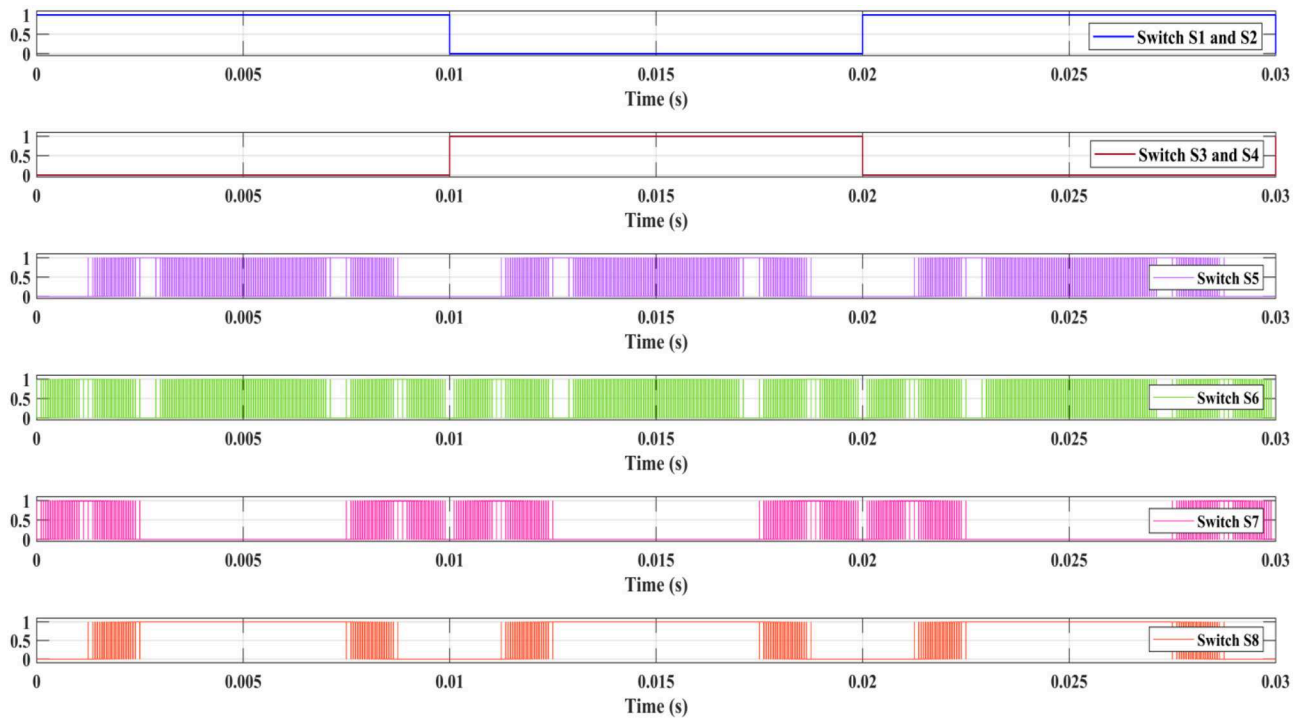

FIGURE 8 | Pulse sequence of DCL MLI.

generation of output voltage and the remaining four switches are used for H bridge to form positive half and negative half cycles. Different voltage sources V_{DC1} with 72 V and V_{DC2} with 144 V are used along with a resistive load of 100 Ω. Proposed methodology is applied for the switching sequence of DCL MLI shown in **Table A2**. Switching sequence operation of switch S_6 is presented with analysis of the proposed methodology.

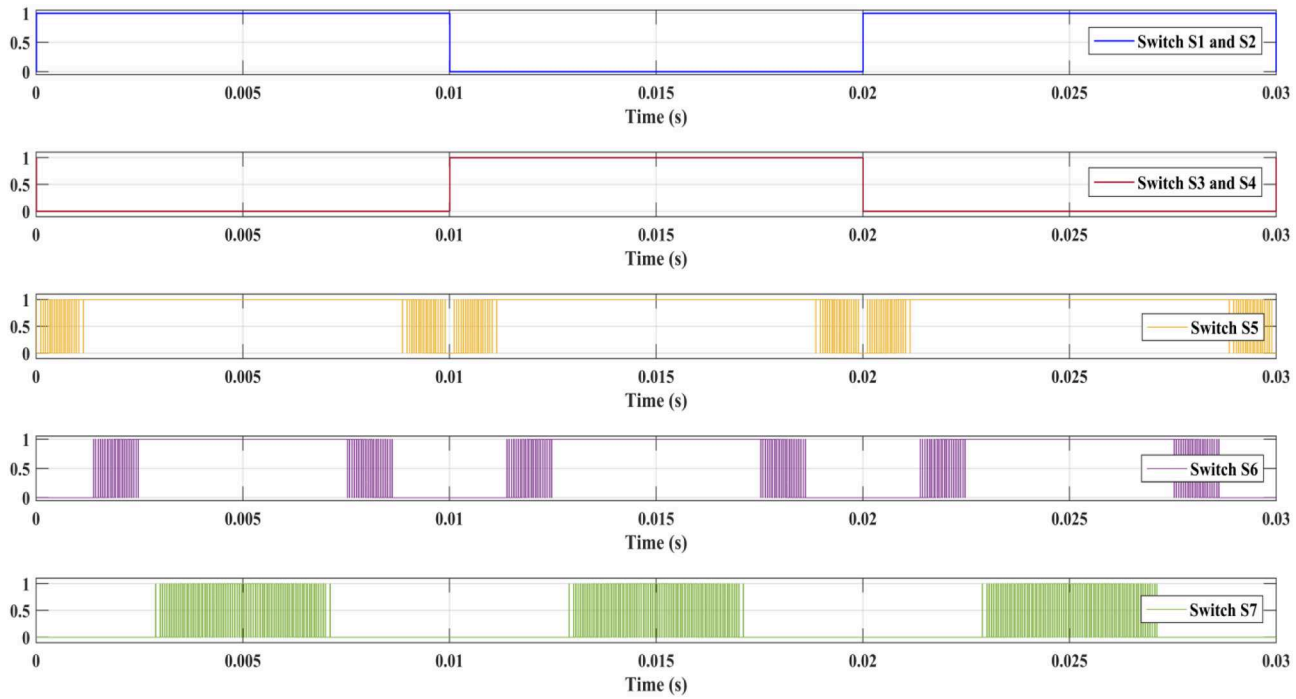

FIGURE 9 | Pulse sequence of DCL MLI.

TABLE 4 | Voltage THD comparison of RSMLIs with PWM techniques.

Modulation index	APOD			POD			PD		
	RSMLI (%)	SCSD MLI (%)	DCL MLI (%)	RSMLI (%)	SCSD MLI (%)	DCL MLI (%)	RSMLI (%)	SCSD MLI (%)	DCL MLI (%)
1.1	3.90	3.73	3.79	3.90	–	3.79	3.92	3.72	3.81
1	1.09	0.94	0.67	1.06	–	0.64	1.15	0.92	0.66
0.9	1.38	1.10	0.88	1.46	–	1.03	1.37	1.37	0.97
0.8	1.71	1.36	0.98	1.63	–	0.94	1.58	1.43	1.09
0.7	1.85	1.41	1.07	1.88	–	1.10	1.94	1.43	1.13

Switching sequences of the switch S_1 and S_2 of H bridge are operated with zero reference wave pulse sequence PN_0. S_3 and S_4 are operated with pulse sequence of $\overline{PN_0}$. Similar to RSMLI, S_P and S_N are considered and compared with the binary sequence representation of bipolar PWM technique. S_P is partially matched with the two pulse sequence logical combination of "$P_1 \oplus P_2$." Obtained partial match of S_P is compared with the single pulse sequence P_3 and finds the match of S_P results to the logical combination of "$(P_1 \oplus P_2) \oplus P_3$." S_N is partially matched with logical combination of two pulse sequences as "$N_1 \oplus N_2$." Obtained partial match of S_N is logically compared with single pulse sequence N_3 and obtained an equivalent as "$(N_1 \oplus N_2) \oplus N_3$." Overall switching sequence of switch S_6 is obtained with the logical combination of the S_P and S_N as shown in Equation (8). Total binary representation and logical comparisons of each stage of switch S_6 are given in **Table C2**. Switching sequence logical equation for switches S_5, S_7, and S_8 are given in Equation (8) with the analysis of the proposed methodology. The resultant pulse sequence of DCL MLI obtained with the analysis and the logical equations of each switch are shown in **Figure 8**.

$$\begin{aligned} S_1 \text{ and } S_2 &= PN_0 \\ S_3 \text{ and } S_4 &= \overline{PN_0} \\ S_5 &= (P_2 \oplus P_3) \oplus (N_2 \oplus N_3) \\ S_6 &= [(P_1 \oplus P_2) \oplus P_3] \odot [(N_1 \oplus N_2) \oplus N_3] \\ S_7 &= (P_1 \oplus P_2) \oplus (N_1 \oplus N_2) \\ S_8 &= P_2 \odot N_2 \end{aligned} \tag{8}$$

Analysis of Proposed Methodology for SCSD MLI Switching Sequence Logical Equation

Symmetric Cascaded Switch Diode MLI is simulated with seven MOSFETs and three diodes. Four MOSFETs are used for the H bridge, and three MOSFETs and three diodes are used for the

level build process of the SCSD MLI as shown in **Figure 1C**. Three symmetric voltage sources (V_{DC}) each of 72 V are used for the generation of seven-level output voltage across a resistive load of 100 Ω. Switching sequence of the SCSD MLI is shown in **Table A3**. Switching sequence of operation of the SCSD MLI is performed with the unipolar PWM technique.

Binary pulse sequence representation of each carrier wave in unipolar PWM technique is presented in **Table B1**. Switching sequence operation of SCSD MLI is simple as compared with DCL MLI and RSMLI. S_1 and S_2 switch sequence are matching with the pulse sequence of P_0. Switches S_3 and S_4 sequences are matching with the zero reference wave pulse representation P_0. Switches S_5, S_6, and S_7 are directly operated with pulse sequences P_1, P_2, and P_3 as shown in Eq. 9. Binary representation of switching sequence operation of switch S_7 is given in **Table C3**. The resultant pulse sequence of SCSD MLI obtained with the analysis and the logical equations of each switch are shown in **Figure 9**.

$$\begin{aligned} S_1 \text{ and } S_2 &= P_0 \\ S_3 \text{ and } S_4 &= \overline{P_0} \\ S_5 &= P_1 \\ S_6 &= P_2 \\ S_7 &= P_3 \end{aligned} \tag{9}$$

THD Comparison of MLIs by Proposed Methodology With APOD, POD, and PD Modulation Techniques

By applying the logical equations to the respective switches of RSMLIs, proper seven-level output voltage can be obtained. Input parameters of considered RSMLIs are given in **Table 3** with resultant output voltage, RMS output voltage, RMS current, and output power. THD analysis of seven-level output voltage of symmetric RSMLI without H bridge, SCSD RSMLI with bridge, and asymmetric DCL MLI is presented. The obtained THD values of RSMLIs are within the standards. Comparative studies of obtained THD values are given for APOD, POD, and PD PWM techniques with respect to various modulation index values. Voltage THD analysis of APOD, POD, and PD PWM techniques is given in **Table 4**.

The obtained seven-level output voltage waveform and the FFT analysis of symmetric RSMLI voltage with various PWM methods are shown in **Figure D1** with a modulation index of 0.9. Similarly, the obtained seven-level output voltage waveform and FFT analysis of asymmetric DCL MLI and SCSD MLI are shown in **Figures D2**, **D3**. Comparative THD analysis is presented for over-modulation index and under-modulation index values in the comparative tables. With the proposed methodology, a lower THD value is obtained with the modulation index value of "1." Among the three MLIs, DCL MLI is performing well with less THD value of 0.67% by APOD PWM, 0.64% by POD PWM, and 0.66% by PD PWM with a modulation index value of "1."

CONCLUSION

This paper presents a new analysis of switching sequence operation for various symmetric and asymmetric RSMLIs with logical operators. A comparative study and observation between various published research articles is presented, and the proposed methodology provides simple analysis and better performance parameters than the previous analysis, by analyzing the pulse sequences of bipolar PWM and unipolar PWM techniques as binary representation and comparing each switching sequence of RSMLI with it. A step-by-step analysis is clearly presented with the calculation of number of carrier waves and modulation techniques. Operational analysis of individual switch is properly presented with the flowchart representations for considered RSMLI, DCL MLI, and SCSD MLI. The resultant logical equation of each switch for various RSMLIs is obtained with the application of the proposed method. Comparative analysis of voltage and current THD values is given without deviating the standards of MLI. The proposed method is suitable for generation of gating signals of various RSMLIs with different PWM methods and can be operated as switch sequence order.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation, to any qualified researcher.

AUTHOR CONTRIBUTIONS

VK contributed for analysis of the switching sequence of RSMLIs and wrote the first draft of the manuscript. SR is the corresponding author and takes primary responsibility for communication with the journal and editorial office during the submission process, throughout peer review and during publication. All authors contributed to manuscript revision, read and approved the submitted version.

SUPPLEMENTARY MATERIAL

The Supplementary Material for this article can be found online at: https://www.frontiersin.org/articles/10.3389/fenrg.2019.00164/full#supplementary-material

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Investigation of Standalone Solar Photovoltaic Water Pumping System With Reduced Switch Multilevel Inverter

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Solar photovoltaic-powered water pumping systems are becoming very successful in regions where there is no opportunity for connecting the electric grid. The photovoltaic technology converts solar energy into electrical energy for operating direct current (DC) or alternating current (AC) motor-based water pump. In the case of a solar AC motor water pump, it engages two energy conversion stages (DC–DC and DC–AC) in the power conditioning unit. This usually resulted in increased size, cost, and complexity and decreases the efficiency of the entire system. The existing two-level inverter (DC–AC) stage generates higher harmonics in output voltage and higher electromagnetic interference that deteriorates directly the AC motor performance. Therefore, as a solution to the addressed problems, in this study, an innovative seven-level inverter with five power semiconductor switches for the operation of 0.5 HP single-phase induction motor pump had been investigated. The proposed multilevel inverter has the capability of providing lesser harmonic voltage that reduces filter requirements; along with this, other part components are used lesser when compared to other conventional multilevel inverters. To provide better insight into the work performance of this proposed topology, the simulation is executed in the MATLAB/Simulink environment, and hardware implementation of the same is depicted. From the results, it is observed that the proposed multilevel inverter topology obtained a total power loss of 1.6034 W and efficiency at 98.11%. This quality output voltage acquired from the multilevel inverter had been fed to drive the induction motor water pump; it pumped the water at the desired flow rate accordingly.

Keywords: multilevel inverter, THD, DC-DC, DC-AC, photovoltaic, PWM, switching frequency, induction motor

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INTRODUCTION

Globally, solar photovoltaic-powered water pumping systems (SPVWP) are progressively used in the areas where there is plentiful sunshine and scarce power generation systems. Besides, photovoltaic (PV) system hardware prices declined to 80% in the last two decades. In the last 10 years, the levelized cost of electricity (LCoE) measure has lowered by 75% to USD 69/MWh (Jäger-Waldau, 2019). These developments paved the way to enroll PV systems much faster, especially the standalone alone PV systems. The acquisition of SPVWP is very simple compared

to other conventional diesel or electric-based water pumping systems in consideration of cost and maintenance. Generally, SPVWP is an assembly of a solar PV array, inverter, and motor-pump set. A PV array is a combination of electrically wired solar cells; they are mounted together on a frame, whereas an array is designed by connecting several modules together. The solar inverter is an important building block in a PV system, which makes the conversion of direct current (DC) output from PV panel into alternating current (AC) current that is able to run a motor pump set for groundwater extraction (Biswas and Iqbal, 2018). In addition, the present SPVWP utilizes electronic systems, which majorly helps in increasing output power, efficiency, and performance of the whole system. The controller also has the capability to track water levels in a tank, control motor speed, and utilize maximum power point tracking technology to give efficient output (Poompavai and Kowsalya, 2019). Furthermore, the authors in Odeh et al. (2018) suggested that the performance of SPVWP strongly depends on the head of the operation, irradiance factor, and PV array size. To improve the efficiency of the pump, they recommended to design the pump based on pump-well characteristics, subsystem efficiency, array sizing, average of system, frequency distribution of irradiance, etc. (Al-Shetwi et al., 2016). The advancements also occurred in PV panel tracking mechanism, from manual tracking to automatic dual-axis tracking systems, with the help of microcontroller programming (Chandel et al., 2015).

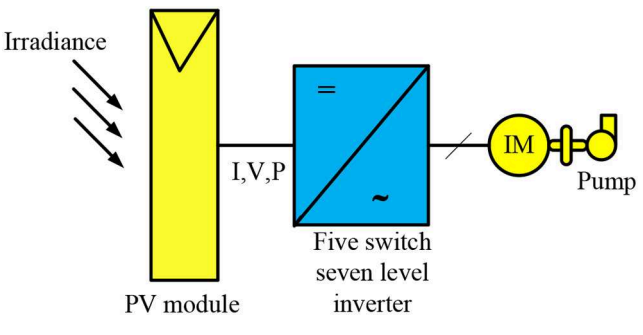

FIGURE 1 | A framework of the proposed system.

In SPVWP, the power conditioning unit (PCU) comprises of all electronic conversion units. Therefore, in the PCU unit, if the system employs a DC–DC converter or DC–AC inverter alone, this is regarded as a single-stage system. Else, if the system employs both converters, this is considered as a double-stage system (Karampuri et al., 2014). In a double-stage system, two PCUs are interfaced: one is applied for extracting maximum power from PV source, and the other is used for controlling a motor pump set. The existing two-level inverter or voltage source inverter (VSI) in PCUs is required to satisfy power quality issues, and it is also found to increase the losses and ripple content in the motor current of the PV system that leads to increased value of filter circuitry (Ramulu et al., 2016). Therefore, there is a requirement of single-stage power conditioning (i.e., single PCU) solution for SPVWP where the inverter is capable

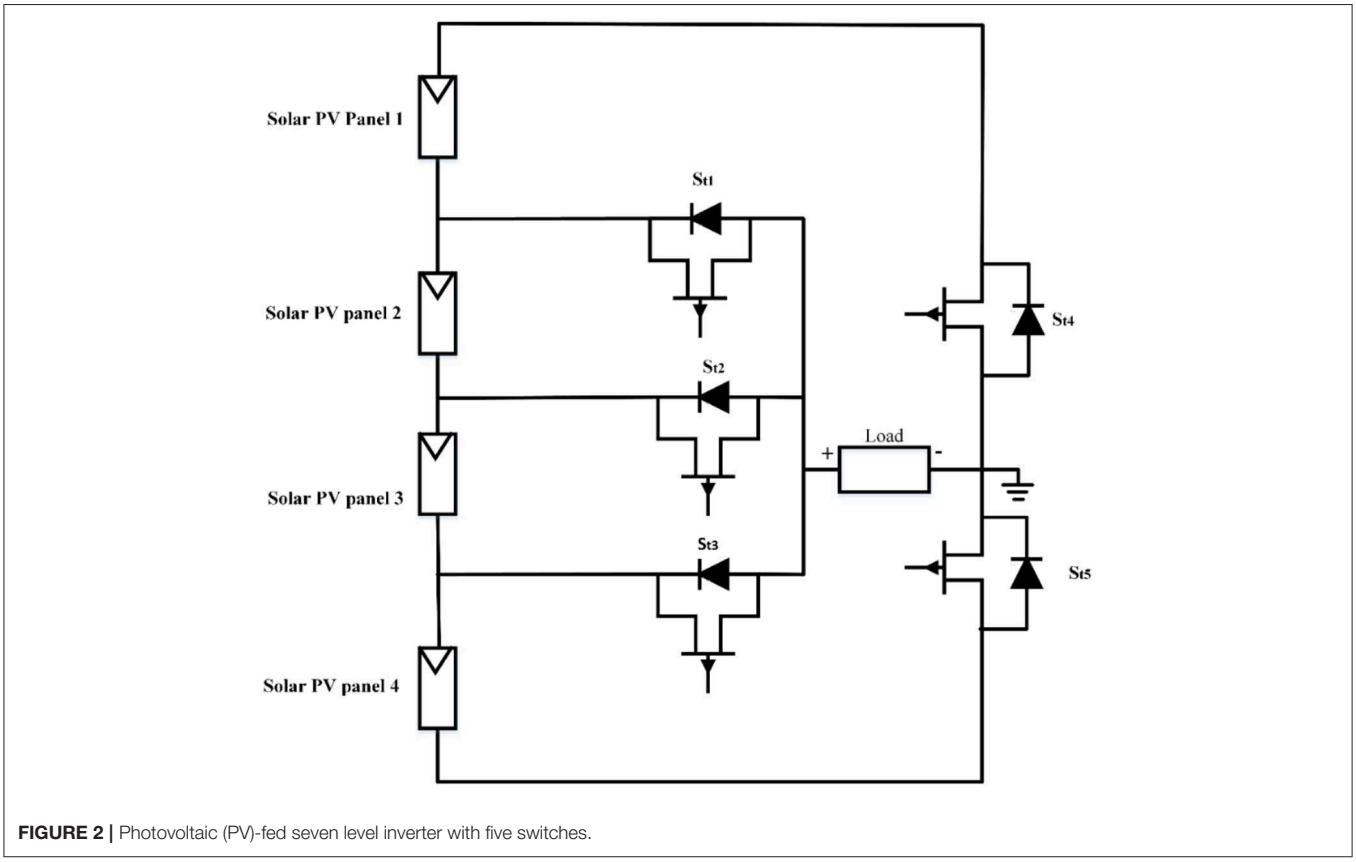

FIGURE 2 | Photovoltaic (PV)-fed seven level inverter with five switches.

of generating more than the two-level voltage in the output (Packiam et al., 2013; Mishra and Singh, 2016, 2018). Multilevel inverters (MLIs) provide the ultimate solution for the addressed issue and capable of delivering high power and medium voltage for industrial applications (Kurtoglu et al., 2019). Moreover, MLI extracts lesser input current functions both at the higher and lower switching frequency, gives lesser dv/dt effects in the load side, and also reduces filter needs that leads to avoiding stresses in bearings of a motor (Poompavai and Vijayapriya, 2017). As of now, many MLI topologies are available based on the mechanism of switching and depending on the input source voltage. Of those, the major three topologies commercially preferred in industries are cascaded H-bridge (CHB) multilevel inverter, diode clamped and flying capacitor type (Akagi, 2017).

The renewable energy-based systems usually take the foremost cascaded H-bridge type since it involves more isolated DC sources (Amamra et al., 2017) and also it eliminates fluctuation problems and the need of additional clamping diodes and flying capacitors. However, the issue with this kind is the switch count; it increases whenever the number of voltage level increases, which results in a bulky, less efficient and most expensive inverter. In an effort to fix this issue, different MLI topologies with reduced switch count had been analyzed (Gupta et al., 2016; Siddique et al., 2019a,b). This type of topologies greatly reduces the requirements of the driver circuit and lowers the size and expense of the entire system. Focusing on this reduced switch count to a maximum and minimizing the complexity, a novel topology was introduced (Umashankar et al., 2013). It utilized only five switches for a seven-level inverter, and this is the very least possible reduction in switch count when compared to other proposed topologies. The quality output voltage generated from the topology could be able to drive an asynchronous motor. To fulfill the water supply needs, induction motors are generally chosen for water pumping operation. Furthermore, the production of induction motors is in a mature stage paving a way to use it in developing countries for SPVWP application. The major advantages of induction motor include high starting torque, less cost durability, speed variation, low maintenance cost, easier operation, etc. This induction motor is followed by a centrifugal pump for pumping operation. The speed and flowrate are regulated with the help of multilevel inverters with minimum total harmonic distortion (THD). Al-Shetwi and Sujod (2018) found an inverse relationship between solar irradiance and THD; they observed that whenever there is an increase in solar irradiance, the THD tends to decrease either in the current and voltage waveform. The quality output voltage waveform obtained from MLI could be controlled, with its magnitude and frequency referred to be V/f control. This way permits the induction motor to attain the desired speed at different rates.

In this study, the operation of a seven-level inverter with five switches inverter had been tested experimentally with 0.5 HP single-phase induction motor water pump with the help of d-SPACE RTI-1104 platform. This topology uses an insulated-gate bipolar transistor (IGBT), as power switches and gate signals are given through a sinusoidal pulse width modulation technique. This proposed system eliminates the need for the DC–DC conversion stage in SPVWP and provides a single-stage solution through the MLI topology. The observed results show that the induction motor pump stayed its operation smoothly by receiving quality output voltage with lesser THD and also with reduced switching losses from seven-level five-switch topology. The speed and flowrate are regulated at the desired value with the help of pulses obtained from the proposed MLI topology.

A FRAMEWORK OF THE PROPOSED SYSTEM

The solar PV standalone water pumping system framework is depicted in **Figure 1**. It comprises of a PV array, followed by a five-switch seven-level inverter and an induction motor water pump. The proposed multilevel inverter with reduced switches is used to provide pulse width modulated voltage to the input of induction motor and pump assembly with a single-stage solution.

Photovoltaic System

The photovoltaic cells are made of customized PN junction diode that converts the visible light into DC, and this process is

TABLE 1 | Switching pattern of seven-level inverter with five switches.

S. No	S_{t1}	S_{t2}	S_{t3}	S_{t4}	S_{t5}	Output voltage
1	OFF	OFF	ON	OFF	ON	+Vdc
2	OFF	ON	OFF	OFF	ON	+2Vdc
3	ON	OFF	OFF	OFF	ON	+3Vdc
4	OFF	OFF	OFF	OFF	OFF	0
5	ON	OFF	OFF	ON	OFF	−Vdc
6	OFF	ON	OFF	ON	OFF	−2Vdc
7	OFF	OFF	ON	ON	OFF	−3Vdc

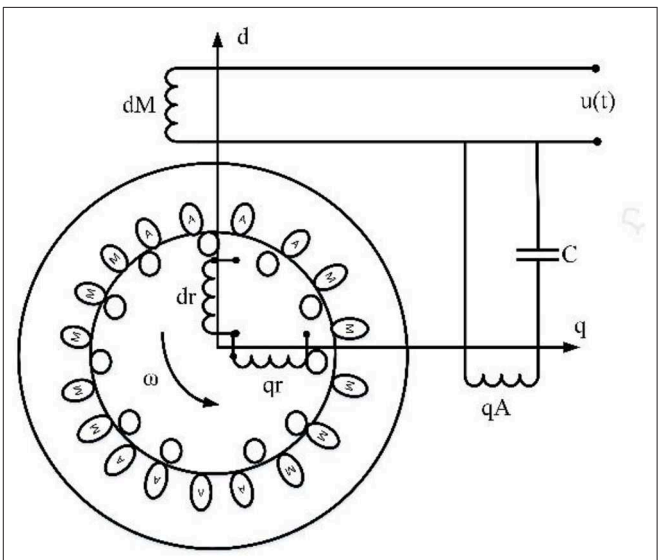

FIGURE 3 | Perspective of dq model representation for single-phase induction motor.

referred to as photovoltaic effect. The PV modules combined in parallel or series to generate higher voltage and currents (Aliyu et al., 2018). The PV unit can be represented by two model: single diode model (SDM) and the double diode model (DDM) (Jordehi, 2016; Sudhakar Babu et al., 2016). The SDM model is the most prevailed model that has less complexity and achieve accurate results.

It represents the individual PV cell; a PV module consists of many cells or an array that includes many modules together. The mathematical equation describing the PV system is expressed in Equation (1).

$$I = I_{pv}N_{par} - I_0 N_{par}\left\{\exp\left[\frac{V + R_s\left(\frac{N_{ser}}{N_{par}}\right)I}{V_t \alpha N_{ser}}\right] - 1\right\} - \frac{V + R_s\left(\frac{N_{ser}}{N_{par}}\right)I}{R_p\left(\frac{N_{ser}}{N_{par}}\right)} \quad (1)$$

where I_{pv} is the current produced by incident light (A), I_o is the leakage current of a diode (A), q is the charge of an electron (1.60217×10^{-19}C), k is the Boltzmann constant (1.38065×10^{-23} J/k), α is the diode ideality constant ($1 < \alpha < 1.5$), R_s is the equivalent PV array series resistance (Ω), R_p is the equivalent PV array parallel resistance (Ω), N_{ser} is the number of cells in series, N_{par} is the number of cells in parallel, T is the PN junction temperature (K), and V_t is the PV array thermal voltage (V).

PV-Fed Multilevel Inverter With Reduced Switch Count

The seven-level inverter with five-switch topology representation is given in **Figure 2**. It is a very simple topology that involves four isolated DC sources, and in the case of nine levels, it would be five DC sources and so on. Since it has isolated DC sources integrating PV as a source is very easy. In this proposed topology, the PV panels replaced those isolated DC sources. Using phase opposition and disposition (POD) technique (Dan et al., 2015), the gating signals are generated and given to the five power IGBT switches. A sinusoidal modulating signal having a magnitude of "A_m" and frequency of "f_m" is taken to generate the gate signal where comparison is made in between reference and the carrier waves. The signals produced would be equal to the number of carrier signals. The modulation index (M_a) can be represented by

$$M_a = \frac{A_m}{f_m} \quad (2)$$

Initially, the first leg of switches S_{t1}, S_{t2}, and S_{t3} had to be fetched with 2 kHz switching frequency followingly the second leg of switches S_{t4} and S_{t5} that should be fed with 50 Hz frequency. The gating signal pattern of the first leg of the switches must be unidirectional; otherwise, the output waveform may get distorted. The second leg of inverter assures the polarity reversal pattern. The switching pattern for the proposed topology

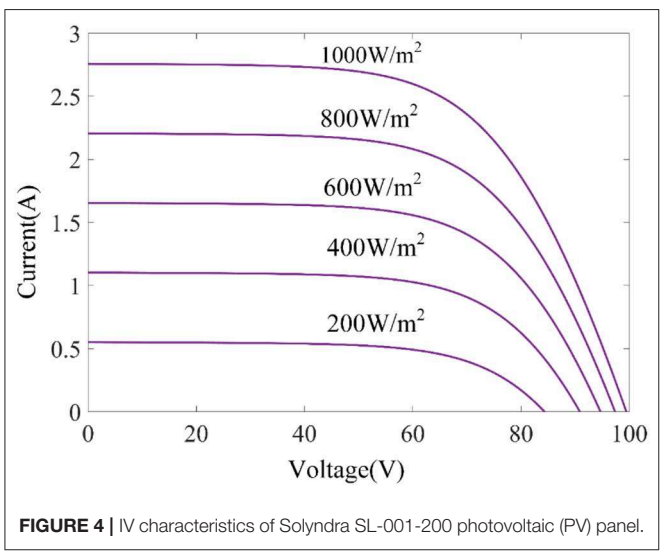

FIGURE 4 | IV characteristics of Solyndra SL-001-200 photovoltaic (PV) panel.

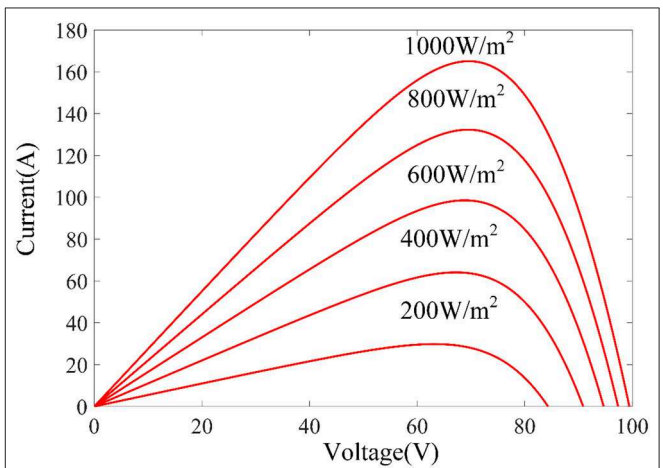

FIGURE 5 | Photovoltaic (PV) characteristics of Solyndra SL-001-200 PV panel.

TABLE 2 | Solyndra SL-001-200 (200 W) solar photovoltaic (PV) panel specifications.

Specifications	Data
STC power rating	200 W
Peak efficiency	10.18%
Power tolerance	−4%/+4%
I_{mp}	2.55 A
V_{mp}	78.3 V
I_{sc}	2.78
V_{oc}	99.7 V
Temp. coefficient of power	−0.38%/K
Temp. coefficient of voltage	−0.289 V/K
Series fuse rating	23 A
Maximum system voltage	600 V

is presented in **Table 1**. From the proposed topology, the seven-level output voltage levels are obtained with the combination of this five-switch operation. The final output voltage levels produced by the topology can be represented by $m = (2 \times n - 3)$, where "m" denotes the number of output voltage levels and "n" refers to the number of power switches. The expression can also be referred by $m = (2 \times v - 1)$, where "v" refers to the number of DC sources.

INDUCTION MOTOR-DRIVEN WATER PUMPING SYSTEM

In a wider range, induction motor is applied in domestic and industrial applications since they are of lower cost and need lesser maintenance. In general, induction motors are of symmetrical rotor cage and two non-symmetrical stator winding (main winding and auxiliary winding with starting or running capacitor), supplied with an equivalent sinusoidal voltage source. In this context, the second type had been chosen for water pumping applications. For modeling and analyzing the single-phase induction motor, two methods are available: one is the double field revolving theory, and the other is the cross-field theory. Of those, the first one is preferred often since it is more akin to the three-phase induction motor theory. In context to the theory, a part of alternating quantity can be resolved into two axes that are able to rotate in relatively opposite directions. Meanwhile, the axes of both stator windings are orthogonal as illustrated in **Figure 3**. Thus, the dq axes of the model may be associated with axes of windings. The basic equations that describe the model of induction motor are given below.

The current flow through the stator is expressed as

$$I(s) = \frac{V_i(s) - V_o(s)}{(R_1 + sL_1)} = I_1(s) + I_2(s) \tag{3}$$

If the current drawn by the rotor as I_2, then the no-load current can be expressed by

$$I_1(s) = I(s) - I_2(s) \tag{4}$$

The voltage across the rotor inductance is given by

$$V_f(s) = I_2(s) * \left(\frac{R_2}{2s}\right) \tag{5}$$

The airgap power developed by the induction motor is given by

$$P_{gf}(s) = I_2(s)^2 * \left(\frac{R_2}{2s}\right) \tag{6}$$

The motor torque is given by

$$T(s) = \left[\frac{P_{gf}(s) - P_{gb}(s)}{2\Pi n_s}\right] \tag{7}$$

The load balance equation is expressed by

$$\omega(s) = \frac{[T(s) - T_L(s)]}{(Js + B)} \tag{8}$$

whenever the load increases, the rotor current of the induction motor tends to increases. Furthermore, the energy generated from an induction motor is converted into kinetic energy in the

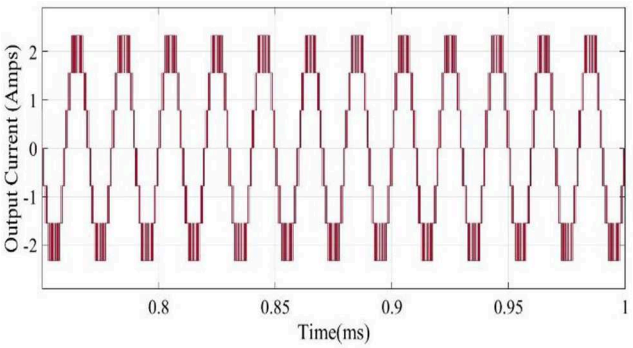

FIGURE 7 | Output current from seven-level inverter with five switches.

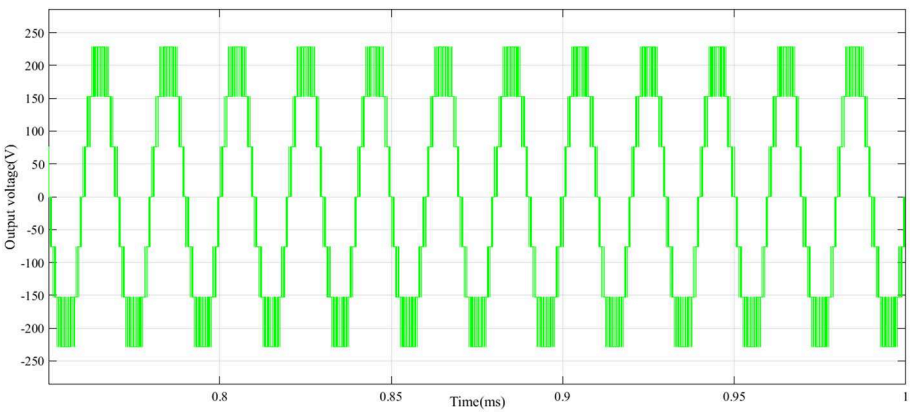

FIGURE 6 | Seven-level output voltage from seven-level inverter with five switches.

liquid flow by triggering the liquid revolution. The centrifugal pump is used for pumping operation due to easy operation. It is particularly intended for fixed head applications, and the pressure difference generated increases along with the speed of the pump. These pumps are a rotating impeller category that radially throws water at a casing to transform water momentum into useful pressure.

SIMULATION RESULTS AND ANALYSIS

Simulations conducted with MATLAB/Simulink environment to verify and confirm whether the proposed multilevel inverter topology can be practically suitable to solar photovoltaic-powered water pumping system or not. Using PV modeling, the IV and PV characteristics obtained for the Solyndra SL-001-200 PV panel, taken at different irradiance conditions, is represented in **Figures 4**, **5**. The maximum open-circuit voltage (V_{oc}) of 99.7 V is obtained at the standard irradiance condition of 1,000 W/m^2. At minimum irradiance of 200 W/m^2, V_{oc} is developing at the range of 84 V. At some point of combination of the current and voltage, the power reaches a maximum value, which locates as I_{mp} and V_{mp}. In this specific point, the maximum power produced is referred to as maximum power or MPP. The solar PV panel specifications are given in **Table 2**.

Following that, using POD technique, the gate pulses are generated for power switches of proposed MLI topology. Based on the pulse pattern, the resulted seven-level output voltage and current attained from multilevel inverter topology is depicted in **Figures 6**, **7**. The fast Fourier transform (FFT) analysis for the proposed topology is given in **Figure 8**. As per the Institute of Electrical and Electronics Engineers (IEEE) 519 harmonic distortion standard, for inverter without a filter in the circuit, 15–25% of THD is allowable. Accordingly, the least THD of 2.63% is developed in the resulted voltage. In case the proposed topology is designed with filter, it may achieve far better results. The logical

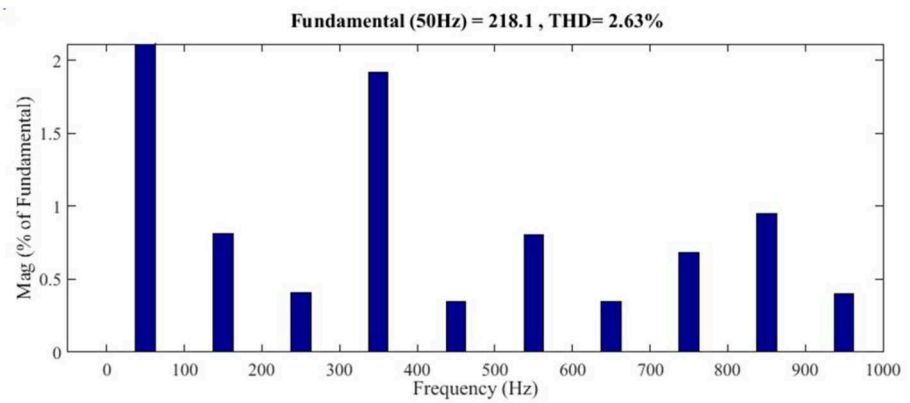

FIGURE 8 | Fast Fourier transform (FFT) analysis of seven-level inverter with five switches.

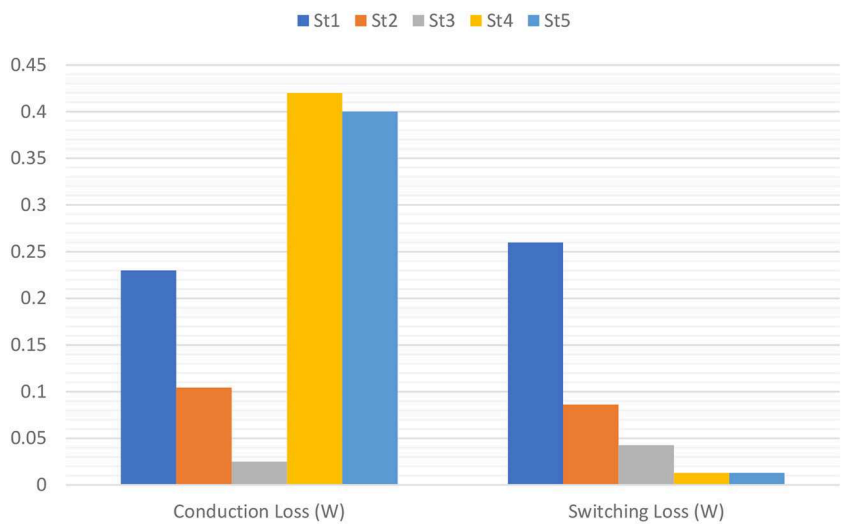

FIGURE 9 | Power loss analysis for seven-level inverter with five switches.

expression for THD can be expressed by

$$\text{Voltage THD}(\%) = \frac{\sqrt{V_{\text{rms}}^2 - V_{1\text{rms}}^2}}{V_{1\text{rms}}} * 100 \quad (9)$$

where $V_{1\text{rms}}$ denotes the root mean square (RMS) value of the fundamental component, which is slightly high because of lower switching losses obtained from the proposed topology. The total power loss in an inverter is the combination of conduction (P_C) and switching loss (P_{Sw}). The expression of total power losses occur in an inverter is given by

$$\text{Total power losses } (P_{\text{Loss}}) = P_C + P_{Sw} \quad (10)$$

By considering the losses, the efficiency of the inverter can be calculated using the following expression,

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_C + P_{Sw}} \quad (11)$$

Hence, considering both the losses calculated for each switch of the proposed inverter is represented in **Figure 9**. The second

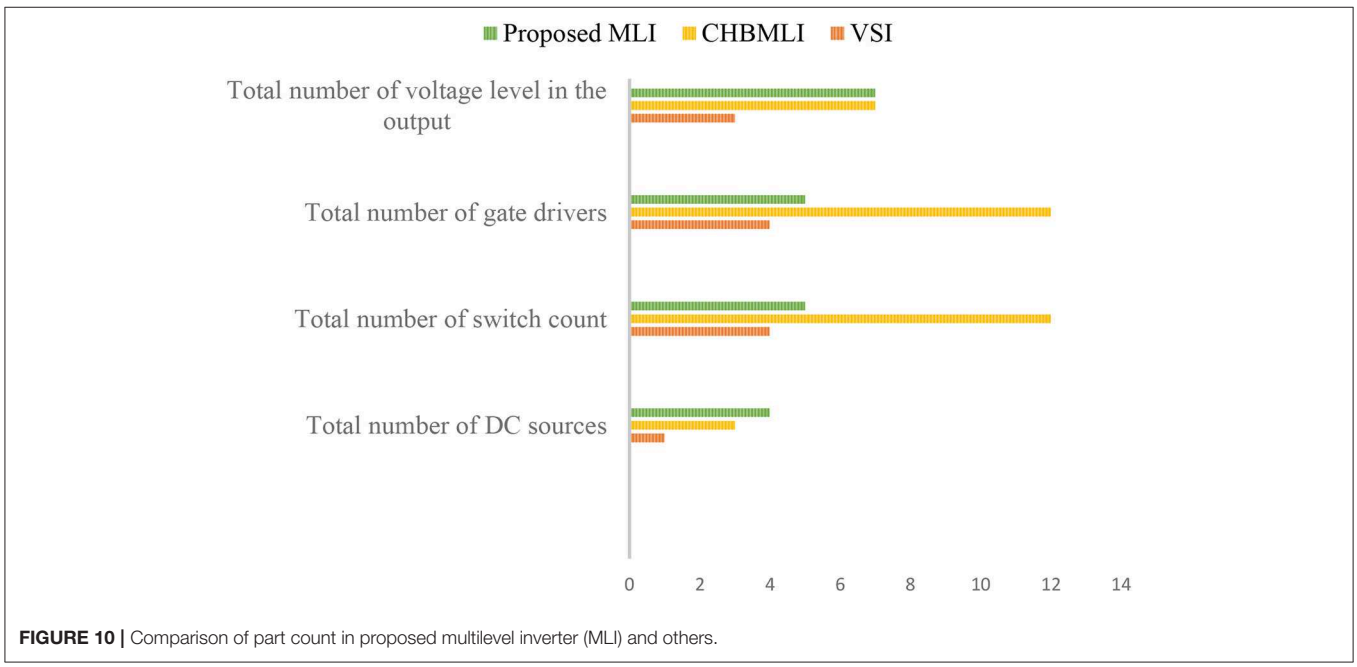

FIGURE 10 | Comparison of part count in proposed multilevel inverter (MLI) and others.

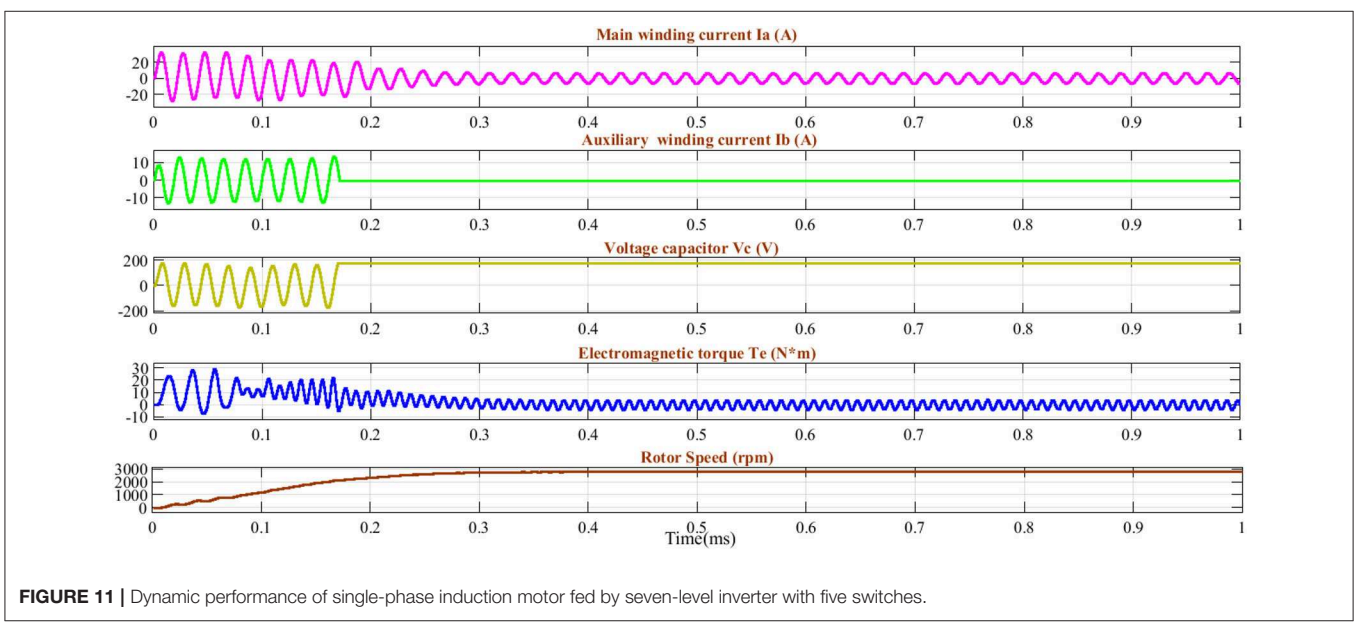

FIGURE 11 | Dynamic performance of single-phase induction motor fed by seven-level inverter with five switches.

leg of switches attained lesser switching losses compared to the first leg because of utilizing lesser switching frequency. The total power loss calculated with the proposed multilevel inverter is 1.6034 W. The efficiency gained for the proposed inverter is 98.11%, whereas the conventional two-level inverter attains only 59.96%. The number of part count comparative analysis of existing and proposed topology is depicted in **Figure 10**. It shows that the proposed one stands far better than the others. The generated output voltage carrying lesser harmonic content is fed to the capacitor, then the capacitor-run single-phase induction motor drive is started to give its striking dynamic performance, which is depicted in **Figure 11**.

EXPERIMENTAL VALIDATION

The hardware prototype for the proposed seven-level five switch inverter fed with a single-phase induction motor water pump had been tested experimentally. The gate signal generated through POD technique had been brought out with the help of digital I/O ports in the d-SPACE RTI-1104 platform. Then, it is passed to the TLP 350 gate driver board and to the power IGBT switches. The triggering of switches could happen only if the gate driver board enhances the voltage from 5 to 15 V. A switching frequency of 2 kHz had been applied to the first leg of three switches, and 50 Hz had been given to the other two switches. This kind of pulse pattern helps to reduce the switching losses significantly. To emulate or approximate the PV source equivalence, a small resistance is connected between the programmable DC supply and the seven-level inverter five switches. The input RMS voltage of 78.3 V and current of 1 A were given as input to the four-DC source input side for the topology from programmable DC supplies, which is fixed to operate at constant voltage mode. As a result, the final output of the seven-level voltage generated at the output side with lesser harmonics, as shown in **Figure 12**, is finally fed to the 0.5 HP single-phase induction motor water pump load that is able to run at a maximum speed of 2,880 rpm. Initially, the auxiliary winding disconnected at 75% of rated synchronous speed. The settled torque of 4 Nm is unidirectional to pertain to the motor in a single direction. Meanwhile, after a certain acceleration, the offset in torque generated by the motor decreases to a load torque. Subsequently, the control of torque, direction of rotation, and speed of the motor are decided by the voltage and frequency of the proposed multilevel inverter. The THD analysis obtained at the hardware side is depicted in **Figure 13**. It can be noted that the harmonic plots of current and voltage are maintained at the same frequency window. Furthermore, the seven-level output voltage and current pattern are similar to those attained from simulation results.

CONCLUSION

The seven-level inverter with five switches had been applied for the investigation of a 0.5 HP single-phase induction motor water pump. The reduced switch count, lesser requirement of

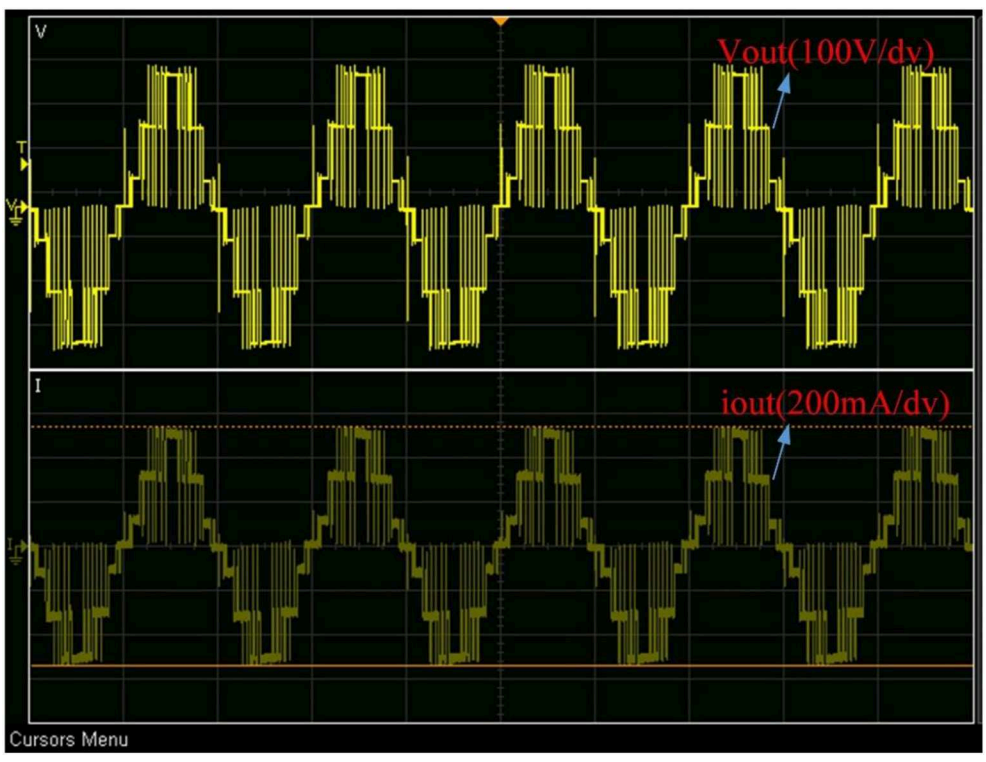

FIGURE 12 | Output voltage and current of seven-level inverter with five switches.

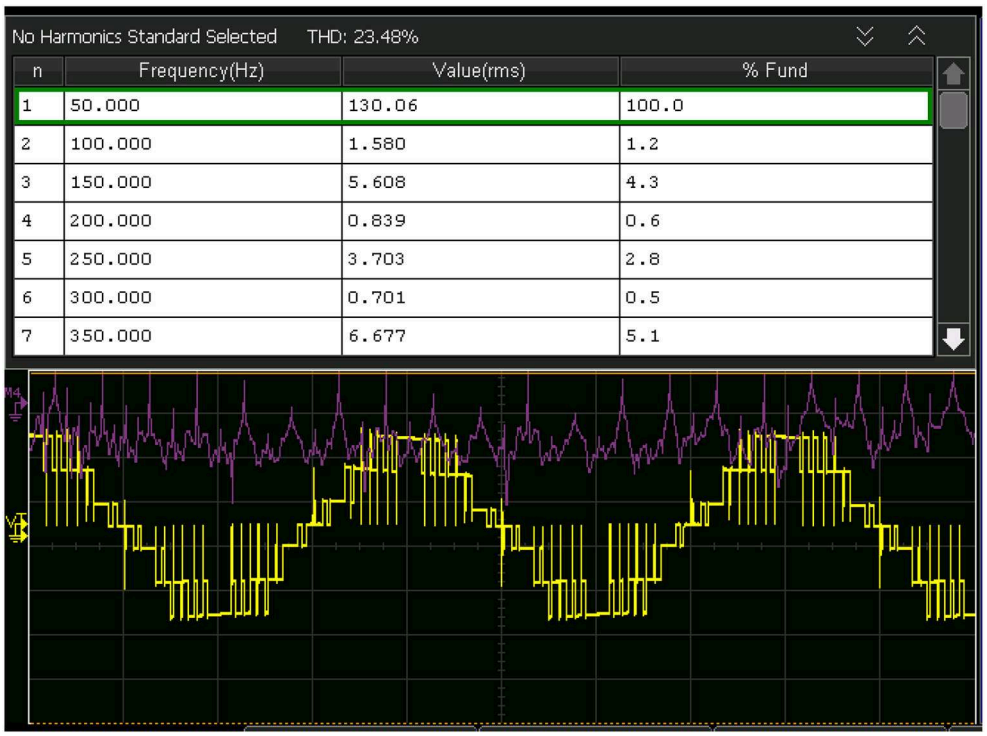

FIGURE 13 | Harmonics generated in seven-level inverter with five switches.

gate driver circuits and DC sources, and increased voltage levels in the output are the main features of the proposed multilevel inverter topology. As a promising source, the photovoltaic system could be able to give constant voltage to the reduced switch multilevel inverter input DC source side that guarantees the standalone operation of a water pump. In summary, the simulation results reveal that the switching losses calculated across each switch are less and the THD content is also very low without any filter compared to other conventional multilevel inverter topologies. The reduced harmonic content in the output voltage enabled the induction motor to deliver its striking dynamic performance, and it pumped water at the desired flowrate with the control in PWM technique. The hardware implementation of the same setup matched with the simulation outcomes, which validate the system, although when implementing practically, thermal resistance and leakage current in the circuit affects the power quality, which differentiates the simulation and practical results. The internal resistance of the auxiliary circuit (gate driver board) used to drive the IGBT also tends to create a difference among the simulation and practical results. The overall system performance found to be satisfactory for operating induction motor water pump, thereby validating the system model.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation, to any qualified researcher.

AUTHOR CONTRIBUTIONS

TP and MK conceived of the presented idea. TP executed simulation and experiment analysis. MK encouraged TP to investigate and supervised the findings of this work. All authors discussed the results and contributed to the final manuscript.

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Novel Filters Based Operational Scheme for Five-Level Diode-Clamped Inverters in Microgrid

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This paper introduces a new operational scheme for several multilevel (five-level diode-clamped) inverters in the microgrid. The presented operational scheme has a central structure (different from the distributed controllers for droop schemes) to alleviate the drawback of the conventional droop control for microgrid operation. The contribution of this paper is focused on the suggested operational scheme, which has two contributory components. The first component is the novel smooth variable structure filters (SVSF), which are formulated to estimate the disturbances of voltage harmonics and voltage unbalance. The second component is an efficient adaptive sliding mode controller to operate these inverters. This proposed operational achieves equal power sharing among working inverters, compensating for voltage unbalance at the point of common coupling (PCC) at loads, and mitigation for voltage harmonics at the PCC. More importantly, the propounded operational scheme efficiently stabilizes voltage with the variation of balanced, unbalanced, and non-linear loads in addition to the seamless transient and steady-state performance for injected power by inverters. The performance of the suggested operational scheme is justified by simulation results.

Keywords: microgrid, multilevel inverters, operational scheme, smooth variable structure filter, adaptive sliding mode controller

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INTRODUCTION

The microgrid has become into the focus of research at the distribution system level because microgrid fetches some merits such as low-carbon emission, its modularity, integration of renewable dispersed energy sources, and its ability to work independently or connected to the central power grid (Jiayi et al., 2008; Mariam et al., 2013). In addition to aforementioned merits, any microgrid has also several challenges such as the stability of voltage and frequency with variable loads, existence of harmonics due to non-linear loads, control of dispersed energy sources, circulating current among inverters, existence of inverters associated with renewable energy sources, and procedure for connection/disconnection to/from the central grid (Parhizi et al., 2015; Hirsch et al., 2018).

The operational scheme for the microgrid becomes a challenging research topic because it is supposed for this scheme to realize several simultaneous objectives. Therefore, some publications survey/review the types/structures of operational/control schemes employed to operate the microgrid (Huang et al., 2011; Vandoorn et al., 2013; Canizares and Palma-Behnke, 2014; Han et al., 2016a; Rajesh et al., 2017; Sen and Kumar, 2018). The idea presented in this paper focuses on how

the voltage harmonics and voltage unbalance are mitigated in addition to stabilizing the voltage at the loads' side with different loading conditions for linear and non-linear loads. Therefore, the coming literature survey explicates the state-of-art for the mitigation and extraction tools for harmonics and voltage unbalance within microgrid environments.

The conventional droop control has two levels (primary and secondary), and the voltage unbalance is compensated at the secondary level by the control action of the proportional integral (PI) controller (Lexuan et al., 2015). This presented droop control in Lexuan et al. (2015) is used to equalize the power among three two-level inverters, and there are no details on how the negative-sequence is extracted. Another enhanced control scheme is designed for a four-leg inverter (Moghaddam et al., 2018). This inverter is powered by a battery based energy storage system under unbalanced and non-linear loads. The operational scheme of this inverter is operated using the decoupled model in the $d-q$ frame such that the total harmonic distortion (THD) and unbalance factors are reduced. A hierarchical droop control of Savaghebi et al. (2012) includes the primary and secondary control levels. Its primary control has a local droop control for active and reactive power. Meanwhile, the central secondary controller is designed to manage the compensation of voltage unbalance at the PCC in the microgrid. An operational scheme including double control loops for the positive and negative-sequence currents in the $d-q$ frame is developed to mitigate the current unbalance (Reyes et al., 2012). This presented control scheme is further improved by adding a filter to get rid of double the fundamental frequency in this frame. The droop control scheme presented in Ren et al. (2018) is integrated with voltage unbalance compensation, but this paper does not give details of how voltage unbalance is extracted and mitigated. Another multi-function operational scheme, which handles voltage unbalance compensation, harmonic power sharing, selective virtual harmonic impedance, virtual fundamental impedance, and conventional droop control is introduced in Han et al. (2016b). Its secondary loop is employed to restore the voltage and frequency to their normal values with help of proportional resonant (PR) controllers. Meanwhile, its primary control loop operates the inverters such that the power is equally divided among the working inverters. A virtual impedance loop inside the droop control scheme is modified to include the voltage unbalance and harmonics compensation (Liu et al., 2014), in which the harmonic voltage drop and unbalanced voltage drop are mitigated by the control action of PR and PI controllers. New cascaded loops of voltage and current for the positive and negative-sequence voltages are proposed in Acharya et al. (2019), and the extraction of the negative-sequence voltage and current is done using passive filters in the $d-q$ frame. The proposed scheme of Acharya et al. (2019) achieves a reduction of the negative unbalance factor to be smaller than 2%. The conventional droop control along with two traditional levels (primary and secondary) is suggested in Savaghebi et al. (2011, 2013), at which the secondary control level of the droop scheme is used to calculate the power of negative-sequence components (voltage and current) and converted into a reference voltage. This reference voltage is summed with other references to operate the primary control level. Another cascaded structure of voltage and current control loops for each working inverter is introduced in Zhao et al. (2015), where the virtual impedance loop contributes to the voltage references, and these references are applied to the voltage loop. The extraction of the negative-sequence voltage in Zhao et al. (2015) is conducted in the $d-q$ frame using a passive filter. Thus, this extracted negative-sequence voltage is converted into a voltage reference that is augmented with other voltage references. Another technique for compensating voltage unbalance is realized by the extraction and mitigation of the negative-sequence current (Shi et al., 2016), which is extracted and converted into a current reference that is applied to the current loop of the primary control level in its droop scheme.

This paper introduces a new technique for the extraction of voltage disturbances (particularly voltage unbalance and harmonics). The forthcoming paragraph gives a brief survey about the different extraction/estimation tools that have been developed to estimate those voltage disturbances. The most common technique to extract the voltage unbalance is to convert the phase voltages from the a-b-c natural frame to the $d-q$ frame, and then a low-pass filter is used to distinguish between the positive and negative-sequence voltages (Reyes et al., 2012; Moghaddam et al., 2018; Acharya et al., 2019). The estimation of voltage unbalance is also reported in Javier Alcántara and Salmerón (2005) by three blocks of the neural network: The 1st block is to estimate the Parks vector and the zero-sequence voltage, while the 2nd block is employed to estimate the harmonics, and the 3rd block is dedicated to estimate the voltage unbalance components. The adaptive linear neuron (ADALINE) is used to estimate the negative- and positive-sequence components, it works well, but its formulation is based on matrix equations, which consume much time for its calculation (Marei et al., 2004). The extended Kalman filter is developed to estimate the positive and negatives-sequence voltage in the $\alpha-\beta$ frame (Sun and Sahinoglu, 2011), and the extended part of Kalman filter is used to detect any variation in the fundamental frequency. The linear Kalman filter is adopted to estimate the positive and negative-sequence voltage (Soliman and El-hawary, 1997), in which the developed model presents the state transitional matrix in the form of an identity matrix, and the measurements matrix varies with time. The presented results in Soliman and El-hawary (1997) show an accurate estimation, but the existence of harmonics is not included.

Most of aforementioned publications (Savaghebi et al., 2011, 2012, 2013; Reyes et al., 2012; Liu et al., 2014; Lexuan et al., 2015; Zhao et al., 2015; Han et al., 2016b; Shi et al., 2016; Moghaddam et al., 2018; Ren et al., 2018; Acharya et al., 2019), are related to the extraction and mitigation of voltage disturbances in the microgrid, and some of these publications suffer some flaws such as,

- The mitigation of the voltage unbalance is done through the droop control scheme at the secondary control level, which adds more complexity to the employed droop operational scheme.
- The voltage unbalance is calculated in the $\alpha-\beta$ frame or $d-q$ frame using the PLL and passive filters,

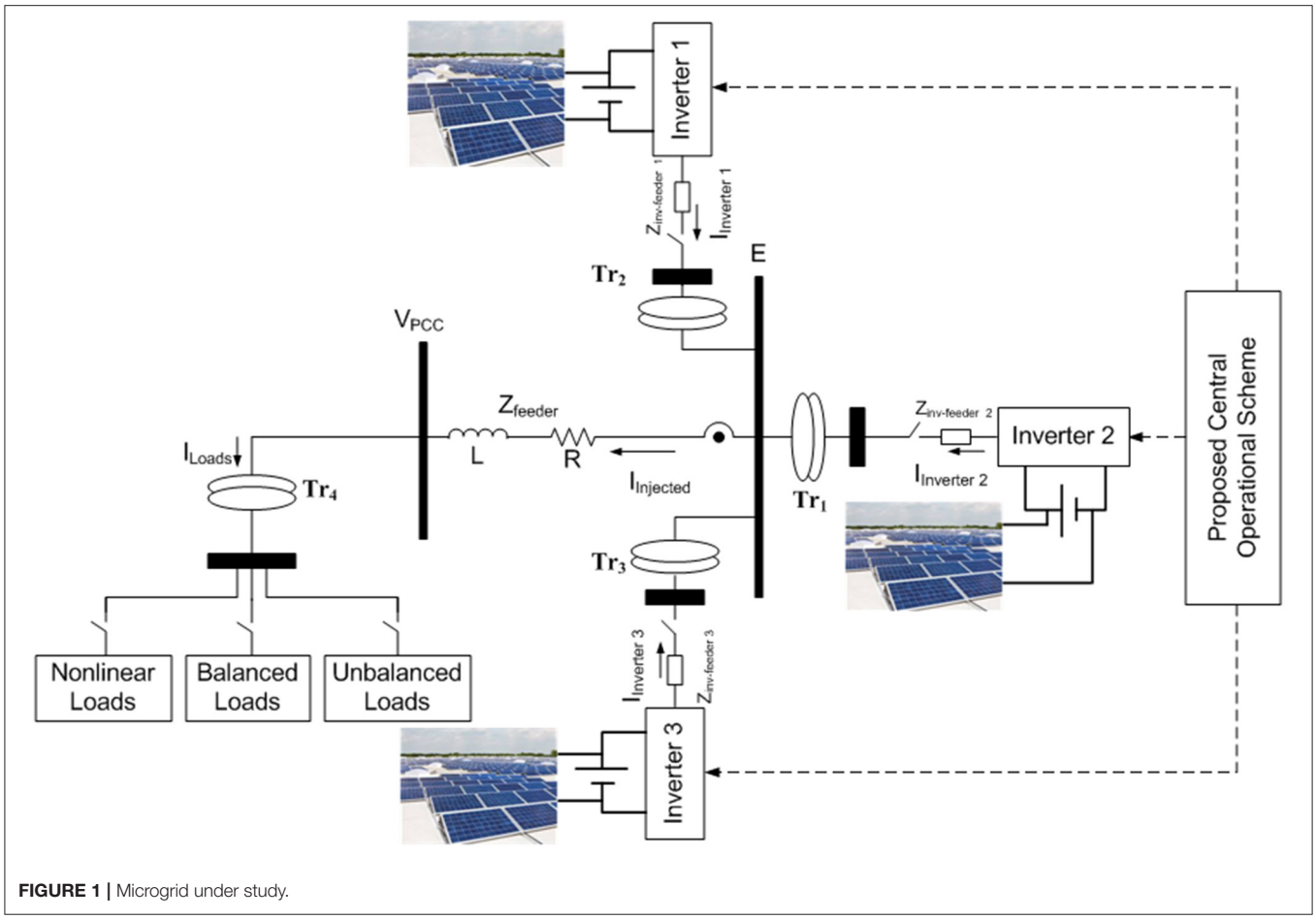

FIGURE 1 | Microgrid under study.

which lead to error in the magnitude of extracted unbalance components.

- The mitigation of voltage unbalance is done through the negative-sequence voltage only; meanwhile, the connection of the microgrid to the ground is common (Mohammadi et al., 2019), which yields zero-sequence components in the microgrid. In the most of publications (Savaghebi et al., 2011, 2012, 2013; Reyes et al., 2012; Liu et al., 2014; Lexuan et al., 2015; Zhao et al., 2015; Han et al., 2016b; Shi et al., 2016; Moghaddam et al., 2018; Ren et al., 2018; Acharya et al., 2019), the zero-sequence voltage is not considered for mitigation in the microgrid.

The contribution of this paper is exemplified in the development of an operational scheme, which is designed in such a way to alleviate the preceding drawbacks in addition to stabilizing the voltage at any variation in loading conditions of the microgrid. The operational scheme has two main contributory points: Estimation of voltage disturbances and controlling of multilevel inverters. The paper is organized in five main sections. The second section demonstrates the microgrid under study. The third section shows the operational scheme along with the formulation of the smooth variable structure filter to estimate the current harmonics and voltage unbalance. The fourth section illustrates simulation results. The last section summarizes the findings of the paper.

MICROGRID UNDER STUDY

The microgrid under study, shown in **Figure 1**, has three dispersed energy sources, which are PV solar arrays connected to battery systems. Their harvested energies are injected to the microgrid through three inverters; each three-phase inverter consists of three single-phase full-bridge five-level diode-clamped inverters whose topology and its output voltage waveforms are already given in **Figures 2A,B**, respectively.

In this research, all inverters are have the same topology as shown in **Figure 2A** and have the same rating as written in **Table 1**. The loads in the microgrid are groups of balanced, unbalanced, and non-linear loads. The parameters of the microgrid are given in **Table 1**.

Each inverter circuit is operated by the phase-disposition pulse width modulation (PD-PWM), where the control signal is compared to four carrier signals with 3-kHz to operate the first leg for switches from S1 to S8 in **Figure 2A** and the inverted control signal is used to operate the other leg of switches from S9

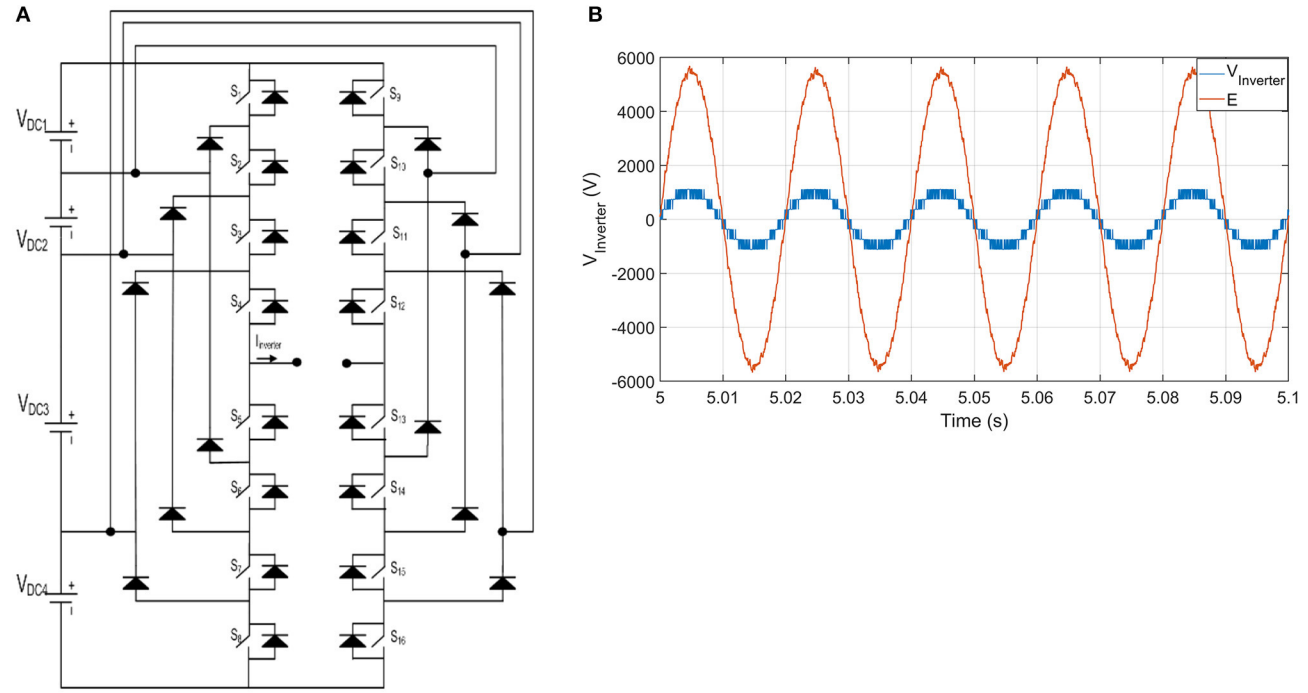

FIGURE 2 | Topology of utilized multilevel inverter with its injected voltage. **(A)** Topology five-level diode-clamped inverter per phase. **(B)** Voltage waveforms before and after transformer Tr1 for one phase of inverter 2.

TABLE 1 | Microgrid and inverter parameters.

Parameter	Value/Description
Rated voltage level	= 6.6 kV
Microgrid rating/base	= 7.5 MVA
Power rating/inverter	= 2.5 MVA
Feeder impedance Z_f	$= 1.2\Omega + 1.5j\,\Omega$
Transformer Tr_1, Tr_2, Tr_3 rating	= 2.5 MVA
Transformer voltage ratio	1.32 *kV* : 6.6 *kV*
Transformer Tr_1, Tr_2, Tr_3 resistance	= 0.0101 *pu*
Transformers Tr_1, Tr_2, Tr_3 inductance	= 0.1 *pu*
Transformer Tr_4 rating	= 7.5 MVA
Transformer Tr_4 voltage ratio	6.6 *kV* : 0.4 *kV*
Inverter type	Three single-phase full bridge. Each bridge is 5-level diode clamped inverter
Number of parallel inverters	Three

to S16 in **Figure 2A**. The details of its operation are documented in Elnady and Suleiman (2017).

PROPOSED OPERATIONAL SCHEME

The contribution of this paper includes two mains components, which are the development of the novel SVSF for the estimation of voltage harmonics/unbalance and the employment of adaptive sliding mode controller to operate the inverters. This section is divided into three different subsections. The first subsection is related to the development of the SVSF to estimate the disturbances, the second subsection shows the formulation of the adaptive sliding mode controller, and the last subsection illustrates the structure of the whole operational/control scheme of the microgrid.

Smooth Variable Structure Filter

The Smooth Variable Structure Filter (SVSF) is a new estimation filter that was recently developed and evolved through several works such as Al-Shabi et al. (2013), Gadsden et al. (2015), and Al-Shabi and Elnady (2019). The basic idea is that the SVSF uses a switching hyperplane from the measurement and forces the estimate to be in its neighborhood. This filter will be newly formulated in this work to estimate the voltage harmonics and unbalance in the microgrid of **Figure 1**. The mechanism of operation for the SVSF is simple, it can be summarized as,

Firstly: an unrefined estimate is obtained as follows:

$$\begin{aligned} X_{unrefined,k} &= AX_{refined,k-1} \\ z_{unrefined,k} &= H_k X_{unrefined,k} \end{aligned} \tag{1}$$

where,

$X_{unrefined,k}$ is the in-phase of the voltage harmonics and is defined as,

$$\begin{aligned} X_{unrefined,k} = [&A_1\cos\theta_1 \quad A_1\sin\theta_1 \quad A_2\cos\theta_2 \quad A_2\sin\theta_2 \quad \dots \\ &A_n\cos\theta_n \quad A_n\sin\theta_n]^T \end{aligned} \tag{2}$$

A and H are the voltage harmonics in the microgrid and measurement matrices are they are defined as,

$$A = I_{2n\times 2n} \tag{3}$$

$$H_K = \begin{bmatrix}\cos\omega_1 kT_s & -\sin\omega_1 kT_s & \cos\omega_2 kT_s & -\sin\omega_2 kT_s & \dots \\ \cos\omega_n kT_s & -\sin\omega_n kT_s\end{bmatrix} \tag{4}$$

T_s is the sampling time, and $z_{unrefined,k}$ is the total voltage harmonics and are defined as,

$$z_{unrefined,k} = \sum_{i=1}^{n} A_i \cos\left(\omega_i kT_s + \theta_i\right) \tag{5}$$

This step is similar to the one used in Kalman filter presented in Girgis et al. (1991).

Secondly, the estimate is refined to its final refined value as follow:

$$X_{refined,k} = X_{unrefined,k} + H_k^{-1} S_{at}\left[\left|z_{unrefined,k} - z_k\right| + \gamma\left|z_{refined,k-1} - z_{k-1}\right|\right] \tag{6}$$

$$z_{refined,k} = H_k X_{refined,k} \tag{7}$$

where

$$S_{at} = \begin{cases} -1 & \frac{z_{unrefined,k}-z_k}{\psi} < -1 \\ \frac{z_{unrefined,k}-z_k}{\psi} & -1 < \frac{z_{unrefined,k}-z_k}{\psi} < 1 \\ 1 & \frac{z_{unrefined,k}-z_k}{\psi} > 1 \end{cases} \tag{8}$$

and ψ is the boundary layer to be tuned to obtain the best results. For simplicity, γ is assumed to have a value of zero.

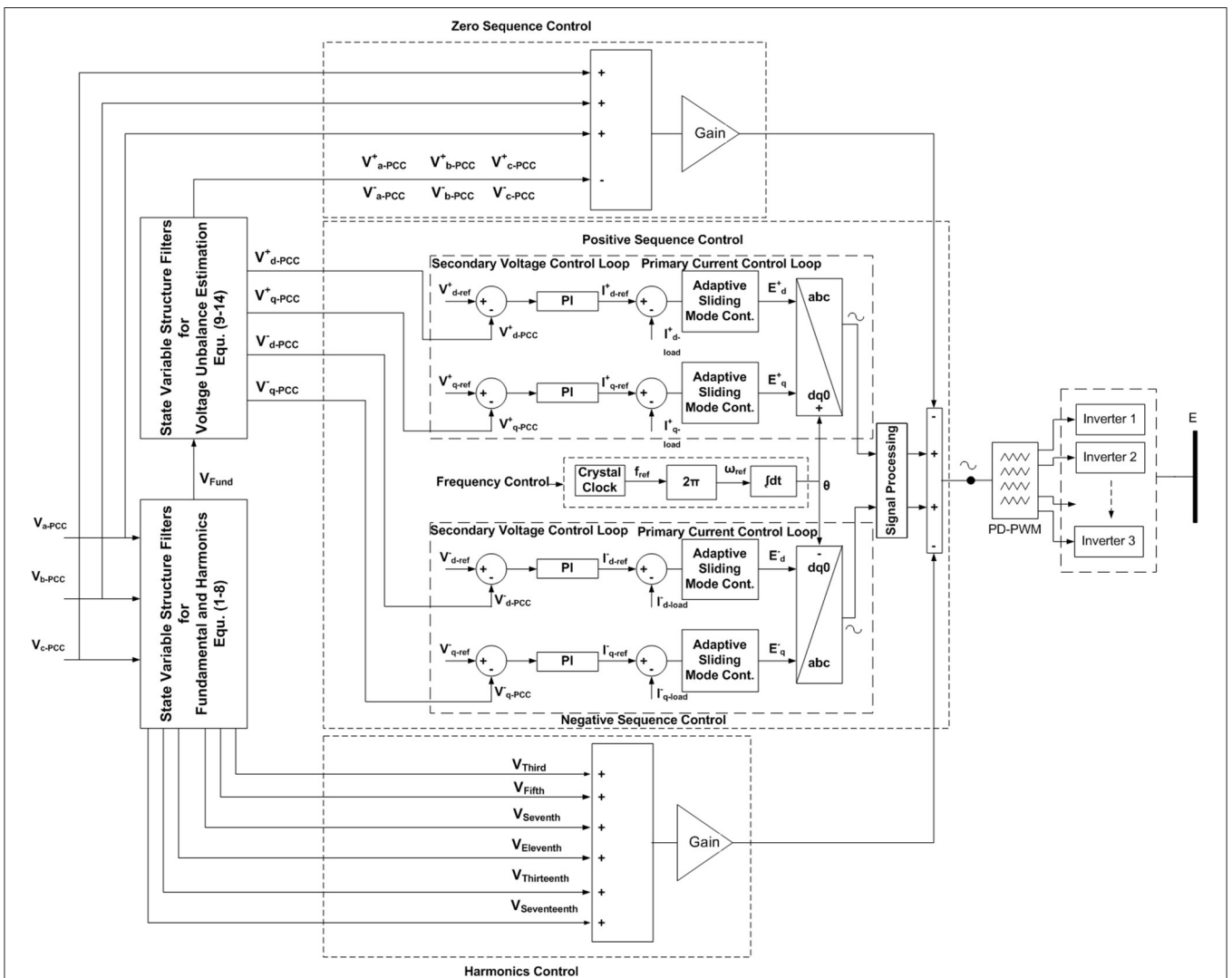

FIGURE 3 | Suggested operational (control) scheme for microgrid.

This proposed filter is simpler than the Kalman filter in three main points

- The formulation using Kalman filter depends on calculating the covariance matrix and updating it continuously. Then, this updated covariance matrix is used to calculate the corrective gain, which is the refined estimate.
- The noise covariance matrices of Kalman filter (Q and R) are not easy to be tuned (Girgis et al., 1991). No information can be obtained for the microgrid noise. Moreover, this noise cannot be assumed as white noise as in Kalman filter, as it includes of voltage and current harmonics.
- Formulation of this proposed filter [as given in (1) and (6–8)] is also easier than the perdition-correction formulation of Kalman filter (Girgis et al., 1991).

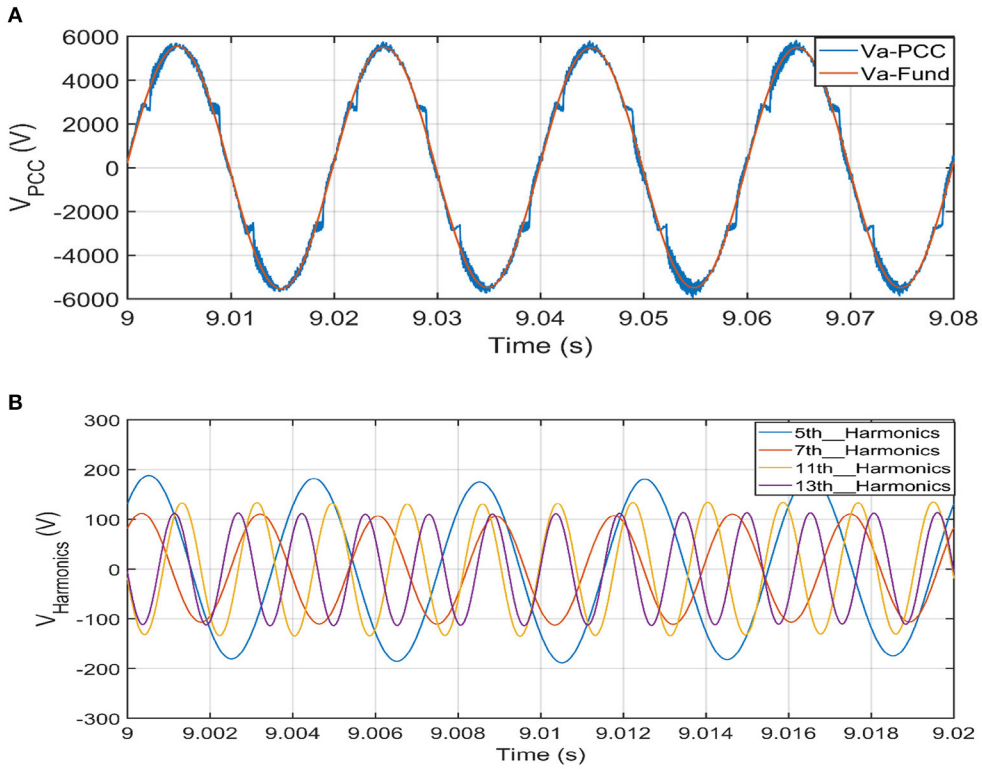

FIGURE 4 | Performance of 1st stage SVSF for fundamental and harmonics voltage at PCC. **(A)** Estimated fundamental voltage with actual voltage. **(B)** Estimated voltage harmonics.

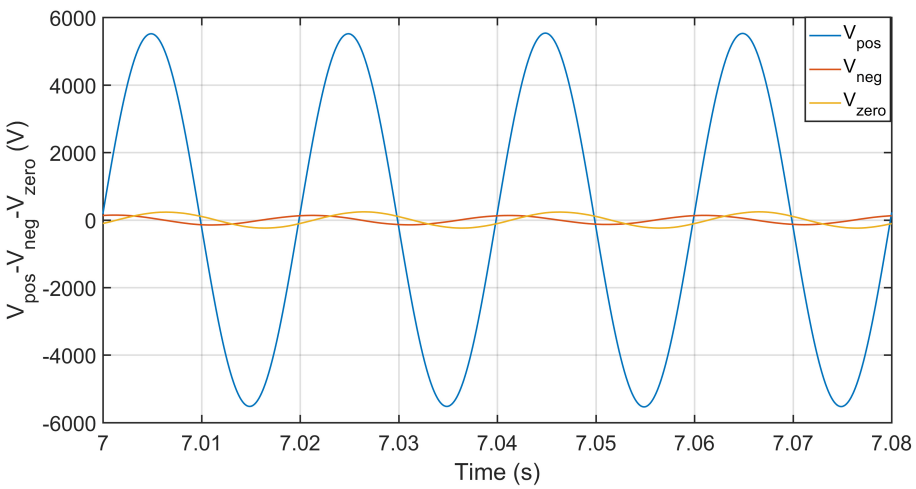

FIGURE 5 | Performance of 2nd stage SVSF for voltage unbalance components at PCC.

After the fundamental voltage and voltage harmonics are estimated using the formulation given in (1–8). This estimated fundamental voltage contains the unbalance components. The same procedure was used to extract the unbalanced voltages. Its formulation is similar to the previous formulation such that the state-space form in (9) for positive and negative-sequence voltages replaces (2), and it is written as,

$$X_{unrefined,k} = \left[A_{50}^{+}\cos\theta_{50}^{+} \quad A_{50}^{+}\sin\theta_{50}^{+} \quad A_{50}^{-}\cos\theta_{50}^{-} \quad A_{50}^{-}\sin\theta_{50}^{-}\right]^{T}, \tag{9}$$

also replacing (3) and (4) with

$$A = I_{4\times 4} \tag{10}$$

$$H_K = \begin{bmatrix} \sin\left(100\pi kT_s\right) & \cos\left(100\pi kT_s\right) & \sin\left(100\pi kT_s\right) & \cos\left(100\pi kT_s\right) \\ \sin\left(100\pi kT_s - \frac{2\pi}{3}\right) & \cos\left(100\pi kT_s - \frac{2\pi}{3}\right) & \sin\left(100\pi kT_s + \frac{2\pi}{3}\right) & \cos\left(100\pi kT_s + \frac{2\pi}{3}\right) \\ \sin\left(100\pi kT_s + \frac{2\pi}{3}\right) & \cos\left(100\pi kT_s + \frac{2\pi}{3}\right) & \sin\left(100\pi kT_s - \frac{2\pi}{3}\right) & \cos\left(100\pi kT_s - \frac{2\pi}{3}\right) \end{bmatrix}, \tag{11}$$

and finally replacing z_k with

$$z_k = [V_a \quad V_b \quad V_c]^T - \frac{V_a + V_b + V_c}{3} \tag{12}$$

The refined estimates are given as follow:

$$X_{refined,k} = X_{unrefined,k} + \frac{1}{3}\begin{pmatrix} H_{1,k}^{-1}S_{at,1}\left[\left|z_{unrefined,1,k} - z_{1,k}\right|\right] \\ +H_{2,k}^{-1}S_{at,2}\left[\left|z_{unrefined,2,k} - z_{2,k}\right|\right] \\ +H_{3,k}^{-1}S_{at,3}\left[\left|z_{unrefined,3,k} - z_{3,k}\right|\right] \end{pmatrix} \tag{13}$$

where $W_{i,k}$ is the *ith* row of the matrix/vector W at time step k. The positive and negative-sequence voltages are then obtained in (14) as,

$$\begin{aligned} \hat{V}_a^{+} &= \left[\sin\left(100\pi kT_s\right) \quad \cos\left(100\pi kT_s\right)\right]\left[A_{50}^{+}\cos\theta_{50}^{+} \quad A_{50}^{+}\sin\theta_{50}^{+}\right]^T \\ \hat{V}_a^{-} &= \left[\sin\left(100\pi kT_s\right) \quad \cos\left(100\pi kT_s\right)\right]\left[A_{50}^{-}\cos\theta_{50}^{-} \quad A_{50}^{-}\sin\theta_{50}^{-}\right]^T \\ \hat{V}_b^{+} &= \left[\sin\left(100\pi kT_s - \tfrac{2\pi}{3}\right) \quad \cos\left(100\pi kT_s - \tfrac{2\pi}{3}\right)\right]\left[A_{50}^{+}\cos\theta_{50}^{+} \quad A_{50}^{+}\sin\theta_{50}^{+}\right]^T \\ \hat{V}_b^{-} &= \left[\sin\left(100\pi kT_s + \tfrac{2\pi}{3}\right) \quad \cos\left(100\pi kT_s + \tfrac{2\pi}{3}\right)\right]\left[A_{50}^{-}\cos\theta_{50}^{-} \quad A_{50}^{-}\sin\theta_{50}^{-}\right]^T \\ \hat{V}_c^{+} &= \left[\sin\left(100\pi kT_s + \tfrac{2\pi}{3}\right) \quad \cos\left(100\pi kT_s + \tfrac{2\pi}{3}\right)\right]\left[A_{50}^{+}\cos\theta_{50}^{+} \quad A_{50}^{+}\sin\theta_{50}^{+}\right]^T \\ \hat{V}_c^{-} &= \left[\sin\left(100\pi kT_s - \tfrac{2\pi}{3}\right) \quad \cos\left(100\pi kT_s - \tfrac{2\pi}{3}\right)\right]\left[A_{50}^{-}\cos\theta_{50}^{-} \quad A_{50}^{-}\sin\theta_{50}^{-}\right]^T \end{aligned} \tag{14}$$

Finally, the previous formulation estimates the voltage harmonics and voltage unbalance in two different stages. The 1st stage [formulation from (1) to (8)] is used to estimate the fundamental voltage and harmonics, while the 2nd stage [formulation (1), (6–8), (9–14)] receives the fundamental voltage from the 1st stage and it produces the voltage unbalance components (positive, negative, and zero-sequence voltages). All these estimated voltage disturbances/components are used in the operational scheme as will explained later.

Adaptive Sliding Mode Control

The adaptive sliding mode control adopted in this paper comprises of two inputs to form its control law. The suggested control law is based on the state-space model of the microgrid depicted in **Figure 1**, this state-space model is deduced and given for the positive sequence components in the d-q rotating frame as,

$$\begin{aligned} E_d &= V_{d-PCC} + RI_{d-loads} - \omega LI_{q-loads} + L\frac{dI_{d-loads}}{dt} \\ E_q &= V_{q-PCC} + RI_{q-loads} + \omega LI_{d-loads} + L\frac{dI_{q-loads}}{dt} \end{aligned} \tag{15}$$

where E is the injected voltage of the inverters, V_{PCC} is the voltage at the loads' side. R and L are the equivalent resistance and inductance of the main feeders inside the microgrid between E bus and V_{PCC} bus. I_{loads} is the equivalent current of loads. The previous equations can be rewritten in a state space form as,

TABLE 2 | Parameters of adaptive SMC.

Adaptive SMC parameters for current loop for positive and negative loops
$\alpha_d = \alpha_q = 0.9$
$k_{1d} = k_{1q} = k_{2d} = k_{2q} = 0.9$
$\beta_d = \beta_q = 20$
$\lambda_{1d} = 1, \lambda_{1q} = 1$
$\lambda_{2d} = 100, \lambda_{2q} = 81$
PI controllers' paramerters for voltage loop for positve and negative loops
$k_{p-d} = 0.282$, $k_{i-d} = 1.333$
$k_{p-q} = 0.423$, $k_{i-q} = 0.111$

TABLE 3 | Parameters of PI controllers.

PI controllers' parameters for current loop for positive loop
$k_{p-d} = k_{p-q} = 1$
$k_{i-d} = k_{i-q} = 18.75$
PI controllers' parameters for current loop for negative loop
$k_{p-d} = k_{p-q} = 0.0625$
$k_{i-d} = k_{i-q} = 6.25$
PI controllers' parameters for voltage loop for positive and negative loops
$k_{p-d} = 0.282$, $k_{i-d} = 1.333$
$k_{p-q} = 0.423$, $k_{i-q} = 0.111$

$$\begin{bmatrix} \frac{d}{dt}I_{d-loads} \\ \frac{d}{dt}I_{q-loads} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega \\ -\omega & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} I_{d-loads} \\ I_{q-loads} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} E_d \\ E_q \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 \\ 0 & -\frac{1}{L} \end{bmatrix} \begin{bmatrix} V_{d-PCC} \\ V_{q-PCC} \end{bmatrix}$$
$$\left[\frac{d}{dt}x\right] = Ax + Bu + Fd \tag{16}$$

Equations (15) and (16) are general and can be used for the positive-sequence and negative-sequence components as well with changing the sign of ω. The suggested control law is expressed as,

$$u = u_{dis} + u_{eq} \tag{17}$$

Each term in (17) represents the required input (injected) voltage by each inverter to the system in order to realize the objective of the control scheme. The u_{dis} is the discrete input that transfers the system's states from a certain sliding manifold (surface) to another, while u_{eq} is the equivalent input that keeps the system's states on a certain sliding manifold. This sliding manifold is innovatively defined by an integral form as,

$$s = \left(\lambda_1 e + \lambda_2 \int e\,dt\right)^{n-1} \tag{18}$$

where n is the number of states, λ_1 and λ_2 are positive constants, and e is the error which is defined as,

$$e = I_{ref} - I_{loads} \tag{19}$$

The u_{eq} is designed such that the system with the sliding mode controller becomes stable, the system stability is justified by Lyapunov stability criterion such that a certain Lyapunov function is selected to express the distance between the system's state and sliding manifold, its definition is written as,

$$V(s) = \frac{1}{2}s^T s \tag{20}$$

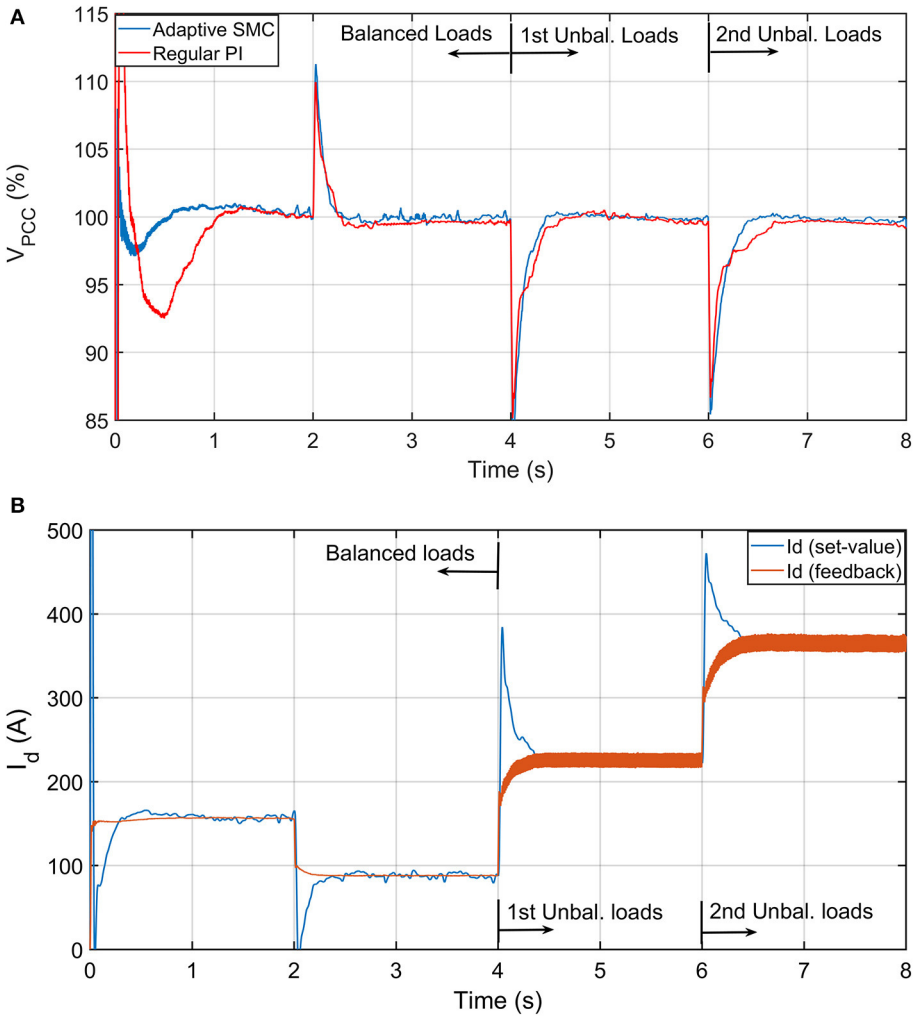

FIGURE 6 | Performance of proposed operational (control) scheme for voltage stability at PCC. **(A)** Performance of adaptive SMC vs. PI controllers for voltage stability. **(B)** Performance of currents in current control loop of d-axis.

The derivative of this function should be less than or equal to zero as,

$$\dot{V}(s) = \frac{dV(s)}{ds}\frac{ds}{dt} = s^T\dot{s} <= 0 \tag{21}$$

For tracking the state variables like the case of this paper $\dot{V}(s) = 0 \rightarrow \dot{s} = 0$, which leads to

$$\begin{aligned} \dot{s} &= \lambda_1\dot{e} + \lambda_2 e = 0 \\ \dot{s} &= \lambda_1(\dot{I}_{ref} - \dot{I}_{loads}) + \lambda_2 e \\ \dot{s} &= -\lambda_1(Ax + Bu_{eq} + Fd) + \lambda_2 e = 0 \end{aligned} \tag{22}$$

Finally, the equivalent input of the control law u_{eq} is given by,

$$u_{eq} = -(\lambda_1 B)^{-1}(Ax + Fd - \lambda_2 e) \tag{23}$$

The matrices (A, B, F) of (23) are obtained from their definition in (16) for positive and negative-sequence components based on the system's parameters of **Table 1**. The discrete input of the control law u_{dis} is deducted from Huang et al. (2008) and defined by its adaptive form for the positive and negative-sequence components as,

$$u_{dis} = \begin{cases} -k_1|s|^\alpha & \rightarrow & s > \beta \\ -s/\beta & \rightarrow & -\beta < s < \beta \\ +k_2|s|^\alpha & \rightarrow & s < -\beta \end{cases} \tag{24}$$

Eventually, the suggested sliding surface in (18) and its control law in (17) along with its two terms in (23) and (24) are employed to control the inverters in such a way to inject a certain voltage, which is used to realize all objectives of the suggested operational/control scheme.

Structure of Operational Scheme

The previous two subsections attribute the contribution of this paper along with the suggested structure of the operational scheme, which is given in **Figure 3**. The operational scheme has two contributory components, which are the estimation for disturbances using SVSF and the adaptive SMC based control scheme to operate the inverters.

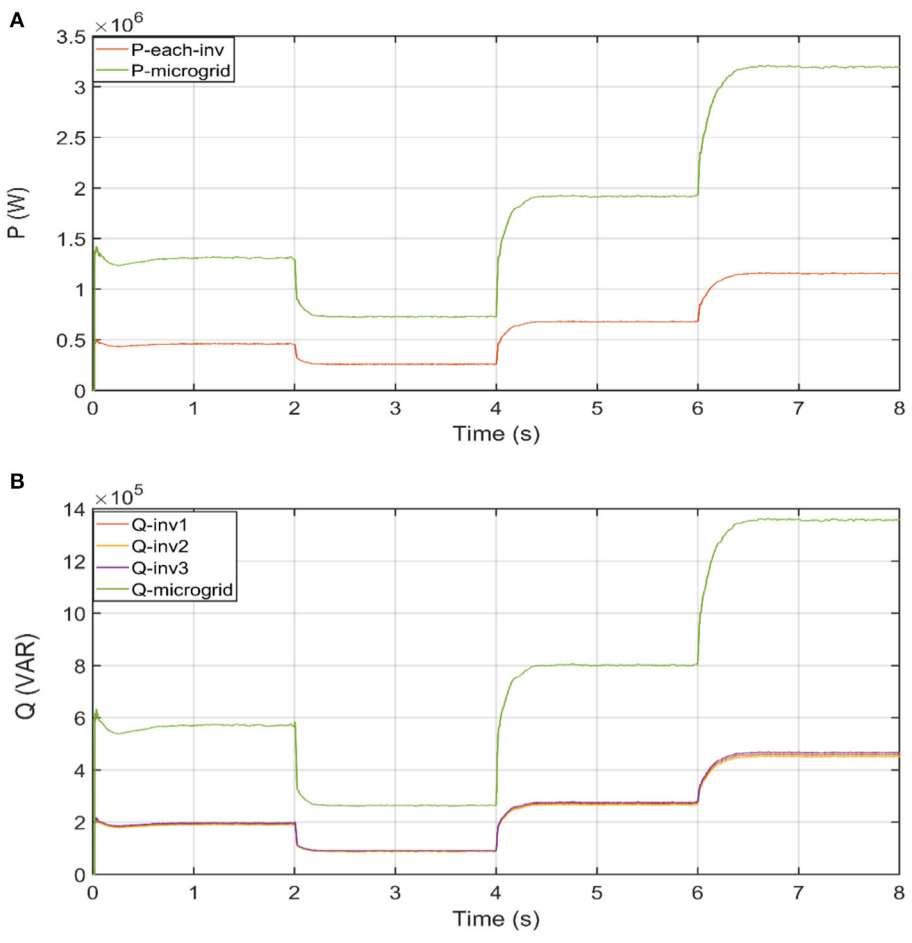

FIGURE 7 | Power sharing among three inverters. **(A)** Active power sharing. **(B)** Reactive power sharing.

The objective of the estimation tool, SVSF, along with the developed state-space models is to estimate/extract voltage harmonics (1–8) and voltage unbalance (9–14), which are used to get the feedback voltages in the operational scheme of **Figure 3**. The positive-sequence voltage represents the dominant voltage in the microgrid, while the negative-sequence voltage represents the most common disturbance in the microgrid. Therefore, these two loops are controlled using cascaded structure of voltage and current control loops. The voltage control loop receives the required voltages (set values) based on the values given in **Table 1**, and it produces current references to the current control loop. The current control loop is the corner stone in this control scheme because it deals with non-linear systems (inverters along with switching modulation and the grid). Thus, its controller should provide adaptive and fast characteristics toward any change in loads. The adopted controller in the voltage loop is the PI controller and the utilized controller in the current loop is the adaptive SMC. Both harmonics mitigation and unbalance compensation are realized after the extraction of their disturbances using the two estimation blocks depicted in **Figure 3**, and then these disturbances are processed to generate corresponding control signals. Consequently, these control signal are augmented to operate the PD-PWM and inject particular voltages as illustrated in **Figure 3**. Finally, these voltages are employed to cancel voltage unbalance and harmonics at the PCC. The frequency of the generated voltage by inverters in the microgrid is constant because the frequency of the control signal, used to drive the PD-PWM and generate the injected voltage, is obtained from a constant crystal clock (fixed frequency source) as depicted in **Figure 3**. More importantly, the frequency of this control signal within the switching modulation (PD-PWM) does not change with any load changes. Thus, the frequency of the injected voltage does not change with any load change accordingly. This point is considered as a great advantage compared to the conventional droop control schemes, at which both the frequency and magnitude of the injected voltage change with any variation in loads (Huang et al., 2011; Canizares and Palma-Behnke, 2014; Sen and Kumar, 2018). These voltage changes should be corrected at the secondary control level within the droop schemes. This voltage correction adds more complexity to the employed control scheme.

SIMULATION RESULTS

This section is divided into several subsections. The first subsection illustrates the performance of the SVSF for estimation of the voltage harmonics and unbalance. The second subsection displays the performance of the presented controller. The last section shows the performance of the whole operational scheme. All results of coming subsections are obtained when the microgrid has several loads (referred to primary side of Tr_4), changing as follows:

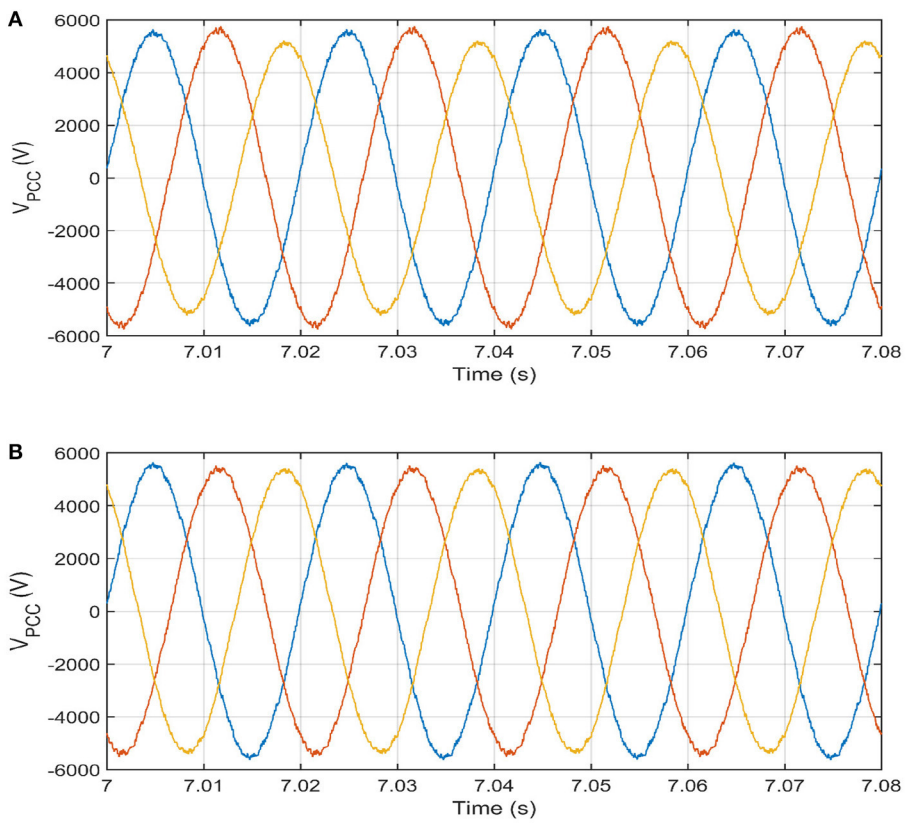

FIGURE 8 | Voltage waveforms before and after the activation for mitigation of voltage unbalance at 2nd unbalanced load (from $t = 6$ s to $t = 8$ s). **(A)** Voltage waveforms at PCC for 2nd unbalanced loads without mitigation. **(B)** Voltage waveforms at PCC for 2nd unbalanced loads with mitigation.

- From $t = 0$ to $t = 2$ s, the 1st balanced three-phase load of $Z_{load1} = 55 + 18.84j$and 2nd balanced three-phase load of $Z_{load2} = 65 + 31.4j$ are connected in parallel in the microgrid.
- From $t = 2$ s to $t = 4$ s, the 2nd load $Z_{load1}$is disconnected.
- From $t = 4$ to $t = 6$ s, the 1st unbalanced three-phase load is connected to the microgrid with the values of $Z_{1-ph-a} = 25 + 6.28j$, $Z_{1-ph-b} = 50 + 31.4j$, $Z_{1-ph-c} = 35 + 15.7j$.
- From $t = 6$ s to $t = 8$ s, the 2nd unbalanced three-phase load is connected to the microgrid with the values of $Z_{2-ph-a} = 30 + 9.42j$, $Z_{2-ph-b} = 33 + 11j$, $Z_{2-ph-c} = 45 + 14.13j$.
- From t = 8 s to t = 10 s, a non-linear load of full rectifier circuit with an inductive load is connected to the microgrid with $R = 100\,\Omega$, $H = 50\,mH$.

Performance of SVSF

The formulation of the SVSF along with the harmonics state-space equations presented before is used to estimate the fundamental voltage and voltage harmonics (1st stage estimation); then, the estimated three-phase fundamental voltages are applied on another SVSF to estimate the positive, negative, and zero-sequence voltages (2nd stage estimation). The instantaneous estimation performance of the 1st stage SVSF for the fundamental and some voltage harmonics is given in **Figures 4A,B** for fundamental voltage and voltage harmonics, respectively. The instantaneous estimated fundamental voltage is displayed with the actual distorted voltage at the PCC for one phase. The voltage harmonics in **Figure 4B** are estimated using the SVSF with the state-space formulation presented in section Smooth variable structure filter. The performance of the 2nd stage SVSF is depicted in **Figure 5**, where it shows the instantaneous estimation of the voltage unbalance components for the 2nd unbalanced loads.

Performance of Adaptive Sliding Mode Controller

The performance of control scheme is displayed in this subsection. The development of the adopted controller is described in section Adaptive sliding mode control. The controller parameters for both loops are given in **Table 2**. This presented controller is compared with regular PI controllers to prove its meritorious performance. Simply, these PI controllers are replaced the adaptive SMC in the scheme of **Figure 3**. The parameters of the PI controllers for their best performance are tuned by the empirical modified Ziegler-Nichols method, and they are listed in **Table 3**.

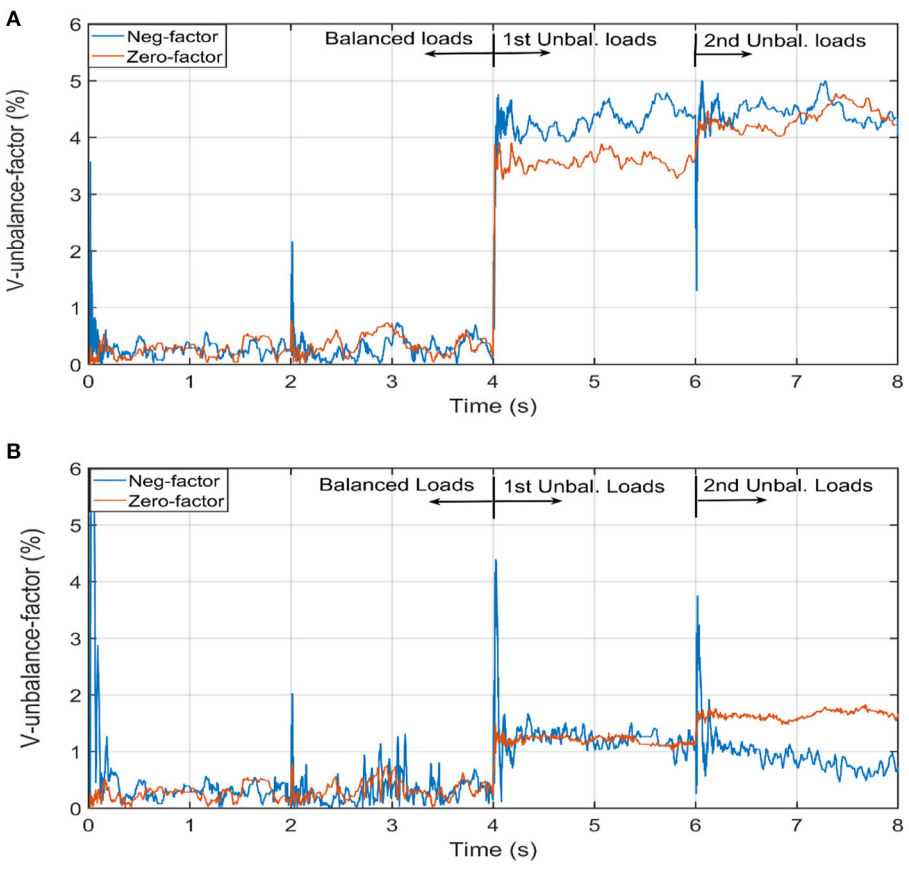

FIGURE 9 | Voltage unbalance factors before and after the activation of unbalance control. **(A)** Voltage unbalance factor without activation of unbalance control. **(B)** Voltage unbalance factor with activation of unbalance control.

The performance of the adaptive SMC is depicted in **Figure 6A**, where it shows its performance with that of the regular PI controllers whose parameters are tuned using Ziegler-Nichols method. The good performance of the voltage stability at the PCC emanates from the control action in the current loops. The current reference and its feedback for the direct axis current control (just as an example) are depicted in **Figure 6B**.

Performance of Operational Scheme

The suggested operational scheme belongs to the central control category and its output is applied to all inverters at the same time (Huang et al., 2011; Canizares and Palma-Behnke, 2014; Rajesh et al., 2017; Sen and Kumar, 2018). This concept brings some important advantages which are

- The power/current is equally divided among working inverters.
- The difference in feeder impedance does not badly influence its operation.
- Its simplicity compared to the droop scheme presented in Huang et al. (2011), Vandoorn et al. (2013), Canizares and Palma-Behnke (2014), Han et al. (2016a), and Sen and Kumar (2018).

Power Sharing Among Inverters in Microgrid

One major advantage of this control scheme is its central structure. Meaning, the output control signals are applied on all inverters at the same time, which yields equal power sharing among the working inverters. Even if one inverter is lost for any reason, the other working inverters share the whole load power. The power of each inverter vs. the total load power is given in **Figure 7**, which shows equal power (active and reactive) for all three inverters. In **Figure 7B**, the reactive power of each inverter is close to the reactive power of other inverters; consequently, they look above each other.

Voltage Unbalance Mitigation in Microgrid

The mitigation of the voltage unbalance starts with the extraction of the unbalance components (positive, negative, and zero-sequence voltages), this extraction process is conducted

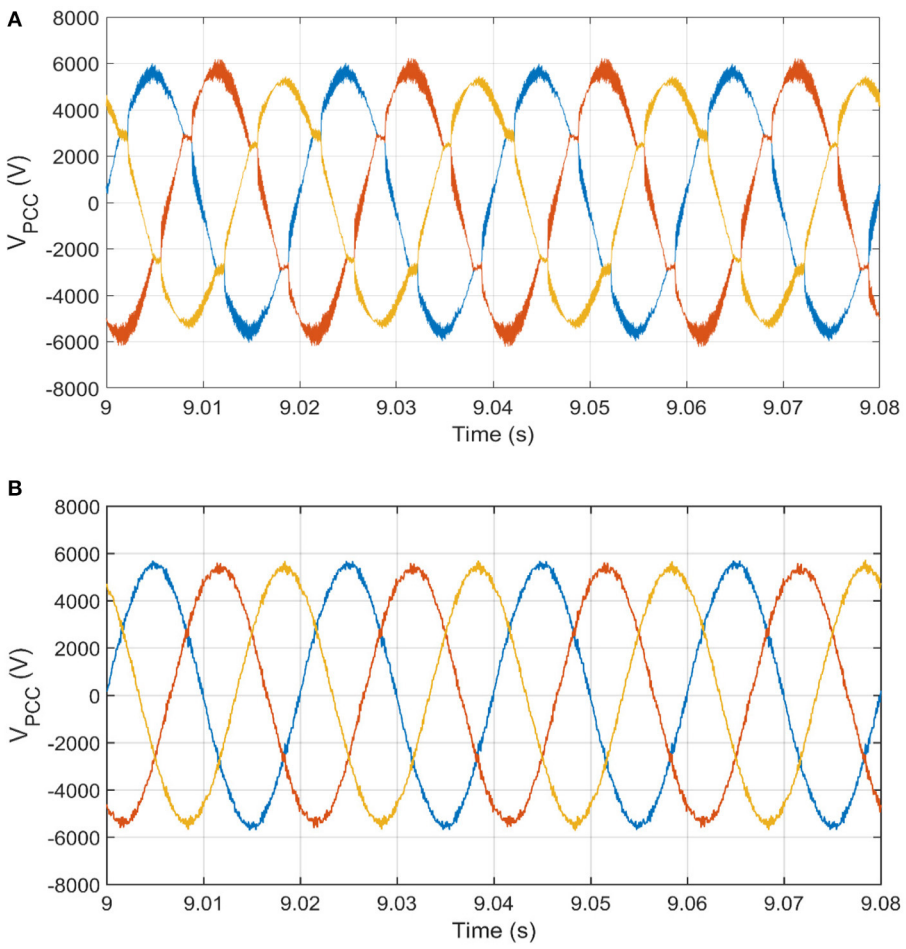

FIGURE 10 | Voltage waveforms at PCC before and after the activation of unbalance and harmonics control. **(A)** Voltage waveform at PCC distorted by harmonics and unbalance. **(B)** Voltage waveform at PCC with mitigation of harmonics and unbalance.

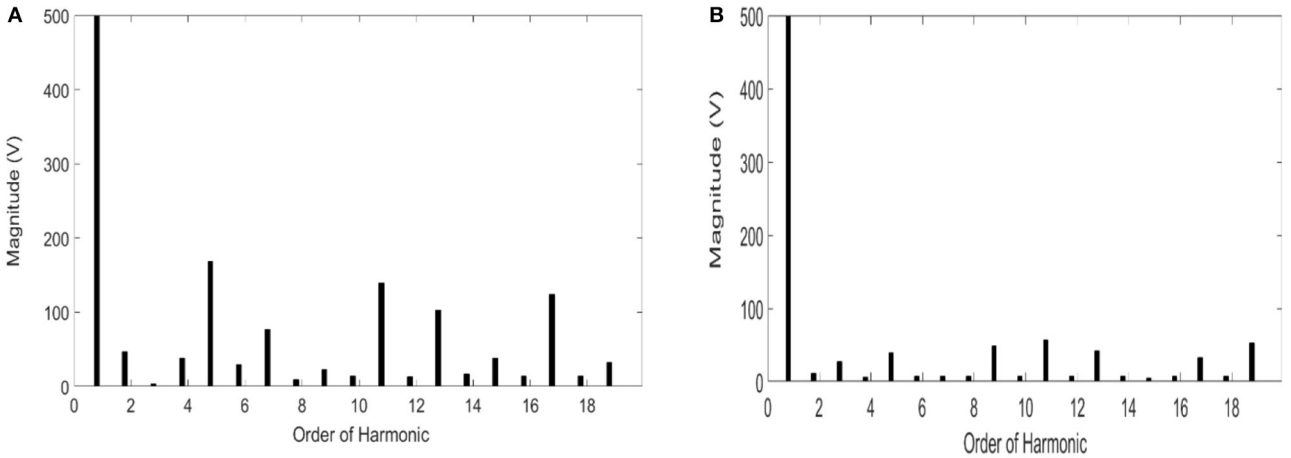

FIGURE 11 | Harmonic spectrum before and after the activation of harmonics control. **(A)** Harmonic spectrum before activation of harmonics loop. **(B)** Harmonic spectrum after activation of harmonics loop.

continuously through the state variable structure filters block for voltage unbalance in **Figure 3**. The output of this block is minimal and neglected in case the loads are balanced. If the loads are unbalanced, then the unbalance components are considerable, and these components are extracted, processed, and mitigated as will be illustrated in **Figures 8**, **9**. The three-phase unbalanced voltages are shown in **Figure 8A**. Their estimated voltage unbalance components are already given in **Figure 5**. These voltages are processed by the scheme of **Figure 3** to generate a voltage reference. The three-phase voltages with the mitigation of the negative-sequence and zero-sequence components are apparent in **Figure 8B**. The efficiency of the mitigation for voltage unbalance is justified by the negative and zero unbalance factor (defined in IEEE Std. 1159–1995) as,

$$UVF^{+} = \frac{V^{+}_{estimated}}{typical\ value},\ UVF^{-} = \frac{V^{-}_{estimated}}{V^{+}_{estimated}},$$
$$UVF^{0} = \frac{V^{0}_{estimated}}{V^{+}_{estimated}} \tag{25}$$

The efficiency of the voltage waveforms given in **Figure 8** is affirmed by the negative- and zero-unbalance factor without and with the activation of the negative-voltage control loop and zero-voltage loop. These negative- and zero-unbalance factors are shown in **Figures 9A,B**, respectively. With the activation of the unbalance loop, the negative- and zero-unbalance factors (UVF^{-}, UVF^{0}) are less 2% as stipulated in IEEE Std. 1159–1995.

Voltage Harmonics Mitigation in Microgrid

Starting from $t = 8$ s, the non-linear load is connected to the microgrid, which injects current harmonics such as 3rd, 5th, 7th, 11th, 13th, … etc. In this research, these harmonics are estimated through the formulation given in section Smooth variable structure filter. The three-phase voltages at the PCC without and with the activation of the harmonics loop is depicted in **Figures 10A,B**, respectively. The efficiency of harmonics mitigation is affirmed by the total harmonic distortion and harmonic spectrum. The harmonic spectrum without and with the activation of the harmonic mitigation loop is illustrated in **Figures 11A,B**, respectively. The harmonic spectrum reflects the THD at the PCC, which is transferred from 9 to 3%.

The good performance for stabilizing the voltage and power sharing at loads side is verified by the preceding simulation results. For the real time implementation, it is expected to have a slight difference in results for equal power sharing because identical inverters along with their operation cannot be practically guaranteed, which may lead to unequal power generation among the inverters and a small circulating current due to a small difference in the generated voltage by each inverter.

CONCLUSION

This paper presents an effective operational/control scheme, which is able to achieve some objectives in the microgrid. These multiple objectives of the operational scheme have been realized because the proposed scheme has two main contributory components. The 1st component is the newly developed SVSF, which is used to estimate all voltage disturbances under study in this paper. The 2nd component is the adaptive SMC along with its integral sliding surface, which gives a seamless transient and steady-space performance for the injected voltage/power of inverters. The integration of the SVSF and adaptive SMC enables the operational scheme to give the optimum required voltage/power performance at the loads. The voltage is stabilized at the PCC to 1 pu for any loading condition. In addition, the unbalance factors (negative and zero-sequence voltages) at the PCC become <2%, and voltage harmonics (3rd, 5th, 7th, 11th, 13th, 17th) at the PCC are smaller than 5%. More importantly, the loads' power is equally shared among the working inverters.

DATA AVAILABILITY STATEMENT

All datasets generated for this study are included in the article/supplementary material.

AUTHOR CONTRIBUTIONS

AE has contributed to everything in the paper including idea under study in the paper, the modeling of the system under study, mathematical equation development, simulation results, analysis of the results, and finally editing and proofreading the whole paper. MA-S has contributed to modeling of the system under study, mathematical equation development, simulation results, analysis of the results, and finally editing the whole paper. AA has contributed to modeling of the system under study, mathematical equation development, reviewing the whole paper, and editing and proofreading.

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Improvement of Power Quality in a Three-Phase System Using an Adaline-Based Multilevel Inverter

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The existence of harmonics in the power distribution system (PDS) is treated as the most serious issue that affects its stability and reliability. The active power filter (APF) therefore plays a vital role in PDS to compensate for the harmonics for the improvement of the power quality (PQ) and to keep the total harmonic distortion (THD) below 5% as per IEEE-519. In this work, a three-phase four-wire (3P-4W) multi-level inverter (MLI)-based APF is proposed to overcome the shoot-through effect (STE) and reduce the distortions in the supply current. The control of the voltage source inverter (VSI) is achieved using an Adaline-based LMS (A-LMS) algorithm with a hysteresis current controller. The proposed filter that uses the A-LMS technique is compared with the conventional recursive least square (RLS) algorithm. The A-LMS approach is mainly operated for maintaining the dc link voltage of MLI, which follows the principle of capacitor energy and reduces the total harmonic distortion (THD) under different load variations. The performance of MLI under different load conditions is designed, developed, and validated by using a MATLAB/Simulink environment, and the preeminent features are established.

Keywords: Adaline-based LMS, multi-level inverter, recursive least square, total harmonic distortion, power quality

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INTRODUCTION

In the era of modern power systems, it is quite a promising task to reduce the harmonics in the PDS. The harmonics are generally caused due to the usage of a non-linear load. Therefore, amongst the probable solutions in recent years, it is observed that multi-level inverter (MLI)- (Siddique et al., 2019a,b) based APF has the capability to control and regulate the electrical disturbances and improvise the PQ by injecting the compensating current (Babu et al., 2015) to the PDS. MLIs are widely used in various areas like HVDC systems (Xu et al., 2014), battery energy storage systems (Soong and Lehn, 2014), as well as wind (Gangui et al., 2012) and solar energy systems (Yousri et al., 2019). Significant developments linked with the circuit topology (Siddique et al., 2019c) and control techniques of the MLI have been noticed in recent days. Recent studies have demonstrated the importance of the MLI, which delivers an ideal functionality for high and medium voltage systems (Ali and Krishnaswamy, 2018). With the use of an MLI, the compensations in current harmonics are very effective in improving the PQ. An MLI can provide improved PQ by operating the power semiconductor devices at a frequency near to the fundamental (Rodriguez et al., 2002). Of course, for low-power applications, the switching frequencies of the switching devices are not restricted, but, at its lower value, the efficiency of the converter increases (Ozdemir et al., 2008). An MLI

TABLE 1 | Comparative analysis between Conventional Inverter and proposed MLI.

Issues	Conventional Inverter	Proposed MLI
Shoot-through phenomenon	Available	Removed
Reliability	Less	More
Switch stress (voltage and current)	High	Low
Switching circuit cost	More	Less

also offers advantages, such as the possibility of direct interfacing to the medium voltage system without using a coupling transformer, the production of output voltages with lower distortions, having high power conversion characteristics, and providing a high equivalent switching frequency effect at rather lower values.

Different configurations of MLIs have been discussed so far in this area. In Rodriguez et al. (2009) and Pratheesh et al. (2017), the neutral clamped MLI is discussed where the authors presented the modulation and control techniques with special attention to the distribution losses. In Zhang et al. (2013) and Lei et al. (2017), the authors have discussed the function of the flying capacitors for harmonics and unbalanced current compensation. In Karasani et al. (2016), and Gupta et al. (2015), the performance of the cascaded MLI (CMLI) has been analyzed. Among the available MLI topologies, the CMLI is extensively used; it provides a modular design and can be directly linked to the grid at PCC instead of using a transformer (Ertl et al., 2002). Moreover, it provides power semiconductors with a lower rating compared to the standard two-level configurations, thereby improving the reliability under faulty situations. The MLI is given higher preference over other switching topologies because the MLI achieves the output of equal voltage by using fewer switching devices.

In this paper, a 3P-4W H-bridge interleaved buck-type active power filter (HILBAPF) (Panda and Patel, 2014) is implemented. HILBAPF has been developed to overcome the problems incurred by the conventional MLI in balancing the capacitor voltages and to exclude the interfacing transformer. Also, the conventional MLIs are not capable of managing faults and fault ride-throughs. Another major factor of the MLI is reliability, which decreases by means of STE. The supply voltages, with an unbalanced and non-sinusoidal supply, combined with the existence of negative and zero sequence components in the supply source, results in huge losses and excessive temperature increases in the PDS. Therefore, compensating for the zero sequence components in the neutral wire has become a primary task in the improvement of the PQ. A comparative analysis between conventional inverter and proposed MLI is provided in **Table 1**.

Various control techniques have been used so far in this area to accomplish the compensation task, which comprises the instantaneous power theory (*p-q*) (Hachani et al., 2017), the synchronous reference frame (SRF) theory (Hoon et al., 2016), the discrete Fourier transform approach (Wang et al., 2016), and the deadbeat controller (Qi et al., 2017). However, adaptive filters (Chilipi et al., 2016) play an important role in compensating for the harmonics by injecting the required current to the power grid. Traditionally, a recursive least square (RLS) (Das et al., 2017) is employed, which offers improved performance, simplicity, robustness, and a lower computational burden. However, they are still altered due to factors like a slow convergence rate, longer iteration rate, and large storage capacity. These issues thus sort out use the Adaline approach (Subudhi et al., 2012). The Adaline approach is the most commonly used artificial neural network (ANN) technique to extract the fundamental and/or harmonic components. ANN has been projected as an attractive estimation and regression technique due to its parallel computing nature and high learning capability.

Moreover, the A-LMS is very simple and produces fewer computational problems. It offers natural linearity and the methodology is fast. In this study, therefore, an A-LMS (Merabet et al., 2017) approach in the MLI for calculating the reference current extractions is presented. The proposed approach provides improved robustness, speed, and efficiency along with a lower switching frequency or lower current ripple as compared to standard two-level topologies. Moreover, it produces a sinusoidal component from a non-linear supply voltage. The performance is realized using a Matlab/Simulink and compared with the conventional RLS to check the effectiveness of the proposed system.

The main idea in this work is to design a power system model with an MLI for compensating for the current harmonics and reactive power compensation by supplying a compensating current and reducing the THD percentage below 5% as per IEEE standard. The proposed system is tested under balanced and unbalanced load cases. The reference source current extraction is realized using an A-LMS. The A-LMS extracts the current in a simpler way with a shorter period of execution. The A-LMS algorithm is very dynamic for severe load variations. The proposed method improves the effective dynamic performance of the MLI for compensating for load currents with a reduced computational burden. The proposed technique is easily realized on digital processors and performs the fewest number of calculations.

The paper is arranged into several sections. Section System Configuration provides detail explanations of 3-phase, 4-wire HILBAPF, section Control Methodology provides proposed Adaline techniques, section Results and Discussion provides the result analysis for PQ improvement, and section Conclusions provides the conclusion.

SYSTEM CONFIGURATION

To obtain the fundamental supply current, the MLI must inject or absorb a compensating filter current. The compensated current must be the same and be in phase opposition to the harmonic components. The 3P-4W with HILBAPF is shown in **Figure 1**. The proposed model is designed especially for high voltage, medium-to-high power applications with an objective to end shoot-through problems. It consists of three single-phase H-bridge inverters. The advantage of this topology is that the voltage

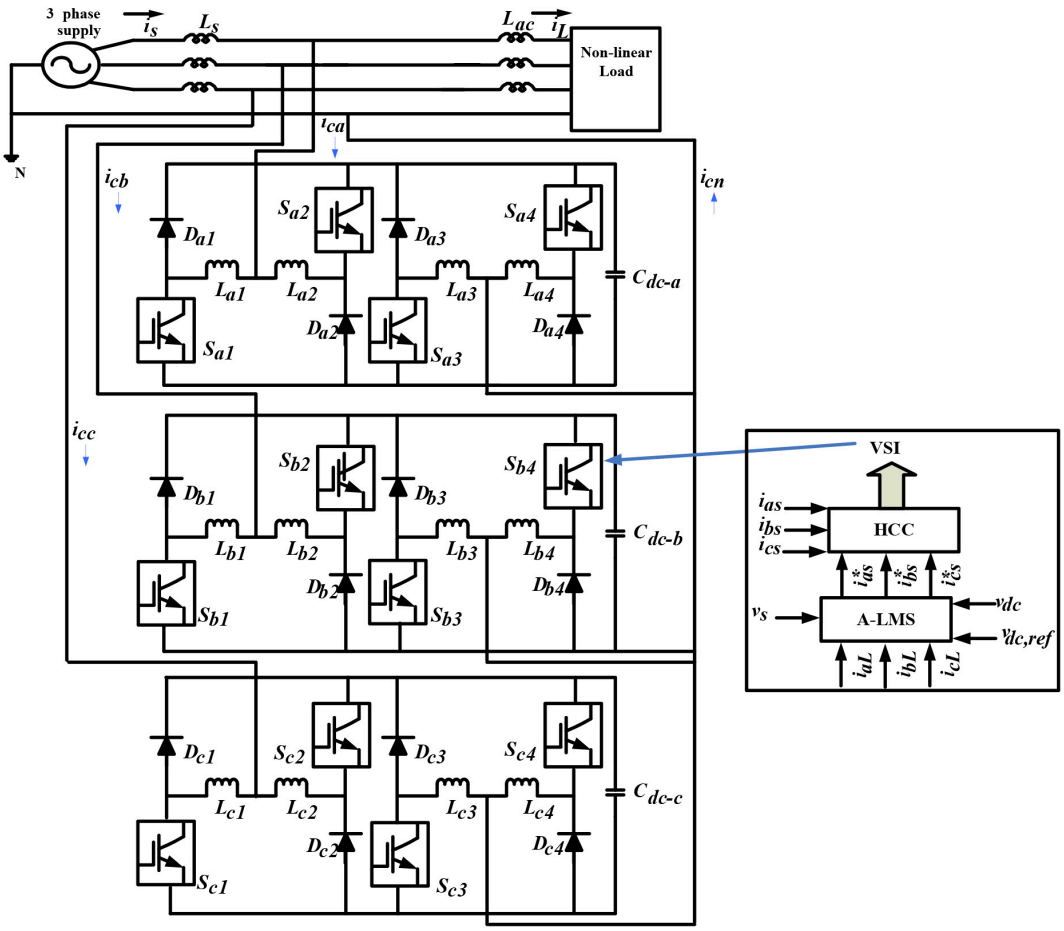

FIGURE 1 | Proposed system configuration.

across in each H-bridge interleaved buck inverter appears at the single phase voltage only, and hence the dc link reference voltage required is decreased by $\sqrt{3}$ times as compared to the other conventional MLI. The proposed topology requires only one dc link capacitor voltage out of the three individual phases for reference current generation, and this consequently reduces the voltage regulation complexness.

For the 3P-4W HILBAPF, the following mathematical equations are presented:

$$\begin{aligned} i_{s(a+b+c)} &= i_{sn} \\ i_{L(a+b+c)} &= i_{Ln} \\ i_{comp(a+b+c)} &= i_{compn} \end{aligned} \tag{1}$$

where, $i_{s(a+b+c)}$, $i_{L(a+b+c)}$, and $i_{comp(a+b+c)}$ represent the corresponding source, load, and compensating current of phase a, b, and c, respectively, while, i_{sn}, i_{Ln} and i_{compn} represent the corresponding neutral supply, load, and compensating currents. Now, in HILBAPF, the compensating current can be presented as the sum of the two coupling inductors current for individual phases:

$$\begin{aligned} i_{compa} &= i_{La1} + i_{La2} = -i_{La3} - i_{La4} \\ i_{compb} &= i_{Lb1} + i_{Lb2} = -i_{Lb3} - i_{Lb4} \\ i_{compc} &= i_{Lc1} + i_{Lc2} = -i_{Lc3} - i_{Lc4} \end{aligned} \tag{2}$$

The dc-side capacitance (C_{dc}) of HILBAPF is given as:

$$0.5 * C_{dc} * \left[\left(V_{dc}^2 - V_{dc\,\min}^2\right)\right] = V_s(t) * I * \Delta t \tag{3}$$

where, C_{dc}, V_{dc}, $V_{dc\,\min}$, I, $V_s(t)$, and Δt are, respectively, the capacitance of the DC-bus, voltage across the DC-side, minimum dc-bus voltage level, phase current, phase voltage, and change of time where the DC-bus voltage is to be improved. The control strategies of VSI using A-LMS are discussed in subsequent sub-sections.

CONTROL METHODOLOGY

To obtain the fundamental supply current, the APF must inject or absorb a compensating filter current. The compensated

current must be the same and be in phase opposition to the harmonic components. The 3P-4W MLI is shown in **Figure 1**. The performance of the 3P-4W MLI depends on the control strategy designed. In this paper for improving the reliability of the proposed system, two different control strategies, the RLS and A-LMS techniques, are used for controlling the VSI of 3P-4W MLI. The details of the controlling techniques are discussed in subsequent sub-sections.

RLS Algorithm

The RLS approach, with its simple structure and robust performance, is extensively implemented in many applications. The RLS technique is very simple; it reduces noise and automatically adjusts parameters. During the steady state, the active power offered by the power system is equal to the active power required by the load, and there is therefore no active current that flows through the MLI. Furthermore, the DC-link voltage is fixed, and its waveform has six ripples. Therefore, if the transient state occurs due to the load variation, the DC-link capacitor will provide the active power variance between the supply system and load, which may in turn produce a fluctuation in the DC link. In order to sustain a fixed DC-bus voltage and weaken the six ripples in the waveform, the MLI employs an RLS filter to get a DC-bus active parameter (A_{dcx}) for each phase.

In this approach for obtaining the compensation current generation, the RLS filter is used in the MLI such that the dc link active current parameter (A_{dcx}) is obtained with a constant dc link voltage and so that it can be ripple free in the waveform. **Figure 2** provides the functioning of the RLS algorithm, where V_{ref} references the dc link voltage, and $V_{dc}\,(i)$ references the dc link voltage, having an instantaneous sampling value. To sustain the dc link, the instantaneous active power required to maintain the DC-link voltage (P_{dc})is specified as

$$P_{dc}(i) = \left[\left(V_{ref} + y(i)\right)^2 - V^2{}_{ref}\right] * C/2 \tag{4}$$

where, C, termed as the DC-bus capacitor, and A_{dcx} can be obtained as

$$A_{dcx} = P_{dc}(i)/V^2{}_x \tag{5}$$

The final A_x, i.e., the active parameter, is obtained as

$$A_x = A_{ax} + A_{dcx} \tag{6}$$

For each phase, the instantaneous current is given as

$$i_x(t) = i_{ax}(t) + i_{nx}(t) \tag{7}$$

where,

$$i_{nx}(t) = i_{rx}(t) + i_{hx}(t) \tag{8}$$

In a grid voltage, harmonics do not exist, and therefore instantaneous voltage is expressed as

$$V_x(t) = V_{ax}(t) \tag{9}$$

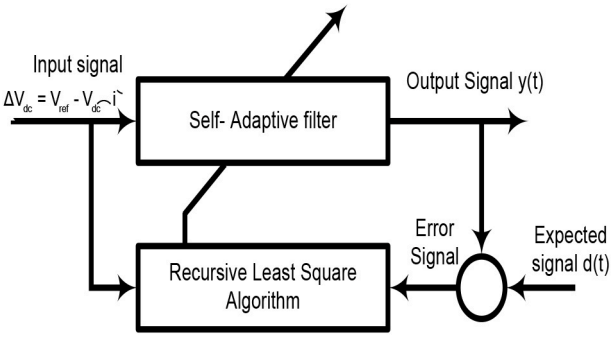

FIGURE 2 | Flow chart of RLS filter.

For each phase, the reference active current is expressed as

$$i_{ax}(t) = A_x V_x(t) \tag{10}$$

The instantaneous reference compensation current is identified as

$$i(t) = i_x(t) - i_{ax}(t) \tag{11}$$

Therefore, for the distortion limit, the reference compensating current is injected into the power system.

A-LMS Algorithm

This algorithm is a combined technique between the Adaline and LMS algorithm. The weights in Adaline are basically updated using the LMS algorithm. Due to its simple structure and robust nature, the A-LMS algorithm is widely implemented in signal processing and control system application. The proposed technique is used to calculate the reference current components for the MLI. The convergence rate of the LMS algorithm depends on the fixed step-size parameter. The A-LMS offers several advantages, such as a simple structure, and it can be realized easily in practical applications. The results of frequency tracking, especially harmonics detection, demonstrate that the A-LMS algorithm can be utilized effectively in analyzing the PQ issues. The learning capacity of the ANN supports online adaptation to any variation in electrical parameters. Each neuron in ANN is treated as an elementary neuron. Each neuron collects a number of input variables from upstream neurons. Each input is assigned with a weight "w" representative of the strength of the connection. The output of the neuron acts on the activation function of the weighted sum inputs. **Figure 3** illustrates the configuration of the Adaline neural network.

The Adaline output can be computed as per Equation (12):

$$Y = \sum x(i)w(i) = x^T w \tag{12}$$

where x and w (w_0, $w_1 \ldots w_n$) are the input and weight vector, respectively, with n being the dimension, and Y being the estimated output.

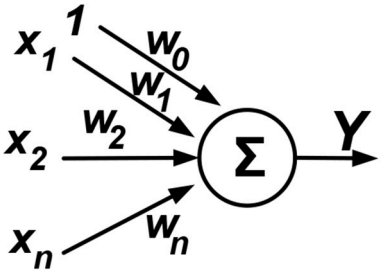

FIGURE 3 | Basic architecture of Adaline neural network.

Weight Value Estimation Using the A-LMS Algorithm

The A-LMS technique is designed for the extraction of the real fundamental frequency component of the load current. For maintaining a fixed DC-bus voltage, a PI controller is employed in which the DC-bus voltage is compared with its reference value.

Considering a three-phase system where the source voltage is sinusoidal and it is expressed as

$$v_s = v_m \sin wt \tag{13}$$

and the current in the non-linear load is given as

$$i_L = I_1 \sin(wt + \phi_1) + \sum_{n=2}^{\infty} I_n \sin(nwt + \phi_n) \tag{14}$$

Equation (14) can be represented as

$$i_L = i_{lp}^{+} + i_{lq}^{+} + i_{lh}^{-} \tag{15}$$

where, i_{lp}^{+}, i_{lq}^{+}, and i_{lh}^{-} are the positive sequence active load current, positive sequence reactive load current, and negative sequence load current (harmonic components), respectively.

In a single phase the current active component (i_p), is expressed as

$$i_p = w_m u_s \tag{16}$$

The unit vector is denoted as u_s, and w_m is denoted as the calculated weight of the A-LMS.

Therefore, the iterated weight is given as

$$w_{m(k+1)} = w_{m(k)} + \mu \left[i_{lk} - w_{m(k)} u_{s(k)} \right] u_{s(k)} \tag{17}$$

where μ is termed as the convergence coefficient.

$$w_m^{+} = \frac{\left(w_{ma}^{+} + w_{mb}^{+} + w_{mc}^{+}\right)}{3} \tag{18}$$

DC Link Voltage Control

The error across the DC-bus is given as

$$v_{dc(n)}^{*} - v_{dc(n)} = \Delta v_{dc(n)} \tag{19}$$

where the output from PI is expressed as

$$I_{sm(n)} = I_{sm(n-1)} + I_{P1} \tag{20}$$

and where, $I_{P1} = k_{pdc}\left[\Delta v_{dc(n)} - \Delta v_{dc(n-1)}\right] + k_{idc}\Delta v_{dc(n)}$ as well as k_{pdc} and k_{idc} are the proportional and integral gain of the controller, respectively.

Generation of Reference Source Currents

The three-phase source reference currents are expressed as

$$i_{sa}^{*} = \left(w_m^{+} + I_{sm}\right) u_{sa} \tag{21}$$

$$i_{sb}^{*} = \left(w_m^{+} + I_{sm}\right) u_{sb} \tag{22}$$

$$i_{sc}^{*} = \left(w_m^{+} + I_{sm}\right) u_{sc} \tag{23}$$

where, i_{sa}^{*}, i_{sb}^{*}, and i_{sc}^{*} are considered as reference source currents. These currents are compared with detected source currents, and their resultant output is supplied to the HCC (hysteresis current controller) for gating signal generation. The detailed algorithm is shown in **Figure 4**. The proposed technique needs less computational workout. Moreover, this technique instantaneously compensates for the source currents, which is not easy in the case of conventional techniques. The weights are computed online using the LMS algorithm. The weights are averaged not for the purpose of averaging at a fundamental frequency but for the canceling of the sinusoidal oscillating components in weights, which are available due to load current harmonics. The weight average in each different phase is depicted in **Figure 4**.

The ADALINE receives the PCC voltage and the individual load current, and it generates the individual weight with the reference source current. From the figure, it is clear that, for switching signal generation, the sensed source currents are subtracted from the reference source currents, and then the individual source current errors are supplied to the HCC.

RESULTS AND DISCUSSION

A power system model in the MATLAB/ SIMUINK and Simpower-System Block set is designed to analyze the function of the proposed controller in the three-phase system using the MLI. The complete system is composed mainly of a three-phase source, a non-linear load (balanced and unbalanced load), the MLI system, and the PI controller with different proposed control strategies.

The performance of the proposed power system model is measured with the conventional RLS technique and the proposed Adaline-LMS technique under balanced and unbalanced loads. The concerned parameters of the system are provided in subsequent subsections.

To investigate the performance of the system, the test is carried out using a three-phase supply source and a non-linear load. The non-linear loads for balanced and unbalanced loads are provided in the **Appendix** section. Due to the presence of harmonics, it is noted that the load current is distorted from the normal sinusoidal current when a non-linear load is connected. The current wave forms of the distorted load currents during an

unbalanced non-linear load are illustrated in **Figure 5A**. From the figure, it can be seen that the distortion with a current dip is found from 0 to 0.05 s. After 0.05 s, the distorted load current is maintained at a rated value up to 0.2 s. The THD value found during the unbalanced load is around 38.97%, which is illustrated in **Figure 5B**. Now, the proposed model is operated during the balanced load. The distortion in the load current is found around 28.53%, which is found to be less compared to the case of unbalance load. The waveforms of the load current distortions are illustrated in **Figures 5C,D**. It is observed that in both of the cases the distortion of harmonics is not maintained as per the IEEE-519 standard. Therefore, to reduce the harmonics and to improve the PQ, the power system is run under the MLI using the RLS and A-LMS harmonics estimation technique. The individual test for both the RLS and A-LMS are analyzed under different load conditions. The performances of both techniques are observed individually to show the feasibility of the control technique.

Balanced Loading Condition

The performance study of the proposed power system model using the MLI is operated under a balanced load using the RLS and A-LMS techniques. Initially, it was observed that, with the use of the RLS technique, the distortion of voltage harmonics was improved as compared to the case that did not use the compensating device. The case study is designed for the case of balanced load conditions. **Figure 6** provides the simulation

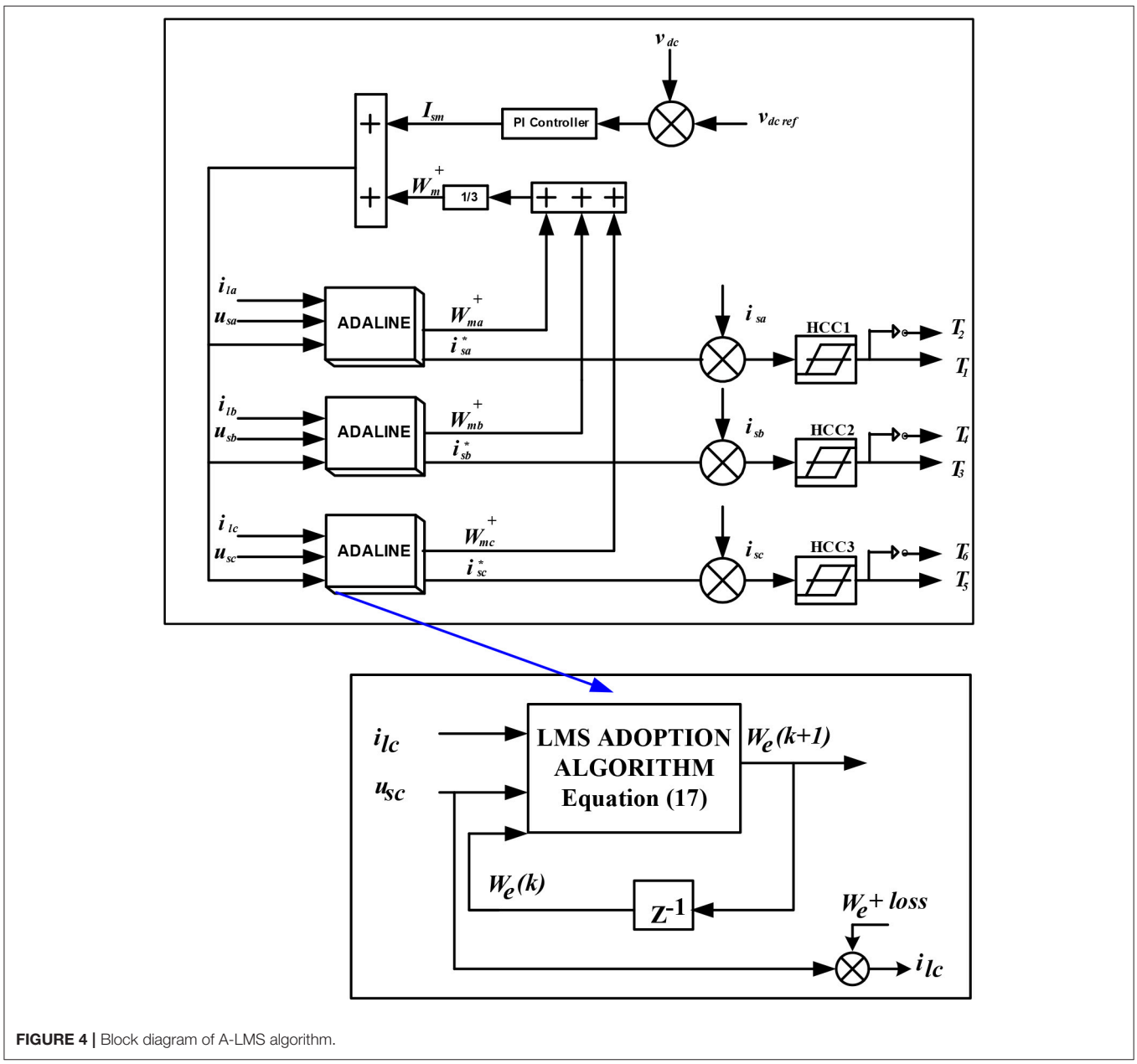

FIGURE 4 | Block diagram of A-LMS algorithm.

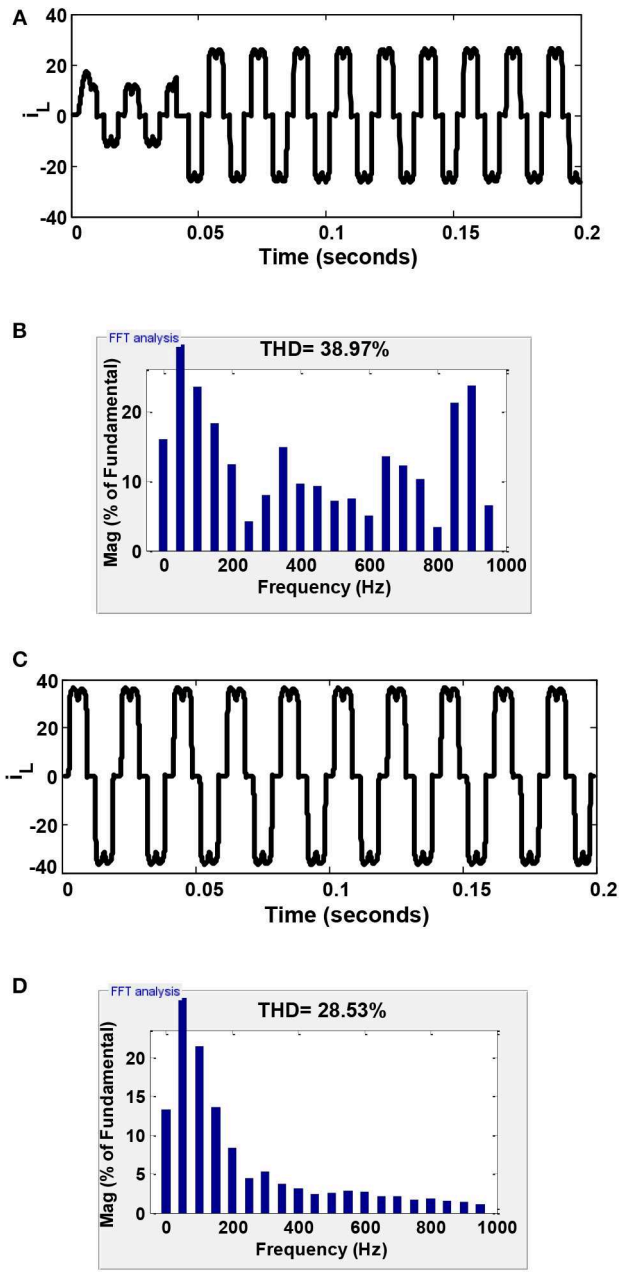

FIGURE 5 | Performance of the load current without using the MLI: **(A)** during an unbalance load; **(B)** THD value under an unbalance load; **(C)** during a balanced load; and **(D)** THD value under a balance load.

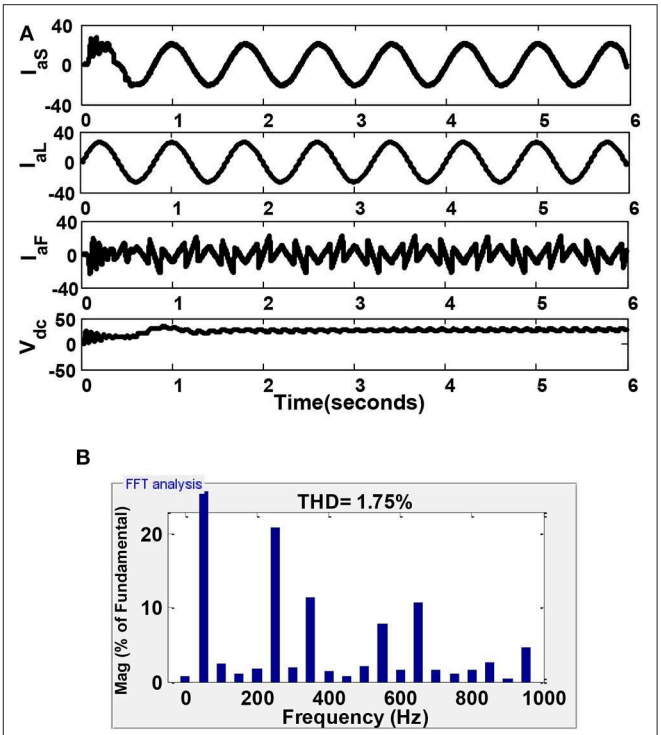

FIGURE 6 | Power quality analysis in the three-phase system using the RLS algorithm under balanced load conditions: **(A)** simulation results showing supply current, load current, filter voltage, and DC-bus voltage; and **(B)** THD value of 1.78%.

outcomes of three-phase system using the RLS algorithm. **Figure 6A** provides the simulation outcomes of single-phase source current, load current, filter voltage, and dc-link voltage. The THD analysis is shown in **Figure 6B**, and was found to be 1.75%. From the simulation results, it was proven that the load current, which is composed of harmonics, is compensated for by the MLI, and the compensated RLS technique was found to maintain the IEEE-519 standard.

Furthermore, the proposed model was operated using the A-LMS technique and the corresponding results are depicted in **Figure 7**. The source and load current, filter voltage, and dc-link voltage are provided in **Figure 7A**. The THD results are shown in **Figure 7B** and found to be 1.21%. It is observed that, when using the A-LMS technique under balanced load conditions, the distortions in the harmonics was improved compare to the RLS technique.

Unbalanced Loading Condition

In this sub-section, the MLI under the unbalanced non-linear loading condition is observed. In the first case, the system is run using the RLS technique. The corresponding results are shown in **Figure 8**. The source and load current, filter voltage, and DC-link voltage are produced in **Figure 8A**. The THD value was found to be 4.20% and is produced in **Figure 8B**.

Furthermore, the test was carried out using the A-LMS technique. The simulation outcomes of the source and load current, the filter voltage, and the DC-link voltage for the single phase is shown in **Figure 9A**. The corresponding THD results were found to be 3.70%. The THD analysis is shown in **Figure 9B**.

The simulation outcomes revealed that the distortion in the harmonics with the non-linear loads were compensated for using the MLI with the proposed A-LMS technique. It was noticed that the proposed model using the A-LMS provided satisfactory results. The THD of the load voltage was implied to display the better operation of the MLI under such conditions. The comparative analysis of THD is shown in **Table 2**.

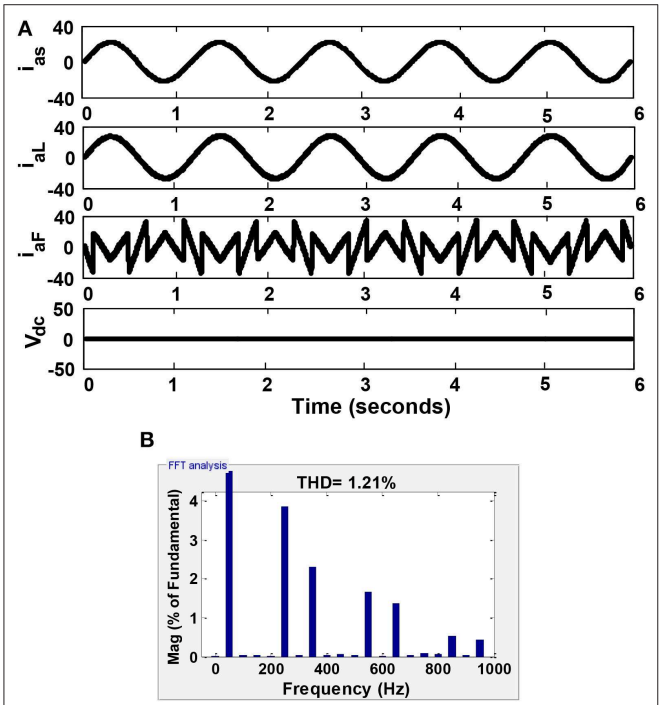

FIGURE 7 | Power quality analysis in three-phase system using the A-LMS algorithm under balanced load conditions: **(A)** simulation results showing supply current, load current, filter voltage, and DC-bus voltage; and **(B)** THD value of 1.21%.

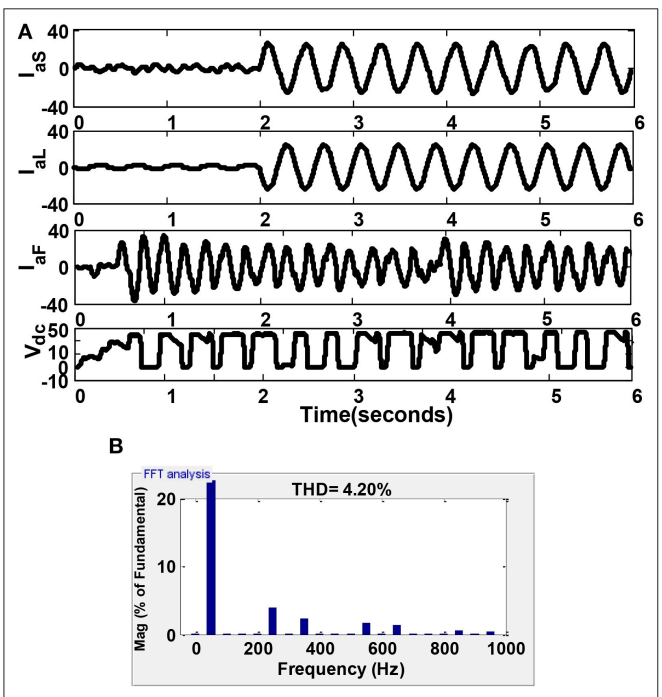

FIGURE 8 | Power quality analysis in three phase system using the RLS algorithm under unbalanced load conditions: **(A)** simulation results showing supply current, load current, filter voltage, and DC-bus voltage; and **(B)** THD value of 4.26%.

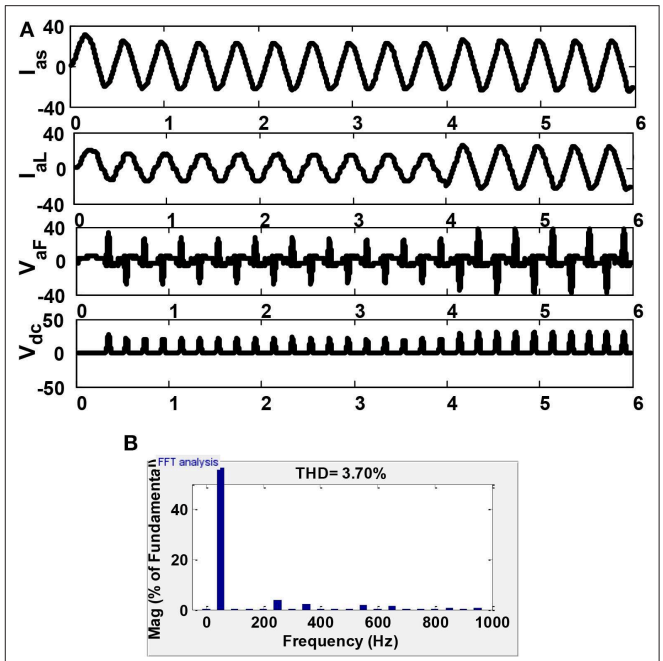

FIGURE 9 | Power quality analysis in three phase system using the A-LMS algorithm under unbalanced load conditions: **(A)** simulation results showing supply current, load current, filter voltage, and DC-bus voltage; and **(B)** THD value of 3.72%.

TABLE 2 | Comparative THD analysis of proposed technique under different load conditions.

Parameters	Unbalanced load (% THD)	Balanced load (% THD)
Without using MLI	38.97	28.53
Using MLI with RLS	4.20	1.75
Using MLI with A-LMS	3.70	1.21

CONCLUSIONS

The proposed power system model employed a 3P-4W MLI. The proposed MLI used the A-LMS technique for reference current generation and was compared with the conventional RLS technique. The performance of the proposed MLI was tested the using Matlab/ Simulink tool. The MLI was operated under balanced and unbalanced loads using both the RLS and A-LMS techniques. Even though both of the techniques were capable of compensate for the harmonics, it was concluded from simulation outcomes that the A-LMS techniques gave better results compared to the conventional RLS technique. The fall in %THD was found to be more satisfactory in the A-LMS technique, which proves the effectiveness of the proposed technique. It was concluded that the compensation in the load current using the A-LMS technique was found to satisfactory compared to the RLS technique. Moreover, the proposed MLI needed only one DC-link voltage to operate, and it was thus simple to control.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation, to any qualified researcher.

AUTHOR CONTRIBUTIONS

All authors listed have made a substantial, direct and intellectual contribution to the work, and approved it for publication.

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Conflict of Interest: KB was employed by the company Offshore Technology Development Private Ltd.

The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

APPENDIX

TABLE 1A | Parameters of the system.

Parameters	Values
Grid voltage	415 v
Supply frequency	50 Hz
Boost inductor	300 μH
Capacitor across dc side	1,000 μF
Voltage across dc link	320 v
Resistance across load	$R_L = 60\ \Omega$, ($R_1 = 2\ \Omega$, $R_2 = 4\ \Omega$, $R_3 = 6\ \Omega$)
Inductance across load	10 μF
Learning rate	0.5
Controller gain	$K_P = 0.05$, $K_I = 0.025$
Sampling time	$2e^{-5}$ s

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A New 1-ϕ, Seventeen Level Inverter Topology With Less Number of Power Devices for Renewable Energy Application

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In this paper, a new seventeen level inverter topology is proposed for single-phase grid-connected renewable energy applications. The proposed inverter topology can provide seventeen levels in the output voltage while using a lesser number of power devices. This proposed inverter topology comprises nine power switches, five power diodes, and two sets of DC sources (two 3 V and two V) which are in the ratio of 1:3. By properly arranging the input DC sources, power switches, and power diodes through different possible combinations the seventeen voltage levels are generated. The main advantage of this seventeen level inverter is that a maximum of six power devices conducts in any mode. Thus, conduction losses are lesser compared to existing seventeen level inverter topologies which results in a highly efficient system. Further, the detailed comparison of proposed inverter topology with the existing multilevel inverter (MLI) topologies shows that the number of required power devices count is considerably lower. The possible extension of the proposed inverter topology for the three-phase application is also discussed. Further, a level-shifted based pulse modulation strategy is proposed to control the output of the proposed inverter. To verify the operation, the proposed inverter topology is simulated in MATLAB/Simulink for a 500 W grid-connected system. All the major results are included in the paper. The experiments are performed to validate the proposed inverter topology for a 500 W grid-connected system and all the key results are included in the paper.

Keywords: multilevel inverter, seventeen level inverter, level-shifted modulation strategy, level generation circuit, polarity changer circuit

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INTRODUCTION

In the present days, the grid integrated renewable energy systems are drawing huge attention due to their several advantages. Solar photovoltaics (PV) is the most popular renewable energy source among the existing renewable energy sources. However, the grid integration of solar PV involves several challenges. To realize high voltage source from low voltage solar PV modules requires a series connection of several PV modules which may lead to module mismatch and partial shading problems (Sharma and Agarwal, 2014). The alternate solution is to use a low voltage PV module with the high gain DC-DC converter as a frontend to the inverter for boosting the output

voltage to be compatible with the 1-ϕ, 230 V or 3-ϕ, 415 V grid. Another alternate solution is to use the line-frequency transformer at the output of the PV inverter. But the use of additional transformer increases system cost, size, and losses in the system. This demands the utilization of high voltage gain DC-DC converters (Liu and Li, 2006; Tao et al., 2006; Duarte et al., 2007; Das and Agarwal, 2016) at the front end for boosting the voltage from low voltage solar PV source. The important features which are required from the high voltage gain DC-DC converters are that they should provide high voltage gain while maintaining high efficiency which is not possible with the conventional switched-mode DC-DC converters. To fulfill the above-mentioned requirements, the special high gain DC-DC converter topologies were proposed and developed. Another interesting feature of these high gain DC-DC converters is that they have isolated multi outputs which is more suitable for multi-input DC-AC inverter for interfacing with utility grid or load.

Figure 1 shows the typical block diagram of the grid-connected renewable energy source [PV or fuel cell (FC)] fed high gain DC-DC converter based multi-input DC-AC converter system. Here, the single input and multioutput DC-DC converter do the maximum power point tracking (MPPT) of the PV/FC source. The isolated multi-outputs of the high gain DC-DC converter acts as multi inputs of the MLI. The multi-inputs of the MLI can be regulated either through the grid side converter control (shown in **Figure 1A**) or battery supported DC-DC converter (shown in **Figure 1B**). Additionally, the configurations are shown in **Figure 1** will not allow the flow of common-mode current into the grid due to the galvanic isolation between the PV source and the grid. This paper concerns a novel multi-input MLI topology as a solution to this requirement.

Nowadays multilevel inverters (MLIs) have been gaining huge popularity as a single-stage inverter for renewable energy applications (Rodriguez et al., 2002; Lezana et al., 2008; Peng et al., 2010). The stepped output voltage waveform can be realized in MLIs through various arrangements of power devices using several input DC sources. Due to their salient features, MLIs became very suitable for medium voltage and high power applications compared to two-level converters. The applications of MLIs are not only limited to solar PV systems (Essakiappan et al., 2015) but also for wind energy systems (Yuan, 2014), drive systems (Ahmadi and Wang, 2014), and active power filters (Mathew et al., 2013). Even though MLIs require more number of power devices (Phanikumar and Agarwal, 2013a,b), they are still looked after due to their several advantages. They are lesser THD in output voltage, lesser filter requirement, lesser dv/dt, and lower electromagnetic interference (EMI). The conventional MLIs are

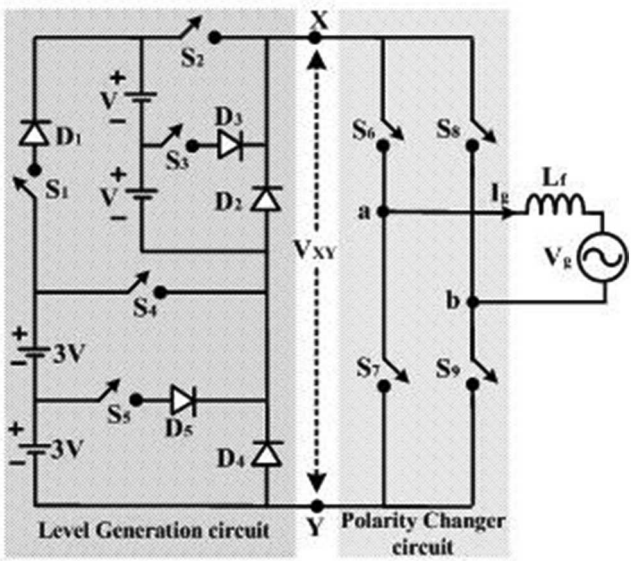

FIGURE 2 | Proposed configuration of seventeen level inverter topology.

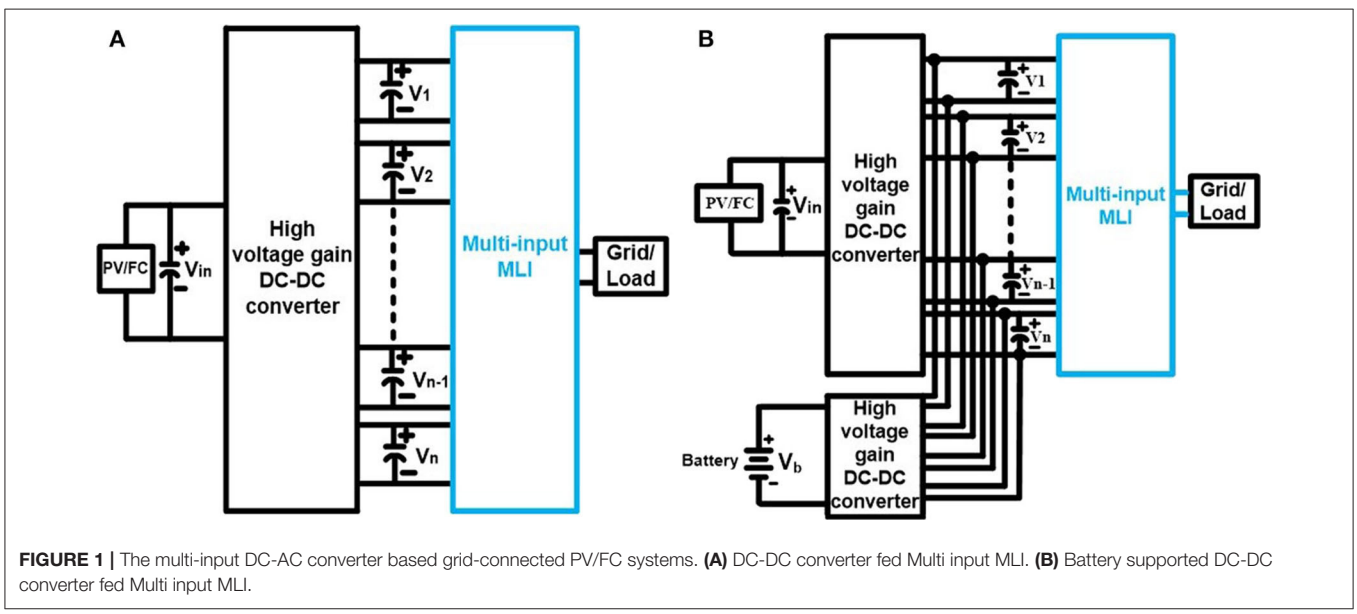

FIGURE 1 | The multi-input DC-AC converter based grid-connected PV/FC systems. **(A)** DC-DC converter fed Multi input MLI. **(B)** Battery supported DC-DC converter fed Multi input MLI.

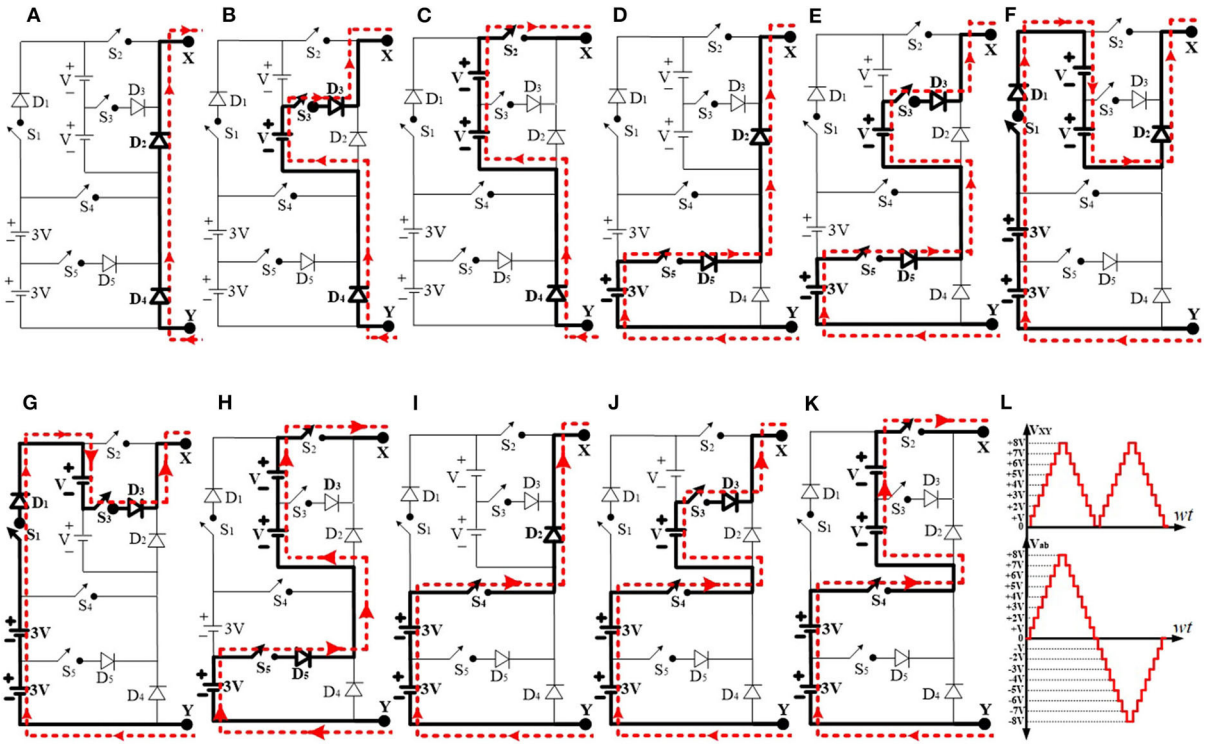

FIGURE 3 | The all possible voltage levels of the level generation circuit: **(A)** V_{XY}=0; **(B)** V_{XY}= +V; **(C)** V_{XY}= +2V; **(D)** V_{XY}= +3V; **(E)** V_{XY}= +4V; **(F)** V_{XY}= +4V; **(G)** V_{XY}= +5V; **(H)** V_{XY}= +5V; **(I)** V_{XY}= +6V; **(J)** V_{XY} = +7V; **(K)** V_{XY} = +8V; **(L)** synthesis of the output voltage of the seventeen level inverter.

classified as diode clamped (Nabae Takahashi and Akagi, 1981), capacitor clamped (Meynard and Foch, 1992), and cascaded H-bridge (Peng et al., 1996) MLIs.

The diode clamped and capacitor clamped MLIs are not preferred by researchers over CHB MLI due to their several drawbacks (Zare, 2008). Because they require large capacitors, unbalance in the voltages of input DC capacitors, and high voltage stress across power devices. Moreover, the CHB MLI accommodates a lesser number of power devices among conventional MLIs to produce the same number of voltage levels in the output (Gupta et al., 2016). The elementary concept of CHB MLI is to produce a staircase output voltage waveform through several combinations of power devices and DC sources. For solar PV applications, these DC sources can be replaced with solar PV modules as well. The presence of several steps in the output voltage waveform produces the higher quality sinusoidal waveform with a small output filter. But with the increase in the number of steps (i.e., the number of levels "*n*") in the output voltage, the number of power devices count also increases rapidly.

The researchers in Zare (2008) and Gupta et al. (2016) have done an extensive literature review on the state of the art of various topologies of MLIs. The authors in Babaei and Hosseini (2009) considered two power switches for a DC source to generate one positive voltage level. These modules are cascaded in series, and their output is connected to a full-bridge inverter to generate both positive and negative voltage levels. The authors in Babaei et al. (2014b) have modified the MLI topology in Babaei and Hosseini (2009) by adding two DC capacitors in each module with the DC source to achieve more levels in modules. In this topology, each module requires one full-bridge inverter which increases the number of components in the system.

Another type of MLI topologies which accommodate unequal input DC sources also can produce high quality of output. These topologies are called as asymmetrical MLI topologies. The advantage of these topologies is the requirement of a reduced number of power devices compared to conventional CHB MLI topologies. These topologies use fewer power components with optimal use of input DC sources. The authors in Gupta and Jain (2012) and Farhadi Kangarlu and Babaei (2013) uses a cross-connection of switches to produce more number of levels in the output with reduced stress on the devices. Further, extended MLI topologies with unequal DC sources were proposed in Babaei et al. (2014c) and Babaei et al. (2014a). Even though this topology can generate more voltage levels in the output than the other existing topologies the stress across devices is higher which requires high rated devices in the topology. It can be understood that the topologies in Farhadi Kangarlu and Babaei (2013) and Babaei et al. (2014a) have reduced switch count and the number of input DC sources. But they ended up with high stress across devices.

Another drawback of MLI topologies is DC capacitor voltage balancing. The authors in Shi et al. (2011), She et al. (2014),

TABLE 1 | All switching states of the proposed seventeen level inverter.

Switches states (1 = ON, 0 = OFF)														Output voltage V_{ab}	Mode of operation
Level generation circuit										Polarity changer					
S_1	S_2	S_3	S_4	S_5	D_1	D_2	D_3	D_4	D_5	S_6	S_7	S_8	S_9		
0	1	0	1	0	0	0	0	0	0	1	0	0	1	8V	10
0	0	1	1	0	0	0	1	0	0	1	0	0	1	7V	9
0	0	0	1	0	0	1	0	0	0	1	0	0	1	6V	8
0	1	0	0	1	0	0	0	0	1	1	0	0	1	5V	7
1	0	1	0	0	1	0	1	0	0	1	0	0	1	5V	6
1	0	0	0	0	1	1	0	0	0	1	0	0	1	4V	5
0	0	1	0	1	0	0	1	0	1	1	0	0	1	4V	4
0	0	0	0	1	0	1	0	0	1	1	0	0	1	3V	3
0	1	0	0	0	0	0	0	1	0	1	0	0	1	2V	2
0	0	1	0	0	0	0	1	1	0	1	0	0	1	V	1
0	0	0	0	0	0	1	0	1	0	1	0	0	1	0	0
0	0	0	0	0	0	1	0	1	0	0	1	1	0	0	11
0	0	1	0	0	0	0	1	1	0	0	1	1	0	–V	12
0	1	0	0	0	0	0	0	1	0	0	1	1	0	−2V	13
0	0	0	0	1	0	1	0	0	1	0	1	1	0	−3V	14
0	0	1	0	1	0	0	1	0	1	0	1	1	0	−4V	15
1	0	0	0	0	1	1	0	0	0	0	1	1	0	−4V	16
1	0	1	0	0	1	0	1	0	0	0	1	1	0	−5V	17
0	1	0	0	1	0	0	0	0	1	0	1	1	0	−5V	18
0	0	0	1	0	0	1	0	0	0	0	1	1	0	−6V	19
0	0	1	1	0	0	0	1	0	0	0	1	1	0	−7V	20
0	1	0	1	0	0	0	0	0	0	0	1	1	0	−8V	21

Sochor and Akagi (2016), and Zeng et al. (2016) have come up with balancing methods for asymmetrical MLI topologies and some topologies have inherent voltage balance capability (Lai and Shyu, 2002; Lee et al., 2009; Chattopadhyay and Chakraborty, 2014; Raushan et al., 2016; Samadaei et al., 2016; Vahedi et al., 2016; Ravi et al., 2017; Majumdar et al., 2018, 2020; Mahato et al., 2019a,b; Sinha Das and Jana, 2019; Sinha et al., 2019). The inherent voltage balancing MLI topologies have a symmetrical operation, which makes it easier to control the voltages.

To mitigate the issues of the existing MLI topologies, this paper proposes a seventeen level inverter topology with a lesser number of power devices and input DC sources. The power devices are arranged in an intelligent way to generate seventeen voltage levels with optimized input DC sources which reduce the system cost and improves the power quality. This proposed topology uses two sets of DC sources (two V and two 3 V) and produces eight positive voltage levels, eight negative voltage levels, one zero voltage levels which makes total seventeen voltage levels. To produce seventeen voltage levels the proposed topology uses just fourteen power devices. Further, there is a possibility to extend the proposed inverter topology to higher levels by cascading the modules in series so that high AC output voltage can be achieved.

This paper is organized as follows: section-proposed configuration of seventeen level inverter topology presents the proposed seventeen level inverter topology along with its various modes of operation. Section-proposed pulse width modulation strategy discusses the proposed pulse width modulation strategy, current control strategy to feed power to the grid, comparison of the proposed inverter topology with various existing MLI topologies, and extension of the proposed inverter to higher levels, the 3-ϕ extension of proposed seventeen level inverter. The simulation results of the proposed inverter topology are discussed in section-simulation results and the experimental results are presented in section-experimental results respectively. The major conclusions are presented in section-conclusions.

PROPOSED CONFIGURATION OF SEVENTEEN LEVEL INVERTER TOPOLOGY

This section presents the configuration proposed seventeen level inverter topology and its various operating modes.

Proposed Seventeen Level Inverter Topology

Figure 2 shows the proposed seventeen level inverter topology. It comprises of two circuits, a level generation circuit, and a polarity changer circuit. The level changer circuit consists of five switches (S_1-S_5), five diodes (D_1-D_5), and the polarity changer circuit consists of four switches (S_6-S_9). The level generation circuit produces nine voltage levels (0, +V, +2 V, +3 V, +4 V,

+5 V, +6 V, +7 V, +8 V) at the output V_{XY}. These nine voltage levels can be generated through several possible combinations of five power switches (S_1-S_5), five power diodes (D_1-D_5), and four input DC sources as shown in **Figure 3**. The polarity changer circuit produces AC output voltage at V_{ab} with seventeen voltage levels (0, ±V, ±2 V, ±3 V, ±4 V, ±5 V, ±6 V, ±7 V, ±8 V) by using the switches (S_6-S_9) as shown in **Figure 3L**. The all the possible switching states of the level generation circuit and polarity changer circuit are given in **Table 1** to produce the seventeen level output voltage (V_{ab}). The modes of operation of the level generation circuit are shown in **Figures 3A–K**.

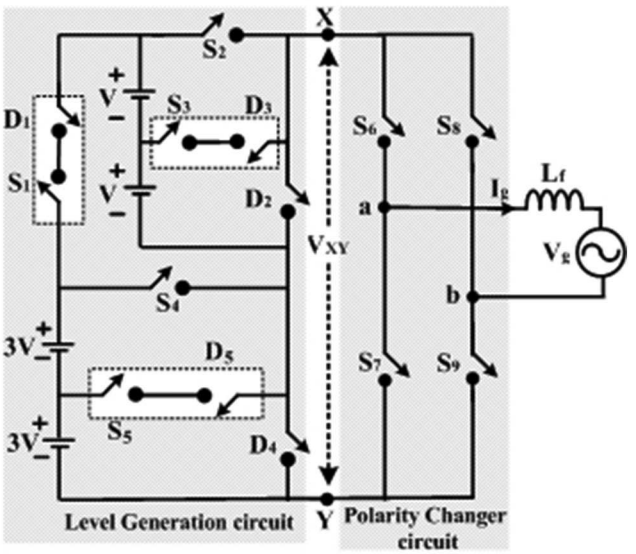

FIGURE 4 | The proposed Bi-directional seventeen level inverter topology.

Various Modes of Operation of Level Generation Circuit

The modes of operation of the level generation circuit are discussed below:

Mode-0: During this mode of operation the all the switches of the level generation circuit are turned OFF. The current will flow through the diodes D_2 and D_4, as shown in **Figure 3A**. The terminals X, Y of the level generation circuit are shorted through D_2, D_4. Hence the voltage across the level generation circuit is zero (i.e., $V_{XY} = 0$). The current path during this mode of operation is indicated through the dotted line as shown in **Figure 3A**.

Mode-1: In this mode of operation the power switch S_3 of the level generation circuit is turned ON. The current will flow through the D_4, S_3, and D_4 as shown in **Figure 3B**. The terminals X, Y of the level generation circuit experience a voltage of "V"

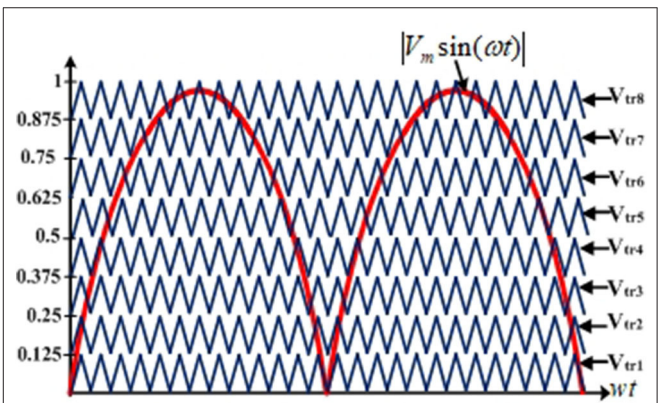

FIGURE 5 | The PWM strategy of the proposed seventeen level inverter topology.

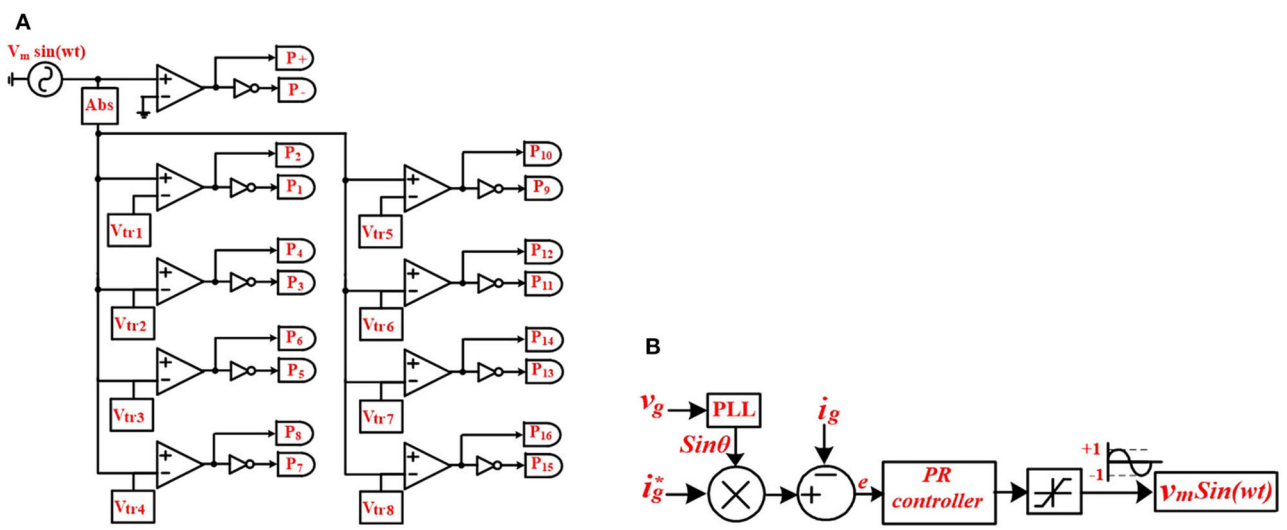

FIGURE 6 | The modulation and control strategies for proposed inverter topology; **(A)** proposed modulation logic; **(B)** current control strategy for the grid-connected seventeen level inverter (She et al., 2014).

though S_3, D_3, and D_4. Hence the voltage across level generation circuit is +V (i.e., $V_{XY} = +V$). The current path during this mode of operation is indicated through the dotted line as shown in **Figure 3B**.

Mode-2: During this mode of operation the power switch S_2 of the level generation circuit is turned ON. The current will flow through the D_4, S_2 as shown in **Figure 3C**. The terminals X, Y of the level generation circuit experience a voltage of "2 V" though S_2 and D_4. Hence the voltage across the level generation circuit is +2 V (i.e., $V_{XY} = +2$ V). The current path during this mode of operation is indicated through the dotted line as shown in **Figure 3C**.

Mode-3: In this mode of operation the power switch S_5 of the level generation circuit is turned ON. The current will flow through S_5, D_2, and D_5 as shown in **Figure 3D**. The terminals X, Y of the level generation circuit experience a voltage of "3 V" though S_5, D_2, and D_5. Hence the voltage across the level generation circuit is +3 V (i.e., $V_{XY} = +3$ V). The current path during this mode of operation is indicated through the dotted line as shown in **Figure 3D**.

Mode-4: During this mode of operation the power switches S_5 and S_3 of the level generation circuit are turned ON. The current will flow through the S_5, D_5, S_3, and D_3 as shown in **Figure 3E**.

TABLE 2 | The expressions of gate pulses for all the switches.

S.no	Gate pulse of switch	Gate pulse expression
1	G_{S1}	$P_8 \times P_{13}$
2	G_{S2}	P_{14}
3	G_{S3}	$(P_4 \times P_5)+(P_{12} \times P_{13})+(P_{16})$
4	G_{D2}	$(P_2 \times P_3)+(P_{10} \times P_{11})+(P_{14} \times P_{15})$
5	G_{S4}	$P_6 \times P_7$
6	G_{S5}	$(P_1)+(P_6 \times P_9)$
7	G_{D4}	P_5
8	G_{S6}	P_+
9	G_{S7}	P_-
10	G_{S8}	P_-
11	G_{S9}	P_+

The terminals X, Y of the level generation circuit experience a voltage of "4 V" though S_5, D_5, S_3, and D_3. Hence the voltage across the level generation circuit is +4 V (i.e., $V_{XY} = +4$ V). The

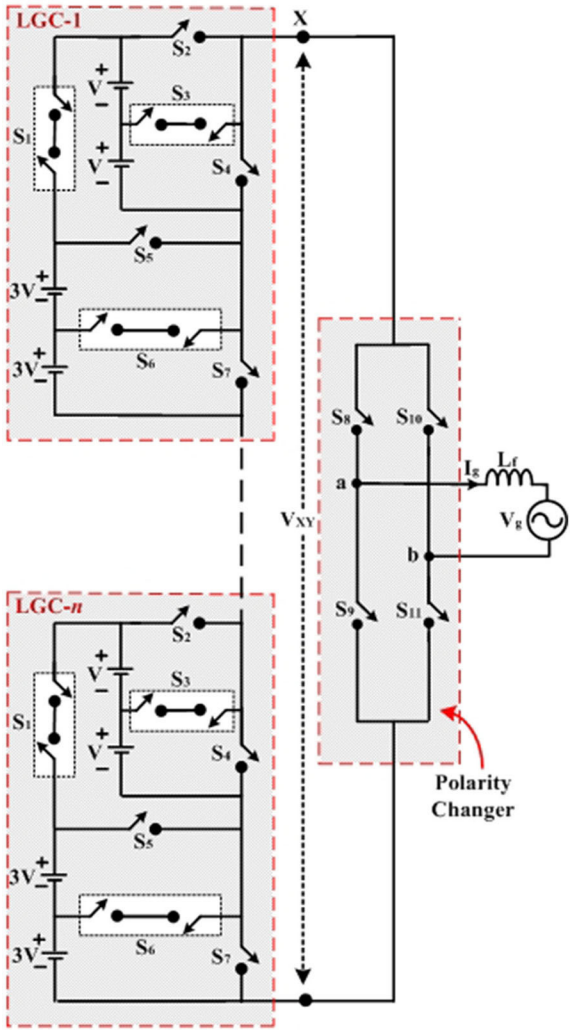

FIGURE 7 | The possible extension of 1-ϕ seventeen level inverter to *n*-level.

TABLE 3 | The comparison of proposed seventeen level inverter topology with the existing MLI topologies.

Parameter	Babaei and Hosseini (2009)	Babaei et al. (2014a)	Farhadi Kangarlu and Babaei (2013)	Lai and Shyu (2002)	Sinha et al. (2019)	Sinha Das and Jana (2019)	Majumdar et al. (2020)	Raushan et al. (2016)	Proposed inverter	Proposed bi-directional inverter
Input sources	4	4	4	4	6	4	3	9	4	4
Power switches	20	18	18	16	15	16	11	22	9	14
Power diodes	0	0	0	0	20	0	4	28	5	0
Auxiliary capacitors	0	0	0	0	0	0	2	0	0	0
Total components	24	22	22	20	41	20	20	59	18	18
Reactive power capability	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
TSV	$36V_{dc}$	$34V_{dc}$	$34V_{dc}$	$32V_{dc}$	$31V_{dc}$	$32V_{dc}$	$30V_{dc}$	$34V_{dc}$	$16V_{dc}$	$30V_{dc}$
Efficiency (%)	94	94	95	95	93	96	95	94	97	96.5
Driving signals	20	18	18	16	15	16	11	22	9	14

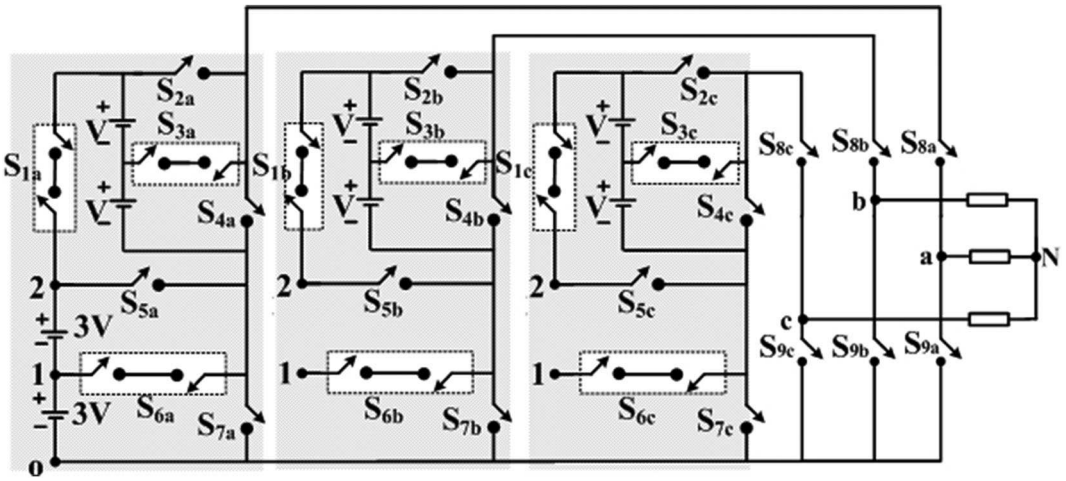

FIGURE 8 | The extended 3-ϕ seventeen level inverter topology (All the nodes marked '1' are connected, similarly all nodes marked '2' are connected).

current path during this mode of operation is indicated through the dotted line as shown in **Figure 3E**.

Mode-5: In this mode of operation the power switch S_1 of the level generation circuit is turned ON. The current will flow through the S_1, D_1, and D_2 as shown in **Figure 3F**. The terminals X, Y of the level generation circuit experience a voltage of "4 V" though S_1, D_1, and D_2. Hence the voltage across the level generation circuit is +4 V (i.e., $V_{XY} = +4$ V). The current path during this mode of operation is indicated through the dotted line as shown in **Figure 3F**.

Mode-6: During this mode of operation the power switches S_1 and S_3 of the level generation circuit are turned ON. The current will flow through the S_1, D_1, S_3, and D_3 as shown in **Figure 3G**. The terminals X, Y of the level generation circuit experience a voltage of "5 V" though S_1, D_1, S_3, and D_3. Hence the voltage across the level generation circuit is +5 V (i.e., $V_{XY} = +5$ V). The current path during this mode of operation is indicated through the dotted line as shown in **Figure 3G**.

Mode-7: In this mode of operation the power switches S_5 and S_2 of the level generation circuit are turned ON. The current will flow through the S_5, D_5, and S_2 as shown in **Figure 3H**. The terminals X, Y of the level generation circuit experience a voltage of "5 V" though S_5, D_5, and S_2. Hence the voltage across the level generation circuit is +5 V (i.e., $V_{XY} = +5$ V). The current path during this mode of operation is indicated through the dotted line as shown in **Figure 3H**.

Mode-8: During this mode of operation the power switch S_4 of the level generation circuit is turned ON. The current will flow through the S_4 and D_2 as shown in **Figure 3I**. The terminals X, Y of the level generation circuit experience a voltage of "6 V" though S_4 and D_2. Hence the voltage across the level generation circuit is +6V (i.e., $V_{XY} = +6$ V). The current path during this mode of operation is indicated through the dotted line as shown in **Figure 3I**.

Mode-9: In this mode of operation the power switches S_4 and S_3 of the level generation circuit are turned ON. The current will flow through the S_4, S_3, and D_3 as shown in **Figure 3J**. The terminals X, Y of the level generation circuit experience a voltage of "7 V" through S_4, S_3, and D_3. Hence the voltage across the level generation circuit is +7 V (i.e., $V_{XY} = +7$ V). The current path during this mode of operation is indicated through the dotted line as shown in **Figure 3J**.

Mode-10: During this mode of operation the power switches S_4 and S_2 of the level generation circuit are turned ON. The current will flow through the S_4 and S_2 as shown in **Figure 3K**. The terminals X, Y of the level generation circuit experience a voltage of "8V" though S_4 and S_2. Hence the voltage across the level generation circuit is +8V (i.e., $V_{XY} = +8$V). The current path during this mode of operation is indicated through the dotted line as shown in **Figure 3K**.

The nine voltage levels obtained from the level generation circuit are used to obtain the seventeen voltage levels by using the polarity changer circuit, as shown in **Figure 3L**.

The proposed seventeen level inverter topology can be made bi-directional by replacing unidirectional devices (D_1-D_5) with controlled power switches. The proposed configuration of the bi-directional seventeen level inverter is shown in **Figure 4**.

PROPOSED PULSE WIDTH MODULATION STRATEGY

This section discusses the proposed pulse width modulation (PWM) strategy, the control strategy of the grid-connected seventeen level inverter topology.

Proposed PWM Strategy

To control the output voltage and generate the seventeen voltage levels, a PWM strategy has been proposed along with its modulation logic. The **Figures 5**, **6A** show the PWM strategy and proposed modulation logic of inverter. In this PWM strategy, a reference waveform ($|Vm\ sinwt|$) is compared with the eight

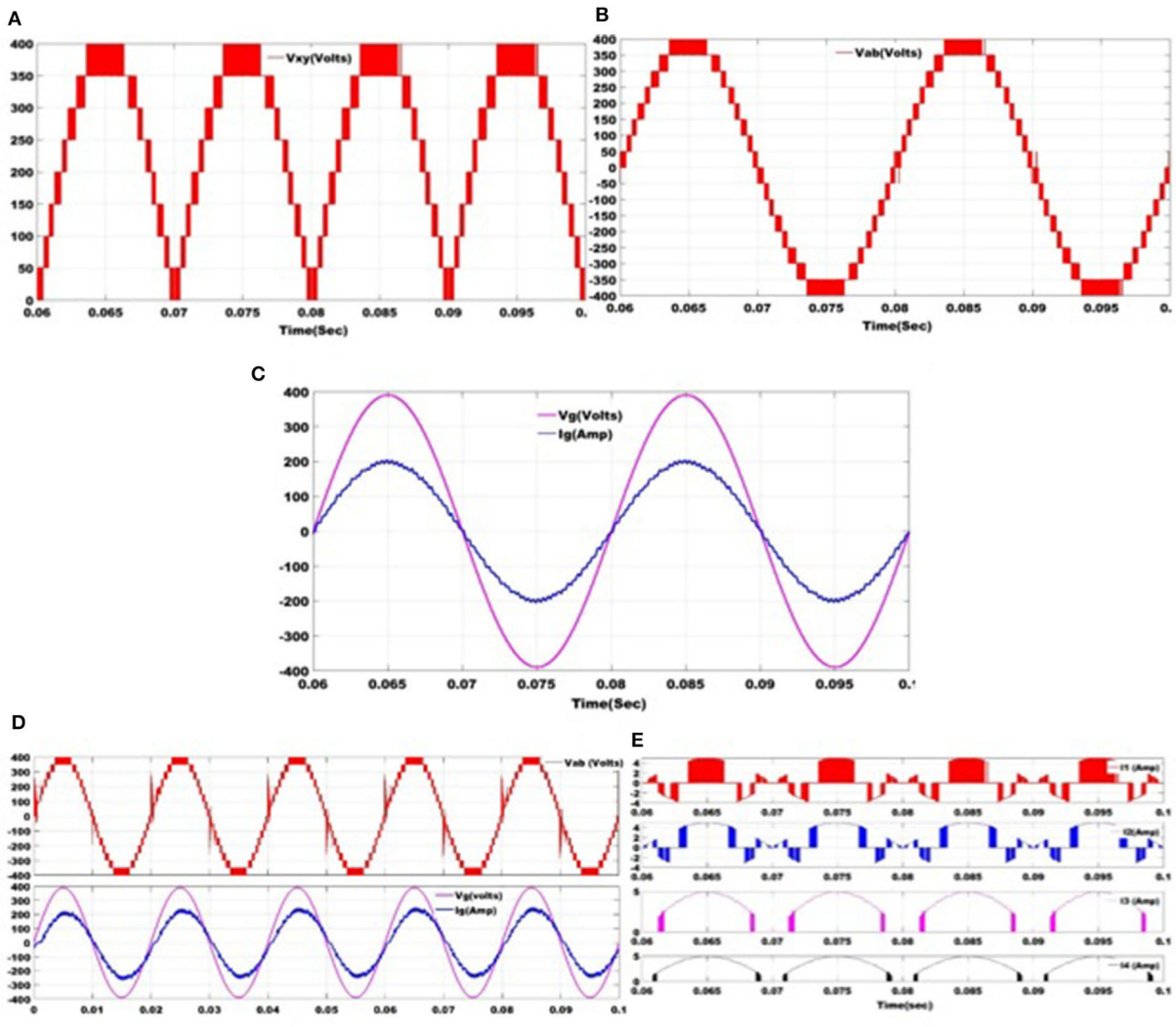

FIGURE 9 | The simulated waveforms of the grid connected seventeen level inverter topology; **(A)** output voltage of the level generation circuit (V_{XY}); **(B)** output voltage (V_{ab}); **(C)** voltage across the grid and current through the grid (Grid current is scaled up 70 times to fit into the graph); **(D)** output voltage (V_{ab}), voltage across the grid and current through the grid for non UPF (Grid current is scaled up 70 times to fit into the graph); **(E)** current through input DC sources I_1, I_2, I_3, and I_4 (Input currents are scaled up two times to fit into the graph).

carrier waveforms (V_{C1}-V_{C8}) to generate signals P_1-P_{15}, as shown in **Figures 5**, **6A**. These signals P_1-P_{15} are modified to obtain the gate pulses for the switches S_1-S_9 and D_1-D_5. The obtained expressions for the gate pulses of all switches are given in **Table 2**.

The Current Control Strategy for the Grid-Connected Seventeen Level Inverter

Figure 6B shows the current control strategy, which is used to control the current feeding into the grid (Lee et al., 2009). In this control strategy, the grid current (i_g) is compared with the reference grid current ($i_g^* sin\theta$) which gives the error signal (e) as output. Here, i_g^* is the peak amplitude of reference current, and $sin\theta$ is obtained from the PLL. The error signal is sent through the proportional resonant (PR) controller which generates the modulating wave $V_m(sinwt)$. This modulating wave is used to generate reference waveform $|V_m(sinwt)|$. This reference waveform is used to generate the gate pulses for all the switches by using the proposed modulation strategy shown in **Figures 5**, **6A**. The PR-controller's transfer function is given as:

$$T_{PR}(s) = K_p + \frac{2K_i w_{cut} s}{s^2 + 2w_{cut} s + w^2} \quad (1)$$

The PR controller is designed by considering the phase margin as 50^0 and maximum permissible steady-state error of 0.1% of the rated current. The designed values of the PR controller are given as:

$K_p = 0.4$; $K_i = 15$; $\omega_{cut} = 20$ rad/sec and $\omega = 2 \times \pi \times 50$ rad/sec.

Comparison of the Proposed Seventeen Level Inverter Topology With the Existing MLI Topologies

The proposed seventeen level inverter and bi-directional seventeen level inverter topologies are compared with the existing seventeen level inverter topologies. The proposed inverter topologies require fewer input DC sources, power devices, and lesser requirement of the number of drive signals which reduces the size, cost of the system, and increases the reliability of the system. In addition to that, the total standing voltage (TSV) of high-frequency switches are smaller compared to the existing MLI topologies (given in **Table 3**). Thus, the proposed inverter topologies incur lower switching losses. The efficiencies of proposed seventeen level inverter topology and bi-directional seventeen level inverter topologies are calculated to be 97 and 96.5%, respectively.

The detailed comparison of the proposed seventeen level inverter topology with the existing seventeen level inverter topologies is given in **Table 3**. From **Table 3**, it can be observed that the proposed inverter topology doesn't have the reactive power capability even though it uses a lesser number of power devices. However, this issue can be tackled by using the proposed bi-directional inverter topology.

The Extension of Proposed 1- ϕ Seventeen Level Inverter Topology to *n*-Level

There is a possibility to extend the proposed 1-ϕ seventeen level inverter to higher levels by adding the level generation circuits (LGC) in a cascaded fashion as shown in **Figure 7**. This is possible due to the modularity of proposed inverter topology, which supports the extension for *n*-levels. For example, the cascaded connection of level generation circuits (LGC_1 and LGC_2) generates voltage levels +16, +15 V,…+V, and 0 in the output voltage (V_{XY}). Thus, the +16, +15 V,…+V and 0 voltage levels in the obtained voltages of V_{XY} are used to generate ±16, ±15, ±14, ±13, ±12 V,…. ±V and 0 output voltage V_{ab} associated with the polarity changer. **Figure 7** shows the cascaded connection of level generation circuits of LGC_1 and LGC_2. In this manner, the *n*-level MLI can be realized by cascading the level generation circuits LGC_1, LGC_1,…$LGC_{(n-1)/16}$ in series. The number of level generation circuits (N_{LGC}), DC sources (N_{DC}), switches (N_s), diodes (N_D), and total power devices (N_{PD}) required for obtaining *n*-levels are given by the following equations:

$$n = 16(N_{LGC}) + 1 \quad (2)$$

$$N_{DC} = (n-1)/4 \quad (3)$$

$$N_s = \frac{5}{8}(n-1) + 4 \quad (4)$$

where $n = 17, 33, 49, \ldots$ and $N_{LGC} = 1, 2, 3, \ldots$.

Extension of Proposed 1-ϕ Seventeen Level Inverter for 3-ϕ Application

The possible extension of the proposed 1-ϕ seventeen level inverter topology for 3-ϕ application is shown in **Figure 8**. It consists of a total of four sets of DC sources (three V and one 3 V) and 12 controlled switches, nine bi-directional switches. In this 3-ϕ topology, the three legs share a common DC source (two 3 V) which minimizes the required DC sources' count.

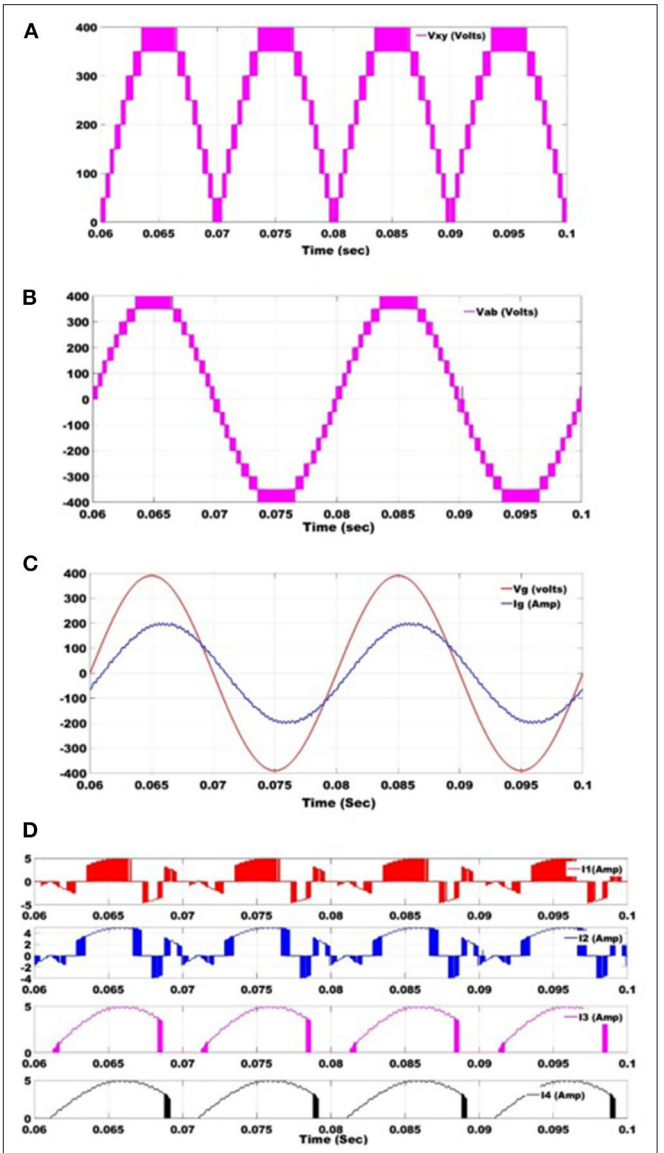

FIGURE 10 | The simulated waveforms of the grid connected bi-directional seventeen level inverter topology at power factor of 0.95; **(A)** output voltage of the level generation circuit (V_{XY}); **(B)** output voltage (V_{ab}); **(C)** voltage across the grid and current through the grid (Grid current is scaled up 70 times to fit into the graph); **(D)** current through input DC sources I_1, I_2, I_3, and I_4 (Input currents are scaled up two times to fit into the graph).

SIMULATION RESULTS

The proposed grid-connected 1-ϕ seventeen level inverter topology is simulated for a power rating of 500 W at a switching

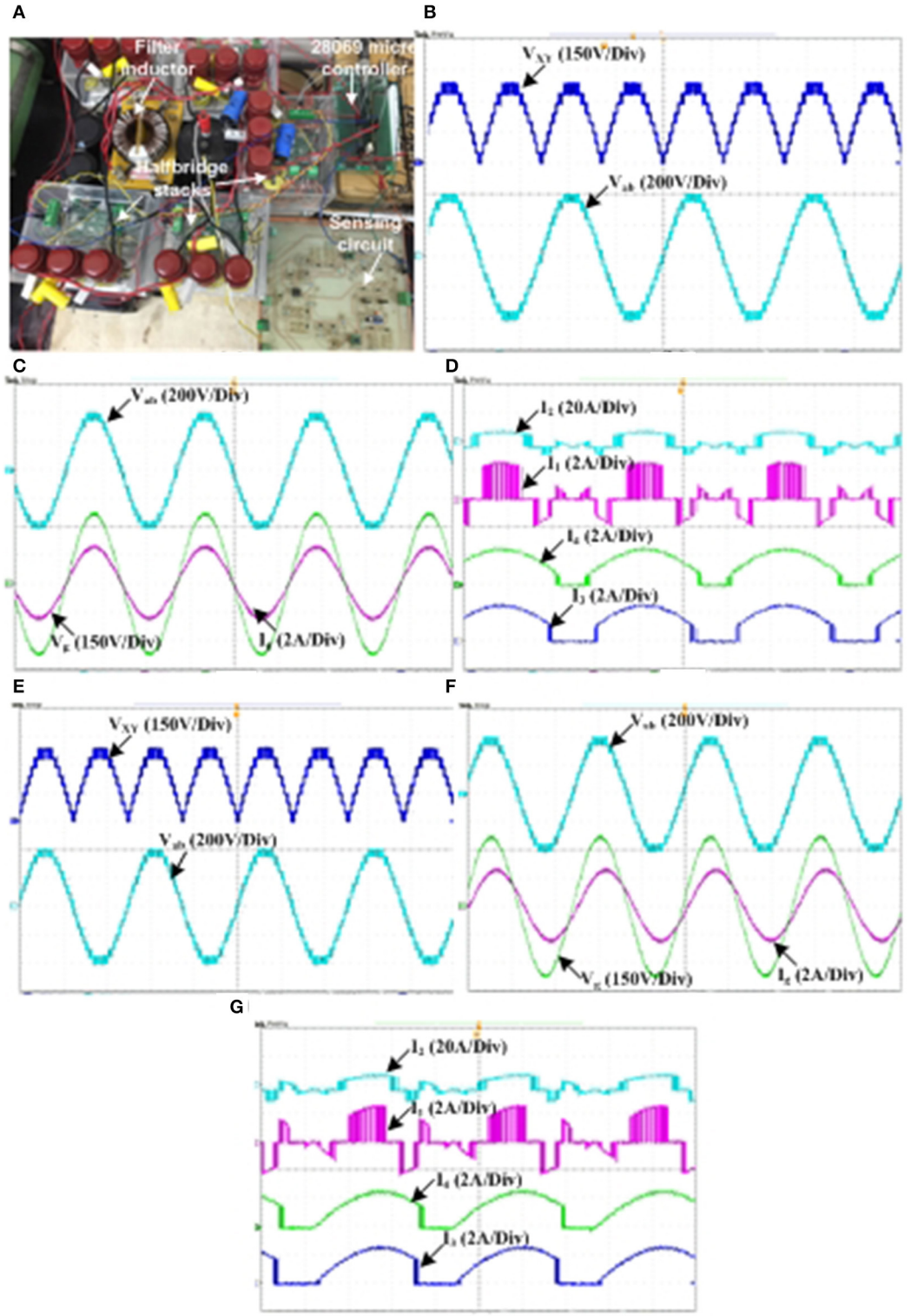

FIGURE 11 | The experimental waveforms of the grid connected seventeen level inverter topology; **(A)** experimental setup of the grid-connected system; **(B)** the output voltage of the level generation circuit (V_{XY}) and inverter output voltage (V_{ab}); **(C)** the grid voltage (V_g) and current through the grid (I_g); **(D)** the current through the input DC sources (I_1, I_2, I_3, and I_4); **(E)** the output voltage of the level generation circuit (V_{XY}) and inverter output voltage (V_{ab}); **(F)** The grid voltage (V_g) and current through the grid (I_g); **(G)** the current through the input DC sources (I_1, I_2, I_3, and I_4).

TABLE 4 | Parameters used in system evaluation of seventeen level inverter topology.

1	The power rating of the system	500 VA
2	Input DC sources	50 V (2 no.s)
		150 V (2 no.s)
3	Grid voltage	230 V (RMS)
4	Filter inductor: L_f	4 *mH*
5	Switching frequency: f_s	3 *kHz*
6	Power switches	BSM50GB60DLC
7	Power diodes	RM200DY1-24S
8	DSP controller	TMS320F28069

frequency of 3 kHz. The MATLAB/Simulink environment is used for the simulation studies. The considered values of two sets of input DC sources are 50 and 150 V. To filter the high-frequency harmonics the filter inductor (L_f) is chosen as 4 mH. The simulated waveforms of the voltage across the level generation circuit (V_{XY}) are shown in **Figure 9A**. It consists of nine voltage levels 0, 50, 100, 150, 200, 250, 300, 350, and 400 V. By using these nine voltage levels, seventeen voltage levels (0, ±50, ±100, ±150, ±200, ±250, ±300, ±350, and ±400 V) are generated at the output of polarity changer circuit (i.e., output voltage V_{ab}) as shown in **Figure 9B**. The waveforms of grid voltage and current are also shown in **Figure 9C**. It can be observed from **Figure 9C** that the proposed inverter topology is feeding high quality of current into the grid because of the presence of multi-levels in the output voltage. Further, the proposed grid connected inverter topology is simulated at lagging power factor of 0.9 and corresponding waveforms of the output voltage, grid voltage and current are shown in **Figure 9D**. The waveforms of the current through two sets of input DC source two V and two 3 V (i.e., I_1, I_2, I_3, and I_4) are also shown in **Figure 9E**. The parameters used for the simulation studies are given in **Table 4**.

Further, the proposed bi-directional seventeen level inverter topology is also verified through simulations for a 500 VA grid-connected system. The simulated waveforms of the voltage across the level generation circuit, output voltage (V_{ab}), the voltage across the grid, and current through the grid at a power factor of 0.95 are shown in **Figures 10A–C**, respectively. It can be observed from **Figure 10C** that the proposed bi-directional inverter can feed a nice quality of power into the grid at THD of 2.1% due to the presence of a higher number of levels in the output voltage. The waveforms of the current through two sets of input DC source two V and two 3 V (i.e., I_1, I_2, I_3, and I_4) are also shown in **Figure 10D**.

EXPERIMENTAL RESULTS

The proposed seventeen level inverter topology is tested for grid-connected for a power rating of 500 W at switching frequency of 3 kHz on a laboratory prototype (shown in **Figure 11A**). **Table 4** shows the parameters used for the study of the proposed seventeen level inverter topology for the grid-connected system. The experimental waveforms of the output voltage of the level generation circuit (V_{XY}) and inverter output voltage (V_{ab}) are shown in **Figure 11B**. Further, the experimental waveforms current though the grid and voltage across the grid at unity power factor are also shown in **Figure 11C**.

Figure 11D shows the waveforms of the current through the two sets of the input DC sources (I_1, I_2, I_3, and I_4). It can be observed from **Figure 11C** that the inverter output voltage contains seventeen voltage levels and feeds good quality of current into the grid.

Further, the proposed bi-directional seventeen level inverter also tested for grid-connected application at 500 VA power rating. The experimental waveforms level generation circuit output voltage (V_{XY}), inverter output voltage (V_{ab}), grid voltage (V_g), grid current (I_g), and currents through the input DC sources at a power factor of 0.95 are shown in **Figures 11E–G**. The proposed bi-directional seventeen level inverter also feeds good quality of power into the grid with THD of 2.1%.

CONCLUSIONS

This paper has presented a new seventeen level inverter topology for single-phase grid-connected applications. The main advantage of proposed inverter topology is the reduced number of power components. Due to fewer power components, a compact system can be realized. Further, a comparison of the proposed seventeen level inverter topology with the existing MLIs is presented which shows the major advantages of the proposed configuration. The proposed seventeen level inverter has lower conduction losses because at maximum only five switches conduct in any mode of operation. Further, the bi-directional operation of the proposed topology is also presented. The possible 3- ϕ extension of the proposed 1-ϕ seventeen level inverter is also discussed and its extension for higher levels is also investigated. The proposed 1-ϕ seventeen level inverter and bi-directional seventeen level inverters are able to feed high-quality power into the grid with a current THD of 2.36 and 2.1% respectively. The proposed seventeen level inverter topology and its bi-directional operation also validated through experimental results and all the results are presented in the paper which shows the effectiveness of the proposed work.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation, to any qualified researcher.

AUTHOR CONTRIBUTIONS

PC and VA: substantial contributions to the conception or design of the work, or the acquisition, analysis, or interpretation of data for the work. AA-D: drafting the work or revising it critically for important intellectual content. All authors contributed to the article and approved the submitted version.

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REVIEW
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Review of Five-Level Front-End Converters for Renewable-Energy Applications

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With the objective of minimizing environment and energy issues, distributed renewable-energy sources have reached remarkable advancements along the last decades, with special emphasis on wind and solar photovoltaic installations, which are deemed as the future of power generation in modern power systems. The integration of renewable-energy sources into the power system requires the use of advanced power electronic converters, representing a challenge within the paradigm of smart grids, e.g., to improve efficiency, to obtain high power density, to guarantee fault tolerance, to reduce the control complexity, and to mitigate power-quality problems. This paper presents a specific review about front-end converters for renewable-energy applications (more specifically the power inverter that interfaces the renewable-energy source with the power grid). It is important to note that the objective of this paper is not to cover all types of front-end converters; the focus is only on single-phase multilevel structures limited to five voltage levels, based on a voltage-source arrangement and allowing current or voltage feedback control. The established review is presented considering the following main classifications: (a) number of passive and active power semiconductors; (b) fault tolerance features; (c) control complexity; (d) requirements of specific passive components as capacitor or inductors; and (e) number of independent or split dc-link voltages. Throughout the paper, several specific five-level front-end topologies are presented and comparisons are made between them, highlighting the pros and cons of each one of them as a candidate for the interface of renewable-energy sources with the power grid.

Keywords: five-level converters, renewable energy sources, power converters, multilevel, power electronics, power quality

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INTRODUCTION

Power converters capable of synthesizing, more than three voltage levels, are commonly classified as multilevel converters, where a common feature is the possibility to deal with higher voltages (Pandey et al., 2006; Debnath et al., 2015; Gupta et al., 2015). Mainly due to the required voltage levels in an application, multilevel converters are based on simple structures or based on a cascade connection of simple structures (Sadigh et al., 2015; Xiao et al., 2015; Ahmed et al., 2017).

Therefore, approaches with the split dc link, with multiple dc links (independently or not), or a mix of both are possible structures that allow synthesizing the multi-voltage levels. Dependent on the application (i.e., interface of renewable-energy sources, electric mobility, or storage systems), multilevel converters can be distinguished as active rectifiers or grid-forming or grid-tied inverters, with the possibility, in each case, of using a voltage-source or current-source structure. The main objective of a multilevel converter is to synthesize an ac voltage or current with improved quality, also contributing to preserve issues of power quality. Therefore, the key purpose of multilevel converters are to (a) deal with semiconductor limitations in high-voltage applications; (b) deal with limitations of switching frequency; (c) improve the power quality; (d) improve modularity and/or scalability; and (e) deal with controllability (Karwatzki and Mertens, 2018).

Power quality has been a concern in an electrical grid, however, the interest for this topic has increased along the last decades for both residential and industrial levels (Singh et al., 2004; Bollen et al., 2010; Ceaki et al., 2017; Lopez-Martin et al., 2018), leading to the development of various multilevel converter topologies (Singh et al., 2008), as well as control strategies (Nejabatkhah et al., 2019). Moreover, in recent years, due to the advances in semiconductors and digital control platforms, multilevel converters have emerged as a suitable alternative to the conventional static multi-pulse structures (i.e., based on transformers with specific arrangements) as well as an alternative to the conventional two-level converters. The most conventional multilevel converter, i.e., the neutral-point-clamped (NPC), was introduced in the last century, and since that date, several proposals were introduced for different applications. Reviews of multilevel converters can be found in Pandey et al. (2006); Debnath et al. (2015), and Gupta et al. (2015) where besides the analysis of the topologies in terms of required hardware and software for the control, prospective applications are also included. However, since the publication of these reviews, several multilevel converters have been proposed with innovative features in terms of topology, control, and applications (e.g., considering applications of smart grids, on-grid and off-grid renewable-energy sources, electric mobility, microgrids, power transmission, and distribution). Compared to the conventional solutions, increasing the number of voltage levels reduces the size of the passive filters for maintaining similar indices of power quality, consequently allowing to increase the power density of the equipment, which is a key factor in many applications. However, a higher number of levels increase the required hardware resources, which hints to a trade-off between levels, hardware resources, and power density. Based on these criteria, the objective of this paper is not to cover all the multilevel converters but to focus on five-level converters with the possibility to be applied as grid-tied inverters for interfacing renewable-energy sources with the power grid. Therefore, a review of several publications is presented, where the main focus is on voltage-source structures, grid-tied inverters (with current or voltage feedback control), single-phase or three-phase structures, and the five voltage levels. In this context, the main contributions of this paper are related to the following: (a) the more recent and emerging multilevel converters (five-level) identified in the literature are presented; (b) the multilevel (five-level) converters are organized according to the characteristics; and (c) a comparison is established based on the main characteristics in order to identify the pros and cons of each topology.

The paper is directly related with the application of five-level converters to interface renewable-energy sources with the power grid, however, the presented topologies can also be useful for other applications, both for coupling with the power grid (i.e., as grid-tied inverters) or for island operation (i.e., as off-grid inverters). A concrete case is the applications of energy-storage systems. In fact, the energy-storage systems are flexible systems in terms of power operation, which are capable of consuming, storing, or providing energy. Taking into account the flexibility offered, energy-storage systems can offer additional advantages for the integration of renewable-energy sources, e.g., targeting power management in a distributed architecture. The up-to-date energy-storage technologies are compiled and investigated in Yao et al. (2016), mainly from the perspective of technology efficiency, maturity, cost, lifespan, and contextualization with the final application scenarios. A review of energy-storage systems about problems and challenges for microgrid applications is presented in Faisal et al. (2018), and the past and present of the distinct technologies of energy-storage systems are presented in Boicea (2014). An overview regarding the history, evolution, and future status of energy-storage systems is presented in Whittingham (2012). Projects directly related to energy-storage systems are presented in Araiza et al. (2018) and Baxter et al. (2018), while overviews from the power electronics point of view are introduced in Molina (2017) and Mazumder (2019).

The rest of the paper is organized as follows: Section "Standards for Grid-Connected PV Installations" presents an overview of standards for grid-connected converters used for interfacing renewable-energy sources; section "Topologies of Five-Level Front-End Converters" presents the selected topologies of five-level front-end converters; and section "Modulation Techniques for Five-Level Front-End Converters" presents modulation techniques for five-level front-end converters. Section "Comparison Between Topologies" establishes a comparison among the selected topologies; section "Conclusion" ends the paper with the conclusions.

STANDARDS FOR GRID-CONNECTED PV INSTALLATIONS

Over the last decades, the market of PV installations is increasing as a contribution to meet the rising demand. In terms of power, PV installations can vary from few kW to thousands of MW. However, the increased integration of PV-based resources into the power systems can cause diverse effects in practical characteristics that are mainly associated with power-quality issues, power management, demand response, reliability, and safety.

Therefore, the integration of photovoltaic (PV) installations must accomplish with specific standards and guidelines, which

are established according to the country (i.e., the standards and guidelines can vary from country to country). Such standards are an important requirement, which must be considered in the specifications of the PV installation, as well as in the design of power electronics. IEEE 1547 and IEC 61727 are the most widely recognized standards relevant to these applications, which are established by the IEEE (Institute of Electrical and Electronics Engineers) and by the IEC (International Electrotechnical Commission), respectively. Regarding power electronics, the grid-connected front-end converters are designed with the aim to reduce specific harmonic levels, reduce total harmonic distortion (THD), increase power factor, reduce frequency deviation, and eliminate leakage currents.

Summarizing, the IEEE 1547 standard is focused on technical specifications for the interconnection and interoperability among distributed energy resources (DERs) and power systems (at different distribution voltages, emphasizing DER in radial primary and secondary distribution systems) less than 10 MVA. This standard is intended to be universally adopted, where among others, issues such as power quality, safety considerations, islanding, and response to abnormal conditions are addressed. On the other hand, the IEC 61727 standard deals directly with low-voltage non-islanded converters (grid-connected dc–ac inverters). This standard is applied for the interconnection of PV installations (less than 10 kVA) from the power system in the perspective of single-phase or three-phase residences. Regarding the aforementioned standards, **Table 1** summarizes the key points of these standards. Besides the aforementioned standards, there are other relevant standards such as the IEEE 929–2000, which is specific for PV installations with power below 10 kW. This is a recommended practice guidance regarding the interface of PV installations, where there are issues such as power quality, safety, protection, utility system operation, and islanding of PV installations. Other standards, but with lower importance, are established by the NEC, UL, and so on Hester (2002), U. Std, (2002), and Wiles (2005).

TOPOLOGIES OF FIVE-LEVEL FRONT-END CONVERTERS

In this section, a comprehensive review of the more recent topologies with a special focus on single-phase five-level inverters is provided. It should be noted that the anti-parallel diode of a controlled switch is considered a separate component, as is the case in normal applications.

A five-level three-phase inverter is proposed in Sajadian and Santos (2014), however, the three-phase system consists of three separate phases that can operate individually. In each phase, four fully controlled power switches and six diodes are needed. This topology is presented in **Figure 1**. A coupled inductor is needed for the topology. The output voltage of the converter can be calculated using (1). It should be noted that S_1 operation is complementary to S_2.

$$V_{out} = \left(\frac{1}{2}(1 - S_2) - S_3\right) V_{dc} = \left(\frac{1}{2}(1 - S_2) - (1 - S_4)\right) V_{dc} \tag{1}$$

The main advantage of this structure is that it requires fewer controlled switches and has no need for complex voltage-control algorithms for dc-link voltage-control algorithms as happens with many other topologies. The authors also claim that the topology improves power loss. However, a coupled inductor and certain operating conditions must be met.

In Korhonen et al. (2014), a five-level single-phase inverter based on neutral point and a flying capacitor is proposed that can produce $\pm v_{dc}/2$, $\pm v_{dc}/4$, and 0. As can be seen in **Figure 2**, it has eight fully controlled power switch and eight diodes. The output voltage of the converter can be calculated using

TABLE 1 | Summary of the grid requirements concerning the IEEE 1547 and IEC 61727 standards.

	IEEE 1547		**IEC 61727**	
Nominal power	**30 Kw**		**10 kW**	
Harmonic level (currents)	**Order**	**%**	**Order**	**%**
	3–9	4	3–9	4
	11–15	2	11–15	2
	17–21	1.5	17–21	1.5
	23–33	0.6	23–33	0.6
	> 35	0.3	> 35	0.3
	Even harmonics < 25% of odd harmonics THD < 5%			
DC current	**< 1% of rated current**		**<0.5% of rated current**	
Voltage variation	ΔV < 50%	0.1 s	ΔV < 50%	0.16 s
	50% < ΔV < 88%	2 s	50% < ΔV < 88%	2 s
	110% < ΔV < 120%	2 s	110% < ΔV < 120%	1 s
	ΔV > 120%	0.05 s	ΔV > 120%	0.16 s
Frequency variation	59.3 < Hz < 60.5	0.2 s	59.3 < Hz < 60.5	0.16 s

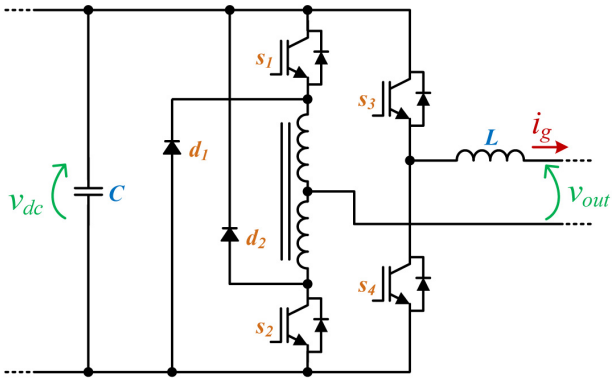

FIGURE 1 | Topology proposed in Sajadian and Santos (2014).

(2). There are multiple alternatives for the $\pm v_{dc}/4$ that can be exploited to maintain the voltage of the floating capacitor within a tight boundary.

$$v_{out} = (S_5\ S_6 - S_7\ S_8)\frac{v_{dc}}{2} + (S_5 S_7 - S_6\ S_8 + S_3\ S_4\ S_6 - S_1\ S_2\ S_7)\frac{v_{dc}}{4} \quad (2)$$

It should be noted that the switches and diodes need different voltage ratings, which can increase maintenance costs. Voltage fluctuation in the flying capacitor can affect output quality, as well as the split power source requirement, which can be limiting, and the utilized switches have different voltage ratings. Moreover, it can only produce half of the total dc-link voltage, which is not desirable. The authors compare the performance of the paper with a commercial NPC-5L topology, and the results show a very slight improvement in efficiency.

The authors in Yuan (2014) modify the structure proposed in Korhonen et al. (2014) and utilize reverse-blocking IGBTs. However, similar to the previous paper, it utilizes the redundant stages to balance the flying-capacitor voltage. The disadvantages are also similar. The authors claim that this topology requires a lower number of semiconductor count, because they are considering each of the reverse-blocking IGBTs as one semiconductor. However, a reverse-blocking IGBT is in effect composed of two back-to-back IGBTs that do not have any anti-parallel diode and this advantage is not very prominent. On the other hand, utilizing the reverse-blocking IGBTs, improves efficiency. **Figure 2** shows the proposed topology.

The output voltage of the converter shown in **Figure 2** can be calculated using (3). Comparing (3) with (2), it can be seen that they are essentially similar and the only difference is that (Yuan, 2014) (c.f. **Figure 2**) utilizes one bidirectional switch instead of two back-to-back unidirectional ones.

$$v_{out} = (S_3\ S_4 - S_5\ S_6)\frac{v_{dc}}{2} + (S_2\ S_4 - S_1\ S_5 + S_3\ S_5 - S_4\ S_6)\frac{v_{dc}}{4} \quad (3)$$

A three-phase five-level topology is proposed in Masaoud et al. (2014). It requires sixteen controlled switches and sixteen diodes. There are five voltage levels for each phase, 0, $v_{dc}/4$, $2v_{dc}/4$, $3v_{dc}/4$, v_{dc}, which, by considering a three-phase operation, would result in nine voltage levels. Although the topology has a relatively low number of switches per voltage levels for all the three-phases, it requires two different sources, where one of them should be a split-voltage source. This topology is presented in **Figure 3**. The output phase-voltage of the converter shown in **Figure 3** can be calculated using (4).

$$v_{out} = (S_3\ S_6\ S_8)\frac{v_{dc}}{2} + (S_1\ S_2\ S_5\ S_7)\frac{3v_{dc}}{4} + (S_1\ S_2\ S_6\ S_7)\frac{v_{dc}}{2} + (S_1\ S_2\ S_5\ S_8)\frac{v_{dc}}{2} \quad (4)$$

Authors in Vahedi et al. (2016) utilize a seven-level converter previously proposed by Kamal Al-Hadad called PUC to build a five-level converter with simplified control. This topology is presented in **Figure 4**. It is argued that the previously proposed seven-level converter has a very complex control and requires a high switching frequency as well as additional sensors. However, the simplified five-level converter changes the ratio $V_1 = 3V_2$ to $V_1 = 2V_2$ and also introduces a self-balancing algorithm to simplify the control. The output voltage levels are $\pm\ v_{dc}/2$ and $\pm\ v_{dc}/4$, 0, which achieve a unity voltage ratio between output and input voltage. The split power source being unnecessary is another advantage of such a system. The output phase voltage of the topology shown in **Figure 4** can be calculated based on the switch states using (5).

$$v_{out} = (S_1\ S_5\ S_6 - S_2\ S_3\ S_4)\frac{v_{dc}}{2} + (S_1\ S_3\ S_5 + S_1\ S_2\ S_6 - S_3\ S_4\ S_5 - S_2\ S_4\ S_6)\frac{v_{dc}}{4} \quad (5)$$

A single-phase five-level structure is proposed in Saeedian et al. (2018) based on the switching capacitor technique. **Figure 5A** shows the proposed structure, and the phase output voltage can be calculated using (6). Since the capacitors utilized in the topology can be easily balanced without needing any complex closed-loop control, one of the advantages of this system is a simple control. However, the most important benefit of the presented circuit is its voltage boosting capability. For an input source with a voltage v_{dc}, it can produce a five-level ac output voltage with voltage levels of 0, $\pm\ v_{dc}$, and $\pm\ 2\ v_{dc}$. For achieving this goal, one power supply, two capacitors, ten diodes, and seven power switches are required. This structure has a high number of active and passive components; however, one main advantage of this method is that it can produce an output twice the voltage level of the power supply.

$$v_{out} = (S_1\ S_7 - S_2\ S_6)\,2v_{dc} + (S_1\ S_4\ S_5\ S_7 + S_2\ S_3\ S_4\ S_7 - S_1\ S_4\ S_5\ S_6 - S_2\ S_3\ S_4\ S_6)\,v_{dc} \quad (6)$$

In Madhukar Rao and Sivakumar (2015), a single-phase five-level inverter with fault tolerance is proposed. The proposed converter consists of seven power switches as well as twelve power diodes. A diode bridge in combination with a power switch in

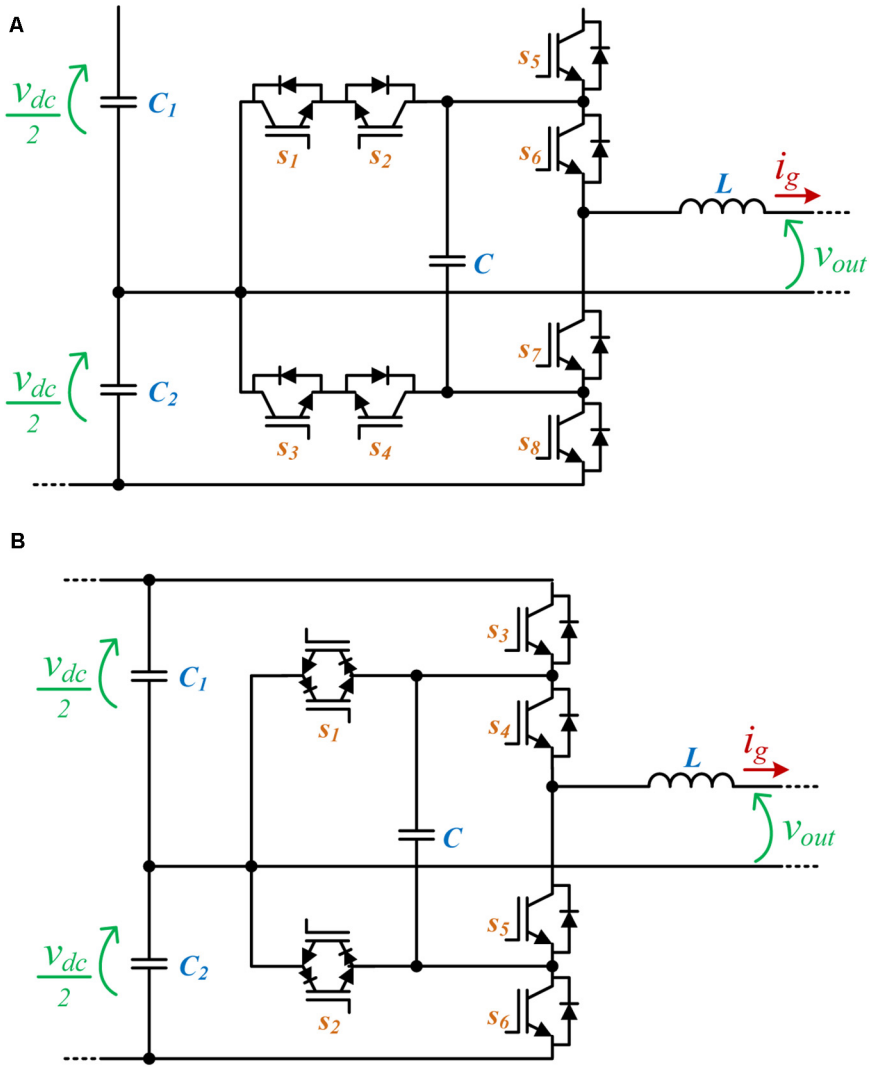

FIGURE 2 | Topologies: **(A)** proposed in Korhonen et al. (2014); **(B)** proposed in Yuan (2014).

the output is utilized to cut off the fault current. However, the utilized diode bridge of the fault circuit breaker in the output can severely hinder the efficiency of the converter. **Figure 5B** shows the structure of the converter proposed in Madhukar Rao and Sivakumar (2015). The output voltage of the topology shown in **Figure 5B** can be calculated based on (7), while S_1 can be used for interrupting the current path during faults.

$$v_{out} = (S_3\ S_4\ S_5 - S_2\ S_6\ S_7)\, v_{dc} + (S_3\ S_5\ S_6 - S_2\ S_5\ S_6)\, \frac{v_{dc}}{2} \tag{7}$$

A five-level inverter with a modular switched capacitor circuit is proposed in He and Cheng (2016). The main advantage of this topology is that the voltage levels can be increased by adding more switched capacitor bridge modules. As can be seen in **Figure 6**, the topology has twelve diode-switch sets for a five-level inverter. With each extra switched capacitor module, the output voltage amplitude can be increased to four times the input voltage v_{dc}. The first two switch groups are defined by (8) and (9).

$$S_P = S_3\ S_7\ S_9\ S_{10} \tag{8}$$

$$S_N = S_4\ S_6\ S_8\ S_{11} \tag{9}$$

Considering the defined switching groups and the remaining switches, it is possible to calculate the output phase voltages, according to (10). It should be noted that the S_P and S_N are complementary.

$$v_{out} = (S_P + S_N)[(S_2\ S_5 - S_1\ S_6)4v_{dc} + (S_2\ S_6 - S_1\ S_5)2v_{dc}] \tag{10}$$

Another five-level fault-tolerant structure is proposed in Gautam et al. (2017). This topology is presented in **Figure 7**.

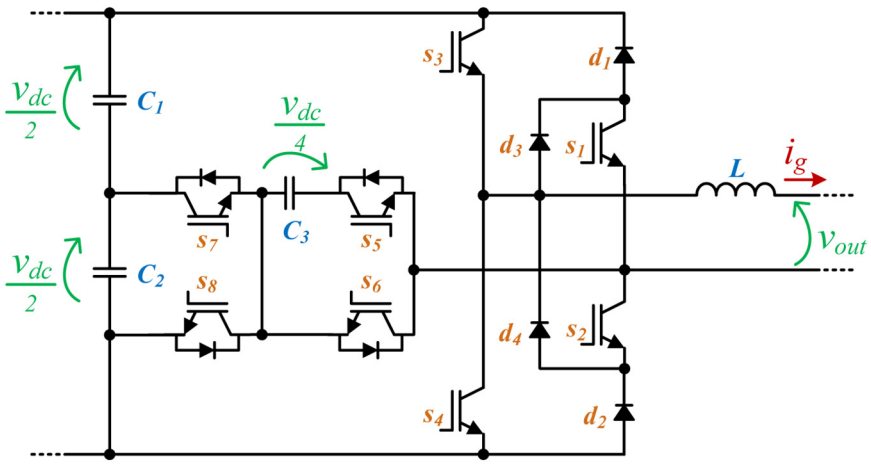

FIGURE 3 | Topology proposed in Masaoud et al. (2014).

It consists of six IGBT-diode sets, as well as a bidirectional switch and an NPC leg. Compared to many other topologies with fault current limiting capability, this one has a moderate number of switches and capacitors. The required NPC can be considered one of the disadvantages of such topologies. Moreover, this topology can produce output voltages in the range of $\pm\ v_{dc}$. The output voltage levels based on the input source and the capacitor voltage can be calculated using (11). In the case of $v_{c2} = v_{dc}/2$, there are five symmetrical voltage levels.

$$v_{out} = (S_1\ S_2\ S_6 - S_3\ S_4\ S_5)\, v_{dc} + (S_1\ S_2\ S_7 + S_2\ S_3\ S_7)\left(v_{dc} - v_{C_2}\right) - (S_3\ S_4\ S_7 + S_2\ S_3\ S_5)\, v_{C_2} \tag{11}$$

A five-level inverter for medium-voltage applications is proposed in Narimani et al. (2016). Although the paper focuses on a three-phase structure, it can be easily utilized as a single-phase system too. The system includes eight switch-diode sets as well as two extra diodes for each phase. One of the disadvantages of such a topology is the requirement of a split-source supply and three additional capacitors. The output voltage

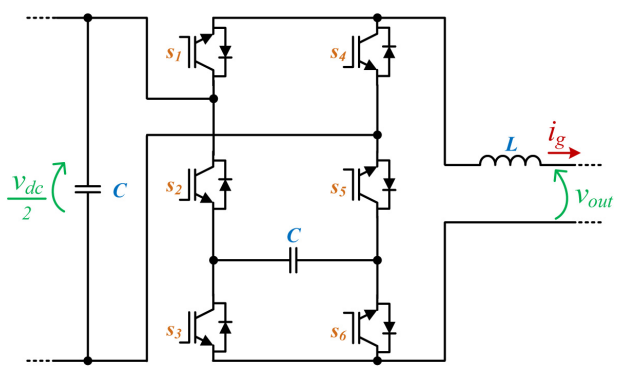

FIGURE 4 | Topology proposed in Vahedi et al. (2016).

levels include $v_{dc}/2$, $v_{dc}/4$, 0, $-v_{dc}/4$, and $-v_{dc}/2$. **Figure 8A** shows the abovementioned topology. Another disadvantage of this topology is a relatively complex balancing procedure for the three flying capacitors in each phase. Although the authors claim that the number of diodes is reduced compared to many previous topologies, the number of semiconductor devices is still relatively high. The output phase voltage of the topology shown in **Figure 8A** can be calculated based on the switch states using (12).

$$v_{out} = (S_1\ S_2\ S_3\ S_4 - S_5\ S_6\ S_7\ S_8)\frac{v_{dc}}{2} + (S_1\ S_2\ S_4\ S_5 + S_2\ S_3\ S_4\ S_8 + S_1\ S_3\ S_4\ S_7 - S_4\ S_5\ S_7\ S_8 - S_1\ S_5\ S_6\ S_7 - S_2\ S_5\ S_6\ S_8)\frac{v_{dc}}{4} \tag{12}$$

Figure 8B depicts another five-level inverter based on a split-source supply (Aly et al., 2018). It requires fourteen switch-diode sets and four extra diodes. Although this topology requires a higher number of semiconductor devices compared to the topology proposed in Narimani et al. (2016), it has some other significant advantages including: simpler control, no flying capacitor, and fault-tolerant structure. The output voltages are $-v_{dc}$, $-v_{dc}/2$, 0, $v_{dc}/2$, and v_{dc}, which can be calculated using (13).

$$v_{out} = (S_1\ S_2\ S_7\ S_8 - S_3\ S_4\ S_5\ S_6)\, v_{dc} + (S_1\ S_2\ S_6\ S_7 + S_2\ S_3\ S_7\ S_8 - S_2\ S_3\ S_6\ S_7 - S_3\ S_4\ S_6\ S_7)\frac{v_{dc}}{2} \tag{13}$$

A bidirectional topology based on a half-bridge front-end structure and two flying-capacitor cascade structures is proposed in Naderi et al. (2015). This topology is shown in **Figure 9**. This topology has a split dc link and two flying capacitors, which represents the main disadvantage of this topology since it increases the control complexity. When compared with other topologies, this one requires a significant number of switching devices. Each of the flying capacitor cells is formed by four switching devices,

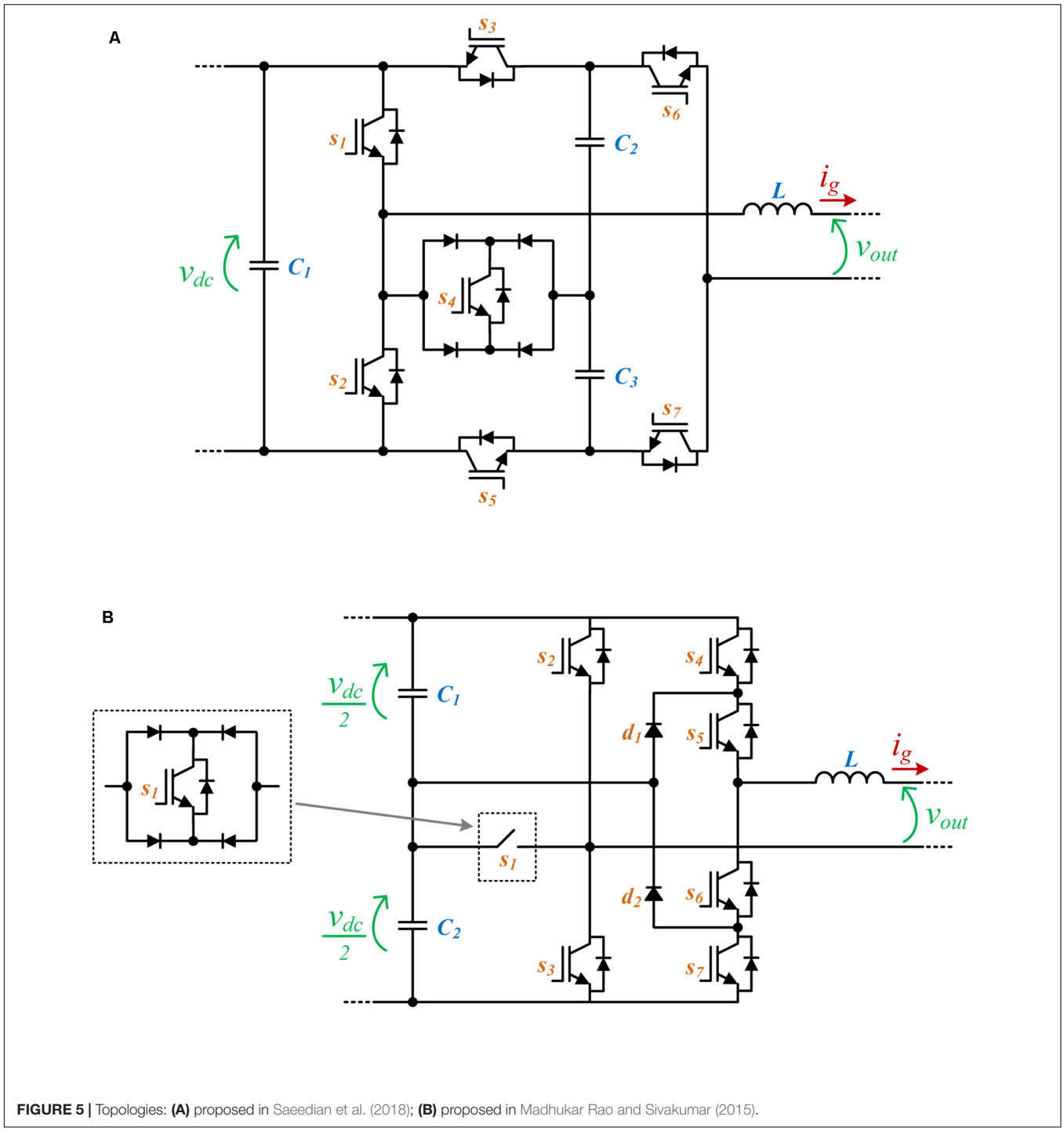

FIGURE 5 | Topologies: **(A)** proposed in Saeedian et al. (2018); **(B)** proposed in Madhukar Rao and Sivakumar (2015).

which are responsible for producing three voltage levels. The output phase voltage of the topology shown in **Figure 9** can be calculated based on the switch states defined in (14).

$$v_{out} = (S_1\ S_3\ S_4 - S_2\ S_9\ S_{10})\frac{v_{dc}}{2} + (S_1\ S_3\ S_6 + S_1\ S_4\ S_5 - S_2\ S_8\ S_9 - S_2\ S_7\ S_{10})\frac{v_{dc}}{4} \quad (14)$$

In this case, the following switches work in a complementary manner.

$$S_5 = 1 - S_3$$

$$S_4 = 1 - S_6$$

$$S_7 = 1 - S_9$$

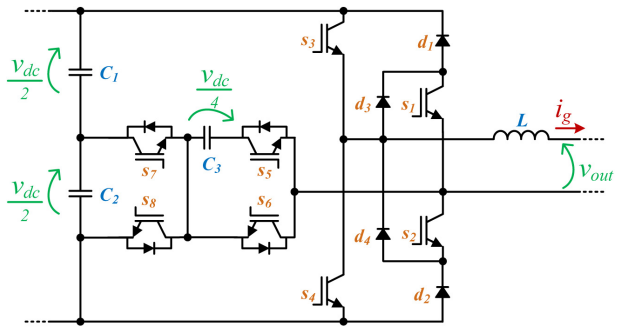

FIGURE 6 | Topology proposed in He and Cheng (2016).

$$S_8 = 1 - S_{10}$$

$$S_1 = 1 - S_2 \tag{15}$$

A bidirectional topology based on a full-bridge front-end structure and a bidirectional-bipolar cell connected between the neutral wire and a split dc link is presented in Monteiro et al. (2016). This topology is presented in **Figure 10A**. The full-bridge structure is responsible for obtaining three voltage levels ($+ v_{dc}$, 0, $-v_{dc}$), while the bidirectional-bipolar cell is responsible for obtaining the other two voltage levels ($+ v_{dc}/2$, $-v_{dc}/2$). The output phase voltage can be calculated using (16). In order to optimize the efficiency, the switching devices S_1 and S_2 can be switched at a low frequency (i.e., the frequency of the power grid voltage), while the other switching devices are switched at high frequency.

$$v_{out} = (S_2\ S_3 - S_1\ S_4)\, v_{dc} + (S_3\ S_5 - S_4\ S_5)\, \frac{v_{dc}}{2} \tag{16}$$

A bidirectional topology based on a full-bridge front-end structure and a back-end dc–dc structure with a split dc link is presented in Leite et al. (2018). This topology, shown in **Figure 10B**, operates with five voltage levels, according to the operation of the back-end dc–dc converter. The switching devices s1 and s2 are switched at a low frequency (i.e., the frequency of the power grid voltage), while the other switching devices are switched at high frequency. As claimed in the paper, this is an import aspect since it is possible to optimize the operation of the converter, reducing the switching losses. The output phase voltage of the topology shown in **Figure 10B** can be calculated based on the switch states using (17).

$$\begin{aligned} v_{out} &= (S_2\ S_3\ S_7\ S_8 - S_1\ S_4\ S_7\ S_8)\, v_{dc} \\ &+ (S_2\ S_3\ S_6\ S_7 - S_1\ S_4\ S_5\ S_8)\, \frac{v_{dc}}{2} \end{aligned} \tag{17}$$

Modular multilevel converters (MMCs) are another type of circuit that can realize five-level output voltage (Wang et al., 2019; Xu et al., 2019). In a way, MMCs are an extension of the earlier multilevel circuits based on the flying capacitors, with the exception that MMCs are much more feasible in higher voltage levels (Dekka et al., 2017). Theoretically, there is no limit to the number of voltage levels that an MMC can achieve, but the practical considerations such as controller complexity and cost would limit the number of voltage levels. Since the main advantage of the MMC topologies is in higher voltage and higher voltage levels, here only two of the more basic topologies that utilize half-bridge and full-bridge submodules are considered that are shown in **Figures 11–C**. The output voltage of the submodules shown in **Figures 11A–C** can be calculated using (18), (19), and (20), respectively.

$$v_{SM} = (S - S_2\ )\, v_C \tag{18}$$

$$v_{SM} = (S_1\ S_4 - S_2\ S_3)\, v_C \tag{19}$$

$$v_{SM} = (S_1\ S_3\ S_6\ S_8 - S_2\ S_4\ S_5\ S_7)\, v_C \tag{20}$$

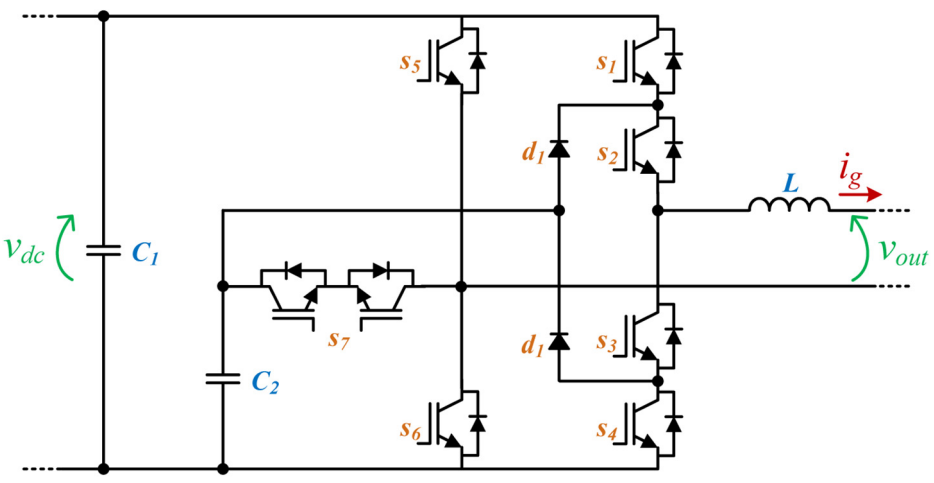

FIGURE 7 | Topology proposed in Gautam et al. (2017).

In Zhou et al. (2018), each MMC submodule has a half-bridge structure requiring two switches and two diodes. With the structure proposed in Zhou et al. (2018), eight switch-diode sets, two inductors, and four capacitors are required (Xu et al., 2018). However, it is possible to reduce the number of required modules to half, if the switching technique in Hu and Jiang (2014) is utilized. Based on the control technique proposed in Hu and Jiang (2014), four switch-diode sets, two inductors, and four capacitors are required. On the other hand, the size of the required inductor increases. The structure proposed in Hu et al. (2018) requires double switch-diode sets, than the one proposed in Zhou et al. (2018); however, because of the control proposed in Hu et al. (2018), smaller capacitors can be used while at the same time increase the output to input voltage ratio to around $0.7v_{dc}$. Another advantage of these MMCs is better fault tolerance.

There are other MMC topologies that focus on additional features such as sensorless balancing and/or parallel connection (Xu et al., 2018; Jin et al., 2019; Li et al., 2019; Xu et al., 2019). As an example, an extra half-bridge is introduced in Goetz et al. (2015, 2016) that brings about the capability to connect neighboring modules in parallel. The parallel connection decreases string impedance, reduces current ripple, and improves the balancing capability of the capacitors. The parallel connection of modules distributes load current among multiple capacitors (Zhu et al., 2018) and reduces requirements on the current rating of the switches to one half. Sizing the switches to lower current ratings compensates double the number of discrete switches of the MMCSP, and the amount of silicon needed is comparable to the MMC topology in Hu et al. (2018). The control method proposed in Li et al. (2017) reduces the complexity of the control algorithm to the level of standard MMCs. Large voltage differences and temporal imbalance might cause inrush currents between paralleled modules and reduce the feasibility of the parallel mode. Means to overcome the inrush currents are presented in Li et al. (2019).

MODULATION TECHNIQUES FOR FIVE-LEVEL FRONT-END CONVERTERS

One distinguishing aspect of the multilevel converters, when compared to the traditional two-level converters, is the wide variety of usable modulation techniques. Multilevel converters require different modulation techniques in order to synthesize all of its possible voltage levels, regardless of being three-level, five-level, or higher-level converters. Moreover, different modulation techniques can be applied to the same converter, as is the case of the most traditional techniques, but some techniques are only feasible to specific converters, as is the case of techniques that are specially developed for a given converter in order to optimize, for instance, the switching losses.

In a voltage-source inverter, the modulation technique is responsible for transforming a given reference voltage into a set of defined states of the switching devices comprising the converter, so that the desired reference voltage or current, depending on the used feedback control, is produced at its ac side. The two most common groups of modulation techniques for voltage-source inverters, regardless of the number of voltage levels, are the pulse-width modulation (PWM) and the space vector modulation (SVM). However, these two groups of modulation techniques must be properly adopted when applied to multilevel converters.

Pulse-Width Modulation (PWM)

PWM is a modulation technique widely used in two-level and three-level inverters, where a single triangular carrier and one (in two-level inverters) or two (in three-level inverters) reference voltages are used. The popularity of this technique is

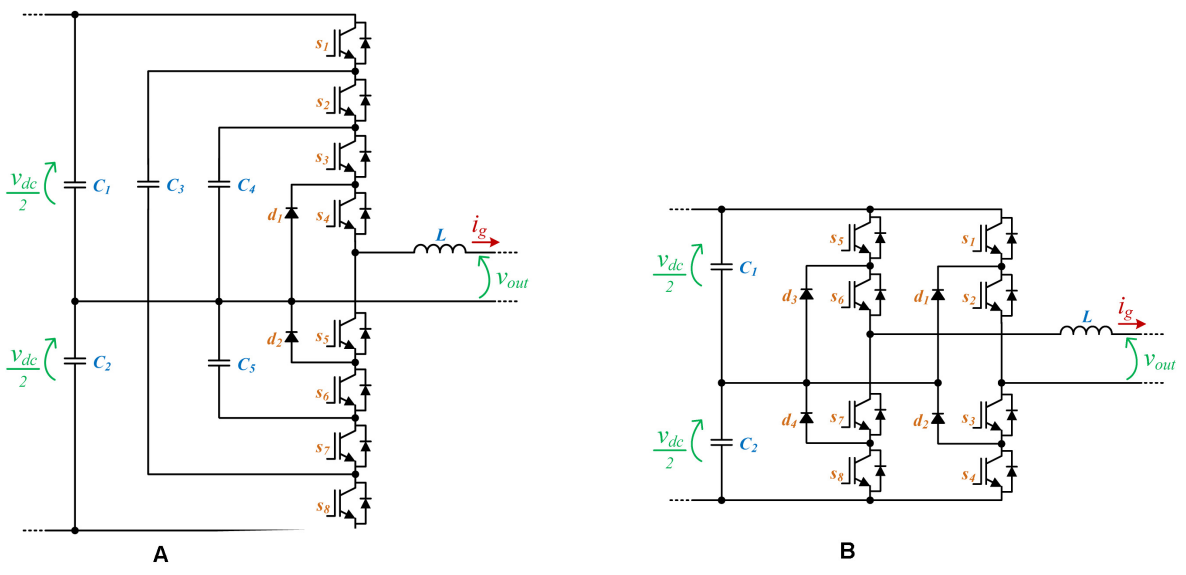

FIGURE 8 | Topologies: **(A)** proposed in Narimani et al. (2016); **(B)** proposed in Aly et al. (2018).

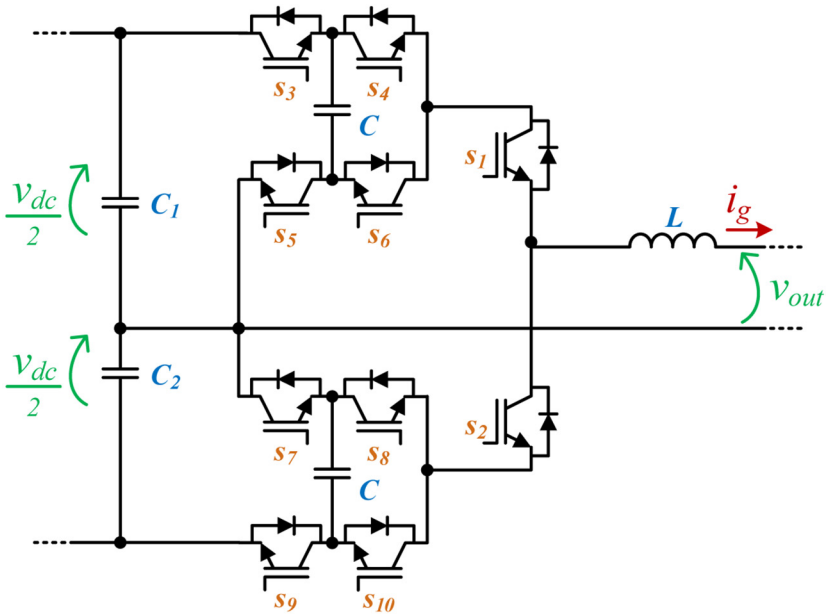

FIGURE 9 | Topology proposed in Naderi et al. (2015).

due to its ease of implementation, especially regarding digital signal processor (DSP)-based control systems, and due to the establishment of a fixed switching frequency, which is useful for sizing the output passive filters of the converter. Besides, since most inverters contain complementary pairs of active switches, one triangular carrier can be used to generate a pair of complementary signals for the switches. However, in multilevel converters, it is mandatory to use either more than one triangular carrier or more than two reference voltages in order to obtain the total number of possible voltage levels.

The classical multilevel PWM techniques consist of increasing the number of triangular carriers, which are either vertically or horizontally distributed, and the number of triangular carriers must be n-1, where n is the number of voltage levels. For the specific case of this paper, i.e., five-level inverters, four triangular carriers and one reference voltage should be used in order to attain a five-level operation with a classical multilevel PWM technique. Besides, taking into consideration the triangular carrier disposition, two main schemes can be feasible, i.e., with vertical disposition and horizontal disposition. In a vertical disposition-based PWM, all the carriers have the same amplitude and frequency but different average values, so that the maximum value of a given carrier coincides with the minimum value of the upper one, and so on. In this case, two of the carriers are only positive and the other two are only negative. In terms of phase, there are three main approaches regarding vertical-disposition PWM schemes: (a) phase disposition, where all the carriers have the same phase (**Figure 12A**); (b) phase opposition, where the positive carriers are 180° phase shifted with the negative carriers (**Figure 12B**); (c) alternative phase opposition, where the consecutive carriers are 180° phase shifted from each other (**Figure 12C**). Vertical disposition is suitable for topologies comprising a split dc link, such as NPC and flying capacitor, but can lead to power unbalances in topologies with independent dc links. Regarding horizontal distribution, this scheme is also termed as phase-shifted PWM, where all the carriers have the same amplitude, average value, and frequency but different phase angles. The phase shift between consecutive carriers should be equal to 360°/n, where n is the number of triangular carriers. Hence, in this case, each triangular carrier is 90° phase shifted from each other, as can be seen in **Figure 12D**. Another possibility is to use two reference voltages 180° phase shifted between each other (as in a unipolar PWM scheme) and only two triangular carriers obeying to a 180°/n ratio. In this case, the carriers are not evenly divided in one switching period due to the additional reference voltage, which emulates the two removed carriers, as can be seen in **Figure 12E**. Horizontal-disposition schemes have the advantage of multiplying the switching frequency (the frequency of each carrier) into the output frequency by a factor of n, (four, in this case), similarly to an interleaved converter. Compared to vertical disposition, this scheme allows a balanced power distribution in topologies such as cascaded multilevel and a natural voltage balancing in the flying-capacitor topology. Nevertheless, vertical-distribution schemes allow a lower THD in the output voltage than the horizontal distribution for the same characteristics of operation (Rodriguez et al., 2002, 2007; Kouro et al., 2010; Malinowski et al., 2010; Debnath et al., 2015; Li et al., 2015).

However, depending on the available resources, the use of multiple triangular carriers can also be an obstacle. One method to suppress this is to use a single triangular carrier but different reference voltages, also called modified reference

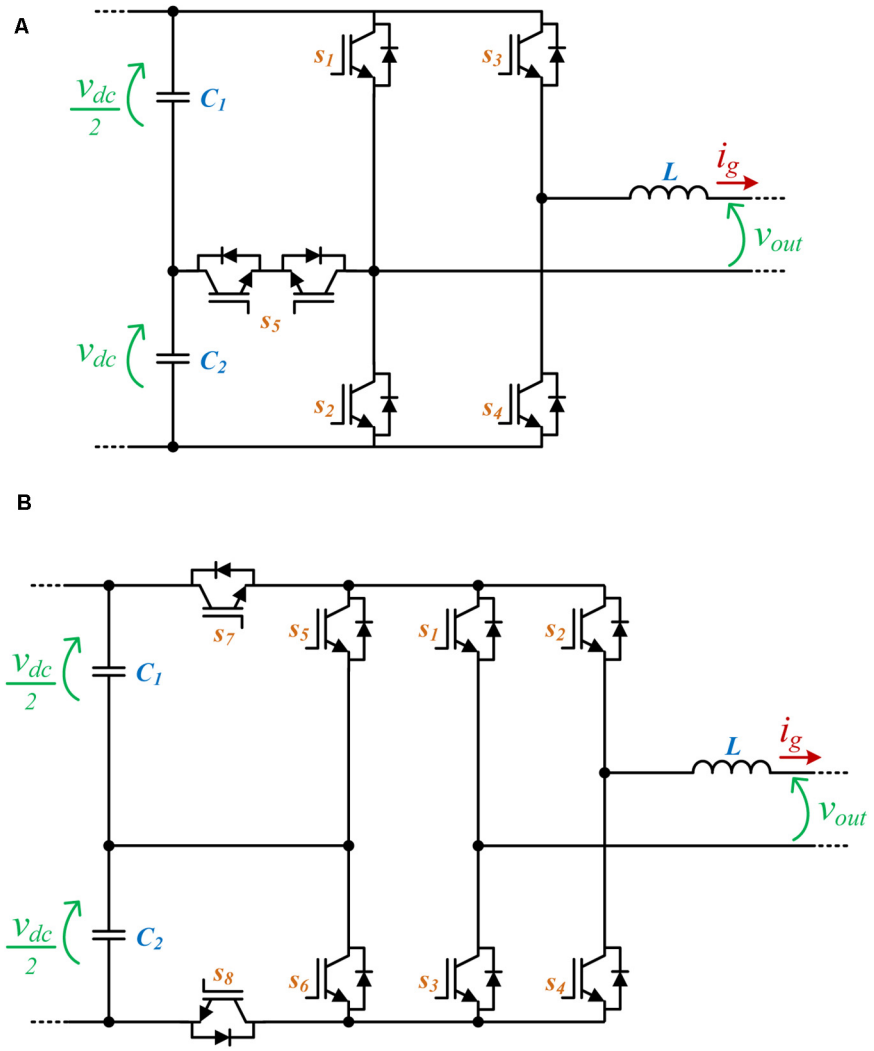

FIGURE 10 | Topologies: **(A)** proposed in Monteiro et al. (2016); **(B)** proposed in Leite et al. (2018).

voltages. Therefore, each complementary pair of signals for the active switches is achieved not from each triangular carrier but from each reference voltage. This approach can also be used to optimize the switching frequency of a multilevel converter. For instance, in Leite et al. (2018), a modulation strategy is implemented that allows an active switch pair to operate with a switching frequency equal to the low-frequency component of the output voltage, i.e., the power grid frequency. This allows reducing the switching losses of the converter or, even further, to apply a different type of power semiconductor that does not need to be fully controlled (e.g., thyristor), offering lower conduction losses and a lower cost. **Figure 12F** shows an example of this modulation scheme, where one carrier and two references can be seen, generating three pairs of switch signals.

Space Vector Modulation (SVM)

While the PWM techniques are based on the modulation of each complementary pair of active switches, the SVM technique consists of acting upon the converter as a whole. This means that, in each instant, the state of all the active switches comprising the converter is determined in order to satisfy a given reference voltage. This is achieved via a coordinate transformation from *a-b-c* to α-β, where the reference frame is divided into sectors that contain a given output voltage. In order to synthesize the desired voltage (which is contained in a given sector), two adjacent voltage vectors (which are produced by a given converter state) should be used, with the length of each one being proportional to the on-time of each converter state. Compared to PWM, SVM also allows a fixed switching frequency but reduces the total number of commutations of a given switch in each output cycle,

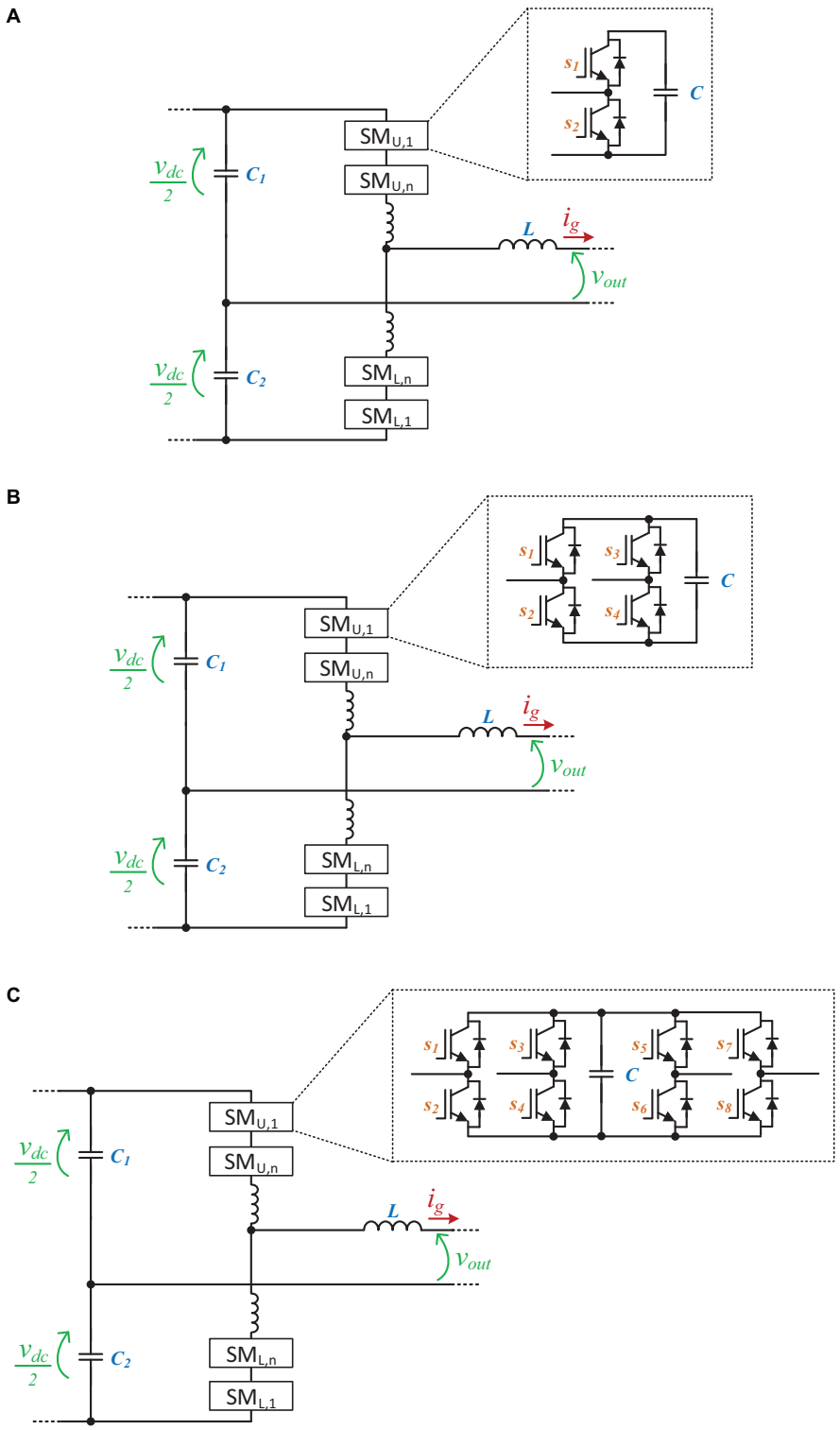

FIGURE 11 | MMC topologies: **(A)** proposed in Zhou et al. (2018); **(B)** proposed in Hu et al. (2018); **(C)** proposed in Goetz et al. (2015).

since each switch state can be assigned in a way that avoids redundant switching. A similar strategy, called pulse decoding, can be seen in Ge and Fang (2008), where only one switch pair switches at high frequency. Moreover, SVM allows a better utilization of the dc-link voltage, since it inherently comprises a third harmonic injection that allows achieving an output

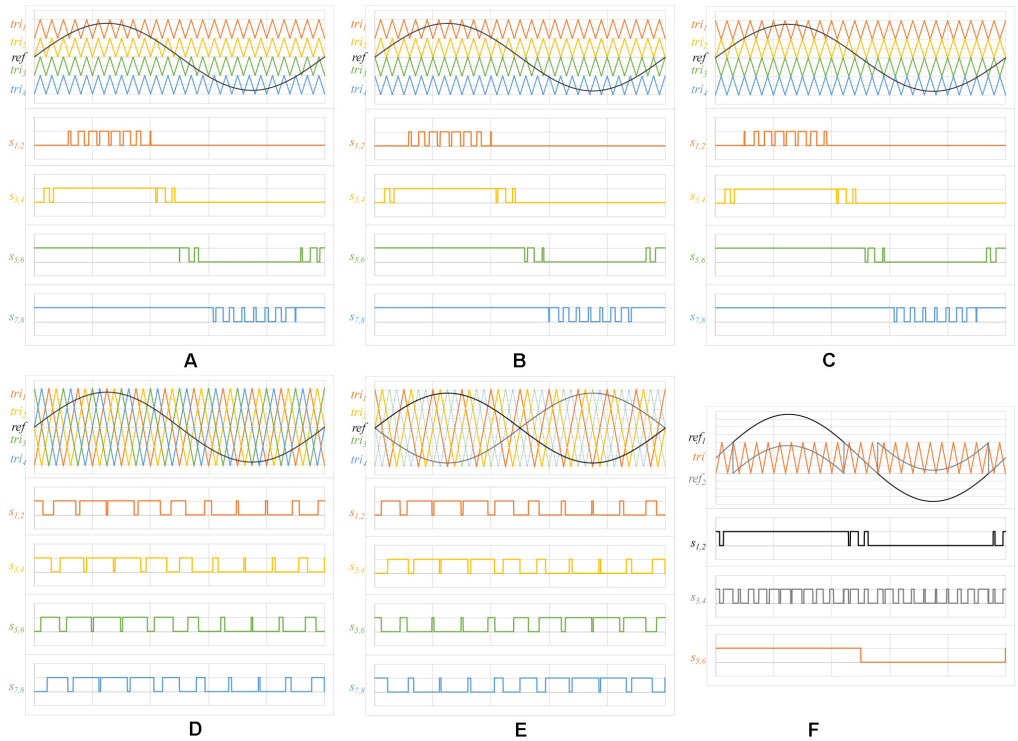

FIGURE 12 | Pulse-width modulation: **(A)** vertical phase disposition PWM carriers for five-level inverters; **(B)** vertical phase opposition PWM carriers for five-level inverters; **(C)** vertical alternative phase disposition PWM carriers for five-level inverters; **(D)** horizontal disposition PWM carriers for five-level inverters using based on four carriers and one reference voltage; **(E)** horizontal disposition PWM carriers for five-level inverters based on two carriers and two reference voltages; **(F)** horizontal-disposition PWM carriers for five-level inverters using a single carrier and a modified reference voltage.

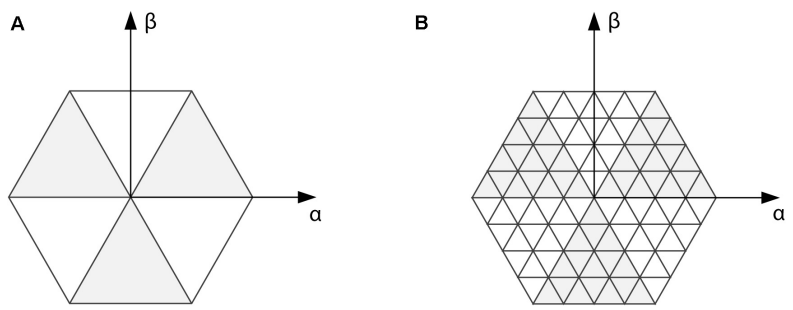

FIGURE 13 | Space vector representation for three-phase inverters: **(A)** two-level; **(B)** five-level.

voltage 15% higher than PWM for the same dc-link voltage and modulation index. Due to this reason, SVM is an interesting modulation technique to be applied in three-phase inverters for three-wire systems, as is the case of traction applications, for instance (Kanchan et al., 2005; Vinod et al., 2018). The main disadvantage of SVM compared to PWM is its complexity, requiring calculations that do not exist in PWM.

In multilevel converters, SVM is attainable through a higher number of sectors, as well as a higher number of voltage vectors. While three-phase two-level converters allow six non-null voltage vectors and six sectors, as can be seen in **Figure 13A**, three-phase five-level converters allow sixty non-null and non-redundant voltage vectors, comprising a total of ninety-six sectors, as represented in **Figure 13B**. Each triangle represents a sector, while each triangle vertex represents one voltage vector. The number of voltage vectors depends on the nature of the converter, i.e., whether it allows redundant states (multiple voltage vectors to produce the same output voltage) or not (only one voltage vector to produce a given output voltage) (Dae-Wook et al., 2003; Ahmed et al., 2016; Li et al., 2017).

TABLE 2 | Comparison between the presented topologies.

Category	References	Number of switches[a]	Number of diodes	Number of sources	Number of caps	Needs split dc link	Number of inductors	$\frac{V_{out,\,max}}{V_{in}}$	Output voltage levels	Control complexity	Fault tolerant
With flying capacitors	Korhonen et al., 2014	8n	8n	1	N	Yes	0	1/2	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	No
	Yuan, 2014	8n	6n	1	N	Yes	0	1/2	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	No
	Vahedi et al., 2016	6n	6n	1	N	No	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	**	No
	Saeedian et al., 2018	7n	10n	1	2n	No	0	2	$\pm 2v_{dc}$, $\pm v_{dc}$, 0	**	No
	He and Cheng, 2016	12n	12n	1	4n	No	0	4	$\pm 4v_{dc}$, $\pm 2v_{dc}$, 0	**	No
	Narimani et al., 2016	8n	10n	1	3n	Yes	0	1/2	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	No
	Naderi et al., 2015	10n	10n	1	2	Yes	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	***	No
Without flying capacitors	Sajadian and Santos, 2014	4n	6n	1	0	No	1	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	*	No
	Masaoud et al., 2014	4n + 4	4n + 4	2	0	Yes	0	1	$\pm v_{dc}$, $\pm 3v_{dc}/4$, $\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	*	No
	Madhukar Rao and Sivakumar, 2015	7n	10n	1	0	Yes	0	1/2	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	*	Yes
	Gautam et al., 2017	8n	8n	1	0	No	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	***	Yes
	Aly et al., 2018	14n	18n	1	0	Yes	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	***	Yes
	Monteiro et al., 2016	5n	9n	1	0	Yes	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	**	No
	Leite et al., 2018	8n	8n	1	0	Yes	0	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	**	No
Modular methods	Zhou et al., 2018	8n	8n	1	4	Yes	2	0.5	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	No
	Hu et al., 2018	8n	8n	1	2	Yes	2[b]	0.71	$\pm v_{dc}$, $\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	Yes
	Hu and Jiang, 2014	4n	4n	1	2	Yes	2[b]	0.5	$\pm v_{dc}/2$, $\pm v_{dc}/4$, 0	***	No
	Goetz et al., 2015, 2016	16n	16n[c]	2	2	Yes	2	1	$\pm v_{dc}$, $\pm v_{dc}/2$, 0	**	Yes

[a]*Anti-parallel diodes of the IGBTs are considered separate components, as is the case in many applications.* [b]*Relatively large inductors.* [c]*With half the rated current on each switch.* ***high; **medium; and *low.*

SVM is advantageous over PWM when the number of levels is very high, i.e., when controlling the converter as a whole is simpler to implement instead of controlling each complementary switch pair.

COMPARISON BETWEEN TOPOLOGIES

This section presents a comparison regarding the topologies identified in section "Topologies of Five-Level Front-End Converters." The comparison was performed considering three main categories: with flying capacitor, without flying capacitors, and MMCs. For all the topologies, the key parameters were considered. **Table 2** shows the comparison between the topologies. Analyzing this table in more detail, the MMC topologies (Goetz et al., 2015, 2016) requires more devices (diodes and switching devices), which can be identified as a disadvantage since it can increase the conduction and switching losses, contributing to a reduction in efficiency. Besides the MMC topologies, the topology (Masaoud et al., 2014) requires two sources and is the only topology with this requisite, which can be impeditive for applications as renewables since two independent sources are required. The topology (Sajadian and Santos, 2014) requires the use of a transformer, which can be a disadvantage, but it only requires a single source and no capacitors for obtaining the five voltage levels. Topologies (Sajadian and Santos, 2014; He and Cheng, 2016; Vahedi et al., 2016; Gautam et al., 2017; Saeedian et al., 2018) require a single dc link, i.e., a split dc link is not necessary for the operation with five levels; therefore, for applications as renewables, this is an interesting aspect. Since fault tolerance and reliability issues are not the main focus of this review, only a few examples of the more recent topologies (Madhukar Rao and Sivakumar, 2015; Gautam et al., 2017; Hu et al., 2018) were considered. Considering the fault-tolerant topologies, it is clear that higher tolerance to fault comes at the cost of a significantly higher number of active components.

The main problem in the methods based on the flying capacitors is the control complexity. When the capacitor voltage is a fraction of the supply voltage, then the controller should monitor the voltage of that capacitor and actively maintain it in a tight boundary. On the other hand, the methods based on the multiple/split sources are more expensive to implement in the end, since they require either separate power sources or keeping the split-source voltage considering all the inherent differences in the system. The capacitors of the split dc link may exhibit a difference in voltage sharing, causing a voltage ripple in the dc link. Consequently, the stabilization of the voltage ripple may require a considerably large dc-link capacitor. In addition, any imbalance in the load causes a neutral current, which causes a perturbation in the split dc-link voltage (Jasna and Anitha, 2014). Consequently, balancing the split dc-link capacitors is the subject of a proper control. Therefore, as happens always in engineering applications, here a trade-off should be maintained on the control complexity, sensor requirements, fault tolerance, and cost. Regarding the topologies based on modular structures, only a few of them are present, since the main advantage of such methods is framed in higher voltage levels. Therefore, as a five-level converter, modular multilevel methods are not very economical.

Regarding the number of semiconductors, it is commonly known that a higher number of passive semiconductors contribute to a decrease in the cost and the control complexity of the inverter but negatively affect its efficiency (Graditi et al., 2011). Consequently, the additional production of heat contributes to an increase in the requirements on system cooling, as well as to an acceleration in the aging of semiconductors (Reynolds, 1974). In this context, higher efficiency is generally achieved by trading the number of passive semiconductors (e.g., diodes) and active semiconductors (e.g., MOSFETs and IGBTs) (Kyono, 2006). Naturally, a higher overall number of components in the inverter, both passive and active, lowers its reliability, if the components do not introduce fault-tolerance itself (Zhang et al., 2014).

CONCLUSION

Worldwide, distributed renewable-energy resources are seen as absolutely fundamental to accomplish with the target to minimize environmental concerns, to obtain access to affordable energy, and to contribute to a sustainable power grid. Over the past few decades, in order to enable the increasingly effective integration of renewable-energy sources, power electronics technologies have played a leading role. In fact, even today, power electronics technologies are seen as one of the fundamental challenges for the widespread use of renewable-energy sources. Embracing this context, this paper presents a review of power electronics converters that can be used for interfacing renewable-energy sources into the power grid, concentrating on front-end converters with a voltage-source structure. More specifically, in a more attractive future perspective, this review is only focused on five-level structures. Thus, throughout the paper, the most relevant five-level topologies for the contextualization of renewable-energy sources in smart grids are presented. As a result, an effective comparison between the topologies is presented, highlighting key aspects that are useful to select a topology in detriment of others, according to the number of passive and active semiconductors, sources, capacitors, split dc links, inductors, and voltage levels. As an example, based on the established comparison, it is possible to conclude that topologies with more than one source are not advantageous and, on the other hand, topologies with a single dc link represent an interesting aspect for renewable-energy source applications. Based on the established comparison, it is possible to conclude that topologies with more than one source are not advantageous and, on the other hand, topologies with a single dc link represent an interesting aspect for renewable-energy source applications. The comparison also shows that topologies with a flying capacitor are not ideal concerning fault-tolerant characteristics, and a topology that accomplishes with the combined criteria such as being fault-tolerant, flying capacitors being unnecessary, and with reduced control complexity, which are three relevant features for obtaining reliable and high-efficiency converters to interface

renewable-energy sources with the power grid, was identified. The topologies that require lower control complexity are all based on structures independent of flying capacitors, which is understandable, since such capacitors require a dedicated control loop. Moreover, such topologies require additional hardware, such as sensors and signal conditioning circuits. On the other hand, the topologies based on modular structures require more control complexity, since these structures are based on submodules (i.e., constituted by half-bridge or full-bridge converters). Notwithstanding, it is important to emphasize that the objective of this paper is not directly related to the identification of a specific topology that complies with all the benefits under study; it has the goal of presenting the different advantages and disadvantages of each topology in order to facilitate the comparison of such topologies for different purposes.

AUTHOR CONTRIBUTIONS

VM, NT, TS, and TK contributed to writing the manuscript. JA and SG contributed to review the manuscript and to present suggestions and corrections. All authors contributed to the article and approved the submitted version.

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