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Coordination and control of power converters in modern power systems

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Coordination and control of power converters in modern power systems

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A switching control method based on a new model considering parasitic capacitance for LLC

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LLC converters are used for linking renewable energy and smart grids. However, the output is higher than the reference caused by its own characteristics, especially in the light load, and the output is limited. A new control method is proposed in this paper based on a new model considering parasitic capacitance, which plays a vital role in keeping the output constant in the light load conditions and widening the output range. In addition, the definition of the light load is given in this paper, which ensures an accurate control. In the switching process, a transition period is set to avoid the components from being damaged due to sudden switching and ensures a smooth output and the stability of the control. Finally, this control method based on the new model is proved valid on a 400 V-36 V-1 kw prototype.

KEYWORDS

DC-DC converter, half bridge, full bridge, digital control, topological changes

1 Introduction

As smart grids advanced, great challenges were faced with power electronic devices (Hu et al., 2022; Wang et al.). The converter connects the smart grid to renewable energy, which requires the output constant, high power density, and high efficiency (Ma et al., 2022). DC–DC converters have two types on account of the transformer (Wang et al., 2022b; Hu et al., 2022). The non-isolated converters are applied to this solution, where the input and output have little difference. The isolated DC–DC converters are applied when the input and output greatly differ in value. Considering the bidirectional energy, DAB has a symmetrical structure that includes an inductor and a transformer (Huang et al., 2016; Liao et al., 2021). In addition, there was too much loss due to the limited range of soft-switching and reflux power, which can strengthen the reactive power (Song et al., 2018; Jeung and Lee, 2019). In Lu et al. (2018), a new topology was proposed to achieve soft-switching and ensure stability but backflow power was not addressed. A new control method that mixes power balance and unified phase shift was discussed, but only the current spike was optimized and additional losses were added (Hou et al., 2019). Although there are many ways to reduce the loss, the problems caused by the structure are not

completely solved. Compared with DAB, LLC has many advantages such like soft-switching, less power loss, and lower stress.

The LLC converter is widely used as an intermediate link in the transmission of energy to keep the voltage constant, which can achieve soft-switching due to its topology. There are one capacitance and two inductors that cause the current flow through the resonance cavity before voltage in this topology (Lee et al., 2014). Many problems come with advantages, such as the loss of the diodes. The transformer current sensing triggers the drive signal for the synchronous rectifier to reduce loss (Zhang et al., 2012). In addition, the transformer coil is added to eliminate the influence of excitation inductance so as to obtain an accurate synchronous rectification conduction time (Wang K. et al., 2022). The additional driver circuits in the aforementioned method also add new losses. By analyzing the small-signal characteristics of the resonant capacitor, the control method has been proposed for precise output voltage (Kang et al., 2017). Hence, digital control is used to avoid extra loss. The drain-to-source voltage of the synchronous rectifier is detected for the synchronous rectifier, but the current caused by the electromagnetic interference can be rough (Feng et al., 2010) By the pulse width-locked loop to get the synchronous rectifier conduction time, the diodes loss is diminished (Feng et al., 2013). Although the proposed control method has a fast reaction speed, the programmer is too complex to finish hard (Li et al., 2020). The reference is lower than the output voltage when the light load condition, the hybrid-adjustable switching-frequency-duty-cycle modulation, is proposed for adjusting the output and improving efficiency (Awasthi et al., 2021). A two-stage voltage modular for LLC converters is discussed by Fei et al. (2017), which can reduce the loss of switches, but add extra circuit loss. In addition, one method is adjusted to avoid noise in the light load condition (Yoon et al., 2018). The commutation direction can be obtained by analyzing the phase between switches to reduce the loss (Kundu et al., 2017). The two stages of converters based on the full load condition are given to the lower output voltage, which is applied to a meagre output (Ahmed et al., 2017). The new topology has been applied for widening the output voltage range but with the addition of an extra loss (Xue et al., 2021). The addition of a switch and a capacitor to is provided to improve efficiency (Lee et al., 2015), and this paper proposes to add SCC to the topology for keeping voltage (Hu et al., 2014). But the loss has been increased invisibly. Meanwhile, the LLC converter has a DC bias in the reversed mode. The symmetric topology called CLLC is proposed for reducing the deviation (Jung et al., 2013). The LLC and DAB converter are combined for dismissing the DC bias with complicated calculations (Liu et al., 2017). In addition, an extra inductor is eliminated to the DC bias in the reversed mode (Jiang et al., 2015), which is adopted in this paper, and a bidirectional three-level LLC resonant converter is given for a widened output (Jiang et al., 2016). The DC bias is eliminated by controlling the synchronous rectification signal, whereas it is too complex to be applied (Li et al., 2022; Li et al., 2022).

According to the aforementioned disadvantages, a switching control method for bidirectional LLC converters is proposed under light load conditions to improve the efficiency and keep the output constant and widen the output range. This paper contributes the following.

1) One LLC converter model with parasitic capacitance is discussed, which can more accurately describe the situation, especially under the light load. The gain curve of this more realistic model is more accurate than that of the traditional model.
2) A control method is presented to make the output voltage close to the reference value and improve the efficiency under the light load, which includes two modes. The HB mode and FB mode are applied in this paper for maintaining the output voltage and widening the output range.
3) The definition of the light load is given in this paper, which is calculated by the gain curve of this new model. The HB and FB switching points vary under different load conditions for precise control. In addition, the switching period is adjusted to ensure the output smoothly and the stability of the control.

The paper is organized as follows. The new model considering parasitic capacitance is given in Section 2. The control method based on this and the definition of the light load is discussed in Section 3. Also, the principle is proved valid in Section 4 by a 400 V-36V-1 kW prototype.

2 The model considering the parasitic capacitance

2.1 The traditional model

There are two inductances that play an essential role in excitation, while another one and capacitance are in resonance. The forwarding mode is only mentioned, and the forwarding mode and reversed mode have the same state due to a symmetrical topology, as shown in Figure 1A. The gain curve of this topology is shown in Figure 1B. The soft-switching is achieved on the right of peak, an ideal operating area for the LLC converter. The peak goes down with the increasing load. The PI controller has been used in this model, which adjusts the output voltage by adjusting the switching frequency. The frequency is varied on the basis of the gain curve: the switching frequency increases when the load decreases. The duty ratio maintains 50%, and S1 and S2 keep complementary, the same as S3 and S4. The synchronous rectification strategy, which reduces the switching loss, is that the secondary switches are controlled by the PI controller, and

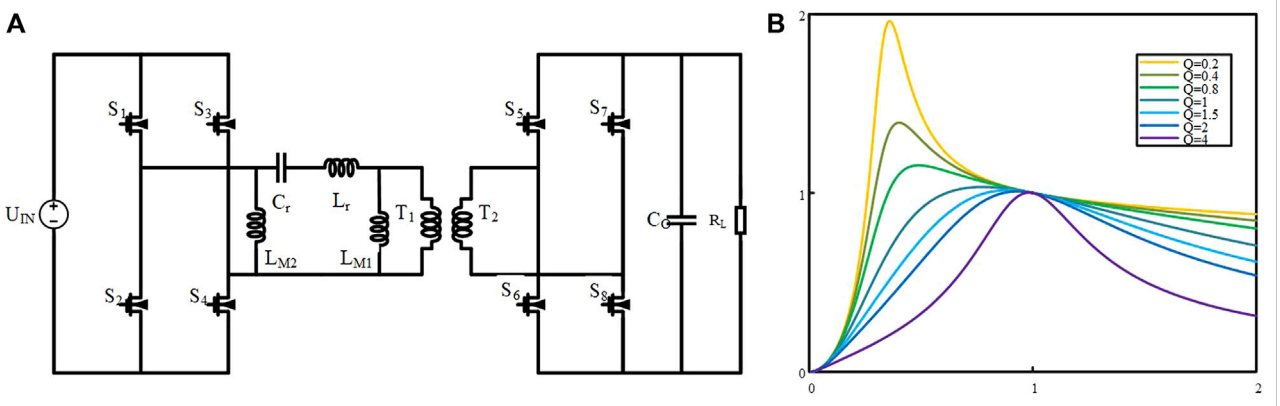


FIGURE 1
(A) Traditional bidirectional LLC model. **(B)** Gain curve of traditional topology.

the drive signal frequency of those switches keeps pace with the primary switches.

Many problems are faced in the traditional model, especially at the light load condition, where the output voltage is limited by its character. The voltage is higher than the reference, which is settled in advance. When the frequency increases to a certain value, the voltage increases instead, which is inconsistent with the obtained gain curve. Therefore, a new model has been established so that the traditional model runs counter to the reality under the light load condition.

2.2 The model with parasitic capacitance

The parasitic capacitance of the transformer is considered in this new model, which is more realistic than the traditional model. The transformer has two windings and stray capacitances, C_1 and C_2, which are the self-capacitances of the transformer. C_0 is the mutual capacitance between the primary and secondary sides. Generally, the parasitic resistances of windings are ignored due to the value being too small, as shown in Figure 2A. The secondary side is converted to the primary side, where the stray capacitances are expressed as in Eq. 1, and the windings are replaced by the inductance and magnetic core in Figure 2B. The stray capacitance can be simplified as in Eq. 2 which is calculated by the two-port net approach (Lu et al., 2003) since the effort of C_{s0} is insignificant. The SR junction capacitance is included in this model, and the parasitic capacitance can finally be described by Eq. 3. The capacitance circled in red is equivalent to the resulting parasitic capacitance in Figure 2D.

$$\begin{cases} C_{s1} = C_1 + (1-n)C_0 \\ C_{s2} = n^2 C_2 + n(n-1)C_0 \\ C_{s0} = nC_0 \end{cases} \quad (1)$$

$$C_{str} \approx C_{s1} + C_{s2} \quad (2)$$

$$C_P \approx C_{str} + C_{SR} \quad (3)$$

Some things are known before analyzing the LLC converter. The switching model is idealized without loss. In addition, the parasitic capacitance is placed in front of the transformer. Voltage commutation and current commutation exist in every cycle, in which the first half and the second half of the cycle are the same. Hence, only the half-cycle has been described based on the PI controller under the light load condition in the following.

Mode1 (t_0-t_1): S_1 and S_4 are turned on and S_2 and S_3 are turned off. At this period, L_r and C_p are in resonance owing to the value of the magnetic inductors being higher than the resonant inductor and the C_p being higher than the C_r. Therefore, the voltage of the resonance cavity is approximately zero, and the current increases gradually as shown in Figure 3A.

Mode2 (t_1-t_2): All switches are all off in this period as shown in Figure 3B. The voltage changes its direction, and voltage V_{ab} is reversed. The L_r and C_P keep resonance until the resonance current equals the magnetic current, as shown in Figure 3D.

Mode3 (t_2-t_3): The resonance current is smaller than the magnetic current. Therefore, the voltage drop is limited by the secondary side. In this period, the resonance cavity has been in resonance where C_r and L_r occur, and there is no other resonance. This mode lasts when the current in L_{M2} equals to the current in the resonator. The current reversal ends when this mode ends, and the second half period is the same due to the symmetric structure.

FHA is adopted for analyzing this model, which only leaves the fundamental component as the object of the study. The circuit, as shown in Figure 4, can be simplified, in which V_{ab} is the voltage at the midpoint of the two bridge arms and R_{eq} is converting the actual load to the original side. The relationship between the input voltage and V_{ab} is described as

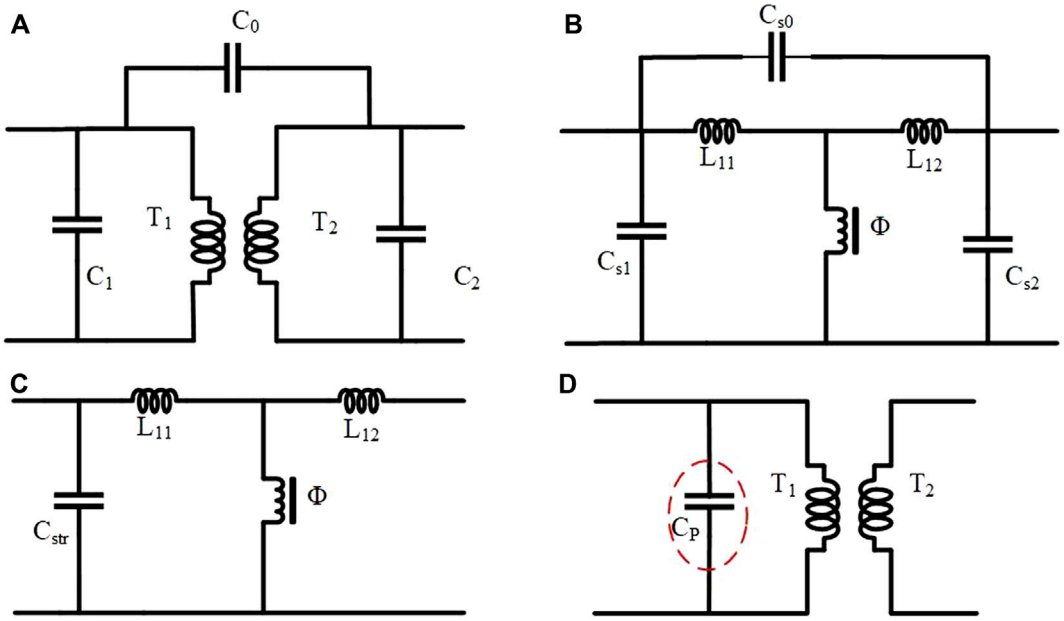


FIGURE 2
(A–D) The model considering parasitic capacitance.

in Eq. 4, and the same can be the relationship between the output voltage and V_{cd} (Eq. 5).

$$V_{ab} = \frac{4V_{in}}{\pi}\sin \omega t \tag{4}$$

$$V_{cd} = \frac{4nV_{out}}{\pi} sin\, \omega t \tag{5}$$

$$G = \frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{\left(1 + \frac{1}{k} - \lambda x^2 - \frac{1}{kx} + \lambda\right)^2 + \left(x - \frac{1}{x}\right)^2 Q^2}} \tag{6}$$

$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{eq}},\ x = \frac{f_s}{f_r}, k = \frac{L_{M1}}{L_r}, \lambda = \frac{C_p}{C_r} \tag{7}$$

The voltage gain shown in Eq. 6 can be obtained by substituting the formula and simplifying it based on the voltage partition principle. λ is the ratio of the parasitic capacitance and resonant capacitance. Q is the quality factor, in which the value equals the ratio of the reactive power to active power. The switching frequency is standardized and shown as x, and the resonant frequency is taken as the reference. k is the ratio of the excitation inductance to the resonant inductance. The aforementioned parameters can be expressed by Eq. 7. The gain curve is shown in Figure 5, which has two voltage peaks. The circuit has come into the inductive region, where soft-switching can be achieved after the first peak, and the circuit works in this region generally. The secondary peak caused by the parasitic capacitance significantly impacts the output voltage, and the gain curve, when Q is fixed, is greater the parasitic capacitance, the higher the peak value.

3 The control method for the model considering the parasitic capacitance

The control method for the new model considering the parasitic capacitance is proposed to solve the problem under the light load condition, which includes two modes: half-bridge (HB) mode and full-bridge (FB) mode. This proposed control method is applied for widening the output range and is kept constant under the light load condition. According to Figure 5, the boundary between the light and heavy load can be calculated. Taking the derivative of the gain, Eq. 8 can be obtained.

$$F(x) = 2\lambda^2 x^8 + \left[\frac{2}{k}\left(1 + \frac{1}{k} + \lambda\right) - Q^2\right]x^2 - \left[2\lambda\left(1 + \frac{1}{k} + \lambda\right) - Q^2\right]x^6 - 2k^2 \tag{8}$$

$$f(x) = R_{eq}^2 - \frac{L_r C_r}{2\left[C_p^2 + C_r C_p\left(1 + \frac{L_{M1}}{L_r}\right)\right]} \tag{9}$$

$$R_{eq} = \frac{8n^2}{\pi^2} * \frac{V_O^2}{P} \tag{10}$$

The curve with two spikes can be denoted as the light load, and the parameters are substituted into Eq. 9. The light and heavy loads are divided by Eq. 9. R_{eq}, which is the equivalent resistance of the secondary side (10), belongs to the pure resistance load, as expressed by Eq. 10, which can be regarded as under the light load condition caused by the load being very small. After sampling the output voltage and current, the calculated resistance is substituted into Eq. 9. When the equation is

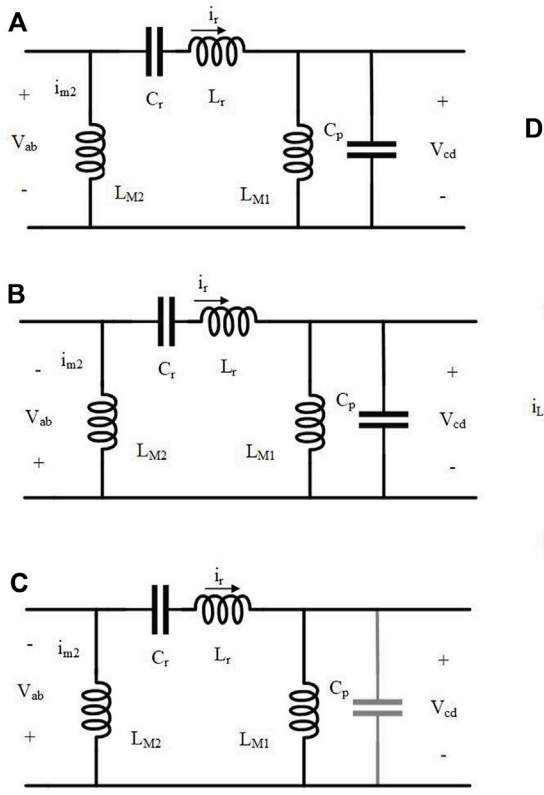


FIGURE 3
(A–C) Mode analysis and **(D)** waveforms of the circuit in full-bridge.

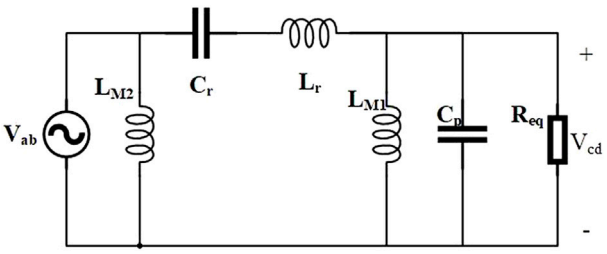


FIGURE 4
The simplified model considering the parasitic capacitance.

greater than zero, the load is deemed as the light one. When the frequency is at the left of the switching point, a traditional PI controller mentioned previously is adopted under light load conditions. At this period, the topology is in the FB mode, in which S_3 and S_4 keep in sync with S_2 and S_1. The topology becomes HB mode when the switching frequency is higher than the switching point.

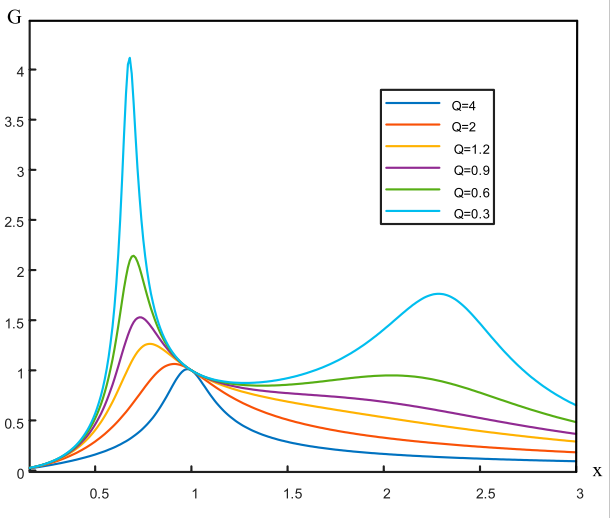


FIGURE 5
Gain curve when Q is fixed.

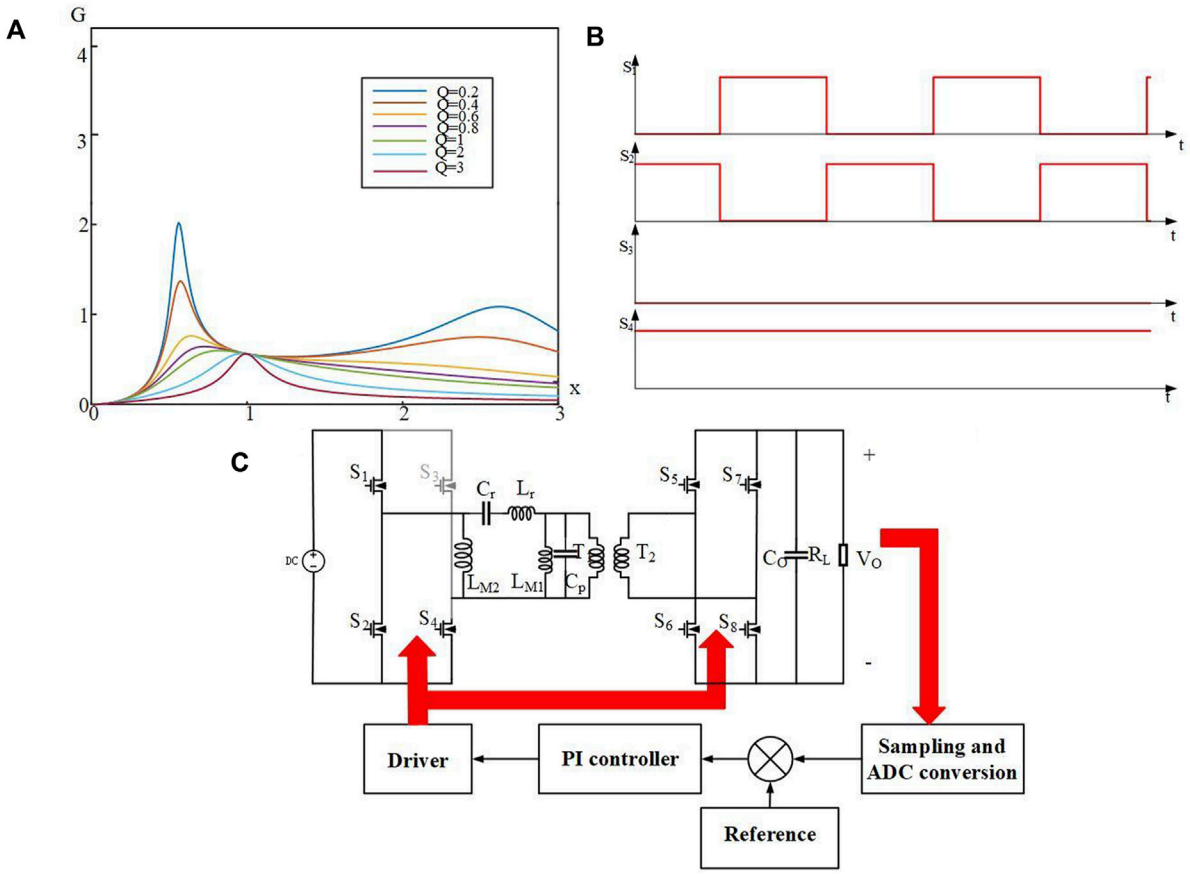


FIGURE 6
(A) The gain curve in the HB mode; **(B)** the driver signal in the HB mode, and **(C)** the LLC converter circuit structure.

S_3 keeps off normally, while S_4 keeps on in the HB mode, as shown in Figure 6A. The first bridge arm has maintained 50% duty approximately and remained complementary, and the frequency of switches is controlled according to the gain curve shown in Figure 6B. V_{ab} becomes half in the FB mode. The secondary side switches are consistent with the primary side in frequency as a synchronous rectification scheme. The working state of the resonator in the HB mode is the same as that in the FB mode, in which the parasitic capacitance and resonance are in resonance before current commutation.

When switching the modes, the output voltage is kept constant without a giant ripple so that the ratio of the voltage and frequency tends to be zero. The ratio is equal to the value of the derivative approximately. In the heavy load, Eq. 8 has only one solution greater than zero, which is the minimum switching frequency. The maximum switching frequency related to the gain range of the output is artificially limited and is defined as f_{P2}. If the output voltage is required to be large, the value of f_{p2} is high, while if the output voltage is required to be small, the value of the f_{p2} is low, as shown in Figure 7A. The switching frequency f_s is greater than f_{p1} at the heavy load when the switching frequency increases and the output voltage decreases.

When Eq. 8 equals zero under the light load, two of the solutions are chosen as the switching point, named f_{s1} and f_{s2}, respectively, as shown in Figure 7B. Due to the parameters in this circuit, there are three possible values of f_{s2}, greater than 1, less than 1, and equal to 1. It is of no sense to discuss the solutions that f_{s2} is less than or equal to 1 due to the reason of the extreme parameter values. The solution of f_{s2} greater than one is discussed as follows. Under the light load, the switching frequency, f_s, is greater than fs1 and less than f_{s2}, and the output voltage decreases with the increase of switching frequency. When the switching frequency is greater than f_{s2}, the output voltage increases with the increase in the switching frequency. Also, the switching points in the half-bridge mode and full-bridge mode are the same.

In the HB mode, the switching frequency decreases when the load increases. When the frequencies of S_1 and S_2 decline to f_{p1} or f_{s1} and the output is still less than the reference value, the mode is switched to the FB mode and the frequencies of S_1 and S_2 keep

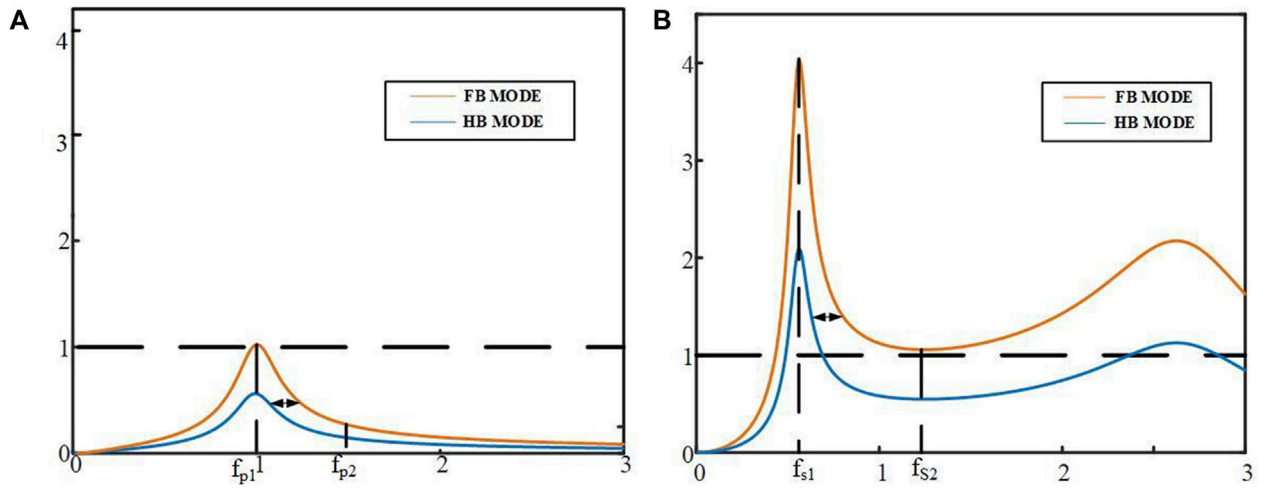


FIGURE 7
(A) Switching topology in the heavy load. **(B)** Switching topology under the light load.

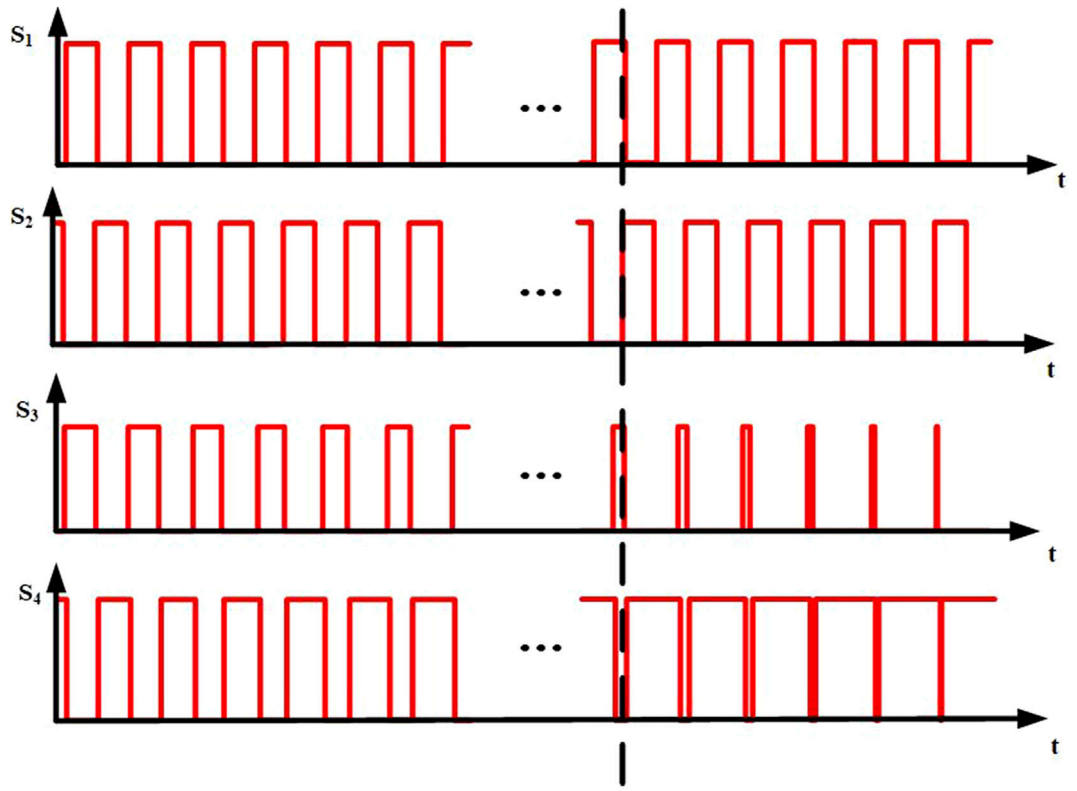


FIGURE 8
Drive signal during transition.

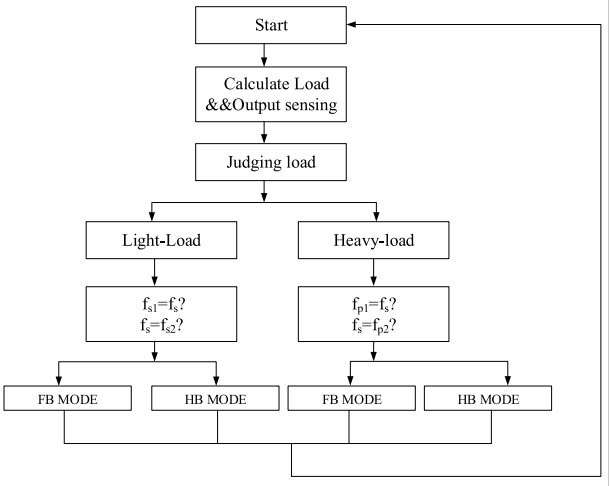
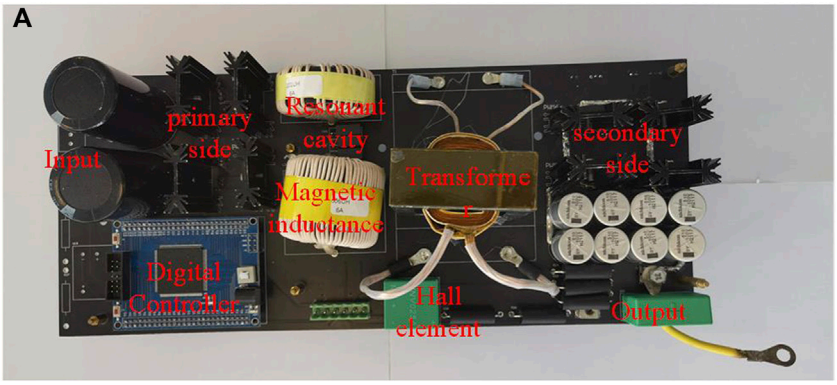


FIGURE 9
Control process.

varying. In the FB mode, the load decreases and the switching frequency increases. When the switching frequency increases to f_{p2} or f_{s2} and the reference value is less than the output voltage, the mode is switched to the HB mode.

Suppose the signals of S_3 and S_4 vary in one period after arriving at the switching point, then the inductors lose the volt-second balance, and the components may be penetrated after reaching saturation due to the tremendous impact caused by topology mutation. Since the controller has a slow signal corresponding to this circuit, the switching time is extended to reduce the influence caused by topology change.

The duty cycle changes in the process of mode switching. The S_3 duty cycle changes from 0 to 50%, and the S_4 duty cycle changes from 100 to 50%. Mode switching is implemented in several cycles to prevent voltage spikes and current spikes in the changing process. In the variation, S_1 and S_4 end simultaneously in one cycle, while S_2 and S_3 end simultaneously, which is kept



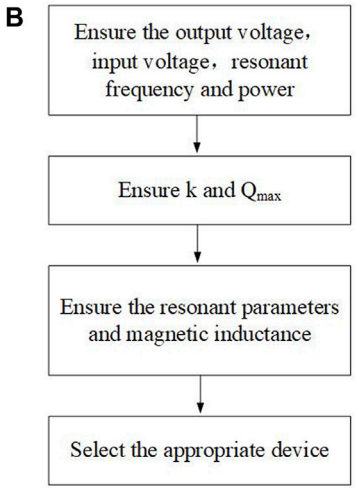


FIGURE 10
(A) The prototype. **(B)** The parameter calculation procedure.

TABLE 1 Detailed parameters in the prototype.

Parameter	Value
Resonance inductor	L_r = 101 μH
Resonance capacitance	C_r = 24.6 μH
Magnetic inductance	$L_{M1} = L_{M2}$ = 606 μH
Ratio of transformer	n = 12
Resonance frequency	100 k

complementary to ensure that the circuit is running correctly, as shown in Figure 8. During transition, the switching frequencies of S_1 and S_2 continue to be regulated by the PI controller. The switching frequencies of S_1 and S_2 are adjusted without considering the duty cycle changes of S_3 and S_4 for maintaining the output constant. The switching frequency of the first arm bridge decreases with the increasing load and increases with the

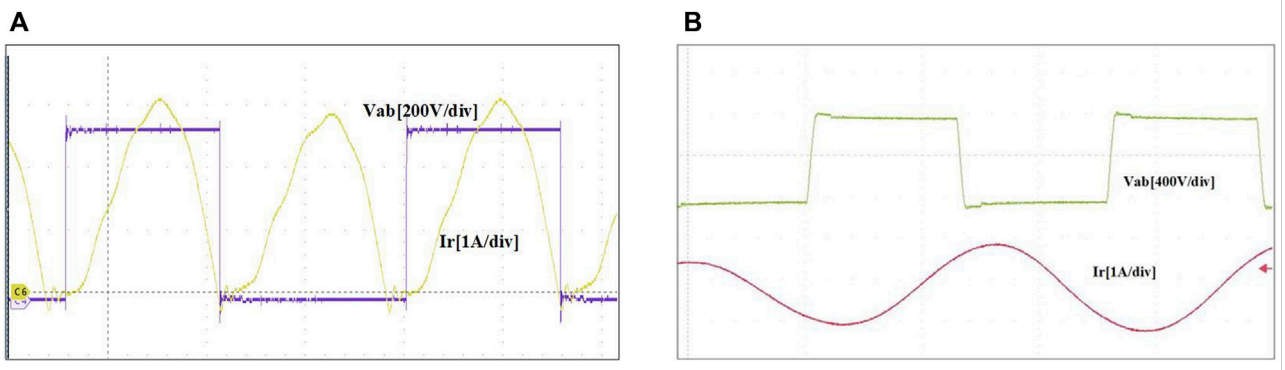


FIGURE 11
(A) Waveforms in the HB mode and **(B)** waveforms in the FB mode.

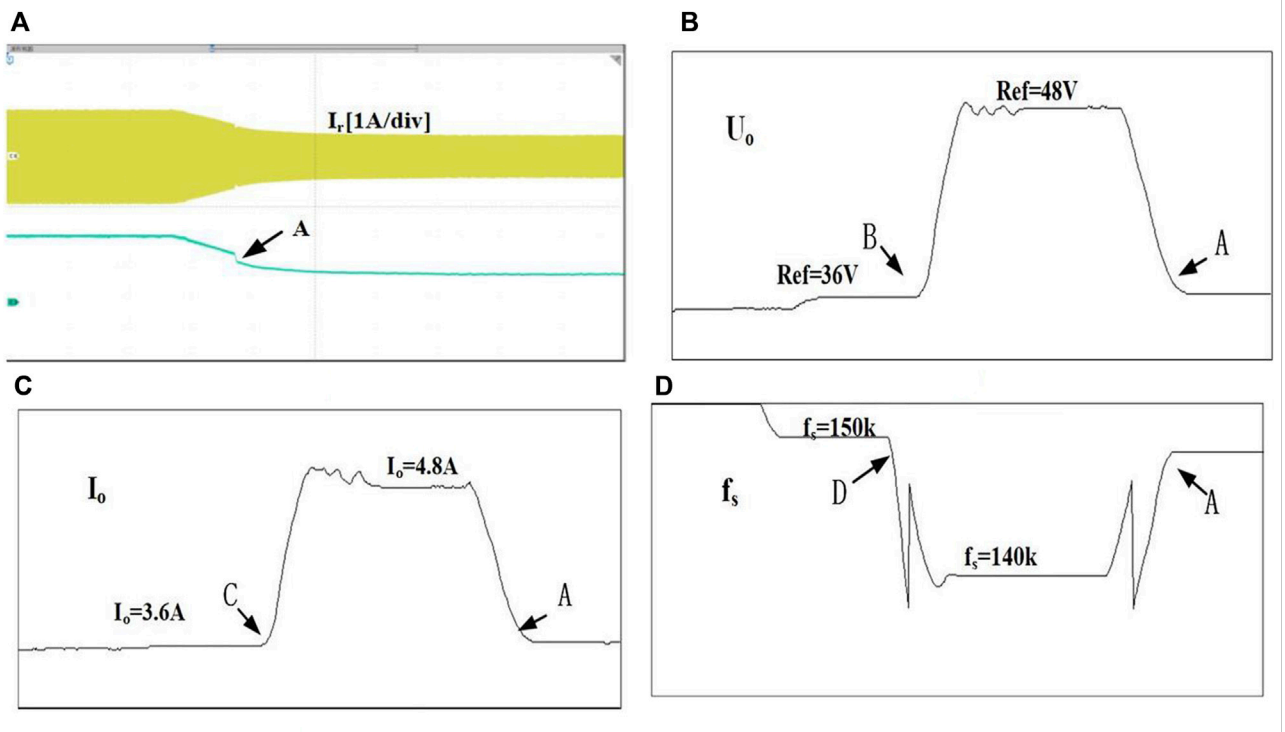


FIGURE 12
Reference change: **(A)** Graph of an oscilloscope. **(B–D)** The waveform monitored by the upper computer.

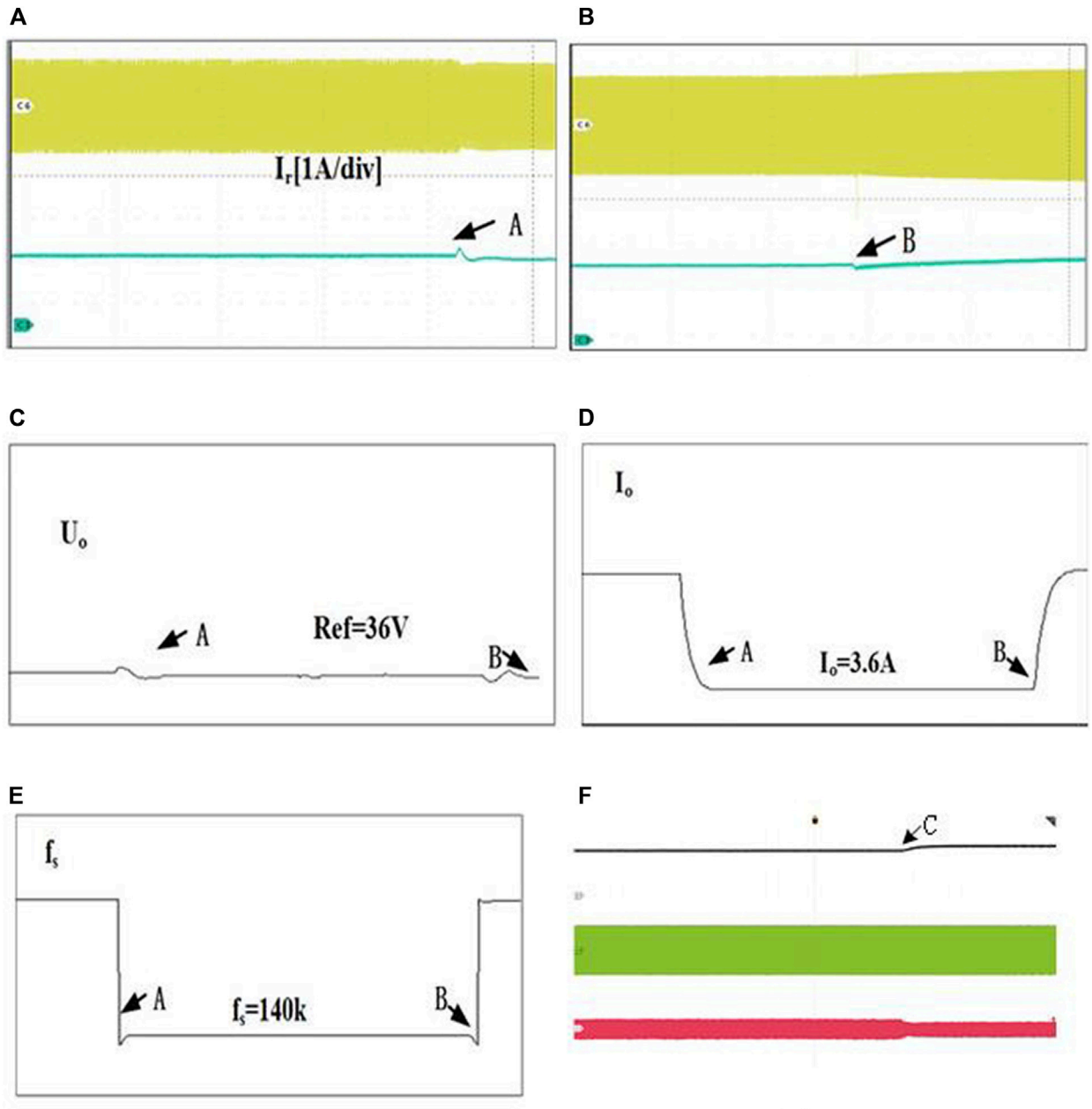


FIGURE 13
Load change. **(A,B)** Graph of oscilloscope **(C–E)** waveform monitored by the upper computer. **(F)** Output waves without considering the parasitic capacitance.

decreasing load. The overall control process is shown in Figure 9.

4 The experiment

The prototype is connected to an energy storage device at one end and a smart grid at the other, as shown in Figure 10. The input voltage is limited from 360 V to 440 V, and the output voltage is kept constant at 36 V. The maximum output current in the forwarding mode equals 27 A, and 2.5 A in the reversed mode, whereas the maximum power is 1 kW. The resonance frequency is set as 100 k, the same as the switching frequency in the full load in theory. Due to the components having parasitic parameters, the actual resonant frequency has some differences from the theoretical one. Considering the current and voltage

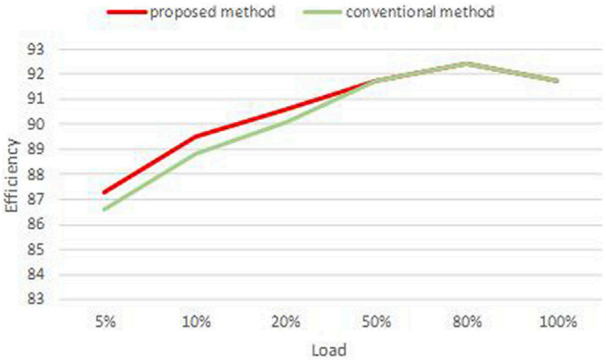


FIGURE 14
Efficiency comparison.

stress, the components have 2–3 times margin. The digital control can be more flexible in various situations compared with the analog control, with the computing power and speed required for existing integrated chips. In this prototype, DSP, TMS320F28335 (Tohid et al., 2018) published by Texas Instruments as the digital controller, plays a role that occurs in the driving signal, performing the digital to analog conversion, sampling unit, and so on. The switching frequency is calculated. The output current and voltage, which are sampled by the Hall element, are converted to a digital form by the analog to a digital converter in DSP. The main converter parameters are shown in Table 1. It is worth mentioning that the prototype is only for principle verification, so the power density is not considered in the design.

Figure 11A shows the waves, including the H-bridge voltage and the resonant current. The voltage is around 400 V in the HB mode, where S_3 keeps 0% and S_4 keeps 100% duty. Figure 11B shows the H-bridge voltage and current in the FB mode, where S_3 and S_4 keep 50% duty. The voltage varies from +400 V to −400 V. The modes are switched due to the input voltage and load variable.

In Figure 12, the load is constant and the reference value is changed. Figure 12A shows the oscilloscope waveform, and Figures 12B-D show the waveforms displayed by the host computer. Point B, point C, and point D are simultaneous and the reference voltage changes from 36 V to 48 V. The reference value increases, the mode switches to full bridge mode, and the frequency drops. Point A indicates that the reference value changes from 48 V to 36 V. The reference value drops, switching from the FB mode to the HB mode. The mode is switched when the reference has been changed, and the output range is widened.

In Figure 13, the reference value is constant at 36 V and the load is changed. Figures 13A, B show the waveforms on the oscilloscope and Figures 13C–E show the waveforms on the host computer. At point A, the load decreases, the current decreases, and the converter is handed over from the FB mode to the HB mode. At point B, the load increases and the converter is handed over from the FB mode to the HB mode. When the load changes, the output voltage transitions smoothly and can maintain the constant voltage under a light load. Although controlled by PI, the reaction speed is faster. A green wave indicates the voltage of the H-bridge, a red wave indicates the current of the resonator, and the black wave indicates the output voltage. At the C point, the load is decreased but the reference is kept constant. There is only switching frequency controlled by PI in the traditional control method.

Compared with the conventional method, S_1 and S_2 are complementary conduction according to 50% duty cycle in the proposed method of the light load. S_3 is kept always on and S_4 is kept always off. Therefore, S_3 and S_4 have lower switching losses. Therefore, the efficiency is improved compared with the traditional method in the light load. The proposed control method is the same as the conventional method, and hence, the efficiency is the same. In Figure 14, the horizontal axis represents the load and the vertical axis represents efficiency. As the load increases, the efficiency gradually increases. The efficiency is the highest when the load reaches 80%, after which the efficiency decreases with the load. The loss can be divided into two types, the fixed loss and the variable loss. The fixed loss includes the transformer loss, the switching loss, and the line loss. Under the light load, the fixed loss accounts for a larger proportion, so the efficiency is low. As the load increases, the proportion of the fixed loss becomes smaller and smaller, with the highest efficiency at about 80% load. With the increase of load, the current increases, the heat loss increases, and the efficiency decreases.

5 Conclusion

The control method is based on the new model considering parasitic capacitance, which plays a vital role in adjusting the output voltage and broadening the output range. In this paper, the model considering parasitic capacitance is more realistic than before, in which the gain curve has two spikes. In addition, the definition of the light load is given on the basis of the gain. Also, the switching frequency, which varies under different load conditions, has been adjusted depending on the gain curve by the PI controller, and there are two modes in this control: the HB mode and the FB mode. The output can be maintained constant under light load conditions and can be widened. The variation of the driving signal is also given to avoid topological mutation causing damage to other devices in transition. It is proven that the model and control method presented in this paper is effective in a 400V-36V-1 kW prototype. Compared with the previous methods, it can improve the efficiency and ensure the constant output voltage under the light load (Wang et al., 2022c).

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material. Further inquiries can be directed to the corresponding author.

Author contributions

All authors listed have made a substantial, direct, and intellectual contribution to the work and approved it for publication.

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QA was employed by Changguang Satellite Technology Co., Ltd.

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Optimization strategy and control technology of four-port SOP for distribution network with PV and BESS

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This paper proposes a four-port soft open point (FSOP) with photovoltaic (PV) and battery energy storage systems (BESS) and its optimization strategy and control technology. Combining PV output, BESS characteristics, peak and valley electric charges, transformer operation efficiency, and soft open point (SOP) characteristics, the operation criteria under different operating conditions are formulated to improve the economy of the distribution network. In this paper, the power distribution optimization algorithm is established based on the transformer consumption characteristic model and the equal consumption incremental rate criterion to improve the power utilization rate and the system's economy. The system doesn't require an additional central controller and transmits control signals through the DC link of FSOP to realize the coordinated operation of all ports. The simulation results show that the system and the optimization strategy can realize the system's coordinated operation and improve the distribution network's economy.

KEYWORDS

PV, BESS, SOP, the consumption characteristic model, the power distribution optimization algorithm, no central controller

1 Introduction

The increasingly diversified load and power demand make the AC distribution network have great problems in safety, reliability, economic applicability, and distribution efficiency (Ji, 2019). With the adjustment of the energy structure and the development of the power system, distributed PV, BESS, and new power electronic equipment are more and more widely used in the power system, which makes the distribution network have more abundant and active regulation capability. Among them, SOP, as a fully controlled power electronic device, has attracted the attention of many scholars.

Access to distributed PV and BESS effectively alleviates the problem of resource shortage and large load fluctuation of the distribution network (Conti, 2012; Bloemink, 2013; Rueda, 2013). However, when they are connected to the distribution network, they are all planned, designed and operated independently, there is a lack of coordination between the systems, as well as the problem of converter redundancy, which leads to a

decrease in the economy and stability of the system. At the same time, the periodic characteristics of PV power generation and the periodic changes of power load make the power flow size and direction of the distribution network change at any time. Therefore, the low-voltage distribution network suffers from large fluctuations in transmission power, difficulties in ensuring transformer operating efficiency, high operating costs, and difficulties in matching power generation and consumption (Verzijlbergh, 2014; Huang, 2015). It is not easy to ensure the economic applicability and distribution efficiency of low-voltage distribution networks.

The power distribution-oriented SOP has flexible, fast, and accurate power exchange control and power flow optimization capabilitiy (Chen, 2020; Wang, 2022; Zhou, 2022), and can realize the integrated coordination and optimization management of "Generation-Grid-Load-Storage" (Jeffrey, 2013; Wang, 2016b; Zeng, 2016). It enables the AC distribution network to balance safety and reliability, economic applicability and distribution efficiency (Wang, 2017; Kashani, 2019; Wang, 2020). Wang (2016a), Xue (2020), and Li (2021) studied the optimal operation and cooperative control strategy of flexible distribution network based on SOP. And the results show that SOP can improve the system power flow and reduce system loss. Wang (2017) studied the SOP siting and capacity fixing problem, and the research results showed that the reasonable configuration of SOP can effectively improve the economy of distribution network. The research on multi-port control of SOP of Huang (2019) and Wu (2019) shows that stable DC link voltage is a prerequisite for stable operation of multi-port system containing SOP, and that with SOP control, the system can achieve power flow between multiple port.

Many scholars have studied the optimal operation of systems containing SOP and proved the effectiveness of SOP in the optimal operation of distribution networks. However, most of the studies are focused on the location of SOP and the setting of BESS capacity. There is little research on the connection mode and collaborative control of PV, BESS, and SOP. The optimization of the operation of the transformers connected to the SOP is also rarely considered.

Based on the above research and analysis, this paper proposes to connect PV and BESS to the SOP's DC link to form a FSOP. Compared with the independent grid connection of distributed power sources, FSOP can save cost by reducing the number of converters and replacing multiple small capacity BESSs with one large capacity BESS. On the premise of comprehensive consideration of PV output, the efficiency characteristics of transformers, and peak and valley electric charges, this paper proposes a novel power distribution optimization algorithm. The algorithm uses the power regulation function of SOP to realize the cooperative operation of multiple converters, and establishes an optimization model to improve the economy and stability of the distribution network. In the power distribution optimization algorithm, an optimal scheduling method based on equal consumption incremental rate criterion is established to improve the economy and stability of the system. In the multi-converters collaborative control strategy, the DC link of FSOP is used as the signal transmission path to realize the cooperative control of each unit without the central controller. Finally, the effectiveness of the proposed optimization method is verified by Matlab/SIMULINK.

2 The structure of four-port soft open point for distribution network with photovoltaic and battery energy storage systems

In this paper, we propose a four-port soft open point, as shown in Figure 1. Two AC ports are directly connected to the distribution network. Two DC ports are led from the DC link of the FSOP and connected to PV and BESS. As shown in Figure 1, the device is connected to two transformer rooms of the distribution network and connected to PV and BESS to form a small distribution network system. The system connects the four ports through a DC link to achieve power flow and regulation between the four ports, creating a hardware foundation for power transfer in time and space (Miu, 2012). In combination with the policy of peak and valley electric charges, the operation strategy is formulated to realize the coordinated operation of each unit, improve the operation efficiency of the system and the economic benefits.

The system mainly includes transformers, FSOP, PV, BESS, user load, and etc. PV output is limited by natural resource conditions, which can be regarded as a relatively uncontrollable power supply to provide certain power support for the system. BESS is connected to the FSOP through a bidirectional DCDC converter, and can change the working state by adjusting the operation strategy to realize the load transfer in the time scale. Transformers can be regarded as the main power supply of the system, and the operation efficiency can be improved by adjusting the load rate. FSOP can change the working mode by changing the control strategy to realize the transfer of load at the spatial scale (Wang, 2013). The overall control architecture of the system is shown in Figure 2.

As shown in Figure 2, the part ① divides the system into different operation states. Then, according to PV output and the state of BESS, the optimal operation criteria is executed and the control signals are generated. The part will be described in detail in Section 3. The part ② represents the hardware structure of the four-port SOP proposed in this paper, which is the carrier of control and optimization operation strategies. The part ③ realizes the control of the four converters in the system based on the control signals generated by the part ①.First, FSOP controls the operation of the two AC/DC converters according to the control signal generated by the operation optimization strategy, and then controls the other two DC/DC

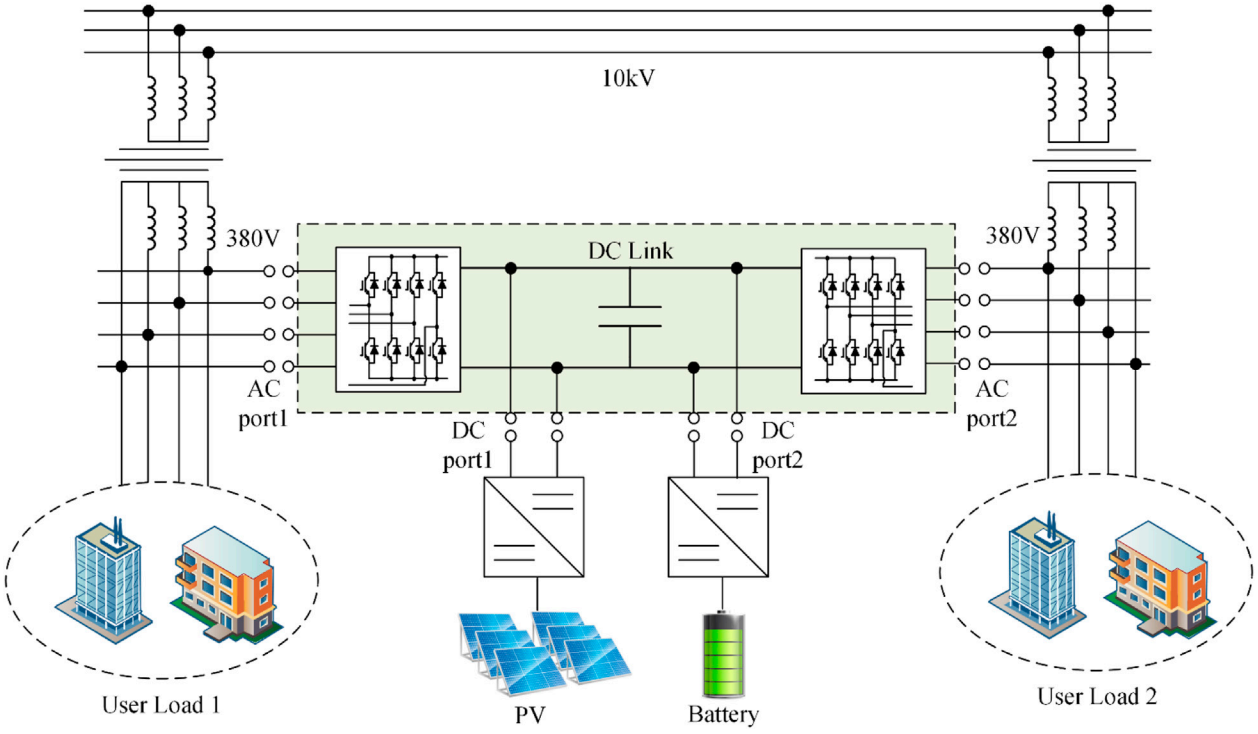

FIGURE 1
Distribution network system with FSOP.

converters according to the voltage of DC link. Among them, 220 V and 50 Hz represent the standard value of mains voltage, and 800 represents a reference value, which can determine the control strategy of BESS by comparing with V. The Section 4 will describe this part in detail.

3 System optimization layer

The system has four ports, which are connected through a DC link. This connection creates the basis for energy flow between the ports. At the same time, the coupling between each unit is enhanced and the difficulty of cooperative operation is increased. In order to realize the cooperative operation of each converter and realize the optimal scheduling of PV, BESS, and FSOP, it is necessary to formulate the optimal operation strategy of the system (Cao, 2016; Ding, 2011; Li, 2015; Zeng, 2016; Zhang, 2020; Zhao, 2015).

3.1 Operation criteria

The purpose of formulating optimization strategy is to realize the stable and economic operation of the system by adjusting the operation state of each unit. Therefore, it is necessary to define the operation criteria of each unit first and then determine the system's overall operation strategy according to each unit's operational criteria. The operation criteria of BESS, PV, FSOP, and the equal consumption incremental criterion of the transformer will be introduced below.

To distinguish the operation state of the system, the following definitions are made in this paper. Transformer overload state means that the output power of the transformer exceeds the rated capacity. System overload state means that the total output power of two transformers exceeds the total rated capacity. Normal operation state means that the system is not overloaded.

3.1.1 Battery energy storage systems operation criteria

BESS can transfer power consumption across time scales to reduce load fluctuations in distribution network and reduce operating costs. Therefore, this paper proposes a BESS charging and discharging operation criterion based on the state of charge (SOC), electricity price, and transformer overload state, as shown in Figure 3.

$$P_e = P_{cnmax} \tag{1}$$

$$P_e = min\{P_{cnmax}, P_{L1} + P_{L2} - E_1 - E_2 - P_V\} \tag{2}$$

$$P_e = min\{P_{cnmax}, -P_{L1} - P_{L2} + E_1 + E_2 + P_V - P_{excess}\} \tag{3}$$

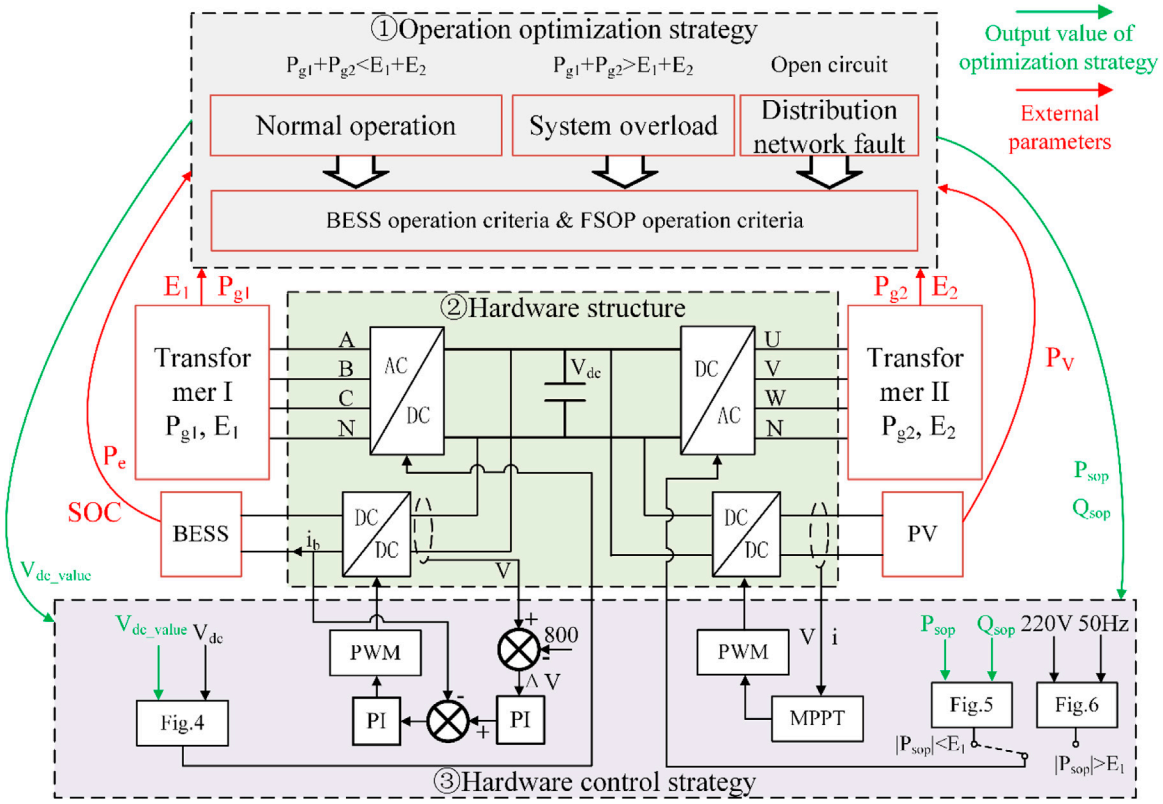

FIGURE 2
System control architecture diagram.

Where, P_e represents the actual charging and discharging power of BESS, P_{cnmax} represents the maximum charging and discharging power of BESS. P_{Li} and E_i respectively represent the user load and the rated capacity of the transformer on side i, and P_V represents the power generated by PV.

3.1.2 PV operation criteria

PV in the system can be regarded as a relatively uncontrollable auxiliary power supply, which can provide a certain power support for the system. Considering the system's economy, PV adopts maximum power point tracking control strategy.

3.1.3 FSOP operation criteria

When distribution network fault occurs, the FSOP operates in V_{dc}Q-Vf control mode. At this time, FSOP does not perform active power regulation and only maintains stable power supply on the fault side. In the system overload state, when one transformer overload, the FSOP operates in V_{dc}Q-PQ control mode for active power regulation to reduce the load rate of the overload side transformer and improve the system's stability. When two transformers overload, FSOP will not conduct active power regulation. In the normal operation state, FSOP determines the power value to be regulated according to the power distribution optimization algorithm. The algorithm is based on the equal consumption incremental rate criterion of the transformer.

3.1.4 Equal consumption incremental rate criterion of transformer

The two transformers in the system are connected with the distribution network as the main power supply of the system. According to the efficiency characteristics and load rate characteristics of the transformer, the consumption characteristic model of transformers is established. And then, the load distribution of the system is optimized through the equal consumption incremental rate criterion of the transformer to improve the operation efficiency of the transformer. The consumption characteris-tics and power inequality constraints of the two transformers are as follows:

$$\begin{cases} F_1 = P_{g1} + P_{O1} + \left(\frac{P_{g1}}{E_1}\right)^2 P_{k1}, 0 \le P_{g1} \le E_1 \\ F_2 = P_{g2} + P_{O2} + \left(\frac{P_{g2}}{E_2}\right)^2 P_{k2}, 0 \le P_{g2} \le E_2 \end{cases} \quad (4)$$

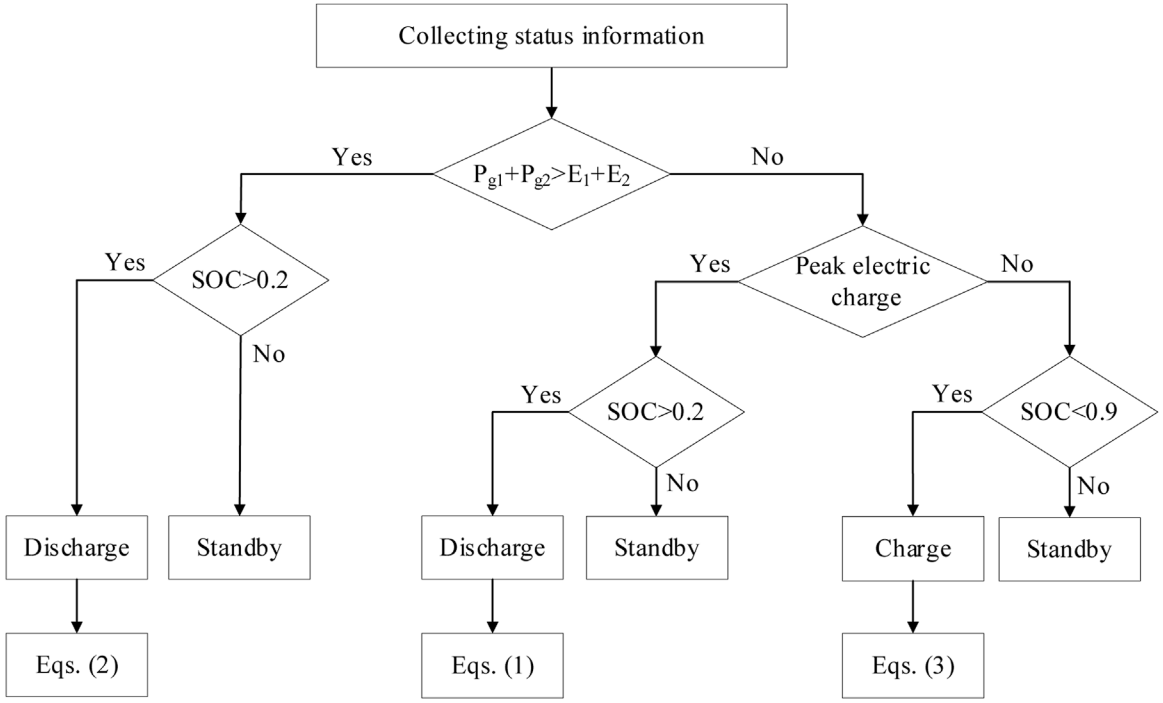

FIGURE 3
Flow chart of BESS operation.

The derivative of the above equation is used to obtain the incremental characteristics λ_1 and λ_2 of the two transformers, thus establishing the constraint conditions as follows:

$$\begin{cases} \boldsymbol{P_{g1} + P_{g1} = T} \\ \boldsymbol{\lambda_1 = \lambda_2} \end{cases} \tag{5}$$

where F_i, P_{gi}, P_{oi}, E_i and P_{ki} are respectively the input power, output power, no-load loss, rated capacity and short circuit current of transformer i. Solve F_i and P_{gi} satisfying (4) and (5).

3.2 System optimization operation strategy

As shown in Figure 2, the system includes three states. In order to realize the stable and economic operation of the system, this paper proposes different operation strategies for different system states, and the optimization time series of system states is shown in Figure 4.

3.2.1 Normal operation state

At the normal operation state, the economic operation of the system is taken as the optimization objective, where the optimization objective can be described as:

$$\boldsymbol{C = \sum_{t=0}^{t=T} (c(t) P_{in}(t) + cbess \cdot P_{bess})} \tag{6}$$

$$\boldsymbol{P_{in}(t) = \frac{P_{g1}(t)}{\mu_1(t)} + \frac{P_{g2}(t)}{\mu_2(t)}} \tag{7}$$

where C represents the total electricity costs of the distribution network, P_{in} (t) and c (t) represent the input power and electricity price of transformers in the period t respectively, $cbess$ represents the electricity cost per kilowatt hour of BESS, and P_{bess} represents the total charge and discharge of BESS. And μ_i (t) means the efficiency of transformer i at time t.

At a certain time, user load, electricity price, and PV output in the system are fixed. Therefore, the system's economy can only be improved by adjusting the charging and discharging power of the BESS and improving the operating efficiency of transformers. To this end, this paper proposes a new optimized operation strategy based on BESS and FSOP. First, FSOP collects signals and determines the charging and discharging power P_e according to BESS operation criteria and determines the net load of the system at the current time. Then, the output power of the transformers on both sides is determined according to the power distribution optimization algorithm, and then the power value and flow direction on the DC link are determined. Finally, the control signals are generated. The operation optimization time series is shown in Figure 4.

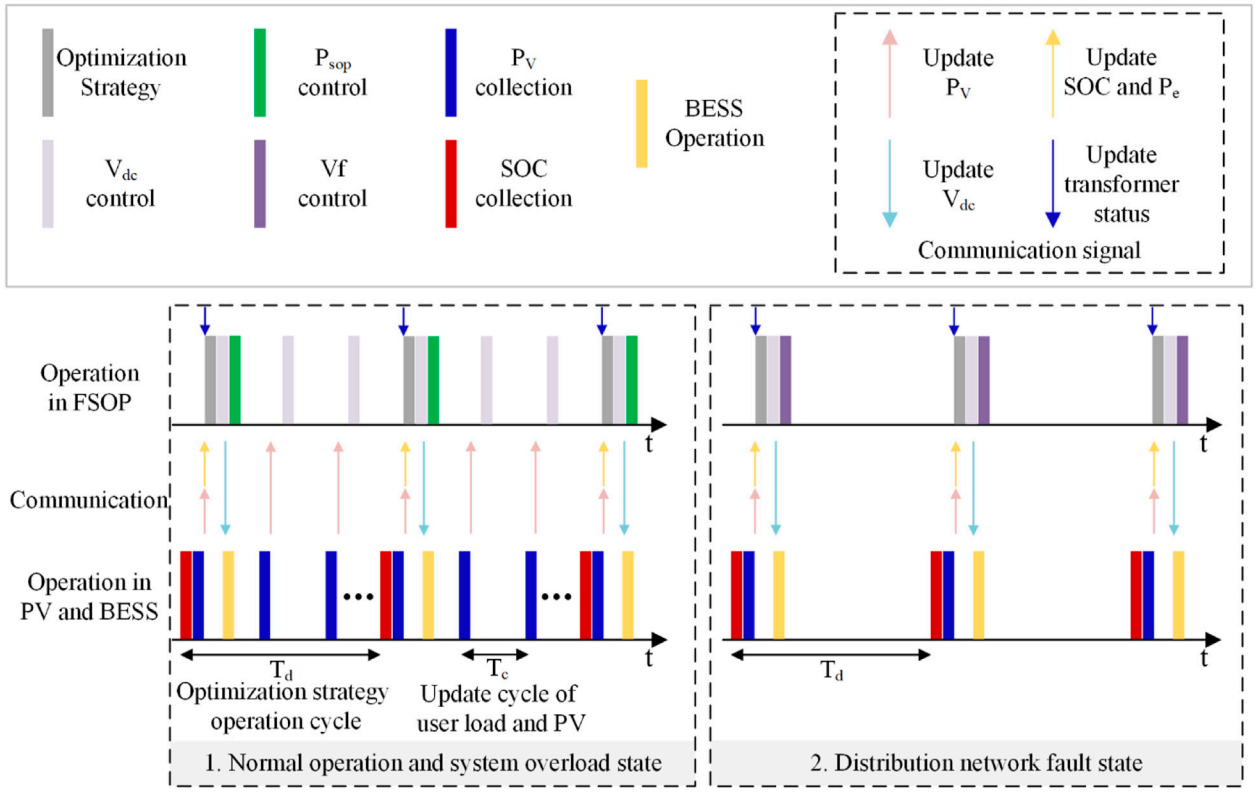

FIGURE 4
Operation optimization time series.

As shown in Figure 4, the optimization strategy operation cycle is T_d, that is, before the next T_d, the control strategy of each converter in the system will not change, and the DC link voltage and the output power of BESS will not change. Only when the next T_d comes, FSOP will collect SOC, the output power of PV and BES. At the same time, FSOP will collect the current load rate of transformers, and then execute optimization strategy to generate new control signals, thereby changing the control strategy of each converter. Among them, BESS operation, P_{sop} control and V_{dc} control shown in Figure 4 have been introduced in Section 3.1.

3.2.2 System overload state

At the system overload state, to ensure the safe and stable operation of the system, the operation strategy shall be adjusted to make the transformer operate within the allowable range of rated capacity or reduce its overload. In this state, BESS constantly discharges at the maximum power, and the output control signal V_{dc_value} is 850. When one side transformer is overloaded (assuming that the load rate of transformer 2 is higher), FSOP conducts active power regulation to reduce the overload rate of transformer 2. At this time, the output control value P_{sop_value} meets (8).

When both transformers are overloaded, FSOP does not conduct active power regulation and only distributes the output power of PV and BESS according to the overload degree of transformers on both sides. First, calculate the power value that needs to be supplemented to the high load rate side when $\beta 1 = \beta 2$ is met, record the value as P_{do}, and then distribute the remaining power according to the condition that the load rates on both sides are the same. The output control value P_{sop_value} meets (9). The operation optimization time series is shown in Figure 4.

$$P_{sop\_value} = P_e + P_V + E_1 - P_{L1} \tag{8}$$

$$P_{sop\_value} = \begin{cases} P_{do} + \dfrac{E_2}{E_1 + E_2}(P_e + P_V - P_{do}), \text{ if } P_e + P_V - P_{do} > 0 \\ P_e + P_V, \text{ if } P_e + P_V - P_{do} < 0 \end{cases} \tag{9}$$

3.2.3 Distribution network fault state

At the distribution network fault state, the system uses the fault isolation function of FSOP to realize uninterrupted power supply of load at the fault side. The FSOP performs V_{dc}Q-Vf control to maintain the fault side voltage and frequency stability,

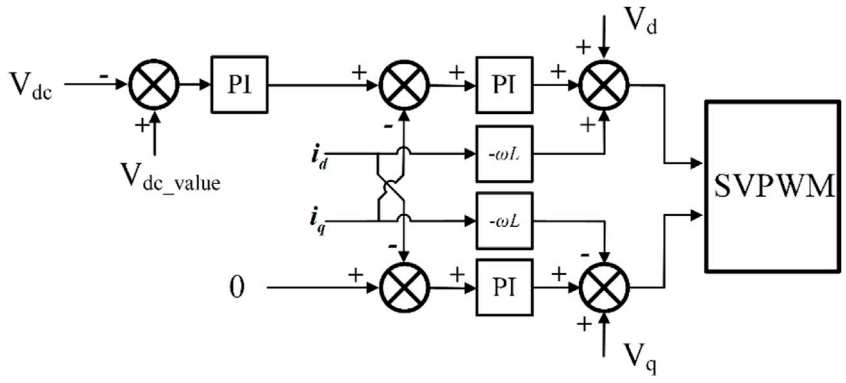

FIGURE 5
Schematic diagram of $V_{dc}Q$ control mode.

and PV and BESS provide power support for the system. The operation optimization time series is shown in Figure 4.

4 Equipment control layer

In the system optimization layer, after FSOP determines the optimization strategy and outputs control signals based on the system state, it is necessary for each unit in the system to work together to realize the economic and stable operation of the system. Since the system involves four converters, in order to transmit the control signal generated by the system optimization to each converter, this paper proposes a control method without a central controller to achieve the coordinated control of each unit in the system.

The operation optimization strategy is implemented in FSOP, so FSOP can directly control both AC/DC converters after outputting control values V_{dc_value} and P_{sop_value}. However, the converter on the BESS side cannot directly obtain the control signal and needs to be transmitted through the signal path. While PV operates under the maximum power point tracking control strategy, it does not need to be regulated by the control signal of the system optimization layer. Therefore, the controlled quantity is single, and the converter on the BESS side can be controlled by transmitting the control signal through the DC link. PV output is greatly affected by the external environment, BESS operation status switches frequently and capacity is limited, which is not suitable for maintaining DC voltage stability. FSOP can realize the stable control of DC voltage, so FSOP maintains constant DC voltage in this system.

4.1 four-port soft open point control

Control signals V_{dc_value} and P_{sop_value} generated by the operation optimization strategy determine the control mode of FSOP. One converter operates in $V_{dc}Q$ control mode, and the other operates in PQ control mode or Vf control mode (Wang, 2013). As shown in Figure 5, when converter operates in $V_{dc}Q$ control mode, V_{dc_value} is input into the control loop as the reference signal of the voltage outer loop, and the DC link voltage is controlled through feedback regulation of the PI controller. As shown in Figure 6, when converter operates in PQ control mode, P_{sop_value} and Q_{sop_value} are input into the control loop as reference signals of the power loop, and the power flow is controlled through negative feedback regulation. When converter operates in Vf control mode, in order to achieve stable power supply of three-phase unbalanced load, the positive sequence, negative sequence and zero sequence voltages are respectively controlled by Vf, and their control block diagrams are shown in Figure 7. When controlling the positive sequence voltage, the reference signal V_{ac} takes the amplitude of the mains voltage 311 V, and when controlling the positive sequence voltage and zero sequence voltage, the reference signal $V_{ac} = 0$. At this time, the converter does not need PLL and the value of frequency f is 50 Hz.

4.2 Battery energy storage systems control

As mentioned above, the control signal needs to be transmitted to the converter on the BESS side through the DC link. During FSOP operation, the DC link voltage within a certain range can maintain the stable operation of FSOP, so BESS can determine its different operation modes and charge and discharge power values through different DC voltage values. For example, in a 380 V distribution network, DC link voltage in the range of 750VDC ~ 850VDC can maintain the system's stable operation. When the DC link voltage is 780VDC ~820VDC, BESS does not work. When the DC link voltage is

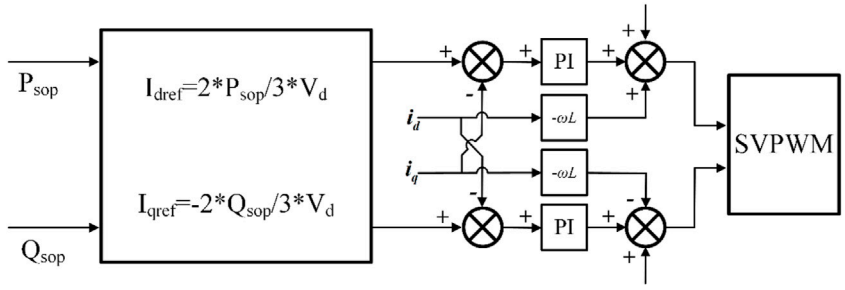

FIGURE 6
Schematic diagram of PQ control mode.

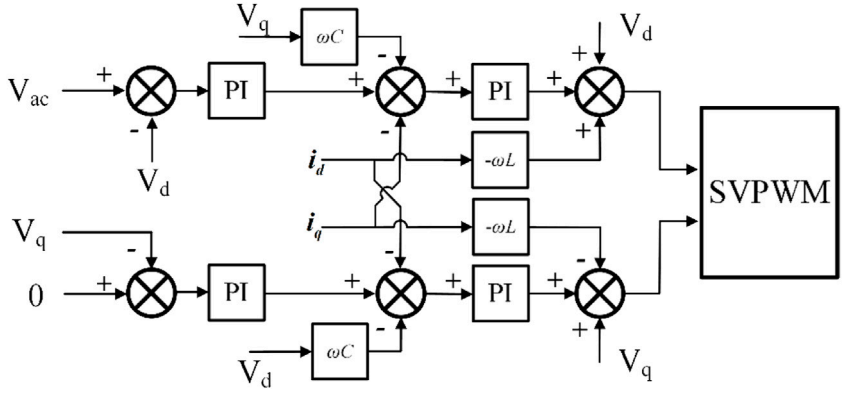

FIGURE 7
Schematic diagram of Vf control mode.

820VDC ~ 850VDC, the BESS is in constant power discharge mode, and the discharge power is (10). When the DC link voltage is 750VDC ~ 780VDC, the BESS is in constant power charging mode, and charging power is (11).

$$P_e = \frac{V_{dc} - 820}{30} P_{cnmax} \tag{10}$$

$$P_e = \frac{V_{dc} - 780}{30} P_{cnmax} \tag{11}$$

5 Simulation results

To verify the effectiveness of the optimized operation strategy proposed in this paper, simulation is carried out in Matlab/Simulink. PV output curve measured at Shandong Province is shown in Figure 8A. The peak time, valley time, and electricity price refer to the standards issued by Shandong Province. The electricity price is \0.5769 at 8:00–22:00 and \0.3769 at 0:00–8:00 and 22:00–24:00. And the transformers used in the simulation are S9-50/10 and S9-100/10. To simplify the model, this paper does not consider reactive power. Figure 8B shows the actual user load and the output power curve of the transformer after FSOP optimization, and the user load is set according to the average daily power load curve of Shandong Province released in 2018. The red line in the figure indicates the actual user load on both sides of the system, and the green line indicates the output power of transformers after the optimization strategy. The black dashed line indicates the SOC variation curve of BESS.

Figure 8C shows the system electricity cost curve. The PV output and the actual user load are shown in Figure 8A and Figure 8B. The main parameters of BESS are as follows: the maximum capacity is 25 kW h, the maximum power is 7.5 kW, the maximum value of the SOC is 0.9, and the minimum value is 0.2. In Figure 8C, the green line represents the total electricity cost without BESS, the black line represents the total electricity cost without optimization, and the red line represents the total electricity cost after optimization. It can be seen from the figure that the FSOP and its operation strategy proposed in this paper reduce the power consumption cost of the system by about 6%

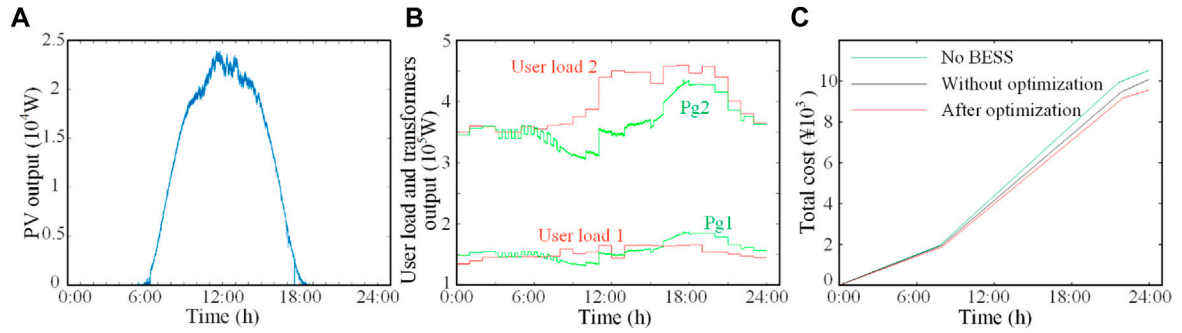

FIGURE 8
24-h **(A)** PV output curve, **(B)** user load and transformers output, **(C)** electricity cost curve.

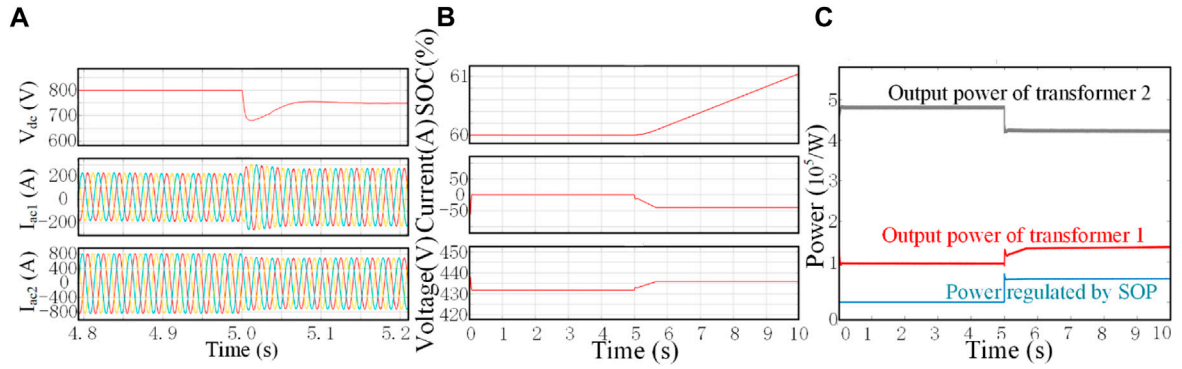

FIGURE 9
(A) DC link voltage and AC/DC converters regulation waveform, **(B)** State change waveform of BESS, **(C)** Power variation diagram within the system.

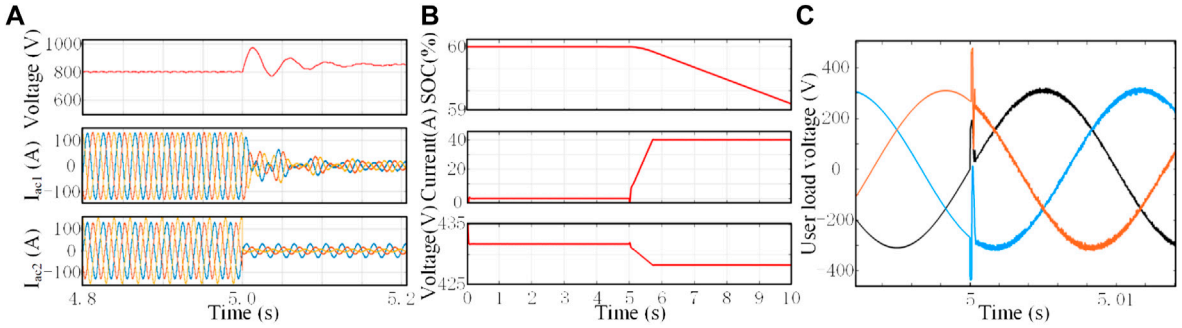

FIGURE 10
(A) DC link voltage and AC/DC converters regulation waveform, **(B)** State change waveform of BESS, **(C)** The voltage waveform of the user load on the fault side.

and 3% respectively compared with the traditional distribution network and FSOP without optimal operation strategy. Therefore, FSOP and its operation optimization strategy can improve the economy of the system.

In this paper, the simulation verifies that the converters in the system can achieve cooperative operation under different operating conditions and strategies. Figure 9 shows the waveforms of FSOP, BESS and DC link power when the system generates a new control signal at t = 5 s and the operating state of each port in the system changes. Figure 10 shows the waveforms of the fault-side user load voltage, FSOP, and BESS when the system is switched from the normal operation state to the distribution network fault state. Wherein, Figures 9A, 10A show the DC link voltage, FSOP side converter regulation waveform in 4.8–5.2 s, Figures 9B, 10B shows the waveform of SOC, charging and discharging current, charging and discharging voltage of BESS in 0–10 s. Figure 9C shows the output power value of the system side transformers and the power value regulated through FSOP in 0–10 s. Figure 10C shows the voltage waveform of user load at fault side in case of system fault.

As shown in Figure 9, within 0 ~ 5 s, the system does not use the power distribution optimization algorithm for optimal regulation. At this time, the DC link voltage is 800 V, the BESS does not work, and the SOC is constant at 60%. At this time, the output and transfer power of transformers on both sides do not change. When t = 5 s, the system optimization layer uses the power distribution optimization algorithm to adjust and control, generate control signals V_{dc_value} and P_{sop_value}, where V_{dc_value} is 750, and P_{sop_value} is 69,200, and transmit them to each converter. It can be seen from Figure 2 that when t = 5 s, the DC link voltage is rapidly adjusted to 750 V, and the current waveform of converters on both sides of FSOP quickly tends to be stable after a short time adjustment. The BESS changes the charging state and reaches the maximum charging power in about 0.6 s. Part of the load of transformer 2 is transferred to transformer 1 through FSOP to improve the system efficiency.

As shown in Figure 10, when t = 5 s, the system changed from the normal operation state to the distribution network fault state. At this time, the BESS was discharging with the maximum power, and the unbalanced user load on the fault side was quickly restored to power under the control of the FSOP. The simulation results show that the system can realize the cooperative operation of four ports and the stable power supply of unbalanced load on the fault side without central controller.

6 Conclusion

In order to improve the economy and stability of the distribution network, this paper proposes a FSOP and its optimization strategy and control technology. In this paper, the consumption characteristic model of transformer and the equal consumption incremental rate criterion are established to improve the operation efficiency of transformers. And establish the power distribution optimization algorithm to improve the economy and stability of the system. The system does not need a central controller and only needs DC link voltage to control the equipment in the system.

The optimization strategy proposed in this paper considers only the active load, and the optimization effect is obvious when the load rates of two transformers differ significantly. In future work, the configuration and siting of energy storage capacity for multi-ports SOP will be studied to give full play to the advantages of energy storage and SOP.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author.

Author contributions

XZ is the main author of the paper and experiment. XG and XZ provide technical support and suggestions, and assist in completing papers and experiments, and help XZ collect data. FG guides XZ to complete the experiment and paper writing, and provides theoretical support.

Conflict of interest

Authors XG and XZ were employed by Yangzhou Huading Electric Co., Ltd.

The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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Three-phase boost-stage coupled current source inverter concept and its space vector modulation

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The current source inverter (CSI) is essentially a converter with inherent boost capability and has been preliminarily applied in the field of renewable energy generation systems. However, conventional CSIs are mostly operated independently. Several existing multilevel CSI topologies entirely rely on parallel combinations, which seems to be not very suitable for capacity expansion. To solve this issue, this paper proposes a concept of three-phase boost-stage coupled current source inverter (BSC-CSI) through the duality principle, which can output multi-level currents with a reduced number of switches as well as hardware costs. Compared with the state-of-the-art CSIs, the proposed BSC-CSI can notably simplify the implementation of the multi-level modulation scheme and meanwhile ensure the power devices switch under lower current stress. To further take full advantage of the modularity and scalability, the BSC-CSI can be constructed by hybrid using silicon-carbide (SiC) and silicon (Si) based semiconductor switches for improving efficiency. The experimental results have verified the theoretical findings.

KEYWORDS

current source inverter, multi-level converter, dual principle, hybrid switch, space vector modulation

1 Introduction

With the increasing attention paid to clean energy, power inverter has become the key component of modern renewable energy network. Generally, power inverters can be classified as voltage source inverter (VSI) and current source inverter (CSI). Although VSI currently dominates the application market, CSI draws scholars' continuous attention and has been considered to be a promising topology. CSI is well known for its inherent short-circuit protection advantage and voltage boost capability, which have been proven to be of the essence and important for grid applications and renewable energy generations. Therefore, it has been used in certain application fields, such as renewable energy systems, active power filters, and some high-power drives (Nishikata and Tatsuta, 2010; Guo, 2017a; Liu et al., 2020). However, CSI still faces the practical challenges of high power loss, bulky inductance, and huge space occupation.

To solve these problems, scholars tried to apply high-performance semiconductor switches, e.g. the reverse blocking IGBTs (RB-IGBTs), silicon-carbide (SiC), and gallium nitride (GaN) based MOSFETs (Su and Tang, 2011; Guacci et al., 2019; Narasimhan et al., 2021). However, these attempts strictly depend on the high investment, so there is still a big gap between hardware all-upgrade solutions and the actual applications. In terms of the three-phase topology innovations, the H7-CSIs have carried out valuable thoughts on reducing switching loss (Guo, 2017b; Wang et al., 2018; Lorenzani et al., 2019), but limited by the power range of the shunt-connect device, they seem to be weaker for high-power applications. For large-scale power fields, the multi-level technique can be a great added value to CSI topologies (Wu, 2006). Multi-level current source inverter (MCSI) is considered to be an effective technology to reduce the switching stress as well as the filter size and has been extensively implemented, e.g. the single/multi-rating inductor MCSI, the paralleled H-bridge MCSI, and the buck-boost MCSI (Gao et al., 2010; Dupczak et al., 2012; Ries and Heldwein, 2020; Alskran and Simoes, 2021; Ding and Li, 2021). However, these state-of-the-art research works are essentially the series/parallel combinations of multiple H6 bridges, which can be classified as the H6-type MCSIs. And they not only inherit the common problems of conventional CSI, but also face the critical disadvantages of the increasing number of components and operational complexity. Therefore, CSI right now still needs a simple, compact and cost-efficient implementation solution.

At the same time, the multi-level voltage source inverters (MVSIs) have been well extensively investigated and implemented for over a decade. When the research perspective of the multi-level technique returns to VSI, it can be easily found that MVSIs have much clearer topological evolution paths, e.g. neutral point clamped (NPC) MVSI (Rodriguez et al., 2010; Wang et al., 2013), flying capacitor (FC) MVSI (He and Cheng, 2016), and cascaded H-bridge (CHB) MVSI (Yu et al., 2016). Among them, the NPC MVSI is one of the most commonly used MVSI topology types, and features a relatively high degree of integration. Inspired by the I-type NPC MVSI structure, this paper proposes a concept of three-phase boost-stage coupled CSI (BSC-CSI), explains its construction rules and operational principles, and further illustrates the space vector modulation (SVM) scheme. The proposed BSC-CSI concept, on the one hand, can effectively reduce the complexity of MCSI as well as the number of components, and on the other hand, can also improve CSI efficiency with an acceptable cost. Besides, the BSC-CSI concept can even integrate some other existing research results of CSI topologies.

This paper is organized as follows. In Section 2, the existing MCSI topologies are first introduced and parsed, while the topological construction mechanism of I-type NPC MVSI is analyzed. And then, with the insight of dual principle, the concept of BSC-CSI is proposed. In Section 3, the compatible SVM strategy is presented in detail. The operational characteristics are also analyzed. Finally, simulation and experimental tests are presented to verify the theoretical findings.

2 Topology of the three-phase boost-stage coupled CSI

2.1 Comparison of multi-level construction mechanism

The basic purpose of multi-level technique is to reduce down the power stress of switches, with the added benefit of improving power quality. As for an MCSI, the significance of reducing the current is not only to reduce the power loss of switches, but also to meet the line loss constraints of the constant current transmission mode. To fulfill this requirement, most existing three-phase MCSIs adopt multi-module integration technology, which has built several types. Figure 1 demonstrates their topologies, which takes five-level MCSI as examples.

Figure 1A shows the single-rating inductor MCSI (SI-MCSI). It has two H6 converter sub-modules and four inductors with the same current rating. Their DC inputs come from the same DC rail, while the AC outputs inject current into the load in parallel. The multi-rating inductor MCSI (MI-MCSI) is one variant of the SI-MCSI, which is shown in Figure 1B. The main difference is the non-uniform inductors used to split the input current. Both SI-MCSI and MI-MCSI have the drawback of circulating current, and it is difficult to control the power fluctuation of each single module. The paralleled H-bridge MCSI (PH-MCSI), as shown in Figure 1C, can solve this problem. It utilizes two independent current sources to decouple the power control of the sub-modules. However, the requirement of equal current supply seriously affects the practical value of this topology. Figure 1D shows the Buck-boost MCSI. It mainly aims at a wide range of output voltage, but lacks the ability to handle high current applications.

As it can be found from the above MCSI, their topology is essentially a series-parallel combination of the H6 converter sub-modules. The modulation process is mainly to control the switching combinations of every H6 converter sub-modules. If there are n resembled sub-modules, MCSI will have 6n power switches and 6n power diodes, to realize the 2n+1 level output phase current. And the total number of the switching combinations will be 6^n. Therefore, with the increase of the current level, these MCSI solutions will have huge hardware costs as well as space occupation, and there exists a great difficulty in modulation implementation, e.g., 5-level CSI has 12 switches with 81 switching combinations, and 7-level CSI has 18 switches with 729 switching combinations.

When the research perspective is shifted back to MVSIs, it can be found that the construction form of topology is completely different. The I-type NPC MVSI, for example, has no integration of three-phase modules in its topology, but its voltage-level generation mechanism is quite clear. The I-type NPC MVSIs mainly include the diode neutral point clamped (DNPC) MVSI and active neutral point clamped (ANPC) MVSI which are commonly used in industry. Their topologies with 3-level outputs as an example are shown in Figure 2.

Both DNPC MVSI and ANPC MVSI integrate capacitor on the DC rail to provide the extra voltage levels in addition

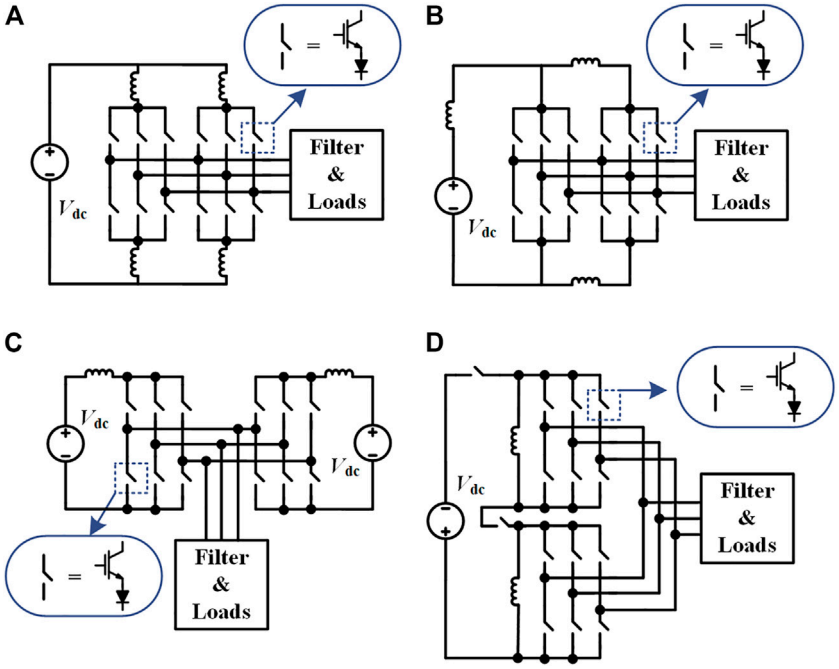

FIGURE 1
(A) Single-rating inductor MCSI **(B)** Multi-rating inductor MCSI. **(C)** Paralleled H-bridge MCSI. **(D)** Buck-boost MCSI.

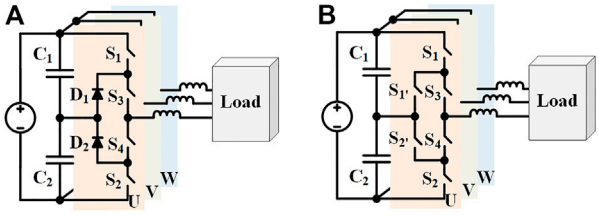

FIGURE 2
(A) I-type DNPC MVSI. **(B)** I-type ANPC MVSI.

to the DC bus. And the output of each phase is connected to the DC bus through several switches whose essential function is to select the voltage state of the output of AC side. The main difference between DNPC MVSI and ANPC MVSI is that ANPC MVSI replaces the diodes (D_1 and D_2 in DNPC MVSI) with two power switches ($S_{1'}$ and $S_{2'}$). They can provide the capability to actively control the potential of the neutral point.

As shown in Figure 2B, from the perspective of each phase, ANPC MVSI can be divided into two parts. Except the power supply, the front-end circuit is composed of two capacitors and four switches (S_1, $S_{1'}$, S_2, and $S_{2'}$), which can provide 3-level voltages, while the rear-end circuit is composed of two switches (S_3 and S_4) with one inductive filter, which can realize the output of each phase. This structural feature can be applied to DNPC MVSI as well, i. g. the front-end circuit is responsible for voltage levels, which includes C_1, C_2 S_1, S_2, D_1 and D_2, and the rear-end circuit uses S_3 and S_4 to implement the phase outputs.

2.2 Duality principle and the BSC-CSI topology

Duality is one of the common basic characteristics among circuitries and is of importance and mathematical insights. In graph theory, one converter can be abstracted as a graph composed of nodes and edges, which have been introduced in (Li and Li, 2020).

For a planar graph, in addition to the typical electrical duality (e.g., voltage/current sources and inductive/capacitive components), geometrical duality can also be used to find out its dual topology, which can be clearly seen between Buck and Boost converters, as well as that between single-phase VSI and CSI.

As for a non-planar graph, it may be necessary to use the Quasi-dual method (dual on each active switching state) to find its dual topology. A typical representative of this method is the duality between three-phase VSI and CSI, whose topologies are shown in Figure 3. It is worth noting that the power switch in VSI needs to reverse parallel with a power diode, which can sustain

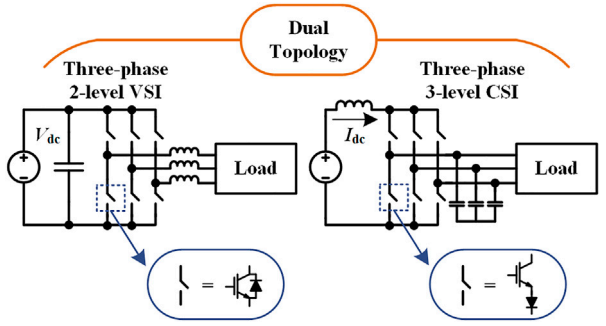

FIGURE 3
Duality between conventional three-phase VSI and CSI.

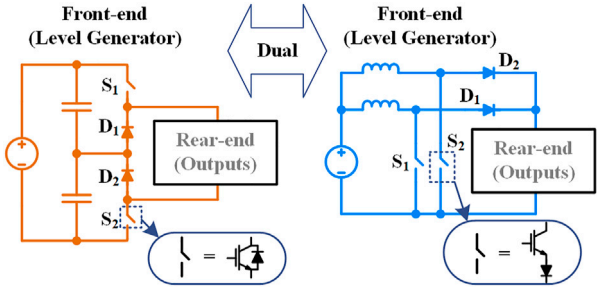

FIGURE 5
Graphs of DNPC phase module and its duality topology.

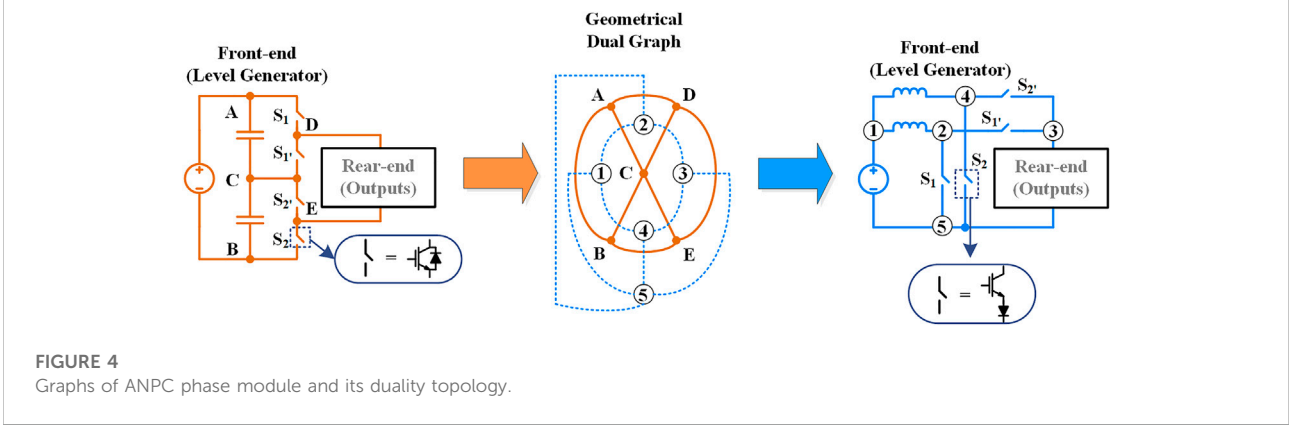

FIGURE 4
Graphs of ANPC phase module and its duality topology.

the reverse power flow path, while by contrast, the power switch in CSI must series connect with a power diode so as to provide the reverse-blocking capability. Besides, the voltage/current level between VSI and CSI is not consistent, e.g., 2-level VSI is dual to 3-level CSI.

The above findings are a brief summary of the duality characteristics of the frequently-used converters. Following a similar approach, clues can be explored for constructing new CSIs with reduced switches. In order to facilitate the study of topology evolution, we can first study the simplest MCSI, i. g. starting from the new construction method of 5-level CSI topology. Therefore, its dual prototype can select with the I-type three-phase NPC 3-level VSI.

On the basis of topological analysis in Section 2.1, if take the rear-end output of one phase as a whole, then the front-end structure of one phase in ANPC 3-level VSI can be abstracted as a graph. Through the geometrical duality method, its dual topology can be found. This duality process is shown in Figure 4. The letters (A-E) are the nodes of the ANPC front-end phase module. The circled numbers represent the meshes of the planar graph and can be mapped as the new nodes of the dual topology. In the same way, the dual structure of DNPC can be obtained, as shown in Figure 5.

In light of the above research results, a multi-level current source generator can be constructed by expanding the front-end structure into multiple branches in parallel. As for the rear-end circuit, since its essential function is to commutate the phase current output, if referring to the commutation structure of conventional CSI, then the topology of the proposed three-phase boost-stage coupled CSI can be obtained, which is demonstrated in Figure 6.

The front-end stage of BSC-CSI contains n T-type boost branches, and each one needs an inductor to store energy and provide constant DC current. The power diodes ($D_{7\text{-}x}$ and $D_{8\text{-}x}$) are responsible for preventing backflow current. The shunt-connected switches ($S_{7\text{-}x}$) can provide a shoot-through channel, and the series-connected switches ($S_{8\text{-}x}$) are employed to decouple the connection between the inductor current and the branch's output, which need to be operated complementary to $S_{7\text{-}x}$, thereby synthesizing the output current level of the front-end stage.

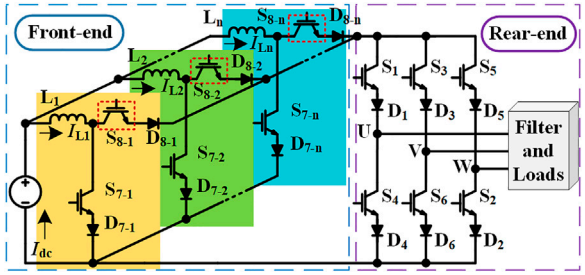

FIGURE 6
Topology of the proposed BSC-CSI.

To go a step further, it can be observed that the existing H7-CSI topology is actually one special form of the BSC-CSI (Wang et al., 2018), which only contains one T-type boost branch and omitted the series power diode. More specifically, as reported in (Wang et al., 2015), when the power factor angle of the AC load is less than 30°, $S_{7\text{-}x}$ can independently implement the shoot-through function. Therefore, $S_{8\text{-}x}$ can be omitted under this load condition, and thus can be regarded as a dual topology derived from the DNPC 3-level VSI.

3 Modulation of the three-phase boost-stage coupled CSI

3.1 Space vector modulation scheme

As described above, the T-type boost branches are in charge of the current injection to the rear-end circuit, and the rear-end H6 bridge is responsible for the phase commutation. Therefore, only when they are well-operated and coordinated, can the whole inverter obtain the correct multi-level output current. To realize the compatible space vector modulation of the proposed BSC-CSI, all the existing space vectors together with their corresponding switching combinations should be listed for the inverter first. Then, in order to synthesize the reference, space vectors must be appropriately selected, which is the key issue in the process of designing the modulation strategy. Next, the dwell time of each selected space vector should be calculated correctly. At last, it is necessary to design the switch combination sequence of the modulation period to optimize the performance of the whole inverter.

In order to accomplish the SVM design tasks, three basic principles should always be followed:

a) To reduce the output harmonics, the nearest space vectors should be priority selected.
b) To suppress switching losses, the rear-end power switches (S_1-S_6) are preferably operated with lower current stress.

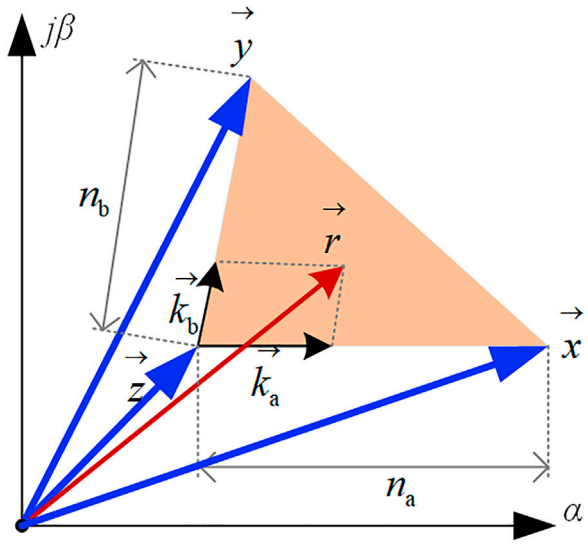

FIGURE 7
Synthesizing the target reference with three arbitrary vectors.

c) To ensure the balance of each front-end T-type branches, the shunt-connected switch ($S_{7\text{-}x}$) should be operated equally in one modulation period.

The general method to select the proper nearest space vectors to synthesize the reference, is to find a triangular region that is composed of the three nearest space vectors and covers the target reference. This process is illustrated in Figure 7. Let three arbitrary vectors ($\vec{x}$, $\vec{y}$ and $\vec{z}$) define a triangular region that covers the location of reference vector $\vec{r}$, then $\vec{r}$ can be synthesized using:

$$\vec{r} = \overrightarrow{k_a} + \overrightarrow{k_b} + \vec{z} = \frac{\left|\overrightarrow{k_a}\right|}{n_a}\vec{x} + \frac{\left|\overrightarrow{k_b}\right|}{n_b}\vec{y} + \left(1 - \frac{\left|\overrightarrow{k_a}\right|}{n_a} - \frac{\left|\overrightarrow{k_b}\right|}{n_b}\right)\vec{z} \quad (1)$$

where n_a and n_b are the distances of the endpoints between two adjacent vectors.

Taking 7-level BSC-CSI as an example, which consists of 3 T-type boost branches and one H6 bridge, For simplicity of illustration, $S_{8\text{-}1}$, $S_{8\text{-}2}$, and $S_{8\text{-}3}$ are omitted from this example since they only work under special load conditions. The overall space vector diagram is shown in Figure 8A. Denote turning ON all of {$S_{7\text{-}1}$, $S_{7\text{-}2}$, $S_{7\text{-}3}$} as TOA, while TO2 refers to turning ON any two of {$S_{7\text{-}1}$, $S_{7\text{-}2}$, $S_{7\text{-}3}$}, TO1 refers to turning ON any one of {$S_{7\text{-}1}$, $S_{7\text{-}2}$, $S_{7\text{-}3}$}, and NULL is to turn off them all. The switching states are summarized in Table 1, where only turn-ON switches are listed, and I_{dc} represents the total DC current.

As shown in Table 1; Figure 8A, there are 19 potentially available space vectors in the proposed 7-level BSC-CSI: six large

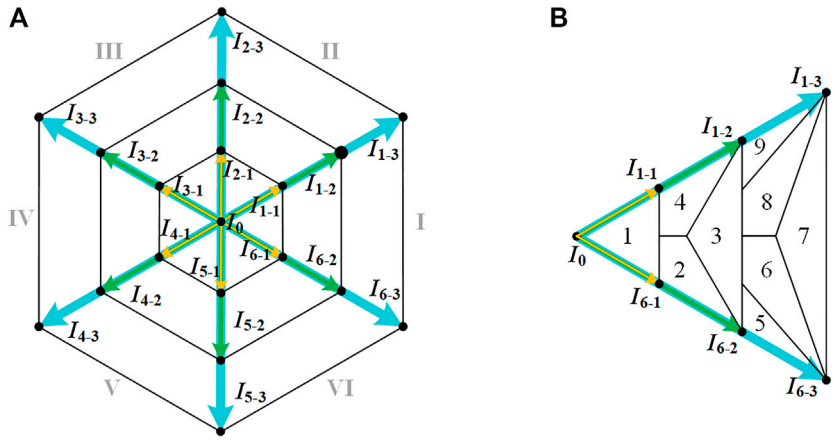

FIGURE 8
(A) Overall space vector diagram. **(B)** Region divisions of Sector I.

TABLE 1 Space vectors and switching states of BSC-CSI (7-level).

Space vectors	Front-end	Rear-end	Phase U	Phase V	Phase W
I_0	TOA	--	0	0	0
I_{1-1}	TO2	S_1 S_2	$I_{dc}/3$	0	$-I_{dc}/3$
I_{2-1}	TO2	S_2 S_3	0	$I_{dc}/3$	$-I_{dc}/3$
I_{3-1}	TO2	S_3 S_4	$-I_{dc}/3$	$I_{dc}/3$	0
I_{4-1}	TO2	S_4 S_5	$-I_{dc}/3$	0	$I_{dc}/3$
I_{5-1}	TO2	S_5 S_6	0	$-I_{dc}/3$	$I_{dc}/3$
I_{6-1}	TO2	S_1 S_6	$I_{dc}/3$	$-I_{dc}/3$	0
I_{1-2}	TO1	S_1 S_2	$2I_{dc}/3$	0	$-2I_{dc}/3$
I_{2-2}	TO1	S_2 S_3	0	$2I_{dc}/3$	$-2I_{dc}/3$
I_{3-2}	TO1	S_3 S_4	$-2I_{dc}/3$	$2I_{dc}/3$	0
I_{4-2}	TO1	S_4 S_5	$-2I_{dc}/3$	0	$2I_{dc}/3$
I_{5-2}	TO1	S_5 S_6	0	$-2I_{dc}/3$	$2I_{dc}/3$
I_{6-2}	TO1	S_1 S_6	$2I_{dc}/3$	$-2I_{dc}/3$	0
I_{1-3}	NULL	S_1 S_2	I_{dc}	0	$-I_{dc}$
I_{2-3}	NULL	S_2 S_3	0	I_{dc}	$-I_{dc}$
I_{3-3}	NULL	S_3 S_4	$-I_{dc}$	I_{dc}	0
I_{4-3}	NULL	S_4 S_5	$-I_{dc}$	0	I_{dc}
I_{5-3}	NULL	S_5 S_6	0	$-I_{dc}$	I_{dc}
I_{6-3}	NULL	S_1 S_6	I_{dc}	$-I_{dc}$	0

vectors, six medium vectors, six small vector and only one zero vector. In light of the above principles and considerations, the SVM scheme of 7-level BSC-CSI is proposed to partition each sector into nine regions, which is shown in Figure 8B. Thus, the overall space vector diagram of 7-level BSC-CSI can be divided into 54 regions.

As exemplified in Figure 8B for Sector I, the segmented nine regions are divided by the angle bisector and the

TABLE 2 Composition vectors of reference in sector I.

Region	Composition vectors	Dwell time	Region	Composition vectors	Dwell time
1	$I_{6\text{-}1}$	$T_a = 3m_aT_s\sin(\frac{\pi}{6}-\theta)$	6	$I_{6\text{-}3}$	$T_a = T_s(3m_a\cos\theta-2)$
	$I_{1\text{-}1}$	$T_b = 3m_aT_s\sin(\frac{\pi}{6}+\theta)$		$I_{1\text{-}2}$	$T_b = \frac{3}{2}m_aT_s\sin(\frac{\pi}{6}+\theta)$
	I_0	$T_c = T_s - T_a - T_b$		$I_{6\text{-}2}$	$T_c = T_s - T_a - T_b$
2	$I_{6\text{-}2}$	$T_a = T_s(3m_a\cos\theta-1)$	7	$I_{6\text{-}3}$	$T_a = T_s[\sqrt{3}\sin(\frac{\pi}{3}-\theta)m_a-1]$
	$I_{1\text{-}1}$	$T_b = 3m_aT_s\sin(\frac{\pi}{6}+\theta)$		$I_{1\text{-}3}$	$T_b = T_s[\sqrt{3}\sin(\frac{\pi}{3}+\theta)m_a-1]$
	$I_{6\text{-}1}$	$T_c = T_s - T_a - T_b$		$I_{6\text{-}2}$, $I_{1\text{-}2}$	$T_c = T_d = \frac{1}{2}(T_s - T_a - T_b)$
3	$I_{6\text{-}2}$	$T_a = \frac{3}{2}m_aT_s(\cos\theta-\frac{\sqrt{3}}{2}\sin\theta)-\frac{1}{2}T_s$	8	$I_{6\text{-}2}$	$T_a = \frac{3}{2}m_aT_s\sin(\frac{\pi}{6}-\theta)$
	$I_{1\text{-}2}$	$T_b = \frac{3}{2}m_aT_s(\cos\theta+\frac{\sqrt{3}}{2}\sin\theta)-\frac{1}{2}T_s$		$I_{1\text{-}3}$	$T_b = T_s(3m_a\cos\theta-2)$
	$I_{6\text{-}1}$, $I_{1\text{-}1}$	$T_c = T_d = \frac{1}{2}(T_s - T_a - T_b)$		$I_{1\text{-}2}$	$T_c = T_s - T_a - T_b$
4	$I_{6\text{-}1}$	$T_a = 3m_aT_s\sin(\frac{\pi}{6}-\theta)$	9	$I_{6\text{-}1}$	$T_a = 3m_aT_s\sin(\frac{\pi}{6}-\theta)$
	$I_{1\text{-}2}$	$T_b = T_s(3m_a\cos\theta-1)$		$I_{1\text{-}3}$	$T_b = T_s(\frac{3}{2}m_a\cos\theta-\frac{1}{2})$
	$I_{1\text{-}1}$	$T_c = T_s - T_a - T_b$		$I_{1\text{-}2}$	$T_c = T_s - T_a - T_b$
5	$I_{6\text{-}3}$	$T_a = T_s(\frac{3}{2}m_a\cos\theta-\frac{1}{2})$			
	$I_{1\text{-}1}$	$T_b = 3m_aT_s\sin(\frac{\pi}{6}+\theta)$			
	$I_{6\text{-}1}$	$T_c = T_s - T_a - T_b$			

connecting lines between vector endpoints. And the working state of the inverter can be classified into three modes: Mode 1 (reference locates in region 1 with 3-level switched currents), Mode 2 (reference rotates among region two to four with 5-level switched currents), and Mode 3 (reference rotates among region five to nine with 7-level switched currents). It is worth noting that these regions are symmetric about the angle bisector of Sector I.

Region one only contains I_0, $I_{1\text{-}1}$, and $I_{6\text{-}1}$, its SVM pattern can be considered the same as the H7-CSI, whose switching sequence can ensure the zero current switching (ZCS) for rear-end switches (S_1-S_6). When the inverter is operated in Mode 2, the reference can be synthesized by small vectors and medium vectors, so that the rear-end switches (S_1-S_6) can be operated with $I_{dc/3}$. To be more specific, Region 2 uses $I_{1\text{-}1}$, $I_{6\text{-}1}$, and $I_{6\text{-}2}$ to synthesize the reference vector, while $I_{1\text{-}1}$, $I_{6\text{-}1}$, $I_{1\text{-}2}$, and $I_{6\text{-}2}$ are employed in Region 3, where $I_{1\text{-}1}$ and $I_{6\text{-}1}$ should theoretically have the same dwell time. In Mode 3, the reference is synthesized in a slightly complicated way, whose selected vectors include small vectors, medium vectors, and large vectors. Region 5 uses $I_{1\text{-}1}$, $I_{6\text{-}2}$, and $I_{6\text{-}3}$ to synthesize the reference, and the rear-end switches (S_1-S_6) are switched with $I_{dc/3}$. Region six includes $I_{1\text{-}2}$, $I_{6\text{-}2}$, and $I_{6\text{-}3}$, while Region 7 uses $I_{1\text{-}2}$, $I_{6\text{-}2}$, $I_{1\text{-}3}$, and $I_{6\text{-}3}$ to synthesize the reference, where $I_{1\text{-}2}$ and $I_{6\text{-}2}$ have the same dwell time. Both Region six and Region seven can switch rear-end switches (S_1-S_6) with $2I_{dc/3}$. The composition space vectors of reference in all the nine regions together with their dwell times are listed in Table 2, where m_a is the modulation index.

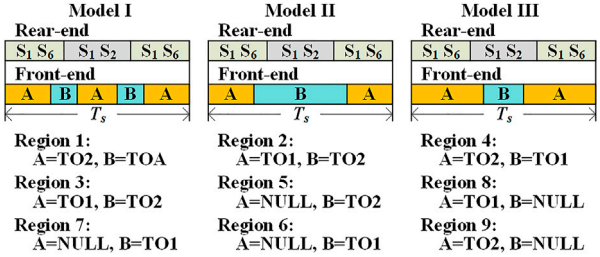

FIGURE 9
The models of switching sequences (in Sector I).

As for the switching sequences, the front-end switches ($S_{7\text{-}1}$, $S_{7\text{-}2}$, and $S_{7\text{-}3}$) should be arranged carefully to keep the T-type branches balance. It should be pointed out that if all the T-type-branch inductors are of the same value, the actual switching operations of $S_{7\text{-}1}$, $S_{7\text{-}2}$, and $S_{7\text{-}3}$ should be treated equally. They will not only occupy the same dwell time during one modulation period, but also evenly be distributed in the switching cycle. In order to achieve this feature, the switching sequences of the proposed SVM scheme can take the symmetrical pattern with three possible models, which are illustrated in Figure 9. T_s is the modulation period. A and B represent two switching states of the front-end stage. For different regions, the two switching states should accordingly be implemented with different switching combinations. These operational arrangements can take

TABLE 3 Comparisons between the H6-type MCSI and the proposed BSC-CSI (7-level).

Topologies	H6-type	Proposed BSC-CSI							
		Front-end			Rear-end				
Power-switch Count	18	3			6				
Switching Combinations	729	43							
Switching Count	24	R. (1 3 5 7 9)		R. (2 4 6 8)	4				
		4		2					
Switching current stress	$I_{dc}/3$	$I_{dc}/3$			Region 1		R. (2 3 4 5 9)		R. (6 7 8)
					ZCS		$I_{dc}/3$		$2I_{dc}/3$
Conducting current	$I_{dc}/3$	$I_{dc}/3$			I_{x-1}		I_{x-2}		I_{x-3}
					$I_{dc}/3$		$2I_{dc}/3$		I_{dc}
Conducting-switch Count	6	I_0	I_{x-1}	I_{x-2}	2		2		2
		3	2	1					

advantage of the bypass function of the front-end T-type branches to reduce the switching current stress of the rear-end switches (S_1-S_6).

3.2 Operational feature benchmarking

The proposed BSC-CSI has some unique characteristics in terms of the number of switching devices and power loss. Taking 7-level as an example, the comparisons between the conventional H6-type MCSI and the proposed BSC-CSI (S_{8-x} omitted) are listed in Table 3, where "R." is short for "Region", and "ZCS" is short for "zero current switching".

The power-switch count of the proposed BSC-CSI has reduced by half. And its number of switching combinations is obviously less than that of the conventional H6-type MCSI, which makes the modulation strategy much easier to implement.

As for the modulation operation, the front-end switches are constantly operated with $I_{dc}/3$, while the switching current stress of rear-end switches depends on the actual modulation index and reference's location. Besides, the BSC-CSI also has a significant advantage in switching counts, which makes a lower switching loss. The current rating through front-end switches is one-third of that in rear-end switches. This feature enables BSC-CSI to configure the rear-end with relatively high power but cheap devices and meanwhile to use the front-end with high-performance devices with a low current rating. Intuitively, it gives the possibility to improve efficiency by only using SiC devices for front-end switches, which can make it cost-effective customization. It is worth noting that other-level BSC-CSIs have similar characteristics in terms of configuration and switching operations.

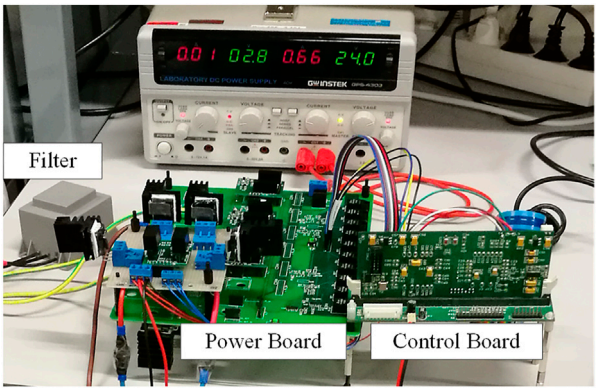

FIGURE 10
Experimental prototype of the proposed BSC-CSI.

4 Experimental results

To validate the performance of the proposed BSC-CSI and its modulation scheme, a 7-level BSC-CSI experimental prototype has been built, which is shown in Figure 10. The control board is integrated with a DSP (TMS320F28335 of Texas Instruments) and an FPGA (xc3s500e of XILINX). Among them, the DSP is used to calculate the dwell times and to judge the region of reference vector, while the FPGA is responsible for the switching selection and the arrangements of driving sequence. On the power board, in order to obtain a cost-effective performance, the front-end switches (S_{7-1}, S_{7-2}, and S_{7-3}) are employed with SiC-MOSFETs (C2M0160120D of CREE), and the rear-end switches (S_1-S_6) are Si-IGBTs (IKW20N60T of Infineon).

TABLE 4 Parameters of the experimental prototype.

Parameters	Values
DC current (I_{dc})	12 A
Inductance of each branch	3 mH
AC filter capacitance	10 μF
Switching frequency	10 kHz
Output AC frequency	50 Hz
Load resistance	16 Ω

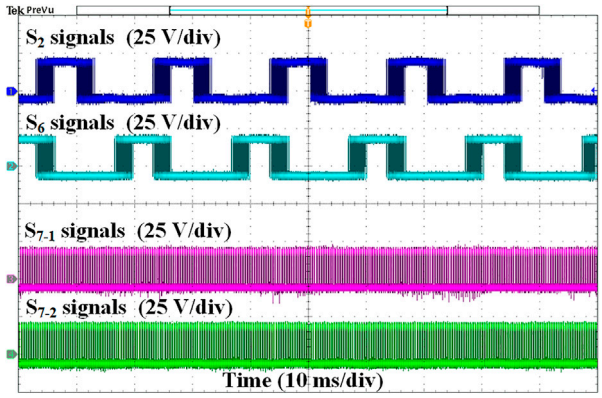

FIGURE 11
Driving pulses of switches (S_2, S_6, $S_{7\text{-}1}$, $S_{7\text{-}2}$).

Besides, all the power diodes are C2D20120D from CREE. The DC power supply is employed with Delta SM 600–10. Other experimental parameters are listed in Table 4

Employed with the proposed space vector modulation scheme, the driving pulses of switches (S_2, S_6, $S_{7\text{-}1}$, $S_{7\text{-}2}$) are captured in Figure 11. It is obvious that the front-end power switches ($S_{7\text{-}x}$) of BSC-CSI are switched more frequently than the other switches (S_1-S_6). Because $S_{7\text{-}x}$ is configured with SiC-MOSFETs, this high switching frequency will not result in the heavy burden of switching loss.

In order to demonstrate and verify the working characteristics of the proposed BSC-CSI in different modes, the modulation index is set to 0.5 and 0.9, respectively. And the corresponding experimental results (output voltages, switched current, and inductor currents) are shown as Figures 12, 13.

When the modulation index is 0.5, the reference will rotate among the medium vectors (green vectors of Figure 8A), and the BSC-CSI prototype outputs the five-level switched current. The output phase voltage performs 50 Hz sinusoidal waveform with the amplitude of 96 V. The inductor currents show the power balance of each front-end

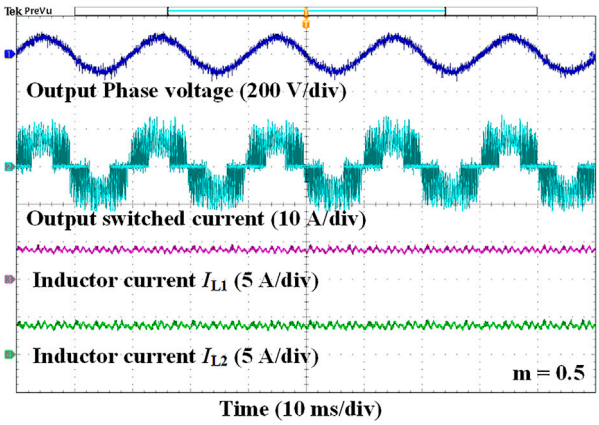

FIGURE 12
Experimental waveforms of output phase voltage, output switched current, and inductor currents under m = 0.5.

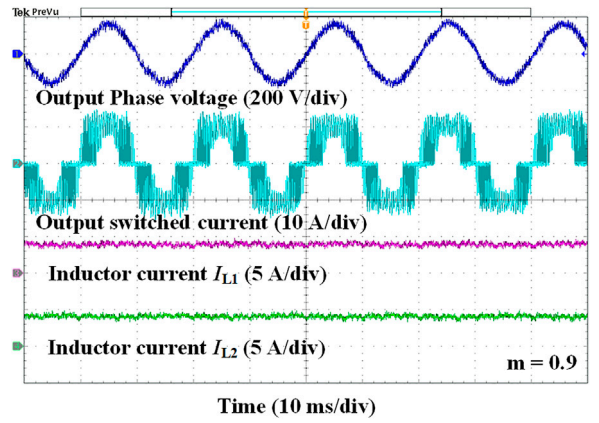

FIGURE 13
Experimental waveforms of output phase voltage, output switched current, and inductor currents under m = 0.9.

branches. This phenomenon is consistent with the expectation of the design in Section 3.1.

When the modulation index is fixed up to 0.9, the reference will rotate among the large space vectors (blue vectors of Figure 8A), and the output results clearly presents the seven-level switched current. As expected, the proposed BSC-CSI can properly output 50 Hz sinusoidal waves, whose amplitude is about 172 V. And the inductor current of each T-type branch keeps balancing at about 4 A.

To validate the efficiency performance, an additional prototype of conventional H6-type 7-level CSI has been built up using the same experimental parameters. Except for the SiC-MOSFETs of BSC-CSI, all the other power devices are employed with the same hardware. Both the H6-type 7-level CSI and the 7-level BSC-CSI were tested under the same conditions. In

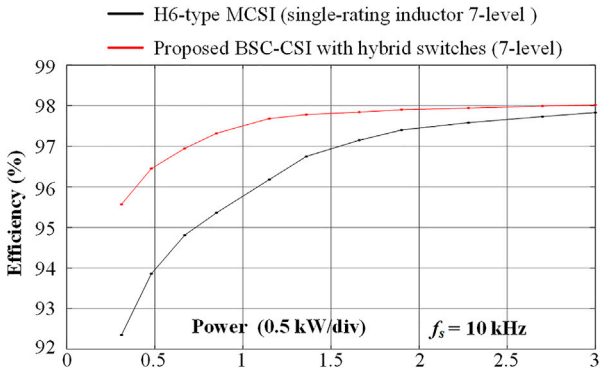

FIGURE 14
Efficiency comparison of the two experimental prototypes.

accordance with a series of operating power points, efficiency data is recorded using a power analyzer (PM6000 of Voltech). Their efficiency carves are shown in Figure 14.

The comparison results show that the 7-level BSC-CSI achieves a relatively higher efficiency over the conventional H6-type 7-level CSI. However, this efficiency promotion has a tendency to weaken as the power increases. It is mainly because the proportion of conduction loss in the total loss will gradually increase as the modulation index increases, thereby weakening its advantages in reducing the switching loss.

5 Conclusion

This paper proposes a concept of three-phase boost-stage coupled CSI and establishes the compatible space vector modulation scheme. The BSC-CSI concept shows a new duality path through NPC VSIs to construct CSI topologies and can cover up the previously investigated H7-CSI topology. Compared with state-of-the-art MCSI, the proposed BSC-CSI has fewer switching components, making the whole converter more compact, and the implementation method of SVM can be simplified significantly. Moreover, with the customization of cost-efficient hybrid switches, the proposed SVM scheme is able to ensure BSC-CSI to perform a higher efficiency. The corresponding performance has been validated through experimental tests.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

WW substantially contributed to the conception of the study, SR helped perform the analysis with constructive discussions, XL and XX conducted supervision. All authors have read and agreed to the published version of the manuscript.

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Conflict of interest

Author SR was employed by the State Grid Shandong Electric Power Company.

The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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Design of single neuron super-twisting sliding mode controller for permanent magnet synchronous servo motor

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Aiming at the control system of permanent magnet synchronous servo motor which is easily affected by external disturbance and parameter uncertainty, a single neuron sliding mode combining single neuron adaptive algorithm and super-twisting sliding mode (STSM) control is proposed. The STSM control is used to overcome the chattering problem in the traditional sliding mode control, and the proportional control and the STSM control are combined to enhance the robustness of the control system. In order to improve the dynamic performance of the system and enhance the anti-disturbance ability of the system, the single neuron adaptive control adopted can adjust the relevant parameters of the designed sliding mode controller online. The simulation and experimental results show that the designed improved sliding mode controller can effectively suppress the chattering of the control system, realize the fast following and no overshoot of the control system, and enhance the robustness of the system.

KEYWORDS

permanent magnet synchronous servo motor, single-neuron adaptive algorithm, super-twisting algorithm, sliding mode control, stability analysis

Introduction

In recent years, permanent magnet synchronous motor (PMSM) has received more and more attention with the continuous research and development of the performance of permanent magnet materials and the progress of power electronics technology (Zhang et al., 2019). It is also more widely used in various aspects of national defense, military industry and daily life owing to its high efficiency, simple and reliable structure, small size and low losses (Du et al., 2016; Wang et al., 2019). The control performance of PMSM drive system is greatly influenced by uncertainties such as load variations and parameter perturbations in actual control. Therefore, suitable controllers need to be designed to reduce the impact of these uncertain external factors on the control system while enhancing the system robustness and improving the system control performance.

Some literatures have proposed various control methods for motor control system, such as sliding mode control (Ali et al., 2019; ZHANG and WANG, 2021), neural network control (Wang and Kang, 2019; Wang et al., 2021), adaptive control (Zhao et al., 2017; Asiain and Garrido, 2021), and fuzzy logic control (Wang and Zhu, 2018; Mesloub et al., 2020), et al. Among them, sliding mode control is widely used in PMSM control system due to its advantages of fast response, insensitivity to parameter changes and perturbations, no need for online system identification, and simple physical implementation (Li et al., 2019; Xia and Zhang, 2019). However, in the actual control system, the sliding mode control cannot achieve the ideal switching and when the system is in the sliding mode surface, it will repeatedly cross

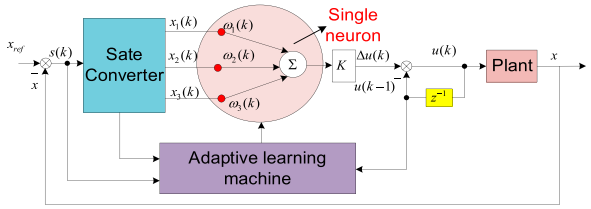

FIGURE 1
Control block diagram of single neuron adaptive sliding mode controller.

the sliding mode surface and so on, resulting in the system chattering and making the control system unstable (Wang et al., 2018). The idea of higher-order sliding mode control algorithm has been proposed to solve this problem. super-twisting sliding mode (STSM) control algorithm is a kind of second-order sliding mode control algorithm, and its control signal is continuous and vibration free, which can suppress the system chattering well. However, since it does not give an estimate of the convergence time and the uncertainty bound of the system is difficult to obtain (Sadeghi et al., 2018; Wan et al., 2018), we need to improve it. In (Zhou et al., 2022), a modified sliding mode self-anti-disturbance control is used to improve the dynamic stability performance of the control system. In (Zhou et al., 2019), the overshoot-free fast following of the control system is achieved using internal mode control. The literature (Abdul Zahra and Abdalla, 2021) combines Super-twisting sliding mode control with fuzzy control to weaken the chattering problem and improve the system robustness.

In this paper, a single-neuron control strategy was combined with super-twisting sliding mode control. In addition to the advantages of strong robustness and fast response of sliding mode control, STSM control can achieve high accuracy and fast following of the reference trajectory as well as suppressing the chattering problem of the control system. The single-neuron algorithm is simple and easy to implement for digital controllers. A single-neuron control strategy is combined with STSM control to reduce system chattering problem, improve system robustness and weaken the effect of uncertainties on the system. The controller can also adjust the parameters of the sliding mode controller online to obtain better control effect. The proposed idea was verified by simulation and experiment, and the results show that the proposed method has good control performance.

Super-twisting sliding mode controller design

Sliding mode controller design

The following first-order non-linear uncertainty system is considered.

$$\begin{cases} \dot{x} = ax + bu + d(t) \\ y = x \end{cases} \tag{1}$$

In Formula. 1, The x, u, $d(t)$ are the state variables, controller and uncertain perturbation terms of the system, respectively, and $d(t)$ satisfies $d(t) = \Delta a{\cdot}x + \Delta b{\cdot}u + g(t)$, where Δa, Δb and $g(t)$ are each uncertain terms and external perturbations of the parameters.

The super-twisting algorithm was applied to design a second-order sliding mode controller to improve the robustness of the control system to load and parameter variations and to reduce the system chattering problem. A sliding surface, s, is defined as follows

$$s = x_{ref} - x \tag{2}$$

Where x_{ref} is the system reference value.

Super-twisting slide controller was used to ensure that the system reaches the slide surface in a finite amount of time, where the equation is as follows

$$u = k_1|s|^{\frac{1}{2}}\mathrm{sgn}(s) + k_2\int \mathrm{sgn}(s)dt \tag{3}$$

Where k_1, k_2 are the gains of the sliding mode controller and satisfy $k_1 > 0$, $k_2 > 0$. Where $sgn(s)$ is a symbolic function and satisfies as follows

$$\mathrm{sgn}(s) = \begin{cases} 1, s > 0 \\ -1, s < 0 \end{cases} \tag{4}$$

The derivative of (2) for the slip surface function and substitution of (1) and (3) can be obtained as follows

$$\begin{aligned} \dot{s} &= \dot{x}_{ref} - \dot{x} = \dot{x}_{ref} - (ax + bu + d(t)) \\ &= -bk_1|s|^{\frac{1}{2}}\mathrm{sgn}(s) - bk_2\int \mathrm{sgn}(s)dt + \dot{x}_{ref} - ax - d(t) \end{aligned} \tag{5}$$

To facilitate stability analysis, (5) can be further simplified as follows

$$\dot{s} = -k_1'|s|^{\frac{1}{2}}\mathrm{sgn}(s) - k_2'\int \mathrm{sgn}(s)dt + \sigma \tag{6}$$

where, $\sigma = x_{ref} - ax - d(t)$, $k_1' = bk_1$ and $k_2' = bk_2$.

Stability analysis

Drawing on the Lyapunov function method constructed in (Moreno and Osorio, 2008), the stability analysis of the system shown in Formula. 6 is carried out. Define the state variables as follows

$$\zeta = \begin{bmatrix} \zeta_1 \\ \zeta_2 \end{bmatrix} = \begin{bmatrix} |s|^{\frac{1}{2}}\mathrm{sgn}(s) \\ k_2'\int \mathrm{sgn}(s)dt \end{bmatrix} \tag{7}$$

The state variable ξ is derived as follows

$$\begin{aligned} \dot{\zeta} &= \begin{bmatrix} \frac{1}{2}|s|^{-\frac{1}{2}}\left(-k_1'|s|^{\frac{1}{2}}\mathrm{sgn}(s) - k_2'\int \mathrm{sgn}(s)dt + \sigma\right) \\ k_2'\mathrm{sgn}(s) \end{bmatrix} \\ &= -|s|^{-\frac{1}{2}}\begin{bmatrix} \frac{1}{2}\left(k_1'\zeta_1 + \zeta_2 - \sigma\right) \\ -k_2'\zeta_1 \end{bmatrix} \end{aligned} \tag{8}$$

The Formula. 8 is further simplified as follows

$$\dot{\zeta} = -|s|^{-\frac{1}{2}}(A\zeta - \phi) \tag{9}$$

Where, $A = \begin{bmatrix} \frac{1}{2}k_1' & \frac{1}{2} \\ -k_2' & 0 \end{bmatrix}$, $\phi = \begin{bmatrix} \frac{1}{2}\sigma \\ 0 \end{bmatrix}$

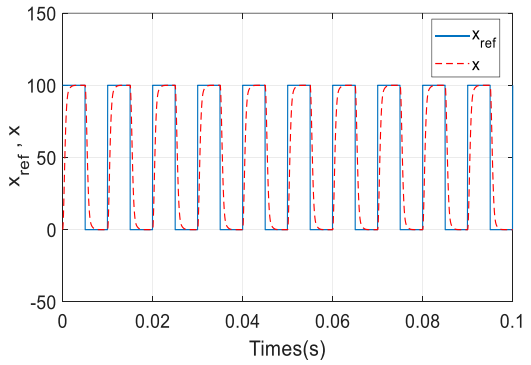

FIGURE 2
Change curve of reference value and actual value.

For the stability analysis of the control system, the Lyapunov function is defined as follows

$$V = \zeta^T P \zeta \tag{10}$$

where P is a real symmetric positive definite matrix and P is designed as follows.

$$P = \begin{bmatrix} \frac{1}{2}{k_1}'^2 + 2k_2' & \frac{1}{2}k_1' \\ \frac{1}{2}k_1' & 1 \end{bmatrix}$$

In order to analyze the system stability, the derivative of Formula. 9 is obtained as follows.

$$\begin{aligned} \dot{V} &= \dot{\zeta}^T P \zeta + \zeta^T P \dot{\zeta} \\ &= -|s|^{-\frac{1}{2}} \zeta^T \left(A^T P + PA\right)\zeta + |s|^{-\frac{1}{2}} \phi^T P \zeta + |s|^{-\frac{1}{2}} \zeta^T P \phi \end{aligned} \tag{11}$$

Assume that ϕ is bounded and satisfies $|\phi| \le \lambda|\zeta_1|$, $\lambda > 0$. Then Formula 11 can be expressed as follows.

$$\begin{aligned} \dot{V} \le & -|s|^{-\frac{1}{2}} \zeta^T \left(A^T P + PA\right)\zeta + |s|^{-\frac{1}{2}} \zeta^T \begin{bmatrix} \lambda & 0 \\ 0 & 0 \end{bmatrix} P\zeta \\ & + |s|^{-\frac{1}{2}} \zeta^T P \begin{bmatrix} \lambda & 0 \\ 0 & 0 \end{bmatrix} \zeta = -|s|^{-\frac{1}{2}} \zeta^T Q \zeta \end{aligned} \tag{12}$$

Where,

$$\begin{aligned} Q &= A^T P + PA - \begin{bmatrix} \lambda & 0 \\ 0 & 0 \end{bmatrix} P - P \begin{bmatrix} \lambda & 0 \\ 0 & 0 \end{bmatrix} \\ &= \frac{k_1'}{2} \begin{bmatrix} {k_1}'^2 + 2k_2' - 2\lambda\left(k_1' + \frac{4k_2'}{k_1'}\right) k_1' - \lambda \\ k_1' - \lambda \qquad\qquad\qquad\qquad 1 \end{bmatrix} \end{aligned}$$

According to Lyapunov stability theorem, if the control system is stable, then (12) should satisfy $\dot{v} \le 0$ Consequently, Q must be a real symmetric positive definite matrix, when the principal sub formula of each order of Q is greater than 0

$$\begin{cases} {k_1}'^2 + 2k_2' - 2\lambda\left(k_1' + \frac{4k_2'}{k_1'}\right) - \left(k_1' - \lambda\right)^2 > 0 \\ k_1' > 0 \end{cases} \tag{13}$$

The simplified (13) is as follows:

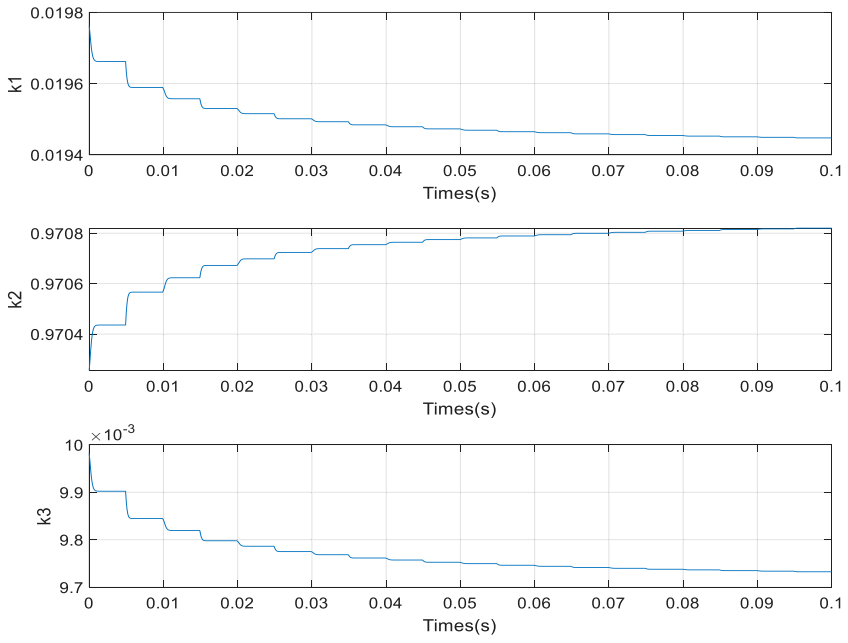

FIGURE 3
The curve of controller parameters k_1,k_2,k_3.

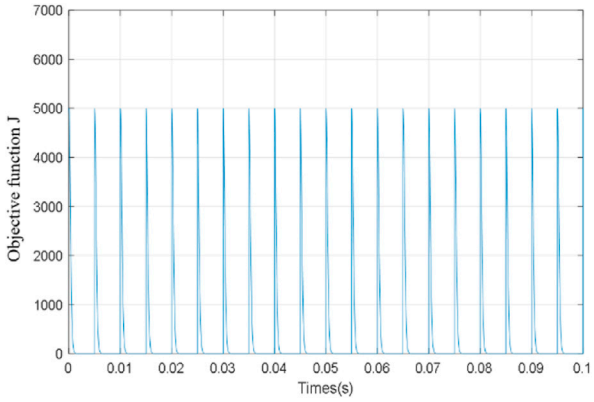

FIGURE 4
The curve of cost function *J*.

$$\begin{cases} k_2' > \dfrac{k_1'\lambda^2}{2(k_1' - 4\lambda)} \\ k_1' > 4\lambda \end{cases} \tag{14}$$

Therefore, under the conditions shown in (14), Q is a real symmetric positive definite matrix. There exists $\dot{V} \leq -|s|^{-\frac{1}{2}}\zeta^T Q\zeta < 0$, which satisfies Lyapunov stability theorem.

Single-neuron sliding mode controller design

Improved sliding mode controller design

The proportional control is combined with the super-twisting sliding mode control to further improve the convergence characteristics and dynamic performance of the Super-twisting sliding mode controller. The improved sliding mode controller is as follows

$$u = k_1|s|^{\frac{1}{2}}\mathrm{sgn}(s) + k_2\int \mathrm{sgn}(s)dt + k_3 s \tag{15}$$

In (15), k_3 is the proportional control gain and satisfies $k_3 > 0$.

Comparing (15) and (3), it can be found that the improved sliding mode controller adds a proportional sliding mode term, and a better control effect can be obtained by designing a reasonable gain of k_3. Although the controller (15) ensures that the system is in a steady state as long as it meets the design requirements of (13) and $k_3 > 0$, however, the specific values of the controller gains k_1, k_2 and k_3 to meet the design requirements cannot be calculated. This posed some difficulties in designing optimal controller parameters k_1, k_2 and k_3.

Thus, in this paper, we designed an adaptive single-neuron sliding mode controller that can adjust the gain of the sliding mode controller online. The control strategy combines the advantages of both the single neuron control strategy with good adaptive capability and simple algorithm with STSM control theory. The detailed design method of the control algorithm is as follows.

Single-neuron sliding mode controller design

Since the single neuron controller uses digital control, the improved sliding mode controller (15) is discretized using the forward difference method to obtain the incremental controller as follows.

$$\begin{aligned} \Delta u(k) &= u(k) - u(k-1) \\ &= k_1\left(|s(k)|^{\frac{1}{2}}\mathrm{sgn}(s(k)) - |s(k-1)|^{\frac{1}{2}}\mathrm{sgn}(s(k-1))\right) \\ &\quad + k_2\mathrm{sgn}(s(k)) + k_3(s(k) - s(k-1)) \end{aligned} \tag{16}$$

The structure of the single neuron adaptive sliding mode controller is shown in Figure 1.

It can be seen from Figure 1 that the controller mainly consists of state converter, single neuron and adaptive learning machine,

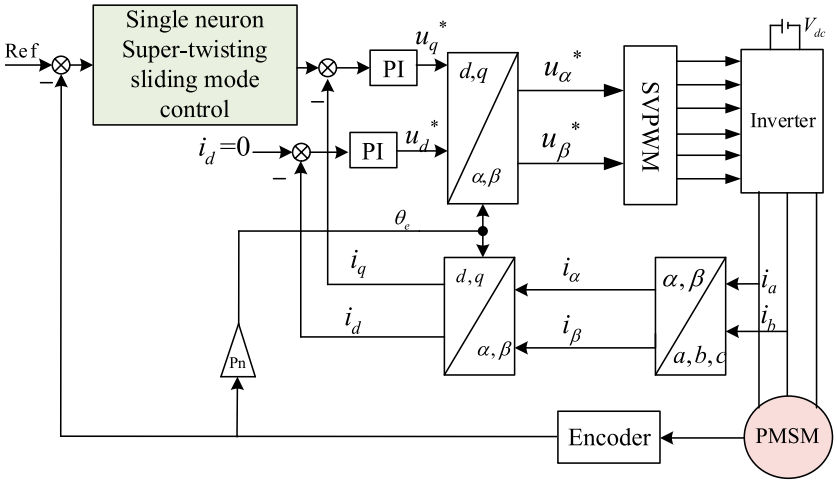

FIGURE 5
Control block diagram for single neuron super-twisting sliding mode control for PMSM system.

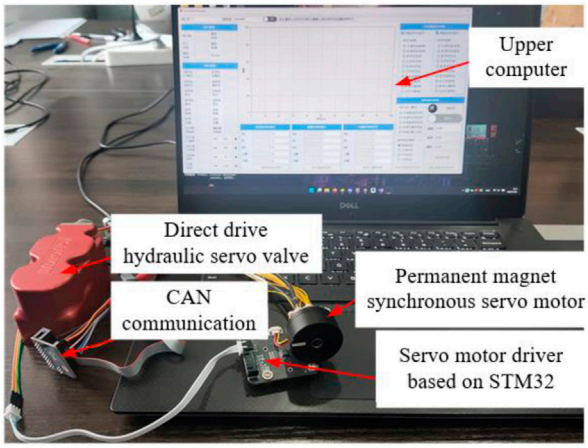

FIGURE 6
Experimental platform of servo motor control.

TABLE 1 Parameters of PMSM.

Parameter and unit	Value
Number of poles pairs	2
Inductance Ld = Lq	1.378 mH
Permanent magnet flux linkage ψ_f	0.0221Wb
Stator phase resistance R	2.15Ω
Moment of inertia	0.175×10^{-4} J/kg.m^2
Viscosity coefficient B/	0.044×10^{-5} N.m.s/rad

and the working principle of each part will be discussed in the following paper.

Define the output $x(k)$ of the state converter as follows

$$\begin{aligned} x_1(k) &= |s(k)|^{\frac{1}{2}}\mathrm{sgn}(s(k)) - |s(k-1)|^{\frac{1}{2}}\mathrm{sgn}(s(k-1)) \\ x_2(k) &= \mathrm{sgn}(k) \\ x_3(k) &= s(k) - s(k-1) \end{aligned} \tag{17}$$

In (17), $s(k)$ is a sliding mode surface function and is the input of a single neuron.

Based on these inputs, the single neuron can calculate the incremental controller. Thus, (16) can be rewritten as follows:

$$\Delta u(k) = K\omega_1(k)x_1(k) + K\omega_2(k)x_2(k) + K\omega_3(k)x_3(k) \tag{18}$$

where K is the gain coefficient of the neuron and satisfies $K > 0$; ω_i (i = 1,2,3) is the weighting coefficient of x_i.

From (16) and (17), we have

$$\begin{cases} k_1 = K\omega_1(k) \\ k_2 = K\omega_2(k) \\ k_3 = K\omega_3(k) \end{cases} \tag{19}$$

Define the objective function of the system as $J = s(k)^2/2$ and the adaptive learning algorithm by the gradient law, we make J converge to zero quickly by adjusting the weights $\omega_i(k)$ along the negative direction of the sliding mode surface of the system makes J converge to zero quickly.

$$\begin{aligned} \omega_i(k) &= \omega_i(k-1) + \Delta\omega_i(k) \\ &= \omega_i(k-1) - \eta_i s(k)\frac{\partial s(k)}{\partial \omega_i(k)} \end{aligned} \tag{20}$$

Where η_i is the learning coefficient.

The learning rule for single neuron weights used the modified Hebb learning rule, and the algorithm was obtained after normalization as follows:

$$\Delta u(k) = K\sum_{i=1}^{3}\omega_i'(k)x_i(k) \tag{21}$$

$$u(k) = u(k-1) + \Delta u(k) = u(k-1) + K\sum_{i=1}^{3}\omega_i'(k)x_i(k) \tag{22}$$

$$\omega_i'(k) = \omega_i(k)\Big/\sum_{i=1}^{3}\omega_i(k) \tag{23}$$

$$\begin{aligned} \omega_1(k) &= \omega_1(k-1) + \eta_1 s(k)u(k-1)(2s(k) - s(k-1)) \\ \omega_2(k) &= \omega_2(k-1) + \eta_2 s(k)u(k-1)(2s(k) - s(k-1)) \\ \omega_3(k) &= \omega_3(k-1) + \eta_3 s(k)u(k-1)(2s(k) - s(k-1)) \end{aligned} \tag{24}$$

Where η_1, η_2, η_3 is the corresponding learning rate respectively.

Simulation verification

To verify the correctness and feasibility of the single-neuron STSM controller proposed in the paper, simulation modeling was performed using Matlab/Simulink simulation software, where the controlled object was a first-order linear system with a transfer function of $G(s) = 1000/(s + 1000)$. In the simulation, the reference value was set to a square wave signal with an amplitude of 100 and a frequency of 100 Hz. The gain coefficient of the neuron was $K = 10$ and the initial value of the gain of the controller was $k_1 = 0.2$, $k_2 = 10$, $k_3 = 0.1$.

The simulation results are shown in Figures 2, 3.

From the simulation results shown in Figure 2, it can be seen that with the single neuron adaptive sliding mode controller, the system output can quickly track the reference value and can achieve overshoot-free operation. The variation curves of controller parameters k_1, k_2 and k_3 are given in Figure 3, and it is obvious from the figure that the single neuron designed in the paper was able to adjust the parameters of the super-twisting sliding mode controller online without manual adjustment, which reduced the workload of parameter adjustment. Figure 4 shows the variation curve of the objective function J. From the figure, it can be seen that the objective function J is 0 at steady state.

Experimental verification of servo motor control system

In order to verify the correctness and feasibility of the proposed single neuron super-twisting sliding mode control method, a single neuron super-twisting sliding mode controller for a permanent magnet synchronous servo motor as shown in Figure 5. The control algorithm used a dual closed-loop control strategy of position loop and current loop, where the position loop used the sliding mode control with online adjustment of controller parameters designed in the paper, and the current loop used PI control. In addition, the experimental platform used STM32F405 chip as the

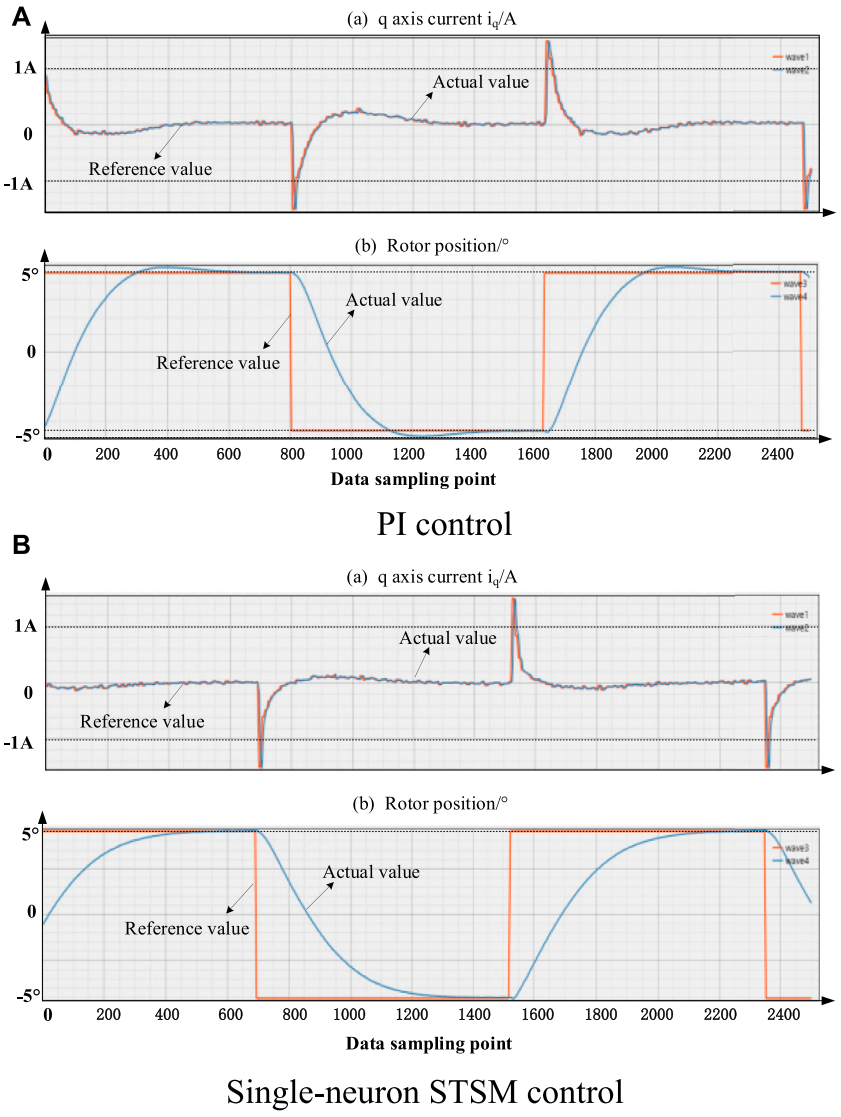

FIGURE 7
Experimental results when the reference value is square wave signal. **(A)** PI control; **(B)** Single-neuron STSM control.

controller, and uploaded the experimental data and state variables of servo motor control to the specific experimental platform through CAN bus as shown in Figure 6. This experimental platform was mainly used for the independent development and application research of direct-drive hydraulic servo valve.

In addition, the parameters of the PMSM are shown in Table 1, and the position loop PI controller parameters are $k_{pp} = 45.5$, $k_{ip} = 15$, the current loop PI controller parameters are $k_{pc} = 145$, $k_{ic} = 6450$. For the proposed single neuron super-twisting sliding mode controller, the gain coefficient of the neuron was $K = 150$ and the initial value of the gain of the controller was $k_1 = 6$, $k_2 = 35$, $k_3 = 2.5$.

The superiority of the proposed control strategy was verified by comparing the analysis with the PI controller for the position loop, and the operating conditions of the servo motor under the two algorithms were identical, and the experimental data were obtained by the host computer. In addition, square wave and sine wave signals were used as command signals to further illustrate the feasibility of the proposed control algorithm, where the amplitude and frequency of the square wave signal are set to 5° and 15Hz, and the amplitude and frequency of the sine wave signal were set to 5° and 20 Hz, respectively. The experimental results are shown in Figures 7, 8.

It can be found that under the action of PI control, the actual position of the servo motor can track the reference value with an overshoot of about 4% by comparing and analysing the experimental results under the two control strategies given in Figure 8. On the contrary, the servo motor can operate without overshoot with relatively short regulation time under the action of the sliding mode controller proposed in this paper.

Similarly, it can be found that under the action of PI control, the actual position of the servo motor is limited by the bandwidth of the PI controller, and there is a large static difference when tracking the sine wave signal, and the q-axis current fluctuates more by comparing and analysing the experimental results under the two control strategies given in Figure 8. On the contrary, the sliding mode control strategy proposed in this paper can track the sinusoidal signal better, and the

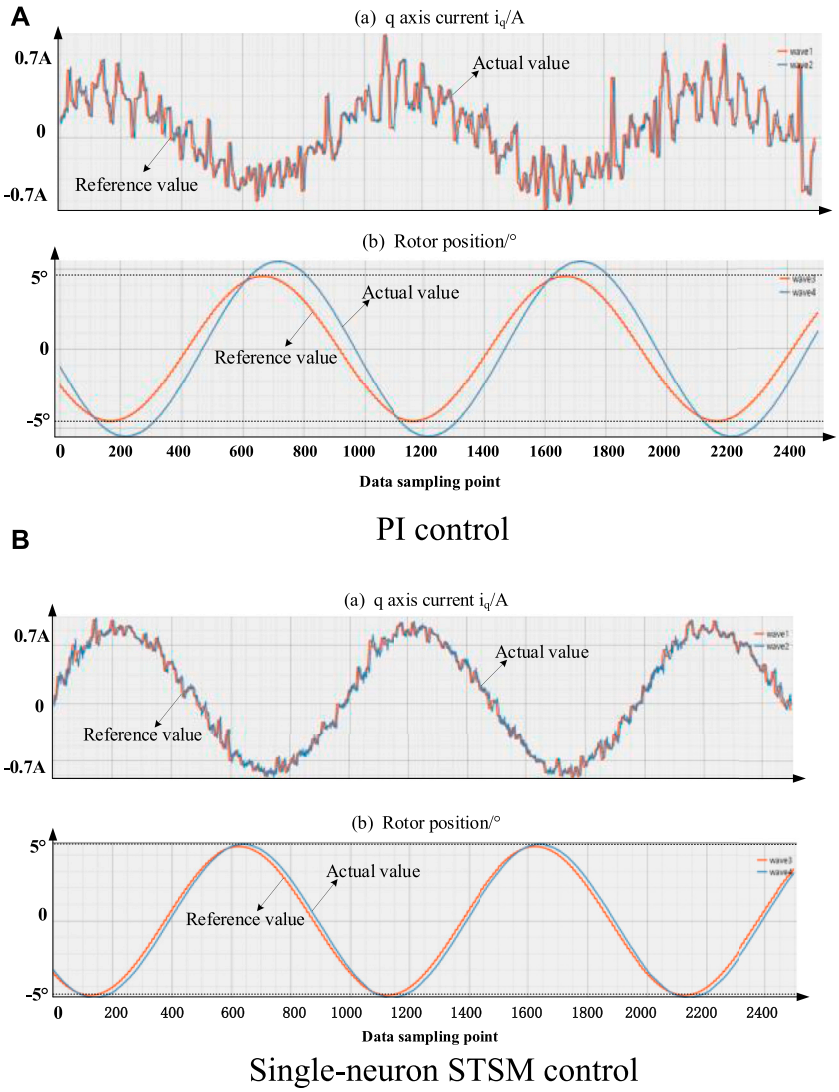

FIGURE 8
Experimental results when the reference value sine wave signal. **(A)** PI control; **(B)** Single-neuron STSM control.

static difference was relatively small, and the q-axis current fluctuation is smaller.

Conclusion

In this paper, a single neuron super-twisting sliding-mode controller was designed based on the control method combining proportional control and super-twisting sliding mode control, using the ability of the single neuron adaptive control algorithm to adjust the controller parameters online. The sliding mode controller designed under this control strategy can realize online adjustment of the controller parameters and had the advantages of simple algorithm, strong robustness, and good chattering suppression effect. The simulation and experimental results demonstrated that the single neuron adaptive control can adjust the parameters of the super-twisting sliding mode controller online and had better dynamic performance and anti-disturbance capability when applied to the servo control system of permanent magnet synchronous motor.

Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

Author contributions

The main work of this paper was completed by LY and PW conducted some theoretical derivation, YL was responsible for writing the paper, and HC and AX were responsible for experimental verification.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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A strategy for improving the SHEPWM commutation speed of CSI through hybrid switches

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High-power current source inverters (CSI) usually operate at a low switching frequency to reduce switching loss. To suppress low-order harmonics and simplify filter design, the selective harmonic elimination pulse width modulation (SHEPWM) technique is a feasible common modulation strategy in industrial applications. This paper proposes an operational strategy that uses an H7 current source inverter (H7-CSI) with hybrid switches to perform the SHEPWM technique. On the basis of retaining the conventional H6 inverter bridge, the commutation speed of the CSI is improved by an additional shunt-connected high-performance power switch. The proposed scheme solves the problem that the CSIs built with low-speed switches (such as GTOs) may have difficulty for implementing the setting pulse widths of null states, while further reducing the switching losses at an acceptable cost. In addition, mitigating the influence of overlap-time by optimizing the driving signal of the H6 converter bridge. Finally, simulation and experiments have verified the effectiveness of the proposed CSI scheme.

KEYWORDS

selective harmonic elimination pulse width modulation (SHEPWM), current source inverter, minimum pulse width, commutation speed, hybrid switch

1 Introduction

With the emergence of the worldwide energy shortage crisis, more and more attention has been paid to renewable energy (Shahbaz et al., 2020). Under the future trend of the energy revolution, power inverters are playing a vitally important role in the future grid (Sahan et al., 2011). From the form of power supply on the DC side, inverters can be classified as voltage source inverter (VSI) and current source inverter (CSI). Compared to VSI, CSI has the advantages of boosting voltage capability and high reliability (Zmood and Holmes, 2001; Azmi et al., 2011), and it is considered to have potential application value in renewable energy conversion, e.g., photovoltaic (Sahan et al., 2008; Lorenzani et al., 2017), wind energy, and ocean energy systems.

At present, the primary problem of CSI is the high power loss of switching devices, which mainly owing to the fact that CSI has to hold the circuit with a constant current (Trzynadlowski et al., 2001). There are two main technical routes to solve the efficiency problem: One is to replace all the switches with advanced semiconductor devices (e.g., Silicon Carbide (SiC) and Gallium Nitride (GaN) power switches but leaving great burden on the hardware cost of the equipment (Abu-Khaizaran and Palmer, 2007; Mudholkar et al., 2014; Hazra et al., 2016; Guacci

et al., 2019). Another one is to try to make CSI work at a much lower switching frequency (Espinoza and Joos, 1997). However, it carries the risk of reducing power quality. With the introduced large amount of low-order harmonics, the filters are more difficult to design.

The selective harmonic elimination pulse width modulation (SHEPWM) technique is one of the effective solutions to address the above challenges. It is characterized by low switching frequency and excellent harmonic performance, particularly suitable for high-power applications that mitigate switching loss by reducing switching frequency (Pontt et al., 2004; Dahidah et al., 2015). During the implementation of SHEPWM, there are two key issues that need to be considered: one is the establishment of the switching sequence model which determines the harmonic performance, and another is the solution of non-linear transcendental equations which determines the difficulty and accuracy of realization. Karshenas, H. and Kojori, H. investigated the unique characteristics of CSI commutation, and carried out the general CSI switching sequence models (Karshenas et al., 1995). Over the past few decades, scholars have proposed many fruitful methods to find the optimal solutions. Siddique, M.D. using a particle swarm optimization (PSO) algorithm to calculate switching angles. (Siddique et al., 2021). The Newton-Raphson iterative algorithm is the most commonly used method to solve the equations, which needs to find the initial value to fast convergence. Maswood, A.I. proposed using Genetic Algorithm to find the initial switching angels (Maswood et al., 2001). In addition, optimized switching angles are calculated using APSO-GA for seven-level and nine-level inverter (Memon et al., 2022).

Operated with SHEPWM, CSI can effectively eliminate low-order harmonics in theory. However, due to the low switching speed of CSI power switches in practical application, the actual output performance is usually inconsistent with the expectation, some low-order harmonics still occupy a large proportion. This paper analyzes this phenomenon and proposes a new SHEPWM implementation scheme to improve the commutation speed through H7-CSI with hybrid semiconductor switches. Compared to the conventional low-speed switch-based CSIs, the proposed scheme can promote the commutation speed without excessive hardware cost to obtain a better output performance.

This rest of paper is organized as follows. In Section 2, it describes the general SHEPWM implementation process of conventional H6-CSI, and analyzes the limitation of switching speed on modulation. In Section 3, the operational principles of SHEPWM with H7-CSI as well as the hardware configurations are presented in detail. In Section 4, simulation and experimental tests are carried out to validate the theoretical findings.

2 SHEPWM of conventional current source inverters

2.1 Conventional current source inverters topology and its switching combinations

The conventional three-phase CSI is also named as H6-CSI, the topology is shown in Figure 1. It usually uses a voltage power supply and a DC-link inductor to achieve the approximately constant current source I_{dc}. H6 inverter bridge can realize the current commutation and output the three-phase switched currents i_a, i_b, i_c. After the AC filter capacitor C_a, C_b, C_c, the output currents are i_{ao}, i_{bo}, i_{co}. For high-power CSI, H6 inverter bridge is mainly composed of six low-speed power switches (e.g., GTOs, IGCTs) (Xu et al., 2023). When IGBTs are selected, it requires series connected power diodes to increase the reverse-blocking (RB) capability.

At any moment during modulation, there are two switches conducting ON, one on the upper arms (S_1 or S_3 or S_5), and another on the lower arms (S_4 or S_6 or S_2). And CSI adopts lateral commutation mode among the bridge arms. There are nine switching states in total, six of which are active states ({S_1, S_2}, {S_1, S_6}, {S_2, S_3}, {S_3, S_4}, {S_4, S_5}, {S_5, S_6}), the rest three are null states ({S_1, S_4}, {S_2, S_5}, {S_3, S_6}). It is worth noting that the null states actually behave as short-circuit status of the circuit, which is also denoted as the short-circuit pulses in this paper.

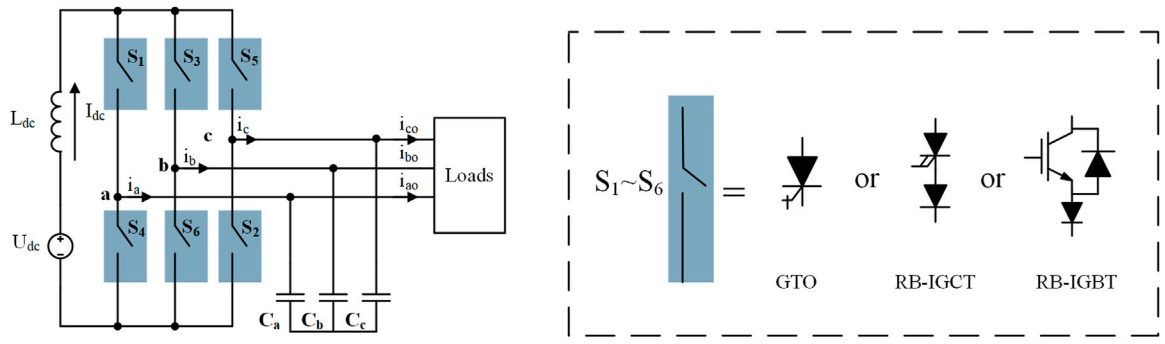

FIGURE 1
Conventional H6-CSI topology and hardware configurations.

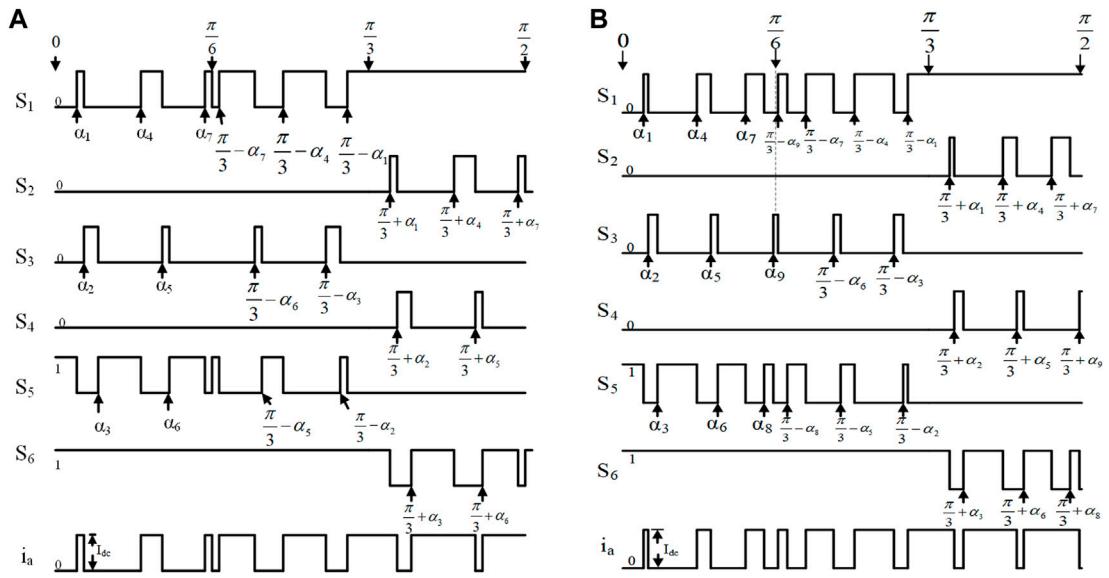

FIGURE 2
(A) SHEPWM scheme of H6-CSI (N = 7), **(B)** SHEPWM scheme of H6-CSI (N = 9).

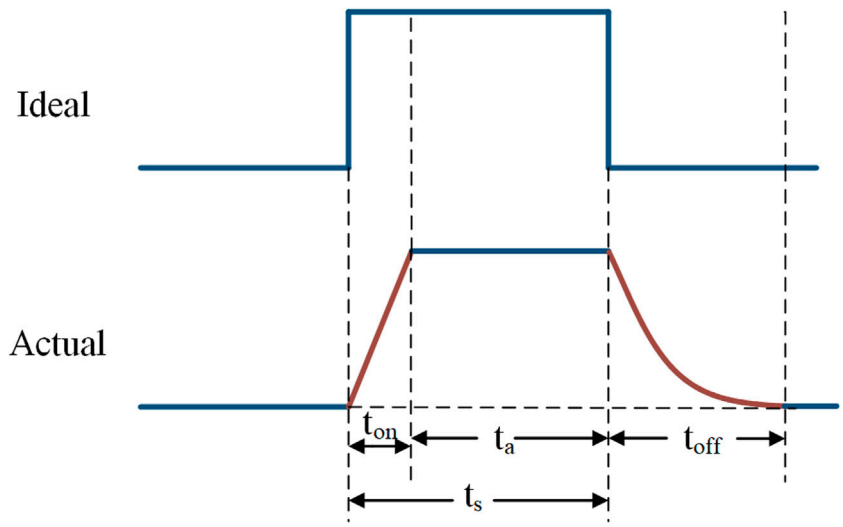

FIGURE 3
The comparison between ideal and actual current waveforms.

2.2 SHEPWM implementation method and the limitations

The SHEPWM method can remove low-order harmonics from the inverter's output by setting the appropriate angles of switching operation. The conventional CSI SHEPWM method is implemented by introducing short-circuit pulses and setting transitions, which is completely different from VSI SHEPWM. Literature (Karshenas et al., 1995) have investigated and listed these differences in the SHEPWM between VSI and CSI in detail.

The operational steps of SHEPWM of conventional CSI are as follows. Step 1: select the low-order harmonics to be eliminated, and set the number of switching angles. N is the number of switching angles and also represents that (N-1) harmonics can be eliminated (e.g., setting N = 5 means to eliminate the harmonics of 5^{th}, 7^{th}, 11^{th}, 13^{th}). It is worth noting that, to maintain the continuity of the current, the switching angles should be set within (0, π/6). Step 2: build the pulse sequences. The characteristic of this scheme is that the driving signals of switches (S_1 ~ S_6) lags π/3 in turn and the output waveform of three-phase current i_a, i_b and i_c lags 2π/3 in turn.

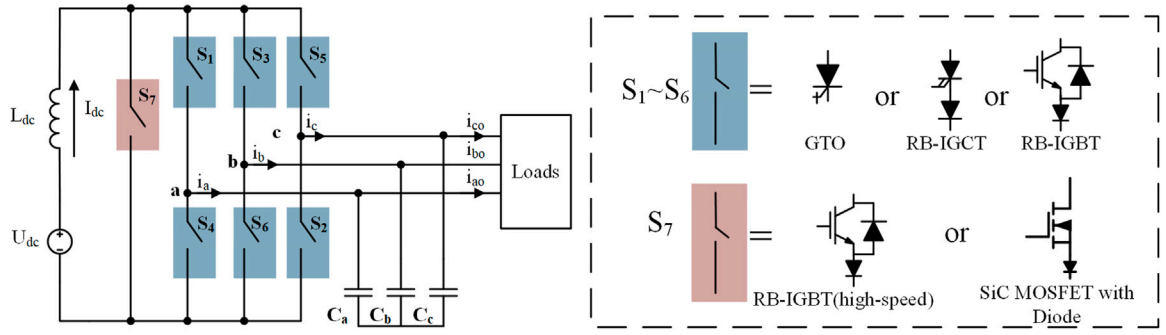

FIGURE 4
H7-CSI topology and hardware configurations.

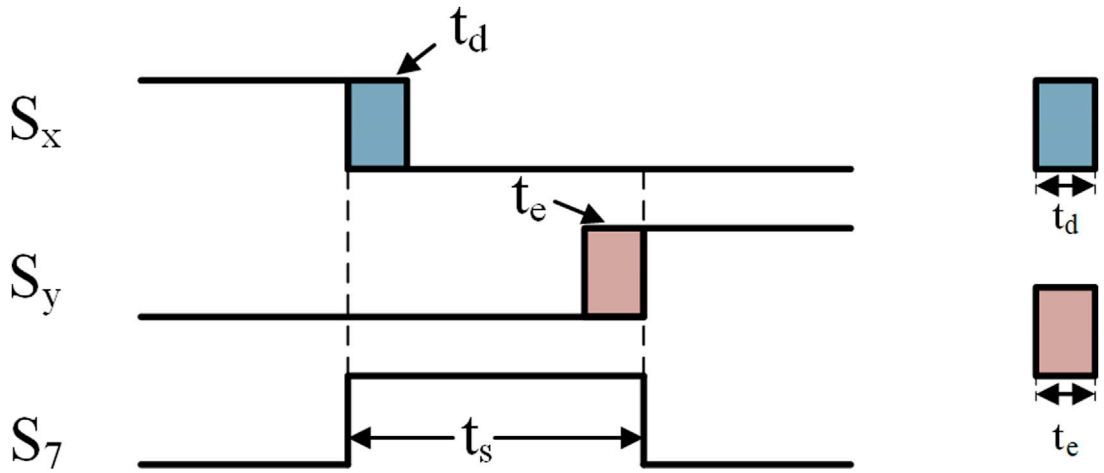

FIGURE 5
Overlap-time optimization scheme.

Step 3: formulate the output current $i(\omega t)$ expression, which owns the features of half-wave symmetry and quarter-wave symmetry. Fourier decomposition is performed on the output current $i(\omega t)$. The decomposition formula is shown as Eq. 1, where $I_{a,n}$ is the amplitude of n^{th} order harmonic of the output phase current i_a, and $I_{a,n}$ can be calculated by Eq. 2.

$$i(\omega t)_{=}\sum_{n=1}^{\infty} I_{a,n}\sin(n\omega t) \tag{1}$$

$$I_{a,n} = \frac{4}{\pi}\int_{0}^{\frac{\pi}{2}} i(\omega t)\sin(n\omega t)d(\omega t) \tag{2}$$

Denote the amplitude of the fundamental current as $I_{a,1}$. Then, the modulation index m can be expressed by Eq. 3. Thus, the switching angles under different modulation index can be solved.

$$m = \frac{I_{a,1}}{I_{dc}} \tag{3}$$

The following takes N = 7 and N = 9 as examples to explain the specific implementation method. When N = 7, the harmonic orders to be eliminated are 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}. Therefore, seven switch angles are set (α_1, α_2, α_3, α_4, α_5, α_6, α_7). The specific pulse sequence in a quarter of one period is shown in Figure 2A. The driving sequence of each power switch has four short-circuit pulses in one period. $I_{a,n}$ can be formulated as Eq.4. Using Eq. 3 and Eq. 4, and set $I_{a,n} = 0$ (n = 5, 7, 11, 13, 17, 19), the switching angles can be solved out.

$$I_{a,n} = \frac{4I_{dc}}{n\pi}\begin{bmatrix} cosn\alpha_1 - cosn\alpha_2 + cosn\alpha_4 - cosn\alpha_5 + cosn\alpha_7 - cos\left(\frac{n\pi}{6}\right) \\ +cosn\left(\frac{\pi}{3}-\alpha_7\right) - cosn\left(\frac{\pi}{3}-\alpha_6\right) + cosn\left(\frac{\pi}{3}-\alpha_4\right) - cosn\left(\frac{\pi}{3}-\alpha_3\right) \\ +cosn\left(\frac{\pi}{3}-\alpha_1\right) - cosn\left(\frac{\pi}{3}+\alpha_2\right) + cosn\left(\frac{\pi}{3}+\alpha_3\right) - cosn\left(\frac{\pi}{3}+\alpha_5\right) \\ +cosn\left(\frac{\pi}{3}+\alpha_6\right) - cos\left(\frac{n\pi}{2}\right) \end{bmatrix} \tag{4}$$

Similarly, when N = 9, to eliminate harmonic of 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23rd, 25^{th}, the n^{th} harmonic expression of the output current can be formulated as Eq.5. The specific pulse sequence in a quarter of one period is shown in Figure 2B. Compared to the previous sequence (N = 7), the driving

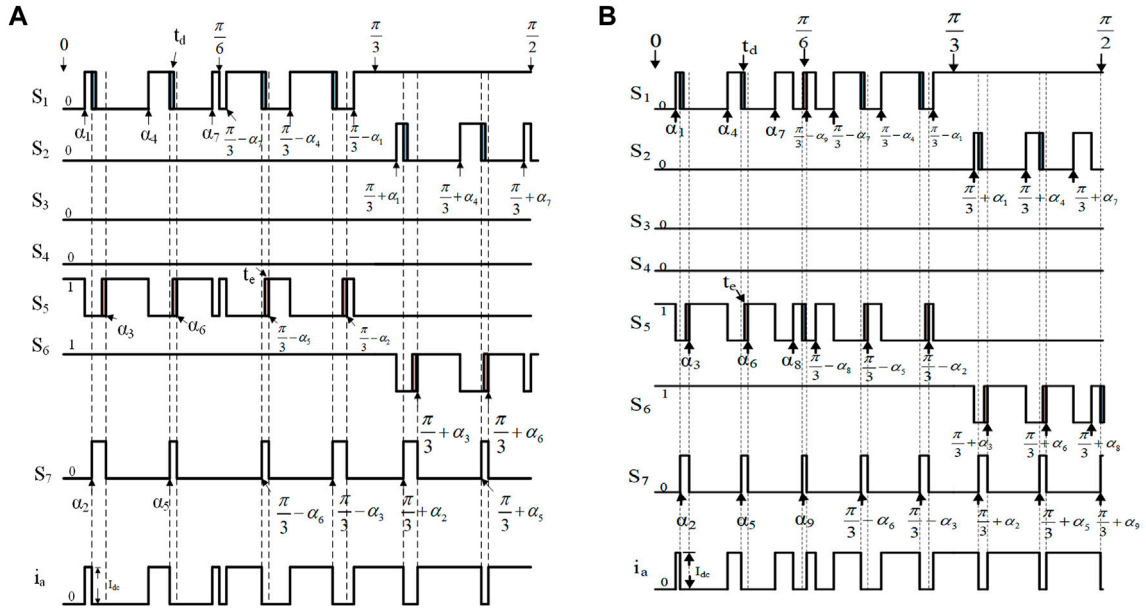

FIGURE 6
(A) SHEPWM sequences of H7-CSI (N = 7), **(B)** SHEPWM sequences of H7-CSI (N = 9).

TABLE 1 Comparison of switching characteristics in one period.

Topology	Commutation speed		Switching loss	
	Active state	Null state	N = 7	N = 9
H6-CSI	Depend on S_1~S_6	Depend on S_1~S_6	180 hard switching	216 hard switching
H7-CSI	Depend on S_1~S_6	Depend on S_7	48 zero current switching	60 zero current switching
			132 hard switching	156 hard switching

pulses (N = 9) of switch S_1 ~ S_6 become denser and have introduced more short-circuit pulses in one period.

$$I_{a,n} = \frac{4I_{dc}}{n\pi}\begin{bmatrix} cosn\alpha_1 - cosn\alpha_2 + cosn\alpha_4 - cosn\alpha_5 + cosn\alpha_7 - cosn\alpha_8 \\ +cosn\left(\frac{\pi}{3}-\alpha_9\right) - cosn\left(\frac{\pi}{3}-\alpha_8\right) + cosn\left(\frac{\pi}{3}-\alpha_7\right) - cosn\left(\frac{\pi}{3}-\alpha_6\right) \\ +cosn\left(\frac{\pi}{3}-\alpha_4\right) - cosn\left(\frac{\pi}{3}-\alpha_3\right) + cosn\left(\frac{\pi}{3}-\alpha_1\right) - \text{cosn}\left(\frac{\pi}{3}+\alpha_2\right) \\ +cosn\left(\frac{\pi}{3}+\alpha_3\right) - \text{cosn}\left(\frac{\pi}{3}+\alpha_5\right) + \text{cosn}\left(\frac{\pi}{3}+\alpha_6\right) - \text{cosn}\left(\frac{\pi}{3}+\alpha_9\right) \end{bmatrix} \quad (5)$$

The above is the modulation scheme under theoretical analysis and ideal conditions. In practical applications, the current of the switch can reflect the commutation process (Bernet et al., 1999). Since the power switch has turn-on time and turn-off time in actual operation, the current of the switch has a rising time (t_{on}) and a falling time (t_{off}), which are different from the ideal waveforms. The comparison between ideal and actual current waveforms are shown in Figure 3. The dwell time of an ideal driving pulse is recorded as t_s, and the dwell time of the actual switching pulse is recorded as t_a. Apparently, the effective pulse width of actual switching is shorter than the ideal setting dwell time. Therefore, the actual current rising and falling process can make the switching angles inconsistent with expectations.

TABLE 2 Simulation parameters.

Parameter	Value
DC source voltage (U_{dc})	100 V
DC-link inductor (L_{dc})	5 mH
AC filter capacitor (C)	20 uF
Output resistive loads (R)	20 Ω
Modulation index (m)	0.9
Modulation frequency (f)	50 Hz

Since high-power CSIs are employed with low-speed switches, the turn-on and turn-off process can last up to a few microseconds. Furthermore, with the increase of the modulation index as well as the number of switching angles, the drive pulses become denser. In particular, the shortest pulse width comes from the null state, so that

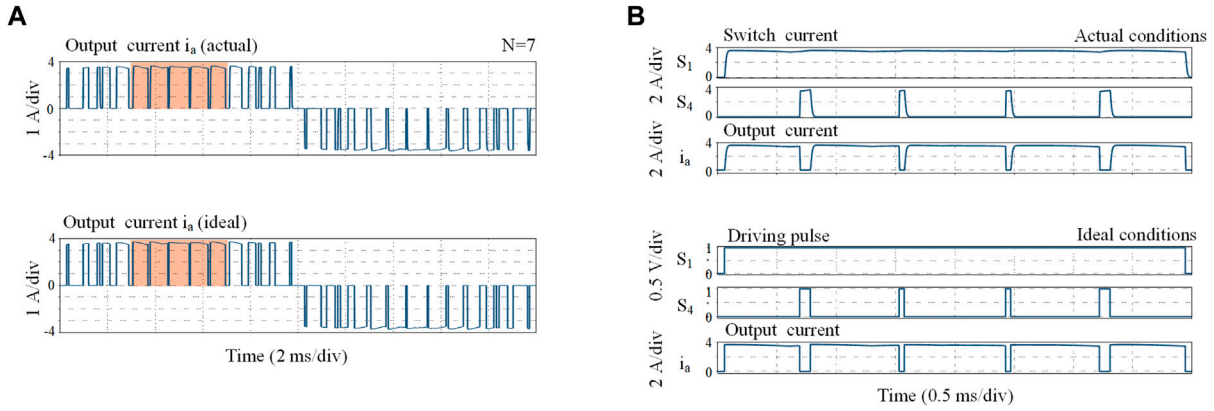

FIGURE 7
(A) Simulated output switched current i_a of H6-CSI (N = 7), **(B)** Corresponding zoomed view within (π/3, 2π/3).

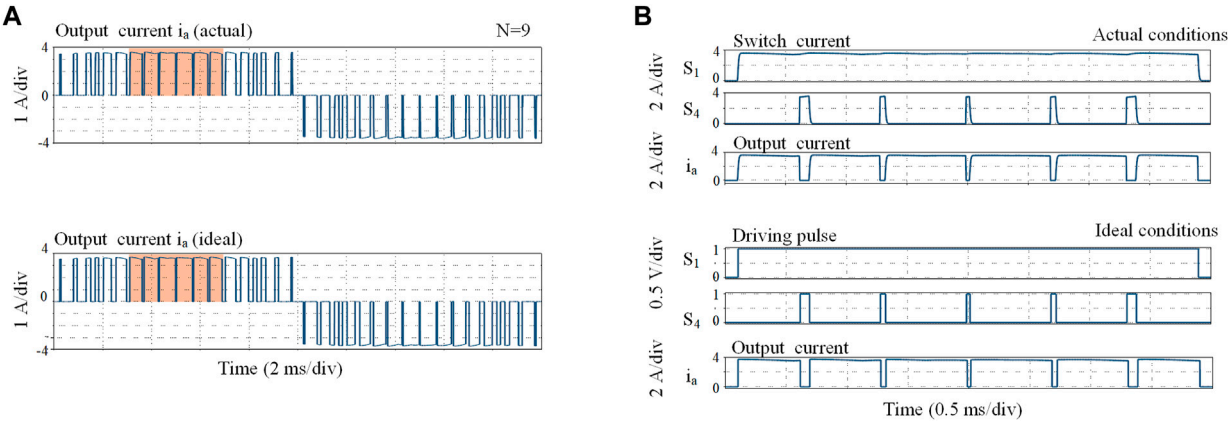

FIGURE 8
(A) Simulated output switched current i_a of H6-CSI (N = 9), **(B)** Corresponding zoomed view within (π/3, 2π/3).

the completion of the short-circuit pulses will be significantly affected by the commutation speed of switches. For example, when m = 0.96 and N = 9, the shortest pulse width occurs at the short-circuit states, which has a width of only about 29 μs. Therefore, conventional CSI who built with low-speed switches (e.g., GTOs, IGCTs) may have difficulty in the switching speed to keep up with the setting short-circuit pulses width, so that the output current cannot reach the expected performance.

In addition, to maintain the continuity of the DC link current, the overlap-time has to be introduced between two switching signals during commutation (Suroso and Noguchi, 2020; Liu et al., 2021). To guarantee the commutation of the low-speed switches is completed, the delay of switching pulses caused by the overlap-time cannot be ignored as well. If not properly set, this phenomenon at short-circuit states will greatly worsen the total harmonic distortion (THD) performance. Therefore, the configuration of overlap-time also need to be carefully considered in conventional CSI.

3 Proposed SHEPWM operational principle with H7-CSI

3.1 Topology and hardware configurations

To improve the commutation speed of low-speed switches of SHEPWM-CSI, this paper proposes a new SHEPWM operational scheme based on the H7-CSI. The topology of the H7-CSI is shown in Figure 4. Compared to conventional CSI, the basic feature of the H7-CSI topology is the added shunt-connected seventh switch, which is the key to improve the inverter's performance (Wang et al., 2018). The seventh switch is connected in parallel with the DC bus, which can be used to replace all the null states. Within 30° power factor angle range, when S_7 is turned on, the current will be quickly switched to this branch, and the remaining six switches can turn on/off with zero current switching (ZCS) capability.

In terms of hardware configuration, the six power switches in the H6 converter bridge retains the same (low-speed switches)

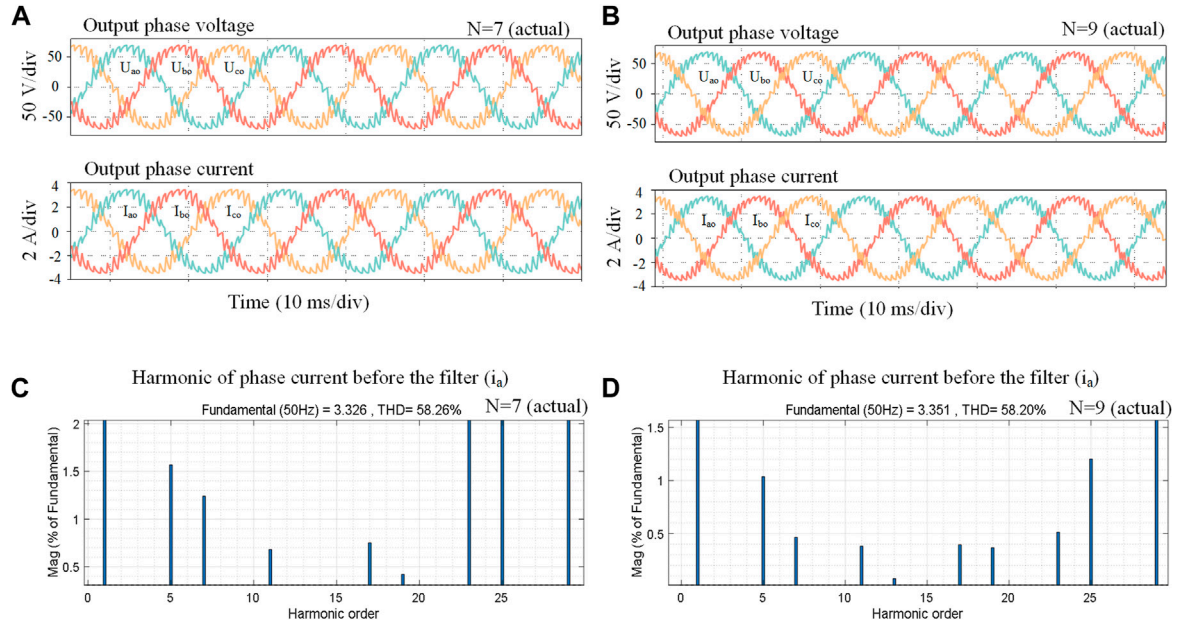

FIGURE 9
Simulated outputs **(A)** Filtered waveforms of conventional SHEPWM-H6-CSI with N = 7, **(B)** Filtered waveforms of conventional SHEPWM-H6-CSI with N = 9, **(C)** Harmonic performance of i_a with N = 7, **(D)** Harmonic performance of i_a with N = 9.

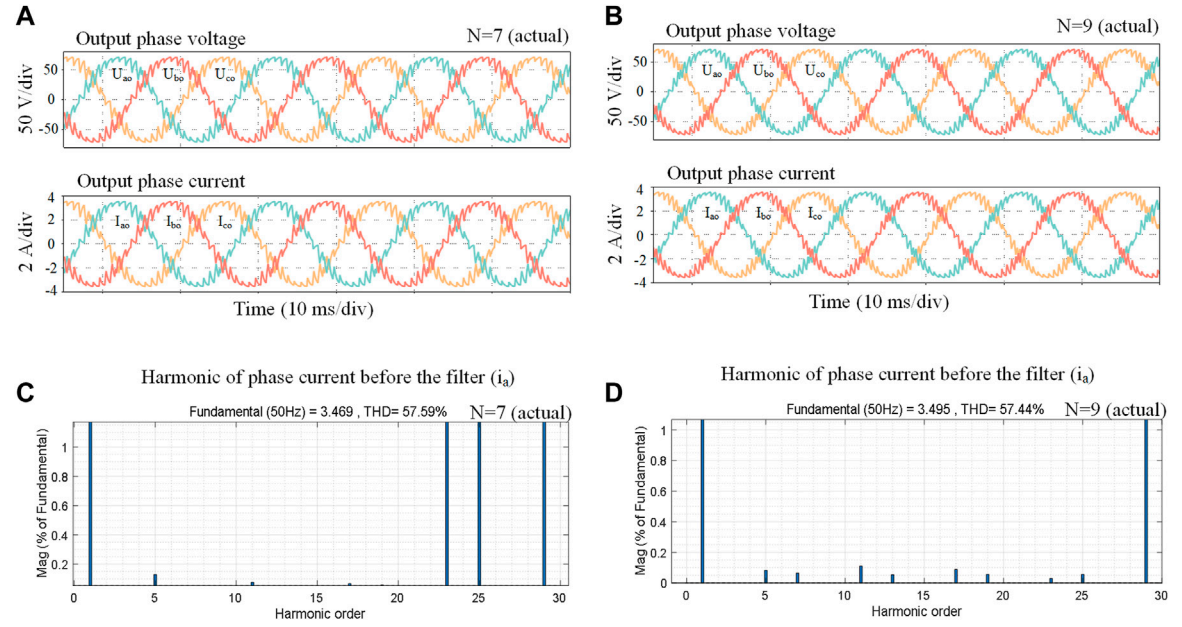

FIGURE 10
Simulated outputs **(A)** Filtered waveforms of proposed SHEPWM-H7-CSI with N = 7, **(B)** Filtered waveforms of proposed SHEPWM-H7-CSI with *N* = 9, **(C)** Harmonic performance of i_a with N = 7, **(D)** Harmonic performance of i_a with *N* = 9.

configuration scheme as the conventional CSI. The key difference is that the seventh switch uses a high-performance power switch. This seventh switch should be characterized by high switching frequency and low loss, which can increase the inverter commutation speed while reducing switching loss. Available choices are high-speed RB-IGBT, or SiC MOSFET with Diode, *etc.* The reverse-blocking capability can be realized *via* series connected power diodes. Compared with the conventional all-hardware-update routine of

TABLE 3 Harmonic performance (% of fundamental).

m = 0.9	5th	7th	11th	13th	17th	19th	23rd	25th	THD (%)
N = 7 (H6-CSI)	1.58	1.25	0.68	0.00	0.75	0.42	—	—	58.26
N = 7 (H7-CSI)	0.14	0.00	0.07	0.00	0.06	0.05	—	—	57.59
N = 9 (H6-CSI)	1.05	0.48	0.39	0.08	0.40	0.38	0.52	1.21	58.20
N = 9 (H7-CSI)	0.09	0.07	0.11	0.06	0.09	0.06	0.03	0.07	57.44

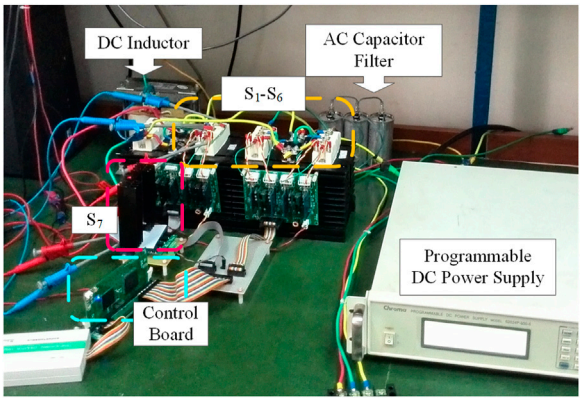

FIGURE 11
Experimental prototype of the H7-CSI.

TABLE 4 Experimental parameters.

Parameter	Value
IGBT-Module (S_1-S_6)	FF100R12RT4 from Infineon
SiC-MOSFET (S_7)	C2M0040120D from Cree
DC source voltage (U_{dc})	120 V
DC-link inductor (L_{dc})	5 mH
AC filter capacitor (C)	20 μF
Output resistive loads (R)	20 Ω
Modulation index (m)	0.9

CSI, the H7-CSI topological solution adopted in this paper can clearly reduce the hardware cost.

3.2 SHEPWM operational principle

The basic idea of proposed SHEPWM solution is to use the seventh switch to help the commutation of other low-speed switches. The specific operating principles are as follows.

1) Select the low-order harmonics to be eliminated, set the number of switching angles, then build the pulse execution scheme of switch S_1~S_6 and formulate the expression of the output current i (ωt), which is basically the same as the conventional SHEPWM-H6-CSI method.
2) Pick out the short-circuit states among the calculated angles, and manage to use switch S_7 to implement these null state pulses.
3) Optimize the driving signal of switch S_1~S_6, regarding the overlap-time issue.

The overlap-time optimization process is pictured as Figure 5. Because the null-state pulses of S_7 are inserted between two different active states (implemented by S_1-S_6), the adjacent turn-off and turn-on operation of S_1-S_6 can be extended with no impact to the output of the circuit. As shown in Figure 5, the original driving sequence is {S_x turn-off, S_7 turn-on} to {S_7 turn-off, S_y turn-on}. To optimize the driving signal, S_x should be delayed for shutdown, the delay time is denoted as t_d, while S_y should be turned on in advance, which is denoted as t_e. Both t_d and t_e should be set within (0, t_s). And the pulse width of S_7 itself remains unchanged. Doing so, on the one hand, it solves the overlap-time issue with no interference to the power quality, and on the other hand, the switching speed challenge of S_1-S_6 can get relieved.

Normally, the delay time and advance time are set as 1–3 μs. Under the premise of meeting the requirements of the rules, the delay time and advance time can be optimized according to the switching speed of the switch.

According to the operating principles described above, pulse sequences of N = 7 and N = 9 can be rebuild, as shown in Figure 6A and Figure 6B. The optimized overlap-time is represented by the shaded area in Figure 6.

The switching characteristics of the proposed SHEPWM scheme with H7-CSI and the conventional SHEPWM-H6-CSI are compared, as shown in Table 1. The proposed SHEPWM scheme basically uses S_7 to improve the commutation speed around the null states, which would be affected by the switching speed most. Since S_7 is characterized by fast switching speed and low switching loss, it is obvious that its actual performance is determined by the hardware selection of S_7.

As for the switching operation, compared to the conventional SHEPWM-H6-CSI, the total number of hard-switching counts of the proposed SHEPWM-H7-CSI is reduced by almost one-third. Moreover, most of the hard-switching transitions are implemented by S_7, which can further reduce the switching loss. In addition, because the implementation of null states uses less power devices, the conduction loss can also decrease. Therefore, it indicates that the proposed SHEPWM-H7-CSI solution can even perform better efficiency.

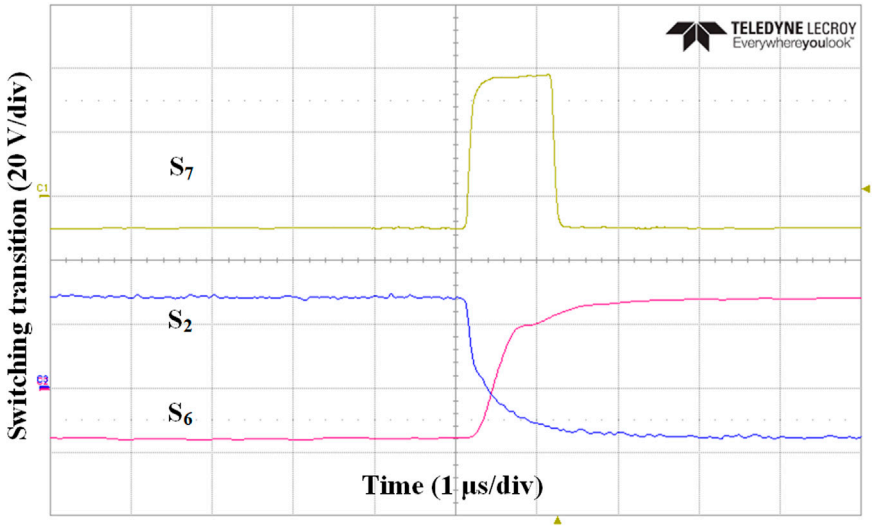

FIGURE 12
Experimental waveforms of switching transition.

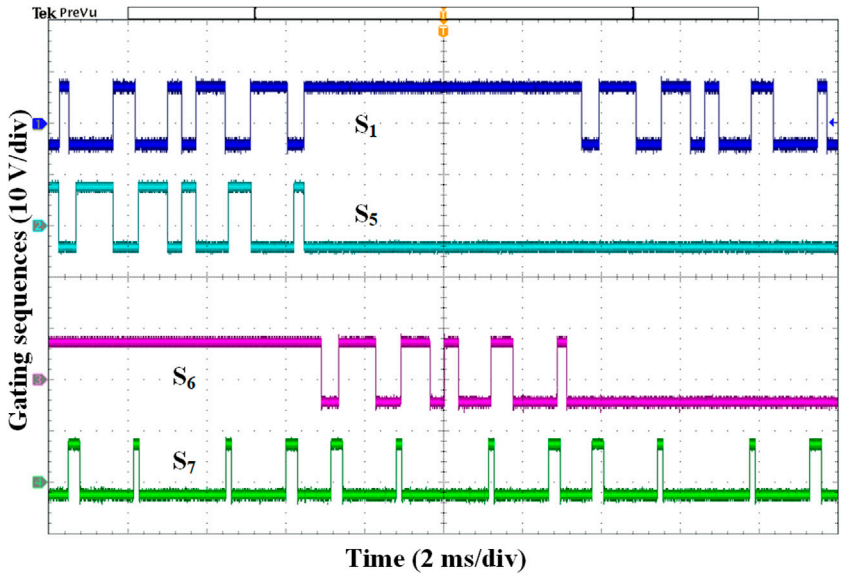

FIGURE 13
Experimental gating pulses sequences.

4 Performance evaluation

4.1 Simulation results

To compare the performance between conventional SHEPWM-H6-CSI and the proposed SHEPWM operational method with H7-CSI, simulation models have been set up using MATLAB with PLECS Blockset, where H6-CSI and H7-CSI are built with the same parameters. The simulation parameters are listed in Table 2.

The conventional H6-CSI using the SHEPWM method is first simulated. The power circuitry is established by PLECS Blockset, which can simulate the turn-on and turn-off process of the power switches. To simulate the behavior of the self-controlled low-speed switches while taking the actual capabilities of the simulation environment into account, the power switch S_1~S_6 are built with the "IGBT with Limited di/dt model", where the "rise time" and "fall time" are configured with 10 s of microsecond. Other parasitic parameters (such as the blocking voltage, stray inductance, on-resistance, *etc.*) are modeled after

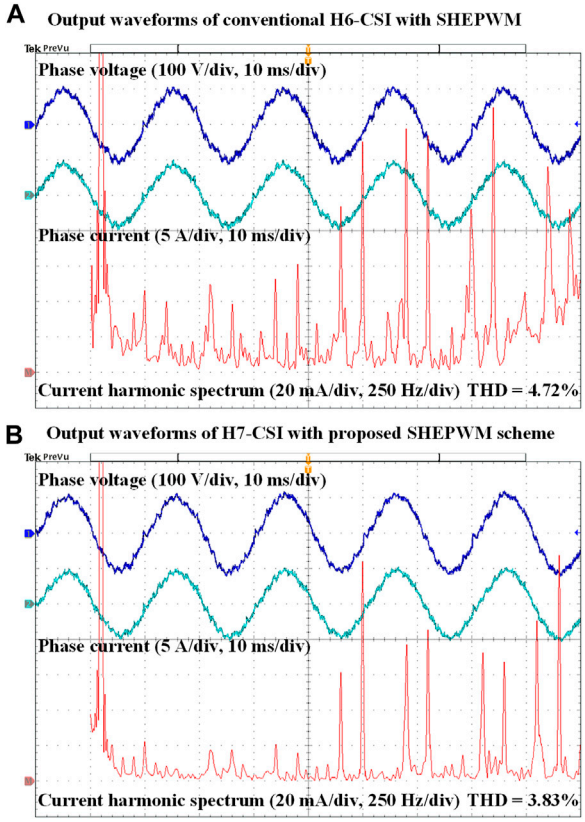

FIGURE 14
(A) Experimental output waveforms of conventional H6-CSI with SHEPWM, **(B)** Experimental output waveforms of conventional H7-CSI with SHEPWM.

the datasheet of typical low-speed switches. MATLAB is used to implement the driving-pulse sequences and analyze the output waveform.

Figure 7A shows the comparison of the output switched current i_a (before the filters) at N = 7. The upper and lower waveforms represent the actual and ideal switched currents, respectively. A zoomed view of the two waveforms during ($\pi/3$, $2\pi/3$) is demonstrated in Figure 7B. During this period, S_1 remains on state, and S_4 performs short-circuit pulses. As can been seen from the comparison, there exists a slight difference in the operating angles as well as the width of switching pulse. The same trend can also be found in Figure 8, which is the waveform comparison of the output switched current with N = 9. Therefore, the phenomenon of actual commutation difference caused by switching speed is reproduced.

Figures 9A,B shows the actual filtered output three phase currents and voltages of H6-CSI using the SHEPWM methods at N = 7 and N = 9, respectively. Figures 9C,D are the corresponding FFT analysis results. These simulation results show that with the increase of switching angles, the pulse sequences become denser. If the low switching speed is taken into account, the low-order harmonics will not be eliminated entirely, which has the high contents of 5^{th} and 7^{th} harmonics.

The following simulation are the verification of the proposed SHEPWM scheme based on H7-CSI method. The power circuitry of H7-CSI is also built in PLECS Blockset. Switch S_7 is set with a shorter turn-on and turn-off time than that of S_1~S_6. Taking N = 7 as an example, the output three-phase voltage and current after the capacitor filters are shown in Figure 10A. And the harmonics of the output current i_a are analyzed by FFT which is shown in Figure 10B. When N = 9, the filtered output waveforms and harmonic analysis of H7-CSI are shown in Figures 10C,D, respectively. The contents of low-order harmonics to be eliminated have been compared and listed in Table 3, which can give a clear view of the harmonic differences. Observing from Figure 10, it can be found that the low-order harmonic contents are almost zero. Compared with the THD value of 58.26% for conventional SHEPWM-H6-CSI with low-speed switches in Figure 9C and Figure 10C, the THD value of proposed SHEPWM based on H7-CSI is 57.59% with the proposed modulation method. These THD values are 58.20% and 57.44% in Figure 9D and Figure 10D, respectively. It is worth noting that low-order harmonics content of 5^{th} and 7^{th} decreased significantly. To sum up, the low-order harmonics that to be eliminated are significantly reduced with the proposed solution. Therefore, the output power quality has been improved.

4.2 Experimental verifications

To verify the performance of the proposed SHEPWM strategy with H7-CSI, an experimental prototype is established displayed in Figure 11. The parameter experimental settings are shown in Table 4. On the controller board, the gating sequences are programmed and implemented by an FPGA of xc3s500e from the family of XILINX Spartan3E. In the power circuitry, the DC inductor, the output capacitor filter and the output resistive loads are consistent with the simulation model. To perform the low switching speed of power switches, S_1-S_6 are selected with modular IGBTs (FF100R12RT4 from Infineon), and the driving resistance is set with 40 Ω S_7 is employed by a silicon carbide power MOSFET (C2M0040120D from Cree).

Figure 12 shows the experimental driving pulses of switches S_7, S_2, S_6 respectively. In Figure 12, the modulation state sequence is from {S_1, S_2}, *via* {S_7}, to {S_1, S_6}. As expected, S_2 and S_6 switch much slower than S_7. To be specific, the turn-on and turn-off time of S_2 and S_6 are nearly 3 μs, while the switching speed of S_7 is less than 200 ns.

Set N = 7 for experimental verification, the gating pulses of switches S_1, S_5, S_6 and S_7 for one period are captured as Figure 13. It is easy to find that the experimental sequences are consistent with the theoretical settings, which have been presented in Figure 6. And the commutation features conform to the description in Table 1.

To go a step further, an additional experimental prototype of conventional H6-CSI with the same hardware has also been carried out to test and compare the harmonic performance. The experimental phase voltage, phase current and the current harmonic spectrum of conventional SHEPWM-H6-CSI with low-speed switches are shown in Figure 14A. The filtered voltage and current waveforms are basically complete sinusoidal waves. The burrs are due to the characteristics of low-speed switching operation. From the spectrum analysis, it can be clearly seen that the output current contains many harmonic components, and the harmonics of 5^{th}, 7^{th}, 11^{th}, 13^{th} still remains a certain content.

By contrast, Figure 14B shows the experimental output waveforms of the proposed H7-CSI with SHEPWM. The inverter also outputs 50 Hz sinusoidal voltage and current. Although the waveforms are not significantly different from that of H6-CSI, spectral analysis shows that

the proposed SHEPWM strategy has less harmonic contents. The THD value of output current has decreased from 4.72% to 3.83%. And the low order harmonics (5^{th}, 7^{th}, 11^{th}, 13^{th}) have almost been eliminated successfully. Thus, the harmonic performance of CSI can be improved with the proposed method.

5 Conclusion

This paper reviews the SHEPWM technique of conventional H6-CSI and investigates the practical effect of low switching speed on the harmonic elimination. In order to enhance the performance of SHEPWM, an operation strategy based on H7-CSI with hybrid switches has been proposed. It utilizes one high-speed switch and six conventional low-speed switches, so that offers an easy and cost-efficient solution to improve the commutation speed of CSI, which can own better harmonic performance with even lower power loss. MATLAB with PLECS Blockset simulations and experimental prototype verify the effectiveness of the proposed method.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

WW and XX substantially contributed to the conception of the study, XM helped perform the analysis with constructive discussions, SR and YZ conducted supervision. All authors have read and agreed to the published version of the manuscript.

Conflict of interest

Author SR was employed by State Grid Shandong Electric Power Company.

The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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A soft start-up method for DC micro-grid based on improved two-level VSC with DC fault ride-through capability

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For the black start-up of DC micro-grids, three-phase charging resistors are required to limit the uncontrollable surge current. The main drawback of this start-up method is the difficulty in determining the appropriate resistance value to achieve a rapid start-up and limit the surge current with the change of grid parameters. To address this problem, this article proposes a soft start-up method for the DC micro-grid based on an improved two-level voltage source converter (VSC). Specifically, an silicon controlled rectifier and anti-parallel diode are added in each up-bridge-arm in the improved VSC. By conducting a dynamic control strategy of the firing angle on the SCRs, the start-up current can always be maintained near a given value to achieve rapid start-up. Moreover, the improved VSC has DC fault ride-through capability. The simulation results based on PSCAD/EMTDC are provided to validate the feasibility of the proposed start-up method.

KEYWORDS

DC micro-gird, AC-DC converter, start-up, topology, control method

1 Introduction

During the past decades, due to the increasing demand for low-carbon power grids and progressive penetration of renewable energy sources, micro-grids with flexibility and high controllability are considered to be one of the most promising solutions to integrate and consume renewable energy sources (Hatziargyriou, 2008; Kakigano et al., 2010). Considering that most of the loads and distributed sources, such as photovoltaic arrays and energy-storage systems, are with DC output (Dragicevic et al., 2014), the DC micro-grid is believed to have advantages over the AC micro-grid (Singh et al., 2021) because of the reduced conversion step (Zhu et al., 2018), higher reliability (SumanthAkash and Modi, 2020), and ease of control (Sreedhar Kumar and Chandra Sekhar, 2015).

A schematic of a DC micro-grid is shown in Figure 1A, where a two-level VSC is the key interface between the AC sources and DC grid due to the simplicity of the control system, small footprint, and less investment (Georgios and Massimo, 2016; Changizian et al., 2022a). For the conventional two-level VSC shown in Figure 1B, its small equivalent resistance can lead to rapidly rising charging currents during the start-up process, which can damage the vulnerable power electronic components inside the converter, therefore a proper start-up strategy for the DC micro-grid is required (Chengyong and Ying, 2006; Li et al., 2007; Liu

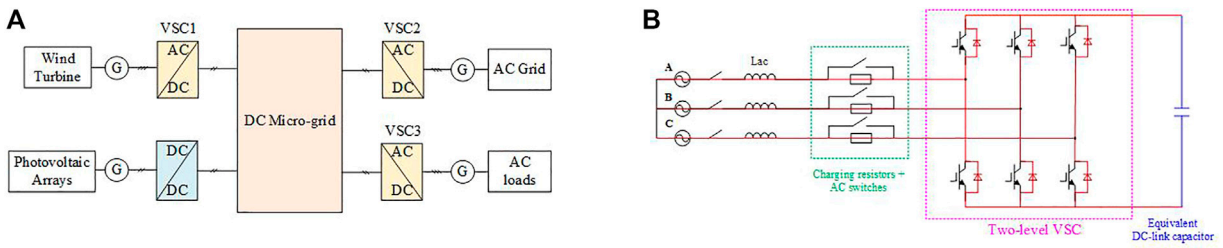

FIGURE 1
Typical schematic of DC micro-grid and the topology of conventional two-level VSC during start-up process. **(A)** Typical schematic of DC micro-grid; **(B)** topology of conventional two-level VSC.

et al., 2019). It has been reported that there were accidents those happened in the Murrylink project and Cross-Sound Cable project because of the lack of a proper start-up operation, which caused power electronic components to burn down and malfunctioning of protection (Mattsson et al., 2004; Railing et al., 2004).

At present, in practical DC micro-grid demonstration projects, only one two-level VSC is being used for start-up. With all the other converters blocked, looking from the DC side, these converters can be equivalent to a capacitor (Díaz et al., 2015; Changizian et al., 2022b). As a result, the start-up of the DC micro-grid could be considered as an equivalent capacitor at the DC side charged by the AC sources through a two-level VSC. Depending on the control strategy of the two-level VSC, this start-up process of the DC micro-grid could be divided into two stages (Lin et al., 2018).

1.1 Uncontrolled rectifier stage

In this stage, the common practice is to block all the Insulated Gate Bipolar Transistors and install three-phase charging resistors at the AC side to limit the starting current (Li et al., 2010; Changizian et al., 2022b). The DC-link capacitors are charged to the maximum line-to-line voltage at the AC side through the charging resistors and AC-side inductor. During this period, the starting current is closely related to the circuit parameters, that is, the charging resistance should match the AC-side sources and DC-link capacitance. If it is too small, an overcurrent will be generated inside the converter, causing potential damage to the power electronic components inside the converter or the false trip of the relay protection on the AC side. If it is too big, the duration of the start-up process would be quite long, that is the power supply reliability would deteriorate, especially the system recovery process would be prolonged significantly. In addition, since numerous converters are connected into one DC micro-grid, the number of converters and the equivalent DC-link capacitance are variable, therefore it is impossible to ensure a perfect match between the charging resistance and equivalent capacitance. Furthermore, as for the two three-phase AC switches shown in Figure 1B used for start-up, its closing and open time is in the order of tens or even hundreds of milliseconds, resulting in additional cost and extra start-up time. According to the real project, the start-up time for a micro-grid could be several seconds.

1.2 IGBT control stage

In this stage, the DC voltage slope controllers (Jing et al., 2009a; Song et al., 2010; Tan, 2013; Wang et al., 2016) are used to control IGBTs such that the DC-side voltage increases gradually according to the reference value with controllable charging current, and thus no overcurrent or overvoltage exists during this period.

To limit the starting current of the uncontrolled rectifier stage, different methods have been proposed. In Ned Mohan and William. (2003); Jing et al. (2009b); Hairong et al. (2009), the most appropriate position to install the charging resistors has been investigated, taking into account the location of the DC outlet of the three-phase bridge, AC side of the converter, and AC side of the power grid. In Ke et al. (2011), a universal parameter design method for the charging resistors on the AC side of the converter has been proposed based on Laplace transform. However, it is also hard to adjust the resistance dynamically according to the variable equivalent capacitance for these charging resistors based start-up methods. A DC voltage regulator was used by Changizian et al. (2022b), where the charging speed and starting current could be controlled at any level needed, but it was not practical in an actual project due to the high cost. An alternative method for the conventional start-up is to use SCRs to replace charging resistors. By slowly reducing the firing angle of the SCRs, the starting current could be limited (Dalian dagong andao ship technology Co. and LTD, 2011). However, the rate at which the firing angle decreases has to be reset when the equivalent DC-link capacitance changes. According to the thorough literature review, the existing start-up methods for the first stage are not suitable for the starting converter of a DC micro-grid because of the variable equivalent DC-link capacitance.

To address this problem, an improved two-level VSC with the advantages of DC fault ride-through and soft start-up is proposed in this article. The topology and control sequence of the improved two-level VSC is briefly introduced in Section 2. The theoretical analysis of the starting current is discussed in Section 3. Simulation is carried out for verification in Section 4. In the end, Section 5 concludes this article.

2 Brief on improved two-level VSC

The topology of the improved two-level VSC is illustrated in Figure 2A. Compared with a conventional two-level VSC, a SCR (T_1~T_3) and an antiparallel diode (DT_1~DT_3) are added in the up-bridge-arm of each phase. Referring to Figure 2A, IGBTs and the

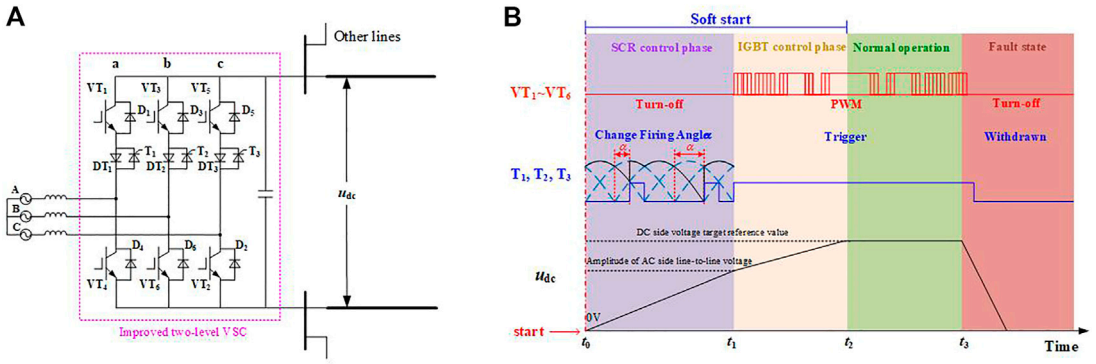

FIGURE 2
Topology and control sequence of the improved VSC. **(A)** Topology of the improved VSC; **(B)** control sequence for the improved VSC.

corresponding freewheel diodes are indicated by VT_1~VT_6 and D_1~D_6, respectively. The corresponding control sequence is shown in Figure 2B.

2.1 Soft start-up process

Suppose the start-up process begins at t_0. During the start-up process, variable firing angle control is employed in the starting converter, and all the other converters are blocked. Before the DC-side voltage (u_{dc}) reaches the amplitude of the AC-side line-to-line voltage (t_1), with VT_1~VT_6 of the starting converter blocked, u_{dc} and the current in the bridge-arm of each phase could be controlled by adjusting the firing angle (α) of T_1~T_3 in the range of 0°–180° dynamically. During this period, the ultimate safety current of the diodes and SCRs is taken as the reference value to adjust α of T_1~T_3 in each control period. In this way, u_{dc} can rise to the amplitude of the AC-side line-to-line voltage at t_1 with the maximum allowable current, meaning the start-up time is the shortest. It should be noted that when equivalent capacitance changes, this control method will still be valid, and the starting current could be the invariant by adjusting α of T_1~T_3 properly. In this case, the start-up time becomes variable with the equivalent capacitance.

The following is the IGBT control stage (t_1~t_2 in Figure 2). Triggering signals are continuously applied on T_1~T_3, that is, T_1~T_3 are equivalent to the diodes and the improved two-level VSC is equivalent to the conventional two-level VSC. The control signals that are generated by the pulse width modulation (PWM) are sent to VT_1~VT_6 to control u_{dc} to follow the preset DC-side voltage reference. It should be noted that the slope reference value is employed to prevent excessive starting current in each bridge. When u_{dc} is finally stabilized to be the rated DC voltage, the soft start-up process of the improved two-level VSC is completed. After this, all the other converters in the DC micro-grid are unlocked and begin to operate normally.

2.2 Normal operation

During the normal operation (t_2~t_3 in Figure 2), with T_1~T_3 continuously triggered and equivalent to the diodes, the improved two-level VSC is equivalent to the conventional two-level VSC. The constant voltage control mode or constant power control mode is adopted by the corresponding converters connected in the micro-grid.

As for the two-level VSC, with the maximum AC-side line-to-line voltage alternates, the corresponding IGBT and diodes constitute a boost chopper to realize conversion from AC to DC. As a result, u_{dc} is higher than the AC-side voltage at any time during the normal operation.

2.3 DC fault ride-through

For the DC micro-grid based on the conventional two-level VSC, when a DC fault occurs, the DC-link capacitors discharge rapidly, resulting in the DC voltage collapsing and surge current with high amplitude, a long decay time constant, and no zero-crossing point (Wang et al., 2021). Triggered by the overcurrent, IGBTs are blocked rapidly, leaving the freewheel diodes exposed to the long-lasting overcurrent, which can lead to the damage of the diodes (Islam et al., 2020). Therefore, the conventional two-level VSC lacks DC fault ride-through ability, which has been regarded as a technical bottleneck that limits the wide industry application of the DC micro-grid.

As for the improved VSC, when a DC fault is detected at t_3 in Figure 2B, triggered by an overcurrent, turn-off signals are sent to IGBTs, and the triggering signals for SCRs are withdrawn after a short time delay. By adding a small inductor at the DC outlet, u_{dc} would drop slowly at the early stage of DC fault. Under the effect of $u_{dc,}$ which is larger than the AC-side voltage, the currents in T_1~T_3 would drop to zero in a short time. As a result, T_1~T_3 can be turned off, and the electrical path from the AC source to fault point can be blocked. In this way, almost no surge current flows through the power electronic components inside the converter, that is, the improved converter has the ability for DC fault ride-through.

3 Theoretical analysis of soft start-up for DC micro-grid

As mentioned before, to achieve soft start-up of the improved two-level VSC, on the one hand, the start-up current is expected to

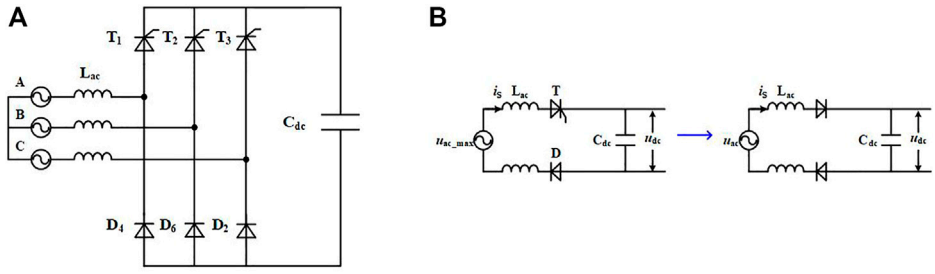

FIGURE 3
Equivalent circuit of the improved VSC in SCR control phase. **(A)** Equivalent circuit and **(B)** simplified equivalent circuit.

TABLE 1 Power electronic devices in on-state at different maximum line-to-line voltages during SCR control phase.

Maximum line-to-line voltage	SCR in high-side half-bridge	Diode in low-side half-bridge
u_{AB}	T_1	D_6
u_{AC}	T_1	D_2
u_{BC}	T_2	D_2
u_{BA}	T_2	D_4
u_{CA}	T_3	D_4
u_{CB}	T_3	D_6

be always within an allowable value of power electronic components, while on the other hand, the DC voltage is expected to rise as rapidly as possible to realize rapid start-up. In fact, there is a contradiction between the starting current value and rise rate of the DC-side voltage. Therefore, the ultimate objective of the soft start-up is to maintain the starting current in each bridge-arm close to the allowable value by adjusting α of T_1~T_3 dynamically, making the starting current independent of the equivalent capacitance, such that the DC voltage could rise as rapidly as possible.

To provide the theoretical basis for the soft-start control strategy, the theoretical analysis about the maximum, generation mechanism of the starting current, and influencing factors are conducted in this part.

3.1 Equivalent circuit of soft-start process

Since DC voltage of the DC micro-grid is established by one starting converter, looking from the DC side, all the other converters are equivalent to capacitors. Therefore, the equivalent circuit in the SCR control stage is shown in Figure 3A, where L_{ac} is the inductor on the AC side and C_{dc} is the equivalent DC-link capacitor. For a DC micro-grid, due to the small value of the AC-side inductor, at any given time, only an up-bridge-arm connected to the highest voltage and a down-bridge-arm connected to the lowest voltage on the AC side are in the conducting state, that is, the maximum AC-side line-to-line voltage source charges the equivalent capacitor of the DC side. Based on Figure 3A, the on-state power electronic components at different maximum line-to-line voltage are listed in Table 1. As a result, the equivalent circuit can be simplified as shown in Figure 3B, where u_{ac_max} is the maximum AC-side line-to-line voltage, T and D indicate the corresponding SCR and diode in Table 1, respectively, and u_{ac} is the equivalent AC-side voltage under the effect of the firing angle of SCR.

By changing the firing angle (α) of T_1~T_3, the waveform of u_{ac} will be changed. When $\alpha = 0^{\circ}$, as shown in Figure 4, each SCR is commutated at the natural commutation point and the waveform of u_{ac} is the envelope curve of the maximum line-to-line voltage. With the increase of α, the average value of u_{ac} gradually deceases and finally drops to 0 when $\alpha = 180^{\circ}$. Furthermore, it is also seen that the triggering signal for SCR in phases A, B, and C should differ by 120°. In this way, by adjusting α, the waveform of u_{ac} can be changed and then affect the starting current in half-bridges and rising rate of u_{dc}. When u_{dc} reaches the amplitude of the AC-side line-to-line voltage, no matter how α changes, u_{dc} would no longer increase, therefore u_{dc} at the end of the SCR control phase would be the maximum AC-side line-to-line voltage.

During the IGBT control phase, the improved two-level VSC is equivalent to conventional VSC, and the control methods are the same. Therefore, to avoid repetition, details about this period is not discussed in this article.

3.2 Relationship between maximum starting current and firing angle (α)

3.2.1 Quantitative calculation method

According to the analysis in Section 3.1, the triggering signal for each SCR differs by 120°, therefore when the rated frequency at the

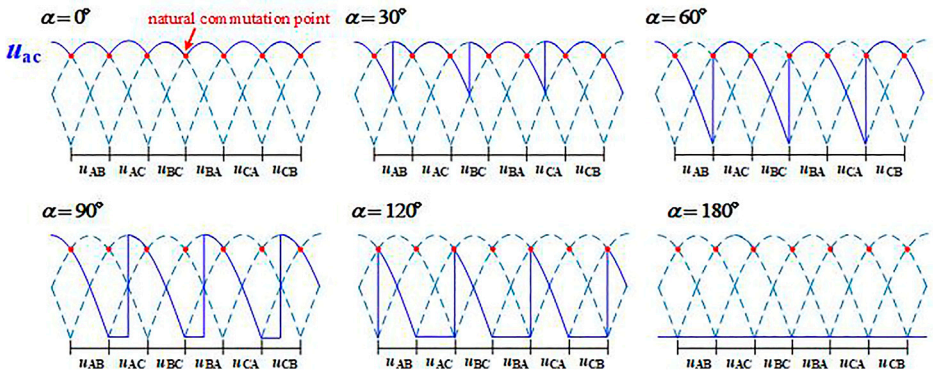

FIGURE 4
Typical waveform of u_{ac} at different firing angles of the SCRs in the improved VSC.

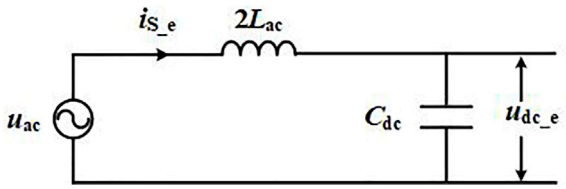

FIGURE 5
Equivalent circuit for the calculation of i_S and u_{dc} in each basic control period.

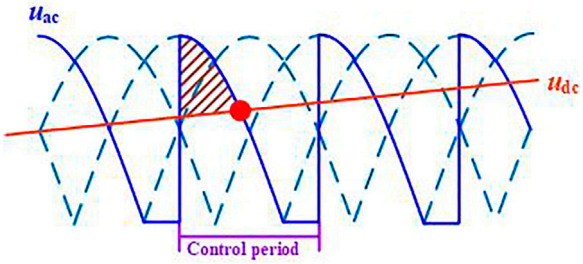

FIGURE 6
Typical waveforms of u_{ac} and u_{dc} when α = 90°.

AC side equals 50 Hz, the basic control period of the firing angle α becomes 6.67 ms.

Referring to the simplified equivalent circuit in Figure 3B, the maximum current in each bridge-arm i_S and DC-side voltage u_{dc} in each basic control period can be calculated based on the equivalent circuit shown in Figure 5, where L_{ac} is the equivalent inductance of each phase at the AC side, and C_{dc} is the equivalent capacitance at the DC side. Due to the existence of diode seen in Figure 3B, there is no discharge loop for C_{dc}, therefore u_{dc} at the end of each basic control period is the maximum of u_{dc_e} as shown in Figure 5, and the maximum of i_S is the maximum of i_{S_e} also seen in Figure 5.

Referring to Figure 5, the differential equation with u_{dc_e} and i_{S_e} as the variables is

$$\begin{cases} C_{dc}\dfrac{du_{dc\_e}}{dt} = i_{S\_e} \\ 2L_{ac}\dfrac{i_{S\_e}}{dt} + u_{dc\_e} = u_{ac} \end{cases}.$$

The corresponding state equation can be derived as follows:

$$\begin{bmatrix} \dfrac{du_{dc\_e}}{dt} \\ \dfrac{di_{S\_e}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{1}{C_{dc}} \\ \dfrac{-1}{2L_{ac}} & 0 \end{bmatrix} \begin{bmatrix} u_{dc\_e} \\ i_{S\_e} \end{bmatrix} + \begin{bmatrix} 0 \\ \dfrac{1}{2L_{ac}} \end{bmatrix} [u_{ac}].$$

During a certain basic control period, the initial value of i_{S_e} is 0. As a result, at a certain α and an initial value of u_{dc_e}, the numerical solutions of u_{dc_e} and i_{S_e} during each control period is obtained by solving the above stated equation with the Runge–Kutta method.

3.2.2 Qualitative analysis

The numerical solution cannot clearly indicate the relationship between the control variable (α) and controlled variable (i_S), therefore a qualitative analysis is conducted in this part. According to Figure 3B, in a control period, based on the Kirchhoff's Voltage Law, the following equation is satisfied:

$$u_{ac} - u_{dc} = 2L_{ac}\frac{di_S}{dt}.$$

Bu integrating both the sides of this equation over time,

$$\frac{\int (u_{ac} - u_{dc})dt}{2L_{ac}} = i_S.$$

Taking $\alpha = 90^\circ$ as an example, the waveforms of u_{ac} and u_{dc} are shown in Figure 6. In the control period shown in Figure 6, i_S reaches its maximum at the red dot, and its peak value is determined by the area of the shaded part enclosed by u_{dc} and u_{ac}. As a result, when i_S exceeds the reference value, by increasing α in the next control phase, the area enclosed by u_{dc} and u_{ac} would be reduced, and thus the maximum of i_S in the next control would be reduced. Similarly, when i_S is lower than the reference value, by decreasing α in the next

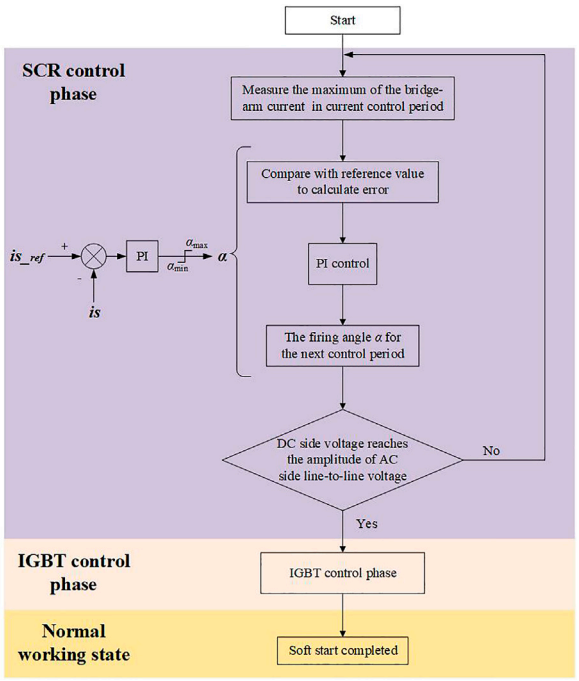

FIGURE 7
Flow chart of the dynamic control strategy of firing angle.

control phase, the maximum of i_S in the next control would be increased. In this way, the maximum of i_S in each control period could be maintained around the reference value to charge the equivalent DC-link capacitor rapidly.

3.3 Dynamic control strategy of firing angle

Based on the above analysis, a dynamic control strategy of the firing angle (α) is proposed with the goal of maintaining the maximum for the current in the bridge-arm close to the reference value, such that u_{dc} could rise up to the maximum AC-side line-to-line voltage as soon as possible without causing any overcurrent.

The flow chart of the control strategy is shown in Figure 7. In every control period, the maximum of the bridge-arm current is measured and compared with the reference value to calculate the control error, which is then used as the input for the PI controller to calculate the reference value of α for the next control period. When u_{dc} reaches the amplitude of the AC-side line-to-line voltage, the SCR control phase is completed.

4 Case study

To verify the proposed soft-start control method, a simplified typical DC micro-grid model, as shown in Figure 8, is established in PSCAD/EMTDC, the parameters of which are listed in Table 2 (Salomonsson et al., 2009). In the simulation model, VSC1 is set as the starting converter. According to the analysis before, in the start-up process of the two-level VSC, the current in each bridge-arm and the duration of the start-up process should be limited. Therefore, the maximum of the current i_{ac} and the duration of the start-up are used to evaluate the effectiveness of the proposed soft start-up method in this part.

4.1 Simulation results

In simulation, the soft start-up process begins at 0 s, taking the rated current of the AC side as the reference value for the maximum current in each bridge-arm in the SCR control phase, which is 800 A. Once the DC-side voltage u_{dc} reaches the amplitude of the AC-side line-to-line voltage (~465 V), triggering signals are continuously applied to the SCRs. By controlling IGBTs with PWM, u_{dc} rises up gradually to the rated DC voltage (500 V) in 0.1 s.

The simulation results of u_{dc} and i_{ac} are shown in Figure 9. As shown in Figure 9, at the early stage of the SCR control phase ($t <$ 0.25 s), due to the small value of u_{dc}, by controlling the firing angle α for SCRs, the maximum bridge-arm current in each basic control period can be maintained at approximately 800 A. After 0.25 s, as u_{dc} rises, the current in each bridge-arm gradually decreases and eventually drops to 0 with u_{dc} reaching the maximum AC-side line-to-line voltage at 0.42 s. After this, the soft-start process enters the IGBT control stage, and u_{dc} follows the slope reference value to the rated DC voltage at 0.52 s. As a result, during the whole start-up process, there is no overcurrent (>800 A) in each bridge-arm, and u_{dc} can reach the rated DC voltage within 0.52 s. The simulation results are consistent with the theoretical analysis in Section 3.

4.2 Discussion and comparison

To present the advantages of the proposed soft start-up method, comparisons between the proposed soft start-up method and conventional start-up method that have been mentioned in Section 1 are conducted in this part. As for the conventional method, the starting resistance is set as 0.2 Ω in the typical DC micro-grid, and the operation time of the AC switch is set to be 0.1 s.

4.2.1 Flexible starting current control

The simulation results of u_{dc} and i_{ac} using the conventional start-up method is shown in Figure 10. As shown in Figure 10, the start-up process begins at time 0. At first, it takes 0.1 s to switch the starting resistors to the AC side. Then, the equivalent DC-link capacitor is charged by a three-phase AC source through the uncontrolled rectifier circuit. Due to the small value of the charging resistor, i_{ac} with the peak value of 1,250 A exceeds the rated AC phase current significantly. When u_{dc} reaches the amplitude of the AC-side line-to-line voltage at 0.33 s, it takes another 0.1 s for AC circuit breaker to close so that the charging resistors are bypassed. In this case, the whole duration of the start-up process using the conventional starting method is 0.53 s. Compared with the proposed soft start-up method, the starting time is the same, but the starting current using the conventional starting method is uncontrollable and exceeds the limit significantly. Increasing the value of the starting resistor is a method to solve this problem, but the duration of the start-up process will be prolonged.

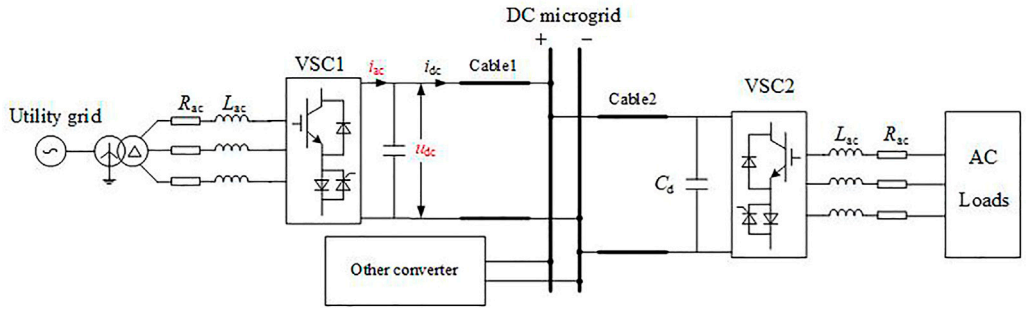

FIGURE 8
Simplified typical DC micro-grid model.

TABLE 2 Parameters of simplified typical DC micro-grid.

Parameter	Symbol	Value
Rated DC voltage	$U_{rated,dc}$	500 V
Rated AC phase-to-ground voltage	$U_{rated,ac}$	190 V
Rated AC phase current	$I_{rated,ac}$	800 A
Resistance of AC side of VSC	R_{ac}	1.36 mΩ
Reactance of AC side of VSC	L_{ac}	43.2 μH
DC-link capacitance of VSC	C_d	28 mF
Length of DC cable	S	100 m
Reactance of DC cable	L_d	0.34 μH/m
Resistance of DC cable	R_d	0.64 mΩ/m

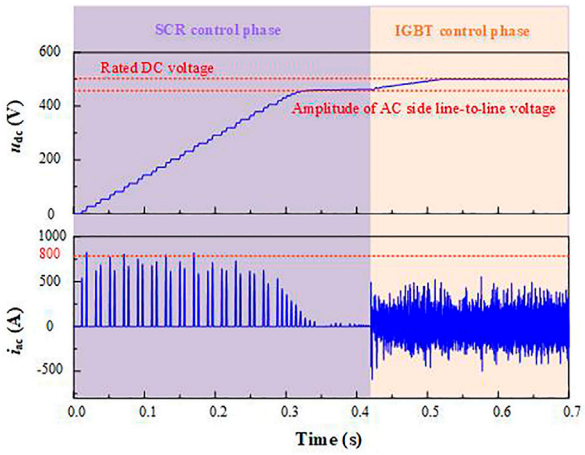

FIGURE 9
Simulation results of u_{dc} and i_{ac} using the proposed soft start-up method.

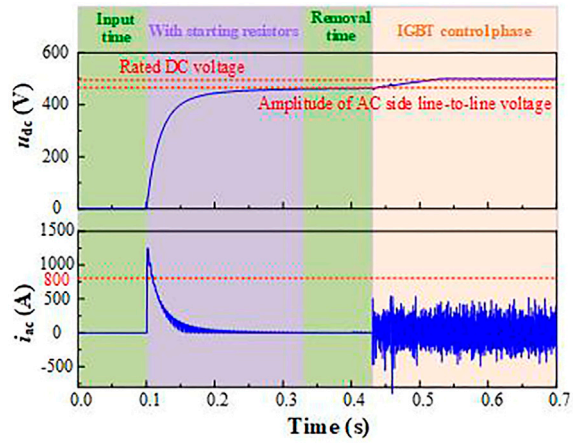

FIGURE 10
Simulation results of u_{dc} and i_{ac} using conventional start-up method.

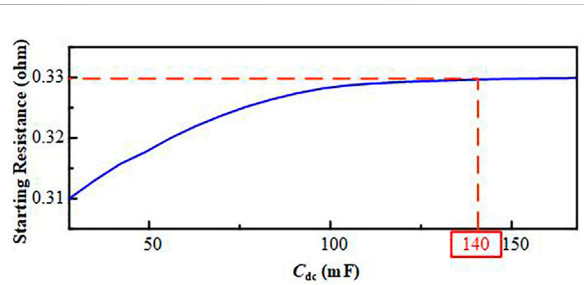

FIGURE 11
Relationship between C_{dc} and charging resistance.

More importantly, as the number of equivalent DC-link capacitors of converters (C_{dc} in Figure 4) in the DC micro-grid is variable, the charging resistance should be adjusted dynamically according to C_{dc}. Since i_{dc} and u_{dc} in the start-up process using the conventional start-up method are only dependent on the circuit parameters before the IGBT control phase, the maximum of i_{dc} will increase with the increase of C_{dc}, thus the starting resistor with a bigger value is required. By calculating numerally, the relationship between C_{dc} and the charging resistance has to limit the maximum of i_{ac} within the rated AC phase current, as illustrated in Figure 11.

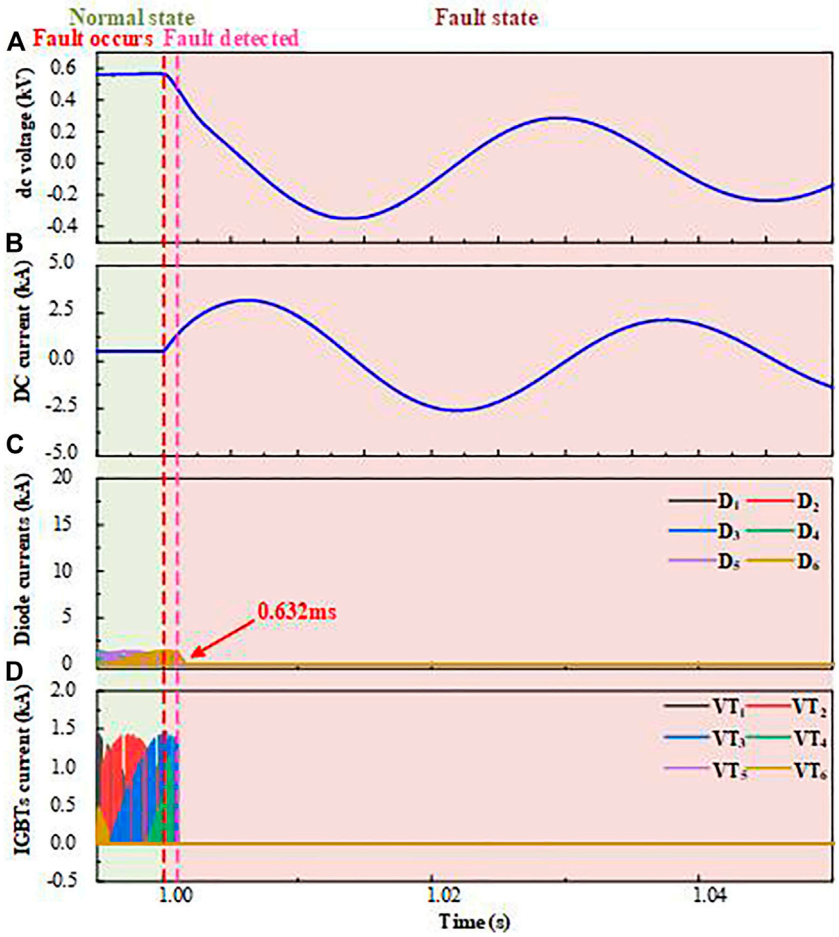

FIGURE 12
Simulation results of the improved VSC during DC fault ride-through. **(A)** DC-side voltage; **(B)** DC-side current; **(C)** currents in D_1~D_6 and T_1~T_3; and **(D)** currents in VT_1~VT_6.

As shown in Figure 11, when C_{dc} is 140 mF in the DC micro-grid during the start-up process, a starting resistance of more than 0.33 Ω is required to avoid overcurrent inside the starting converter, while the increased starting resistance would extend the duration of the start-up process to 0.88 s when C_{dc} is 56 mF.

Based on the above analysis, as for the conventional start-up method, there is a contradiction between the start-up speed and starting current. Therefore, it is almost impossible to adjust the charging resistor dynamically according to the variable C_{dc} without causing any overcurrent.

However, as for the proposed soft start-up method, u_{dc} can always increase at the fastest possible speed, regardless of the equivalent capacitance of the DC micro-grid.

4.2.2 DC fault ride-through capability

As mentioned previously, besides the ability of the soft start-up, the improved two-level VSC is also capable of DC fault ride-through.

In the simulation model shown in Figure 12, taking VSC1 as an example, an inductor with a value of 20 μH is installed at the DC outlet. A DC pole-to-pole fault occurs at t = 1s, and after a fault detection time of 1 ms, the fault is detected. At this point, turn-off signals are sent to VT_1~VT_6, and triggering signals for T_1~T_3 are withdrawn after 400 μs. The simulation results are shown in Figure 12. As shown in Figure 12A, after the DC fault occurs, with the effect of the inductor installed at the DC outlet when the fault is detected, the DC-side voltage is still bigger than the amplitude of the AC-side line-to-line voltage. As a result, fault currents inside the converter are eliminated in 0.623 ms, and there is no overcurrent inside the improved two-level VSC.

As for the conventional two-level VSC, because of the lack of DC fault ride-through capability, there will be a long-lasting overcurrent in the freewheel diodes when DC fault occurs. The simulation results of the conventional two-level VSC during the same DC fault are shown in Figure 13. When the fault is detected, turn-off signals are sent to IGBTs immediately, leaving the freewheel diodes subjected to an overcurrent, which is up to eight times the current during a normal operation and can lead to permanent damage.

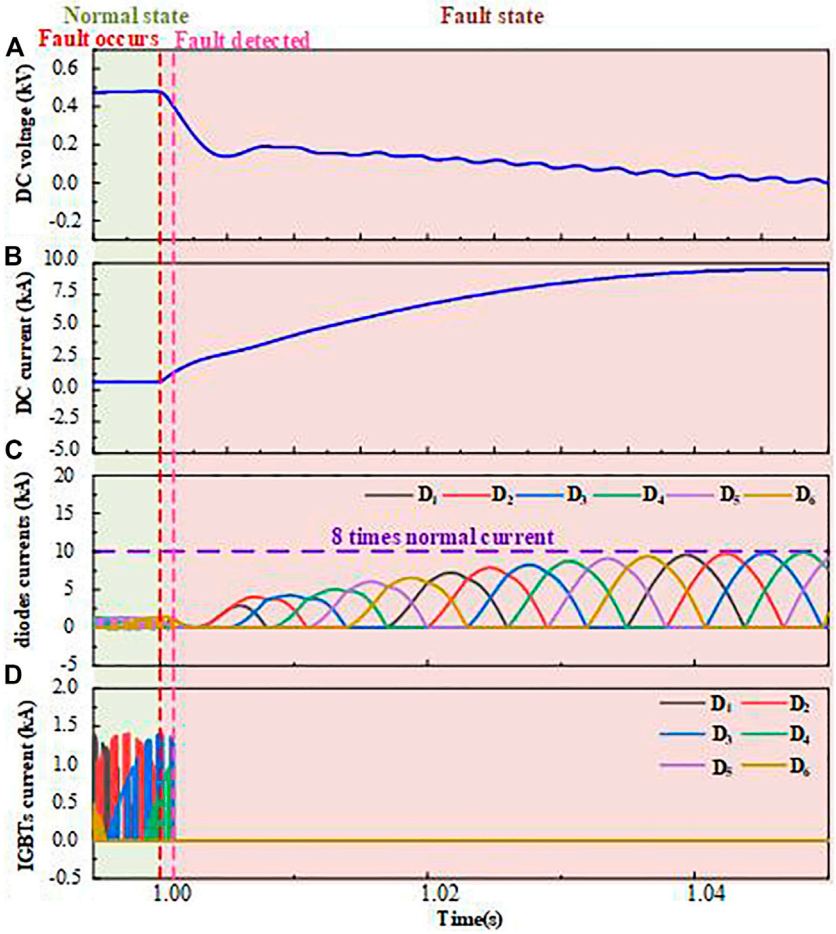

FIGURE 13
Simulation results of the conventional VSC during DC fault ride-through. **(A)** DC-side voltage; **(B)** DC-side current; **(C)** currents in D_1~D_6 and T_1~T_3; and **(D)** currents in VT_1~VT_6.

According to the above analysis, when compared with the conventional two-level VSC and start-up method, the improved VSC can achieve flexible starting current control without depending on the DC micro-grid parameters with the proposed soft start-up method and have DC fault ride-through capability.

5 Conclusion

Due to the vulnerability of the power electronic components inside the DC micro-grid, the surge current caused by charging the DC-link capacitors during the start-up process should be limited. The conventional start-up method for the DC micro-grid is based on the three-phase charging resistors on the AC side which lack controllability, thus it is hard to balance the start-up speed and the value of the starting current. Aiming at this problem, an improved two-level VSC with a module of an SCR and anti-parallel diode in each up-bridge-arm is proposed in this article. By controlling the firing angles of the SCRs with a dynamic control strategy, not only can the starting current be limited to a given value but also can the fast start-up of the DC micro-grid be realized. Moreover, by rapidly turning off all the SCRs after DC faults, the fault currents in the improved VSC can be eliminated, which means it has DC fault ride-through capability. The topology and control sequence of the improved two-level VSC are introduced. The relationship between the transient starting current and firing angles of the SCRs inside the improved VSC is analyzed both quantitatively and qualitatively based on the equivalent circuit during the start-up process. According to the theoretical analysis, a dynamic control strategy of the firing angle is proposed with the goal of maintaining the maximum current in the bridge-arm close to its limits so as to achieve rapid start-up without causing any overcurrent. In the end, a simplified typical DC micro-grid model is established in PSCAD/EMTDC for verification. The results show that for the conventional start-up method based on the charging resistors, the start-up time is long, and the starting current may exceed a given value with the change of grid parameters. For the proposed start-up method in this article, the start-up current can always be controlled to a given value to

achieve rapid start-up without depending on the grid parameters. The proposed start-up method can shorten the start-up time and make the starting current controllable to significantly reduce the risk of damage to power electronic components, thus having the guiding significance for future constructions of the DC micro-grid.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material; further inquiries can be directed to the corresponding authors.

Author contributions

Conceptualization: WW, RL, and BTL; methodology: WW, RL, and HC; software: RL and JY; validation: WW; writing—original draft preparation: WW and RL; writing—review and editing: RL and BL; supervision: BL and MP; project administration: BL and MP. All authors have read and agreed to the published version of the manuscript.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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A sigmoid-based adaptive inertia control strategy for grid-forming inverter to enhance frequency stability

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Introduction: This paper proposes a sigmoid-based adaptive inertia control strategy for grid-forming (GFM) inverter to enhance frequency stability.

Methods: Firstly, the frequency response characteristics under different disturbances are analyzed theoretically. Then, to solve the problem that fixed inertia leads to a contradiction between the maximum frequency deviation and the setting time, a non-linear inertia regulator is investigated. This non-linear inertia regulator, which is based on an improved sigmoid function, is applied to achieve real-time inertia by the frequency deviation. Moreover, the full-order small-signal model of the system containing the nonlinear inertia regulator is established and thus the stability of the proposed strategy is analyzed.

Result and Discussion: The proposed control strategy is implemented without derivative action, which may suffer from high-frequency noises. Finally, the hardware-inthe-loop (HIL) results verify the remarkable performance of the proposed control strategy.

KEYWORDS

grid-forming (GFM) inverter, adaptive inertia control, small-signal model, frequency stability, sigmoid function

1 Introduction

As the integration of renewable energy sources increases, distributed generation systems with inverters as the interface are becoming increasingly important in the conventional grid (Pan et al., 2013; Xie et al., 2021). The massive use of power electronics and the withdrawal of synchronous machines have led to a lack of inertia in the power system, thus making the frequency stability of the system increasingly problematic (Blaabjerg et al.,2006; Li et al.,2018). To address this problem, a concept of GFM inverter generating distributed virtual inertia was proposed (Lasseter et al.,2019; Quan et al.,2019; Liu et al.,2016; Zhong and Weiss, 2010). The GFM inverter using virtual inertia control can effectively increase the inertia of the power system, reduce the frequency deviation and decrease the rate of change of the grid frequency under large disturbances (Fang et al., 2017). Hence, this paper focuses on the virtual inertia of the GFM inverter.

Virtual inertia control simulates the behavior of a real synchronous generator, but because control parameters such as inertia are virtual, this makes the design of its control parameters both flexible and complex. In order to meet the operational requirements of the

system, the parameter design of the virtual inertia control was investigated (Dhingra and Singh., 2018). For example, a step-by-step parameters design method based on the line-frequency-averaged small-signal model of GFM inverter is proposed in (Wu et al.,2016). On the basis of the parallel small-signal model, the effect rules of the eigenvalues by droop coefficient, line parameters, GFM inverter's parameters, and low pass filter parameters are examined and derived in (Zhang et al., 2017). The parameters of the proposed GFM inverter were optimized in (Shintai et al., 2014). However, these criteria strongly influence each other and it is difficult to balance multiple performance indicators. Therefore, attempts were made to improve the traditional virtual inertia control method in order to better control system. A modified virtual inertial strategy is used for the configuration of GFM inverter in (Shi et al., 2018; Xu et al., 2019), which helps the system to be closer to the theoretical analysis conditions of the traditional virtual inertial algorithm.

However, the GFM inverter also faces stability problems under grid disturbances while benefiting from the operation of simulated synchronous generators. In the event of large signal disturbances, such as transmission line faults, critical grid voltage droop and large load swings, the GFM inverter is exposed to stability risks. The transient behaviors of GFM inverter with power-synchronization control were examined in (Wu and Wang., 2018) under various grid fault scenarios. In (Xin et al., 2016; Huang et al., 2017), a fundamental droop-controlled GFM inverter transient instability phenomenon was discovered in the situation of a current saturation caused by the grid voltage sag. The power-angle curve was used to provide a qualitative examination of reactive power management in (Shuai et al.,2018), which shows how it degrades the GFM inverter's transient stability. Although obvious, it does not precisely identify how and to what extent the transitory behavior is impacted by the reactive power control and other control elements. Due to the enormous complexity inherent in large-signal non-linear dynamic reactions, this is in fact a basic difficulty in the study of transient stability.

In addition to large disturbances, small disturbances are also an important research element in virtual inertia control (Li et al., 2004; Zhang et al., 2009; Zhang et al., 2010). However, existing studies show that fixed control parameters always lead to a contradiction between the overshoot and the setting time of the system (Chong et al., 2015). To solve this problem, it is necessary to adapt the values of the control parameters to the different scenarios and disturbances in real-time. An adaptive control method based on reinforcement learning and adaptive dynamic programming (ADP) is proposed in (Wang et al., 2021), but its stability was not verified. The GFM inverter-based adaptive damping control strategy in (Zheng et al., 2016) limits the frequency oscillations to a reliable range and attenuates the output power oscillations. However, the effect of virtual inertia on the system is not considered. In (Markovic et al., 2018), a linear quadratic regulator-based (LQR) optimization technique is used to adaptively adjust the emulated inertia and damping constants. However, only a pure simulation platform was used to verify the feasibility of the strategy and no hardware platform verification was performed. An adaptive control scheme combining virtual inertia control with an additional damping controller was proposed in the literature (Wang et al., 2022). This literature establishes a mathematical model of a wind power grid-forming system with a damping controller. However, only the response effect of the system output power was focused on and the frequency stability aspect was not investigated. All the literature above utilize damping adaption. In contrast, this paper focuses on adaptive adjustment of inertia.

In the control method of adaptive virtual inertia, scholars extensively adopted frequency differentiation as a standard of measurement. An adaptive virtual inertia control strategy based on an improved bang-bang control strategy for a micro-grid is presented in (Li M et al., 2019). On the one hand, it can make full use of the variability of virtual inertia to reduce dynamic frequency deviation. On the other hand, the steady-state interval of frequency and the steady-state inertia are set to improve the system frequency stability. Alternating inertia is also proposed in (Alipoor et al., 2014; Cheng et al., 2015; Li et al., 2016; Wang et al., 2018; Zhang et al., 2020), where the main idea is to give the moment of inertia by evaluating the state of the frequency deviation Δf and its rate of change df/dt. However, df/dt is very sensitive to high-frequency noise, which is inevitable in real physical systems. Therefore, the practical performance of this type of control is influenced by high-frequency noise. A communication-free adaptive virtual inertia control to realize the power oscillation suppression of cascaded-type virtual synchronous generators (VSGs) is proposed in (Li et al., 2023), where the adaptive inertia link contains $d\omega Di/dt$. But the measurement noises caused by direct calculation is avoided by deriving the formula with rounding roots so that $d\omega Di/dt$ is obtained without derivative action. In (Li J et al., 2019), A dual-adaptivity inertia control strategy was proposed, but the system stability was not verified when the adaptive regulator was introduced. Moreover, the theoretical analysis of frequency response under power disturbance is not investigated. A practical control method without derivative action is proposed by (Hou et al.,2020). The control method proposed in this paper also does not have a derivative action. The proposed algorithm conquers this chattering deficit without frequency derivative action. It gives tremendous promise for engineering application backgrounds with high-frequency noise.

In this paper, a sigmoid-based adaptive inertia control strategy for GFM inverter is proposed to enhance frequency stability. The frequency response characteristics under different disturbances are theoretically analyzed at first. Then, a non-linear inertia regulator, which is based on an improved sigmoid function, is investigated to adjust the inertia by frequency deviation. Hence, the proposed strategy can achieve a better overall dynamic performance than the fixed inertia regulator. Besides, the full-order small-signal model of the system containing the non-linear inertia regulator is established in this paper to evaluate the stability of the proposed strategy. Compared with (Alipoor et al., 2014; Li et al., 2016; Wang et al., 2018; Zhang et al., 2020), the proposed adaptive strategy is implemented without derivative action (df/dt) and thus the performance is insensitive to high-frequency noise. Finally, the effectiveness of the proposed strategy is verified by the hardware-in-the-loop (HIL) results.

2 Control structure of GFM inverter

The control scheme of GFM inverter is shown in Figure 1. The main control structure includes an inner voltage and current control loop and an outer power control loop. In the voltage and current

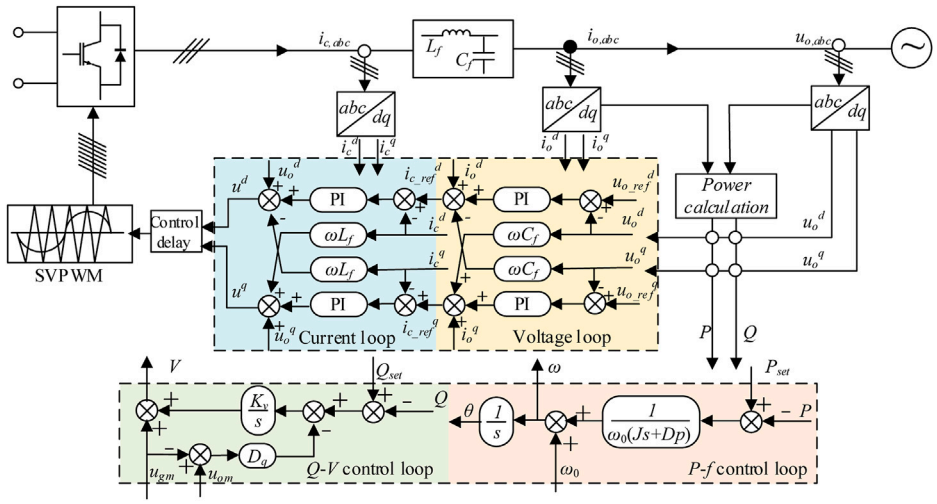

FIGURE 1
Control scheme diagram of GFM inverter.

control loop, PI control is used to track the reference value. Hence, the control formula under the *dq* reference system can be obtained as Eq. 1.

$$\begin{cases} i_{c\_ref}^{d} = \left(K_{vp} + \dfrac{K_{vi}}{s}\right)\left(u_{o\_ref}^{d} - u_{o}^{d}\right) - \omega C_f u_{o}^{q} + i_{o}^{d} \\ i_{c\_ref}^{q} = \left(K_{vp} + \dfrac{K_{vi}}{s}\right)\left(u_{o\_ref}^{q} - u_{o}^{q}\right) + \omega C_f u_{o}^{d} + i_{o}^{q} \\ u^{d} = \left(K_{ip} + \dfrac{K_{ii}}{s}\right)\left(i_{c\_ref}^{d} - i_{c}^{d}\right) - \omega L_f i_{c}^{q} + u_{o}^{d} \\ u^{q} = \left(K_{ip} + \dfrac{K_{ii}}{s}\right)\left(i_{c\_ref}^{q} - i_{c}^{q}\right) + \omega L_f i_{c}^{d} + u_{o}^{q} \end{cases} \tag{1}$$

where u^d and u^q represent the command voltage for modulating the converter, respectively; ${i_{c\_ref}}^d$ and ${i_{c\_ref}}^q$ are the control reference current, respectively; ${u_o}^d$, ${u_o}^q$, ${i_o}^d$ and ${i_o}^q$ are the inverter output voltage and current, respectively; ${i_c}^d$ and ${i_c}^q$ denote the inverter bridge arm current; ω is the angular frequency provided by the outer power control loop; C_f and L_f indicate filter capacitor and inductor, respectively; K_{vp}, K_{vi}, K_{ip} and K_{ii} are the PI control parameters, respectively.

In the *P-f* control loop, the function of GFM inverter to support the frequency stability is realized through virtual inertia, and the control equation is as follows:

$$J\dot{\omega} = (P_{set} - P)/\omega_0 - D_p(\omega - \omega_0) \tag{2}$$

where P and P_{set} represent the active power and its reference, respectively. ω and ω_0 denote GFM inverter's angular frequency and the nominal angular frequency, respectively. J and D_p are the virtual inertia and the damping ratio. Since the objective of this paper is to regulate inertia in *P-f* control loop, the *Q-V* control loop is neglected in this paper.

Digital control has an inherent control delay problem because sampling and calculation take a certain amount of time to complete, making it difficult to control the system in real-time. According to (Vukosavic et al.,2017; Wang et al.,2015), the various delays of the system are included in a delay link, which is placed before the PWM loop.

Assuming that there is a delay of one sampling period in the modulated wave update with respect to the sampling moment, the transfer function of the delay and the zero-order retainer in the continuous domain is:

$$G_d(s) = e^{-\tau s}, G_h(s) = \frac{1 - e^{-\tau s}}{s} G_d(s) \approx \tau e^{-0.5\tau s} \tag{3}$$

where $\tau > 0$ is the system sampling time. $e^{-\tau s}$ is an irrational function, which is not conducive to subsequent analysis. To evaluate the effect of delay on system stability, the second-order Pade approximation is utilized to simplify the analysis process.

$$G(s) = G_d(s)G_h(s) \approx \frac{4.5\tau^3 s^2 - 18\tau^2 s + 24\tau}{4.5\tau^2 s^2 + 18\tau s + 24} \tag{4}$$

Therefore the equation of state for the delayed link is:

$$\begin{cases} \dot{x}_{d1} = -\dfrac{4}{\tau}x_{d1} - \dfrac{16}{3\tau^2}x_{d2} + u_{cd} \\ \dot{x}_{d2} = x_{d1} \\ \dot{x}_{d3} = -\dfrac{4}{\tau}x_{d3} - \dfrac{16}{3\tau^2}x_{d4} + u_{cq} \\ \dot{x}_{d4} = x_{d3} \\ u_{cd,dl} = -8x_{d1} + \tau u_{cd} \\ u_{cq,dl} = -8x_{d3} + \tau u_{cq} \end{cases} \tag{5}$$

where x_{d1}、x_{d2}、x_{d3} and x_{d4} are a set of state variables; $u_{cd,dl}$ and $u_{cq,dl}$ are the voltage control signals obtained from u_{cd} and u_{cq} after a zero-order retainer and a delay time τ, respectively.

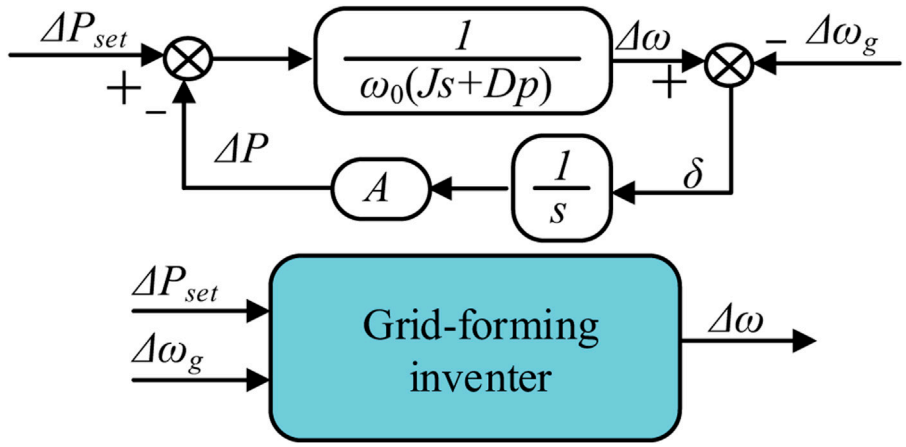

FIGURE 2
Equivalent input and output of the system under small disturbance.

3 Influence of virtual inertia on system frequency output

$$\begin{cases} Js \cdot \Delta\omega = \dfrac{\Delta P_{set}}{\omega_0} - \dfrac{\Delta P}{\omega_0} - D_p \Delta\omega \\ \Delta P \approx \dfrac{3V_n^2}{X}\Delta\delta = A\Delta\delta \\ \Delta\delta = \dfrac{\Delta\omega - \Delta\omega_g}{s} \end{cases} \tag{6}$$

where ΔP and ΔP_{set} are the minor change of P and P_{set}, respectively; $\Delta\omega$ and $\Delta\omega_g$ are the minor change of ω and the grid frequency ω_g, respectively; $\Delta\delta$ is the minor change of the phase difference between inverter voltage and grid voltage.

When the system is subject to a small disturbance, GFM inverter can be regarded as a linearized model near the operating point. At this point, the system can be considered a model with two inputs and a single output, as shown in Figure 2. Based on this, a simplified small-signal model of GFM inverter can be obtained, as shown in Eq. 6.

3.1 Transfer function of the angular frequency

As the power response under various perturbations has been analyzed in detail in (Wang et al.,2021),. the study in this paper focuses on the frequency response, which will be discussed in detail in two perturbation cases.

1. When $\omega_g = 0$, namely, the frequency of common point does not fluctuate and is equal to the nominal angular frequency, the transfer function of angular frequency $f_{\omega - Pset}$ can be derived as:

$$f_{\Delta\omega-\Delta P_{set}}(s) = \frac{\Delta\omega}{\Delta p_{set}} = \frac{s}{\omega_0 J s^2 + \omega_0 D_p s + A} \tag{7}$$

2. When $P_{set} = 0$, the transfer function of angular frequency $f_{\omega - \omega g}$ can be expressed as:

$$f_{\Delta\omega-\Delta\omega_g}(s) = \frac{\Delta\omega}{\Delta\omega_g} = \frac{A}{\omega_0 J s^2 + \omega_0 D_p s + A} \tag{8}$$

When the step change of active power reference value, the transfer function in Eq. 7 may be utilized as an analytical tool. The transfer function in Eq. 8 can be used to investigate how the frequency swings when the short time disturbance of the grid frequency. According to Eq.7 and Eq.8, GFM inverter is a second-order system whose natural frequency ω_n and damping ratio ζ can be expressed as follows:

$$\begin{cases} \omega_n = \sqrt{\dfrac{A}{\omega_0 J}} \\ \zeta = \sqrt{\dfrac{\omega_0 D_p^2}{4AJ}} \end{cases} \tag{9}$$

Since the virtual damping coefficient D_p provides the adjustment ability of the P-f droop, which is determined by the adjustment ability of the energy, it is fixed as a constant in this study. The design of the relevant parameters can be found in (Wu et al.,2016; Zhang et al.,2017).

3.2 Influence of virtual inertia on the frequency response of GFM inverter

1) Step change of active power reference value: when the reference value of active power changes suddenly as Eq. 10, the deviation of active power output can be varied as Eq. 11.

$$\Delta p_{set}(t) = \alpha \cdot u(t) \tag{10}$$

$$\Delta\omega(t) = \frac{4\alpha J}{4AJ - D_p^2\omega_0} \cdot e^{-\frac{D_p}{2J}t} \sin\left(\frac{\sqrt{4A\omega_0 J - \omega_0^2 D_p^2}}{2\omega_0 J}t\right) \tag{11}$$

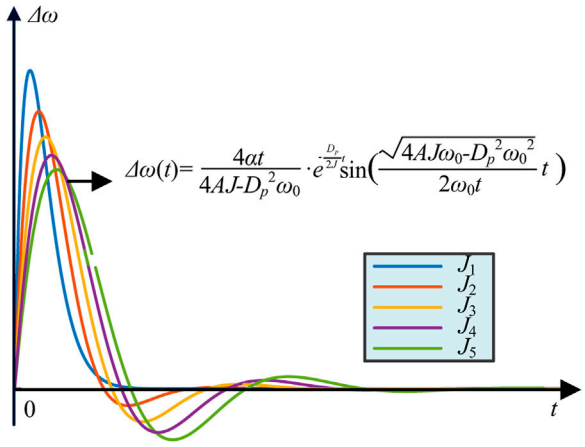

FIGURE 3
Frequency response under different virtual inertia values in the step change of active power reference value.

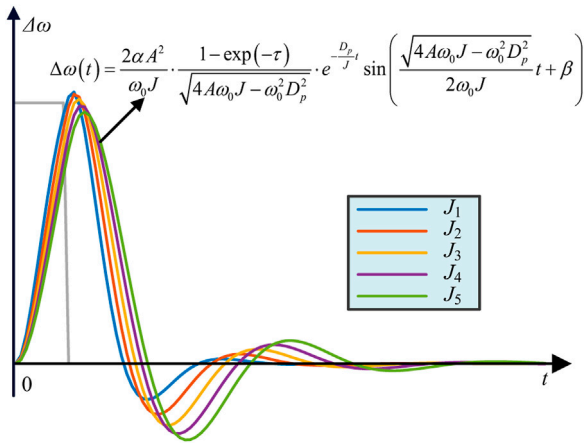

FIGURE 4
Frequency response under different virtual inertia values in the short time drop of the grid frequency.

where α represents the degree of change, $u(t)$ is the unit step function.

The expression of peak time and corresponding angular frequency can be expressed as Eq.12 and Eq.13, respectively.

$$t_P = \frac{\beta}{\frac{\sqrt{4A\omega_0 J-\omega_0^2 D_P^2}}{2\omega_0 J}} \tag{12}$$

$$\Delta\omega(t_p) = \frac{4\alpha}{4A\omega_0 J - \omega_0^2 D_p^2} \cdot e^{\sqrt{\frac{\omega_0 D_p^2}{4AJ-\omega_0 D_p^2}}\beta} \sin\beta \tag{13}$$

where $\beta = \arctan\left(\sqrt{4AJ/(\omega_0^2 D_p^2) - 1}\right)$.

Based on the transfer function in Eq. 11, Figure 3 illustrates the curve of $\Delta\omega(t)$ as the virtual inertia grows from J_1 to J_5. An observation of the graph shows that the highest value of the curve decreases while the duration of the curve oscillation grows as J increases. It can be found that bigger J gives smaller overshoot, but longer peak time. Therefore, in the case of the step change of active power the variation of J has the opposite effect on the overshoot and peak time of inverter frequency.

In contrast to (Li M et al., 2019), this paper gives a detailed derivation of equations and theoretical analysis of the frequency response under the step change of active power reference value, illustrating the effect of virtual inertia J on frequency in this case.

2) Short time disturbance of the grid frequency: the grid frequency will change described in Eq. 14 when the grid is disturbed. Meanwhile, the angular frequency deviation of inverter can be obtained from Eq. 15.

$$\Delta\omega_g(t) = \alpha \cdot u(t) - \alpha \cdot u(t-\tau) \tag{14}$$

$$\Delta\omega(t) = \frac{2\alpha A^2}{\omega_0 J} \cdot \frac{1-\exp(-\tau)}{\sqrt{4A\omega_0 J - \omega_0^2 D_P^2}} \cdot e^{-\frac{D_P}{J}t} \cdot \sin\left(\frac{\sqrt{4A\omega_0 J - \omega_0^2 D_P^2}}{2\omega_0 J}t + \beta\right) \tag{15}$$

where τ indicates the duration of grid frequency.

In this case, the time when the frequency deviation reaches the peak value and the corresponding output are the same as the research method in the case of the step change of active power reference value, so it will not be repeated here. Figure 4 depicts the reaction curve of $\Delta\omega(t)$ as the virtual inertia grows from J_1 to J_5, based on the transfer function in Eq. 11. From Figure 4, it is clear that with the increase of virtual inertia J, the overshoot becomes smaller, but the setting time becomes longer. Therefore, when the grid frequency disturbance for a short time, the change of J has the opposite effect on the overshoot and the setting time of inverter output frequency.

In general, a larger virtual inertia will reduce the overshoot of the angular frequency in the above two cases. However, the setting time of the inverter frequency will become longer after the system is interfered if the virtual inertia J is too large. Therefore, it can be concluded that the change of the virtual inertia has opposite effects on the two indicators of the system output angular frequency dynamic performance: the overshoot and the setting time.

4 A sigmoid-based adaptive inertia regulator

From the analysis in Section 2, it is unrealistic to set a fixed virtual inertia J so that the inverter can meet the requirements of the small overshoot and the short setting time under various disturbances of different amplitude. Therefore, this paper proposes a sigmoid-based adaptive inertia regulator to adjust the virtual inertia. The basic strategy is as follows:

In order to improve the dynamic performance of inverter output frequency, the value of virtual inertia J should be adaptive: when the amplitude of frequency deviation is small, the inverter can ignore the impact of the overshoot and minimize the virtual inertia of the system to achieve rapid response and ensure the system recovery as soon as possible. Once the frequency deviation of the system becomes larger, it should mainly suppress the frequency

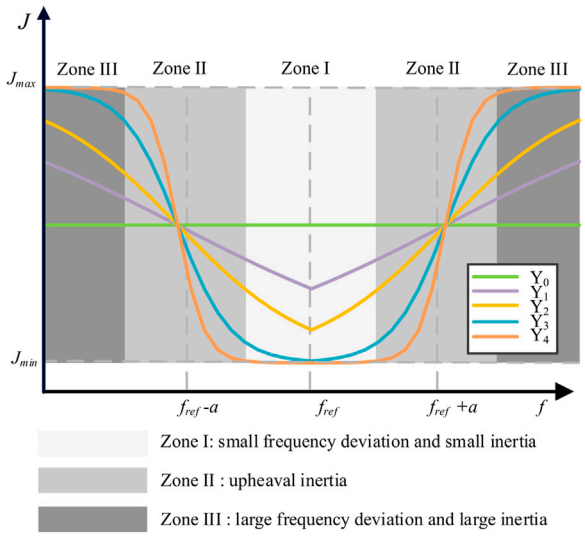

FIGURE 5
Sigmoid-based adaptive inertia regulation curve under different *k*.

oscillation and try to increase the virtual inertia of the system to reduce overshoot.

The virtual inertia generated by the sigmoid-based adaptive inertia regulator is shown in Eq. 16, and its function curve is shown in Figure 5.

$$J\left(|\Delta f|\right) = J_{\min} + \left(J_{\max} - J_{\min}\right)\frac{1}{1+e^{-k\left(|\Delta f|-a\right)}} \tag{16}$$

where $J_{\min}$ and $J_{\max}$ are the lower limit and upper limit of virtual inertia, respectively. a and k denote the adjustment coefficients. Δf is the input of the sigmoid-based adaptive inertia regulator. By using different values of a and k, the shape of the regulation can be changed. In this paper, a is used to control the curve to move right or left. k is used to control the slope of the curve and can be expressed as the sensitivity of the tuning function. According to Eq. 16, $J = (J_{\min} + J_{\max})/2$ when $\Delta f = a$. Hence, a is designed to $|\Delta f|_{max}/2$ in this paper, where $|\Delta f|_{max}$ is the maximum frequency deviation of the power grid.

In order to balance the overshoot and response speed, the range of system damping ratio ζ is generally required (Wu et al.,2016). According to the expression of ζ in Eq. 9, the upper limit $J_{\min}$ and lower limit $J_{\max}$ of Eq. 16 can be calculated.

Figure 5 shows the curves of sigmoid-based adaptive inertia regulation with different k. There are five curves in Figure 5, where k increases from Υ_0 to Υ_4 and Υ_0 means $k = 0$. The inertia regulator can be divided into three Zones, which are Zone I with small frequency deviation and small inertia, Zone II with upheaval inertia and Zone III with large frequency deviation and large inertia. When the frequency deviation is small with ordinary state, the inertia regulator works in Zone I. Hence, the corresponding inertia is very small, which can respond to interference as soon as possible. When a disturbance occurs. The increase in frequency deviation causes the inertial regulator to enter Zone II further leading to a rapid growth in virtual inertia. Then, the inertia regulator is transferred to Zone III to maintain a large inertia with the further increase of frequency deviation. Finally, the inertia regulator is returned to work in Zone I with the decrease of the frequency deviation.

5 Stability analysis

The inertia regulator designed in Section 3 is a non-linear part, and its introduction will inevitably affect the system. In order to analyze the influence of the control strategy in this paper on the stability of the system, a full-order small-signal model of GFM inverter containing the inertia regulator is established in this section and thus the eigenvalue analysis is provided to guide the selection of control parameters.

5.1 Full-order small-signal model

$$\begin{cases}
u_o^d = \dfrac{1}{sC_f}\left(\omega C_f u_o^q - i_o^d + i_c^d\right)\\
u_o^q = \dfrac{1}{sC_f}\left(-\omega C_f u_o^d - i_o^q + i_c^q\right)\\
i_c^d = \dfrac{1}{sL_f}\left(\omega L_f i_c^q - u_o^d + u_c^d\right)\\
i_c^q = \dfrac{1}{sL_f}\left(-\omega L_f i_c^d - u_o^q + u_c^q\right)\\
\dfrac{d\phi^d}{dt} = u_{o_ref}^d - u_o^d\\
\dfrac{d\phi^q}{dt} = u_{o_ref}^q - u_o^q\\
\dfrac{d\gamma^d}{dt} = i_{c_ref}^d - i_c^d\\
\dfrac{d\gamma^q}{dt} = i_{c_ref}^q - i_c^q\\
P = \dfrac{3}{2}\left(u_o^d i_o^d + u_o^q i_o^q\right)\\
Q = \dfrac{3}{2}\left(u_o^q i_o^d - u_o^d i_o^q\right)\\
J\dfrac{d\omega}{dt} = \dfrac{P_{set}}{\omega_0} - \dfrac{P}{\omega_0} - D_p\left(\omega - \omega_0\right)\\
u_{o_ref}^d = \dfrac{K\left[\left(Q_{ref} - Q\right) - D_q\left(u_{om} - u_{gm}\right)\right]}{s} + u_{gm}\\
u_{o_ref}^q = 0
\end{cases} \tag{17}$$

The general form of the linearized small-signal state-space model of the system is ($\dot{x} = Ax + Bu$). According to the control structure of GFM inverter in Figure 1, the control equation of the system can be obtained as formula Eq. 17. Then, combining Eq. 17 with the control delay equation: Eq. 5 and the sigmoid-based adaptive inertia regulator: Eq. 16. The system has 17 state variables and 17 non-linear equations to describe the dynamic characteristics of the system. Finally, the above equations are linearized at the operating point, the full-order small-signal model of the system can be obtained:

TABLE 1 **Parameters of GFM inverter.**

Symbol	Quantity	Value
r_f/Ω	Filter resistance	0.1
L_f/mH	Filter inductance	2
C_f/μF	Filter capacitance	50
r_g/Ω	Connecting resistance	0.14
L_g/mH	Connecting inductance	7
P_{load}/kW	Load active power	10*0.85
Q_{load}/kVar	Load reactive power	10*0.53
P_{set}/kW	Active power reference	10*0.85
Q_{set}/kVar	Reactive power reference	10*0.53
V_{nm}/V_{gm}/V	Rated/grid voltage	$220\sqrt{2}$
ω_n/ω_g/(rad/s)	Rated/grid angular frequency	2π*50
D_p	*P-f* damping ratio	8.6123
D_q	*Q-V* damping ratio	340.7
K	*Q-V* voltage factor	0.1153
K_{vp}	Voltage loop P factor	0.5
K_{vi}	Voltage loop I factor	400
K_{ip}	Current loop P factor	20
K_{ii}	Current loop I factor	15,000
$J_{\min}$	Lower limit of virtual inertia	0.1379
$J_{\max}$	Upper limit of virtual inertia	0.5514
a	Regulator translation	0.1
τ	sampling time of DSP	1/10,000
k	Regulator sensitivity	[0.1,1000]

$$\Delta \dot{x}_{sys} = A_{sys}\Delta x_{sys} \tag{18}$$

where Δ represents small disturbance, x_{sys} denotes the state variable of the system and A_{sys} is the state matrix of the system.

$$\Delta x_{sys} = \left[\Delta\omega; \Delta P; \Delta Q; \Delta\phi^d; \Delta\phi^q; \Delta\gamma^d; \Delta\gamma^q; \Delta i_c^d; \Delta i_c^q; \Delta i_o^d; \Delta i_o^q; \Delta u_o^d; \Delta u_o^q; \Delta x_{d1}; \Delta x_{d2}; \Delta x_{d3}; \Delta x_{d4}\right]^{\mathrm{T}} \tag{19}$$

where $\Delta\varphi^d$, $\Delta\varphi^q$, $\Delta\gamma^d$ and $\Delta\gamma^q$ are the state variables introduced by voltage outer loop and current inner loop, respectively; $\Delta i_c{}^d$, $\Delta i_c{}^q$, $\Delta i_o{}^d$, $\Delta i_o{}^q$, $\Delta u_o{}^d$ and $\Delta u_o{}^q$ are the minor change of $i_c{}^d$, $i_c{}^q$, $i_o{}^d$, $i_o{}^q$, $u_o{}^d$ and $u_o{}^q$, respectively. Δx_{d1}, Δx_{d2}, Δx_{d3} and Δx_{d4} ^{q} are the minor change of x_{d1}, x_{d2}, x_{d3} and x_{d4} in Eq. 5, respectively.

5.2 Root-locus analysis

The parameters of GFM inverter are listed in Table 1. Based on the full-order small-signal model in Eq. 18, the stability of the sigmoid-based inertia strategy is analyzed by using the trajectory of the dominant eigenvalues with k varying from 0.1 to 1000, as illustrated in Figure 6. The trajectory of the dominant eigenvalues with τ varying can be plotted as in Figure 7.

Figure 6 shows that when k is decreased, the dominant eigenvalues moves to the right, indicating that the stability degrades. However, the eigenvalues of the system are all located on the left side of the real axis, which indicates that the system is stable after adding the sigmoid-based adaptive inertia regulator.

Figure 7 shows that the increased of τ causes the stability degrades. The eigenvalues of the system are all located on the left side of the real axis when τ increased from 1/10,000 to 1/6000. However, some of the eigenvalues lie to the right of the real axis when τ = 1/5000, which means that the system become unstable.

In summary, the system becomes unstable after the delay time increases to τ = 1/5000. Therefore, in some high-power situations with low switching frequency, a control delay compensation algorithm should be added to ensure the stability of the system (Pan et al.,2013).

6 Case studies

To fully verify the effectiveness of the proposed strategy, a hardware-in-the-loop (HIL) platform is established. As shown in Figure 8, the HIL platform consists of four parts: an OPAL RT-LAB OP5700 real-time digital simulator, three Ti's TMS320FDSP28377D digital signal processor (DSP)-based control boards, a personal computer (PC) and a Tektronix MOS54 oscilloscope. Firstly, the PC downloads the C-based program to the DSP through the emulator. The RT-LAB is connected to PC via RJ45 Cable. Then, the control commands are sent down from the RT-LAB to the DSP. The DSP implements the control algorithm and generates the modulation signal to the RTLAB. The data transfer between DSP and RTLAB is realized through I/O interface card. Finally, the test results are displayed in oscilloscope which is connected to RT-LAB by the I/O interface card.

6.1 Verification of system stability

To verify the stability of the proposed strategy, k = 0.1, 40 and 200 are compared in this scenario. The disturbances are set as follows: P_{set} is suddenly increased to 17 kW and suddenly decreased to 8.5 kW after 2 s. Besides, the frequency oscillation begins after 4 s and lasts 0.2 s. The HIL test results are shown in Figure 9.

Specifically, Figure 9 shows that the system is stable under disturbances, which verifies the stability of the proposed strategy. Meanwhile, the smaller k (k = 0.1) means that the proposed strategy cannot adjust the inertia according to frequency deviation. The larger k (k = 200) makes the adaptive inertia regulator sensitive to frequency deviation and thus the sigmoid-based adaptive inertia regulator has fast inertia adjustment capability. However, the larger value of k will also cause a sharp increase in the rate of change of frequency (RoCoF), which can cause tremendous damage to the generator of grid, as displayed in Figure 9C. Therefore, a proper k = 40 is designed to balance the adaptive ability of inertia regulator and RoCoF of system.

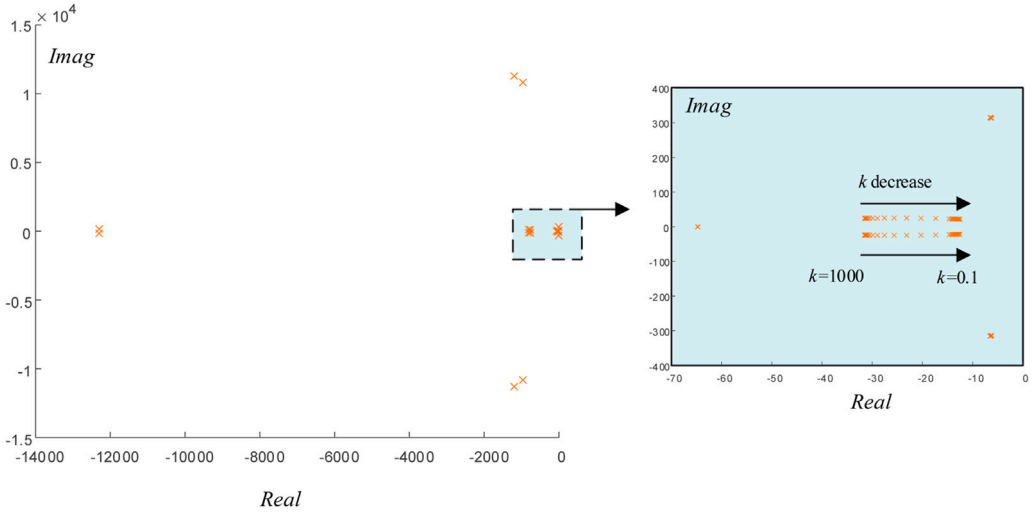

FIGURE 6
The trajectory of the dominant eigenvalues with k varying.

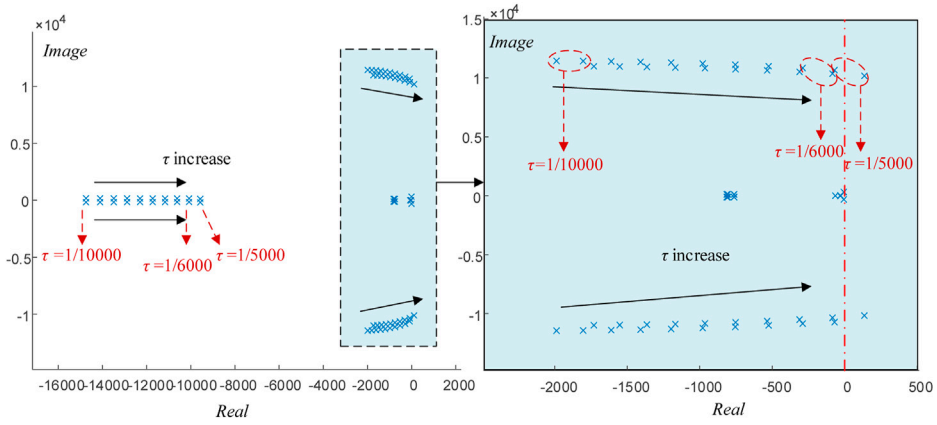

FIGURE 7
The trajectory of the dominant eigenvalues with τ varying.

6.2 Dynamic performance of the proposed strategy

The conventional strategy II with small constant inertia ($J = 0.05$), the conventional strategy III with big constant inertia ($J = 3$), the strategy IV with bang-bang inertia control in (Alipoor et al.,2014), the strategy V (Hou et al.,2020) and the proposed sigmoid-based inertia strategy I are compared in the following scenarios to validate the dynamic performance. In (Alipoor et al.,2014), two kinds of inertia values are determined by evaluating the states of frequency deviation Δf and the rate of its change (df/dt).

Remark1: Each of the aforementioned strategies is implemented independently in the DSP-based control boards. The disturbances, such as sudden changes in active power and frequency fluctuation, are generated in RT-LAB.

Remark 2: The output powers and its references of strategy I, strategy II, strategy III and strategy IV are represented by P_1, P_2, P_3 and P_4, respectively. The power references of strategy I, strategy II, strategy III and strategy IV are denoted by P_{set1}, P_{set2}, P_{set3} and P_{set4}.

Scenario 1: A sudden active power command is given to GFM inverter. The initial $P_{set1} = P_{set2} = P_{set3} = 8.5$ kW. In this scenario, the disturbances are set as follows: All of the P_{set} are stepped up to 17 kW and then P_{set} is set returned to 8.5 kW after 2 s. The HIL test results are shown in Figure 10.

Scenario 2: A sudden fluctuation in the angular frequency of the common coupling point. The initial P_{set} are same as Scenario 1. The disturbances are set as follows: the frequency oscillation begins after 2 s and lasts 0.2 s. The HIL test results are displayed in Figure 11.

Figure 10 shows that the trend of the active power and frequency is similar for the three control strategies. The active power follows

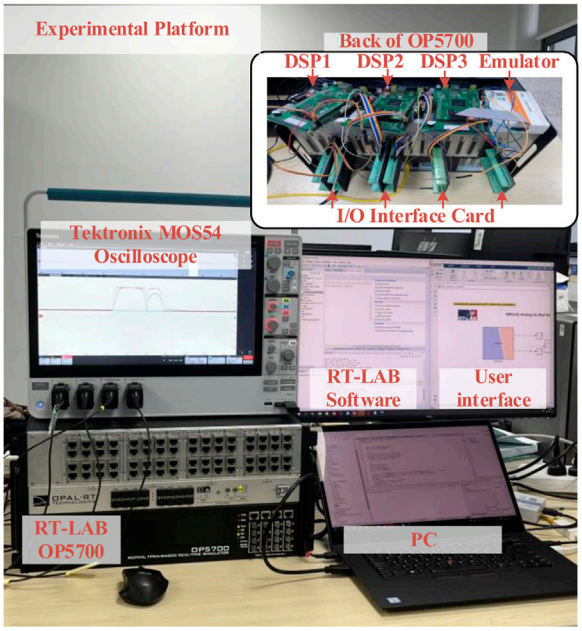

FIGURE 8
Hardware in loop experimental platform.

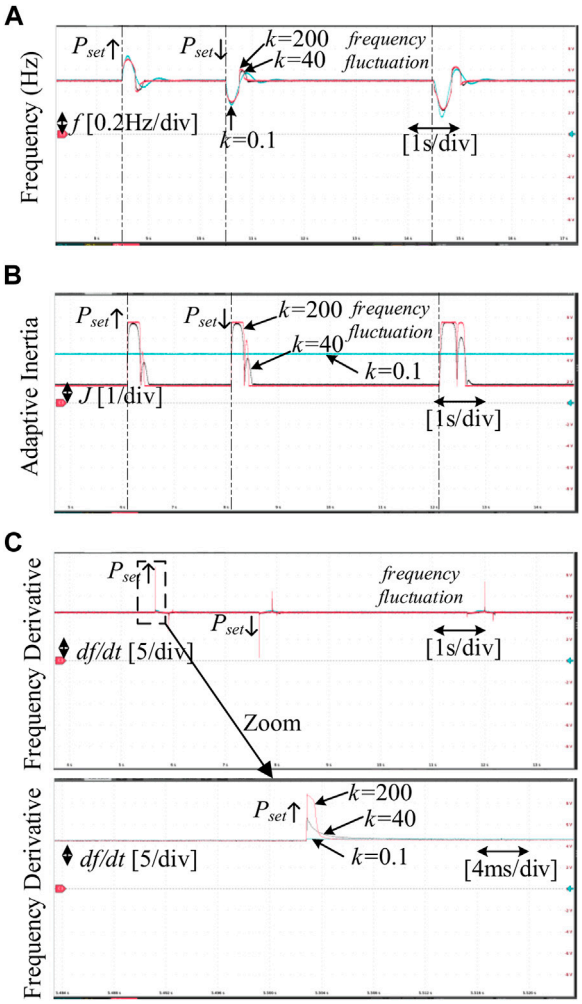

FIGURE 9
The proposed strategy with different K **(A)** Frequency of GFM inverter. **(B)** Adaptive inertia of GFM inverter. **(C)** Frequency derivative of GFM inverter.

the references and the frequency is restored to stability after disturbances. However, their dynamic performances are different. The setting time of strategy II is short due to the small inertia while a large frequency deviation also accompanies it. The large frequency deviation threatens the frequency stability of the system. On the contrary, strategy III has a longer setting time although the maximum frequency deviation is smaller. Hence, Fixed inertia control strategies, such as strategies II and III, always lead to a contradiction between the maximum frequency deviation and the setting time of the system. Fortunately, the maximum frequency deviation of the proposed strategy I is similar to strategy III and is only 2/3 of strategy II. The adjustment time of the proposed strategy I is also significantly shorter than that of strategy III. For the setting time, the proposed strategy I longer than strategy II but significantly shorter than strategy III. Therefore, the proposed strategy I achieves better overall dynamic performance.

Figure 11 also illustrates the good dynamic performance of the proposed strategy I when frequency fluctuations occur. Their specific analysis is similar to the previous one. Hence, it is omitted in this paper.

6.3 Comparison with existing method

Scenario 3: Similar to Scenario 1, a sudden active power command is given to GFM inverter. The initial $P_{set1} = P_{set4} =$ 8.5 kW. Both of the P_{set} are stepped up to 17 kW. Moreover, a high-frequency noises are imposed into the frequency of GFM inverter. To illustrate the difference between the proposed strategy I in this paper and strategy IV in (Alipoor et al.,2014), Scenario 3 is used. The HIL test results of Scenario 3 are shown in Figure 12.

As observed, although strategy IV converges quickly, the frequency deviation is larger than the proposed strategy I. This phenomenon is mostly caused by the sensitivity of alternating inertia to high-frequency noises. Due to the erroneous interference of *df*/*dt*, the alternating inertia cannot always maintain a large value during the disturbance process, as shown in Figure 12B. In fact, when strategy IV is implemented, a first-order low-pass filter has been added to the differential operation. However, the erroneous interference of *df*/*dt* still exists in HIL experiments. It indicates that the sensitivity of alternating inertia to high-frequency noises cannot solve by the first-order low-pass filter. In general, the adaptive control proposed in this paper is not affected by high-frequency noise due to the absence of differential operation. Therefore, the proposed strategy I is more advantageous and valuable in practical use compared to strategy IV.

Scenario 4: Similar to Scenario 1, a sudden active power command is given to GFM inverter. The initial $P_{set1} = P_{set4} =$ 8.5 kW. Both of the P_{set} are stepped up to 21.25 kW. The sudden

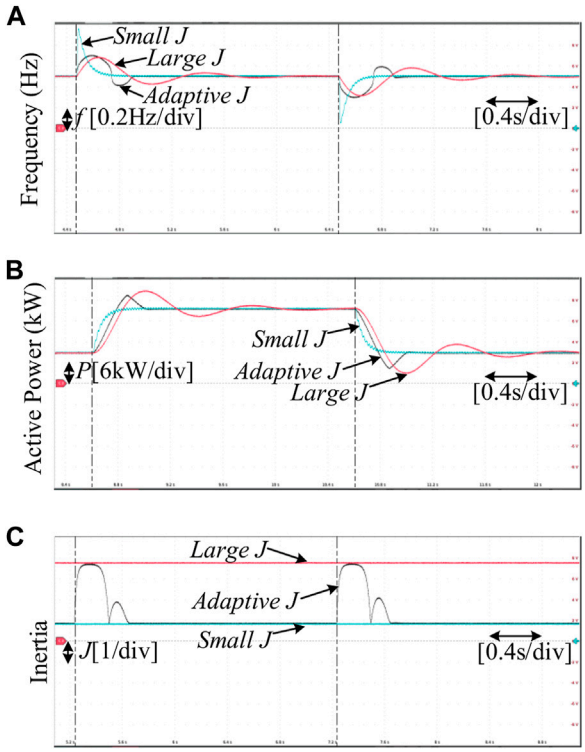

FIGURE 10
Experimental results of Scenario 1. **(A)** Frequency of GFM inverter. **(B)** Active power of GFM inverter. **(C)** Inertia of GFM inverter.

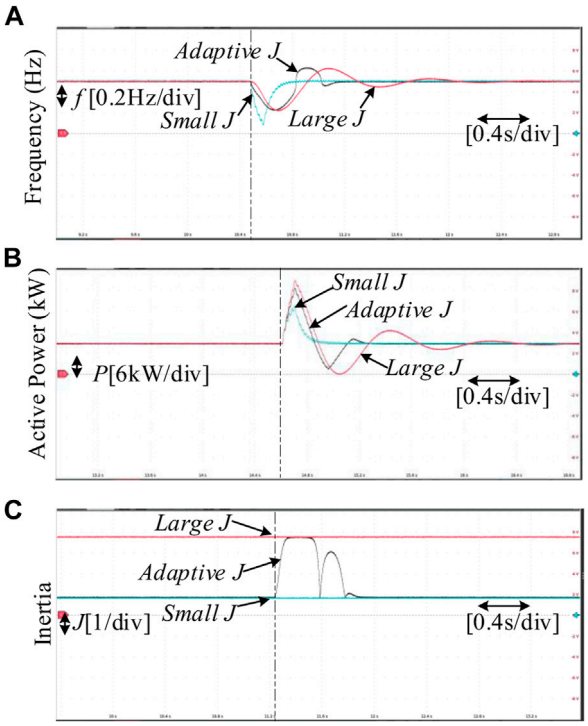

FIGURE 11
Experimental results of Scenario 2. **(A)** Frequency of GFM inverter. **(B)** Active power of GFM inverter. **(C)** Inertia of GFM inverter.

active power command in this Scenarioexceedes the set value, which is 1.5 times larger than in Scenario 3. Scenario 4 helps to analyze the impact of strategy on system uncertainty.

To illustrate the difference between the proposed strategy I in this paper and strategy V in (Hou et al.,2020), Scenarios 1 and 4 are used. The HIL test results of Scenarios 1 and 4 are shown in Figure 13.

As observed, both strategies can adjust the inertia to achieve good dynamic performance in Scenario 1. The maximum frequency deviation of strategy V is slightly lower than that of strategy I, while the setting time of strategy I is slightly shorter. When the frequency deviation is small, the adaptive inertia of strategy I is smaller, that's why setting time of strategy I is slightly shorter. In general, both strategies show good dynamic performance without significant differences.

However, when there is uncertainty in the system, i.e., the power command is out of the preset range. As shown in Figure 13 Scenario 4, the inertia in strategy V is out of the safety range, resulting in system instability. This indicates that the control parameters of strategy V need to be carefully designed and retain some margin. Otherwise there is a risk of system instability when the sudden active power command exceeds a predetermined value (Hou et al.,2020). From the principle of the proposed strategy I, the inertia is strictly limited to the safety range. Hence, the system can still maintain stability in Scenario 4.

Based on the above experiments, Table 2 can be listed. It is clear that the proposed strategy in this paper achieves a small frequency deviation of the same magnitude as a large inertia strategy. And the setting time is also shortened. Compared to the bang-bang control, the proposed strategy reduces frequency deviation and avoids the problem of high-frequency noise. Compared to strategy V, the proposed strategy shows better robustness to the uncertainty of the system.

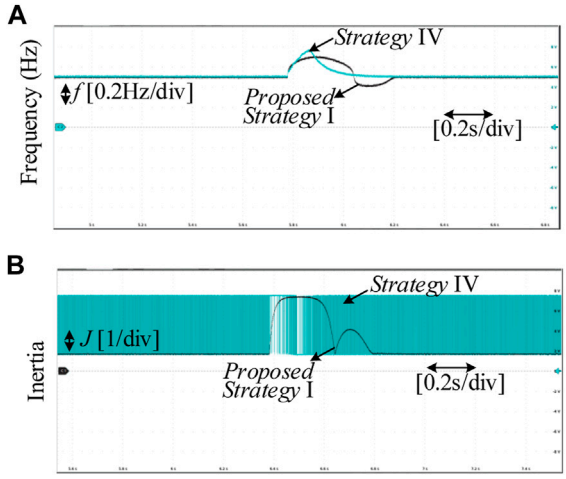

FIGURE 12
Experimental results of Scenario 3. **(A)** Frequency of GFM inverter. **(B)** Inertia of GFM inverter.

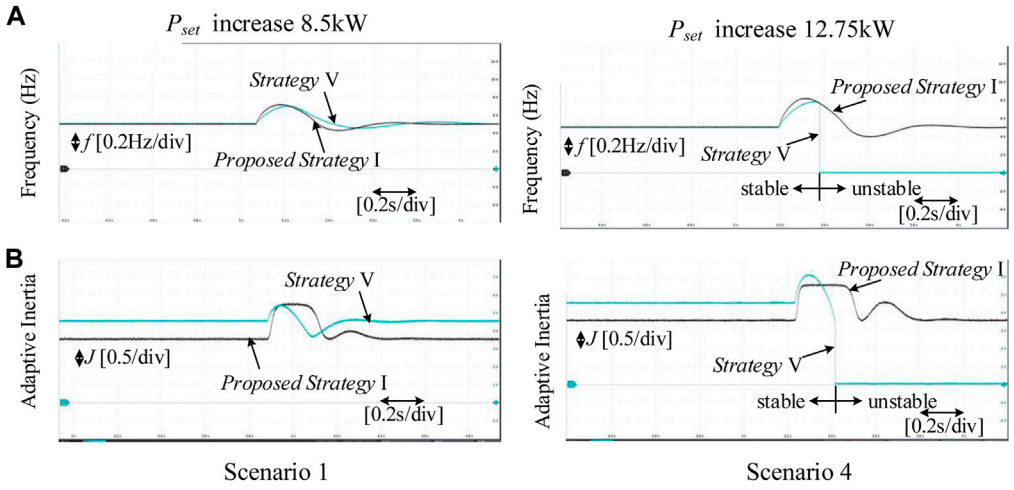

FIGURE 13
Experimental results of Scenarios 1 and 4. **(A)** Frequency of GFM inverter. **(B)** Inertia of GFM inverter.

TABLE 2 **Comparison of dynamic response under different strategies.**

Strategy	Maximum frequency deviation	Setting time
Strategy II (small *J*)	Large	Short
Strategy III (large *J*)	Small	Long
Strategy IV (bang-bang *J*)	Large	Short
Strategy V	Slightly Smaller than Strategy I	Slightly longer than Strategy I
Strategy I (proposed adaptive *J*)	Small	Normal

7 Conclusion

In this paper, the frequency response under the disturbances of active power and frequency are theoretically analyzed. Then, the problem that the fixed inertia leads to a contradiction between the maximum frequency deviation and the setting time is presented. Hence, this paper proposed a sigmoid-based inertia control strategy to solve the problem. The stability of proposed strategy is verified by establishing the full-order small-signal model of GFM inverter containing the inertia regulator. By using the proposed control strategy, the system inertia can be varied by frequency deviation to achieve a good dynamic performance on both maximum frequency deviation and setting time. Moreover, the proposed strategy shows strong robustness with high-frequency noises in system frequency due to the absence of derivative action. The effectiveness of the proposed control strategy is verified through HIL results.

Due to the sensitivity of differencing to high-frequency noise, researchers who want to study further in this field should avoid directly employing frequency differentiation for adaptive regulation in the future. One method is to eliminate the operations of frequency differentiation by mathematical method, such as (Hou et al.,2020). Another method is to directly design a virtual inertia regulator without differentiation.

Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

Author contributions

RH, writing-original draft, writing-review, theoretical analysis and simulation research. CD, writing-original draft, theoretical analysis and simulation research. ZW, conceptualization. All authors participated in the writing and editing of manuscript.

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Conflict of interest

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Synchronous rectification of LLC resonant converters based on resonant inductor voltage

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Synchronous rectification (SR) technology has been a critical technology for LLC converters to achieve high efficiency and power density. However, conventional SR driving methods face challenges in terms of light-load condition, module size, switching accuracy, and circuit complexity. This paper proposes an SR driving strategy based on resonant inductor voltage (RLV) to address those issues. This RLV-SR driving strategy does not require current sensors and is insensitive to rectifier parasitic parameters. In addition, the RLV-SR driving strategy can be applied in a relatively wide operating frequency range and load conditions. Experimental results based on a 100-W/24-V LLC converter are presented to verify the effectiveness of the proposed RLV-SR driving strategy. Furthermore, the error of turn-on time caused by stray inductance is significantly reduced compared with the conventional $V_{DS\text{-}ON}$ sensing method, which improves the power converter's efficiency.

KEYWORDS

LLC resonant converter, resonant inductor voltage, driving strategy, synchronous rectification, DC–DC converters

1 Introduction

LLC converters are widely used in server power supply (Lee et al., 2016; Ahmed et al., 2019), light-emitting diode (LED) drivers (Wang Y. et al., 2016), electric vehicle charging (Wang X. et al., 2016; Lin et al., 2023), renewable energy systems (Tayebi et al., 2019), and solid-state transformers (Zhang et al., 2021) due to the high conversion efficiency brought by its soft-switching characteristics. The secondary side rectifier diode conduction loss is one of the major losses (Yang et al., 2013) through the analysis of the conventional LLC topology loss. Synchronous rectification (SR) has a pivotal role in improving the efficiency of LLC converters. SR technology is to use MOSFETs instead of rectifier diodes. The MOSFET is turned on when rectified current passes through, while the MOSFET is turned off the rest of the time. Since the MOSFET has a small on-resistance, the large loss of the on-resistance on the diode is significantly reduced. As a result, the conversion efficiency is improved. Recent years have seen a considerable increase in the literature concerning the SR driving strategies of LLC converters.

The reported SR driving strategies can be divided into the following four categories: current-driven method, sensorless model-based method, v_{DS} sensing method, and method for high voltage sensing. The basic principles and precautions of the four methods are illustrated in Figure 1.

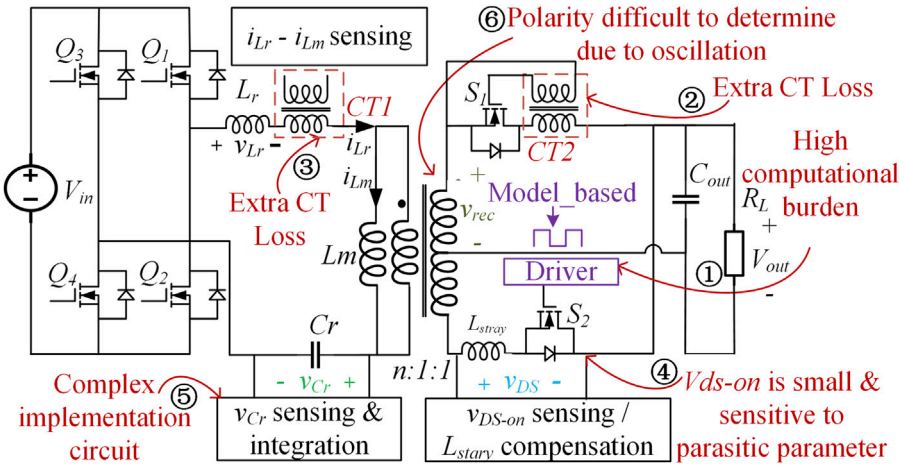

FIGURE 1
Conventional SR driving schemes: ① for sensorless model-based method, ②, ③for current sensing, ④ for V_{DS}-on sensing, and ⑤, ⑥ for high-voltage sensing.

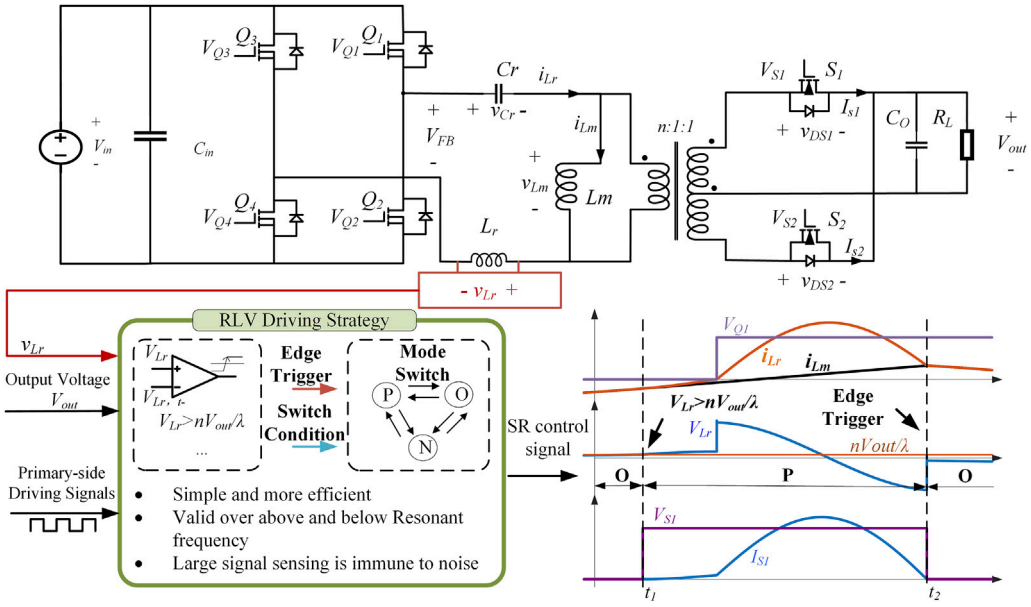

FIGURE 2
Proposed RLV strategy senses large voltage signals.

The first category of SR driving strategies is the sensorless model-based method. Zhu et al. (2021) built a mathematical model to determine that the turn-on instant and conduction time are adjusted adaptively. Li et al. (2021) built mathematical models based on the LLC equivalent impedance to calculate the SR on-time in the forward and reverse modes. Li et al. (2022) built a mathematical model to calculate the SR conduction time online in the forward and reverse modes and to determine the SR turn off instant considering the switching frequency and load. These schemes can modulate the SR control signal with high accuracy in the steady state. These solutions can reduce the cost by eliminating additional sensors; however, the theoretical models of these schemes are complex, leading to a high computational burden on the controller.

The second category is based on detecting primary or secondary side currents. A method to directly drive the SR based on the secondary current is proposed in Xie et al. (2001). The advantage of the direct driving strategy its simplicity and accuracy, and the strategy can be used in different working modes without additional driving power. In Kim et al. (2012), an SR scheme based on the primary side current drive of the transformer is introduced. By generating an auxiliary

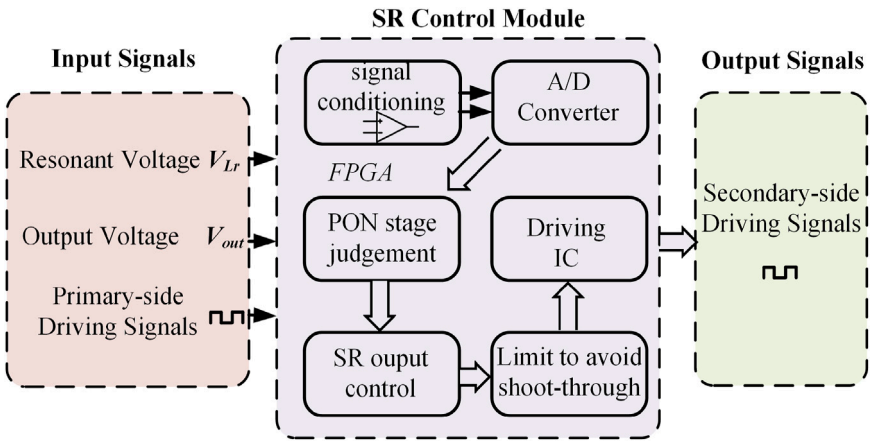

FIGURE 3
Key implementation of the proposed driving scheme.

current source, the magnetizing current (i_{Lm}) can be separated from the resonant current (i_{Lr}), which can be used to generate SR drive signals. The large current passed by the current sensor will lead to a sizeable primary loss of the sensor. In addition, considering the large volume of the sensor, it may not be suitable for cases requiring high power density. Since self-driven SR is needed, it may not be practical in light-load situations.

The third category of the existing technology is the v_{DS} sensing methods. Since the voltage drop of the rectifier is different when the diode is turned on and the MOS is turned on, this difference can be used to generate SR signals. Due to the stray inductance of the MOS package, the v_{DS} will reach the turn-off voltage faster, which results in the early turn-off of SR signals. To solve the problem of inaccurate turn-off time caused by stray inductance, the following two methods are adopted.

One method is to use an RC circuit to compensate for the stray inductance. Fu et al. (2009) used resistors, capacitors, and switches, and the conduction of the SR body diode was almost 0. A compensation circuit based on resistors, capacitors, and diodes was proposed by Wang et al. (2010) and Wang and Liu (2014), which can realize the compensation function more reliably and simply. However, this method needs to obtain an accurate SR parasitic inductance value to set the RC compensation circuit. At the same time, the compensation circuit may require a small switch MOS, which will increase the complexity of the system.

Another method is the use of an adaptive control strategy. The method was introduced by Qian et al. (2022) to improve reverse current. Moon et al. (2019) proposed an adaptive control method based on the last dead time measurement to realize the SR function. Measurement of dead time and a high-speed controller are also needed. The method proposed in Fei et al. (2018) is synchronized with the primary side, in which the switch-on point is at the primary side's turn-on time, and the switch-off point is based on the automatic adjustment process. The main advantage of this method is that it reduces the controller requirements through ripple measurement. These methods may introduce system reliability issues, which may lead to shoot-through. MOS changes in on-time may also introduce loss.

The last category is the high-voltage sensing method. In Hsu et al. (2019), the synchronous rectification function is realized by integrating and comparing the resonant capacitor voltage (v_{Cr}). The resonant capacitor voltage is a large voltage signal and, therefore, insensitive to interference. But integrators and comparators complicate the converter. In Mohammadi and Ordonez (2019), the half-bridge mid-point voltage and the polarity of the transformer voltage are sampled and compared; when the rectifier voltage polarity is the same as the input voltage polarity, the SR should be turned on. However, due to the limitation of circuit parasitics, the oscillation of the rectified voltage will make it difficult to judge the polarity, especially at high frequencies.

To resolve the aforementioned challenges of LLC converters, an SR strategy for LLC resonant converters based on the resonant inductor voltage (v_{Lr}) is proposed, referred to as synchronous rectification based on the resonant inductor voltage (SR-RLV).

The principle of this method is shown in Figure 2. This method can judge the working stage of the LLC resonant converter by measuring the value of the resonant inductor voltage (v_{Lr}). The resonant inductor voltage (v_{Lr}) value and the jump direction are used to derive the working stage of the circuit. The SR strategy is established by judging the current stage and calculation stage duration, and the SR function of the LLC converter is realized.

The proposed RLV strategy can turn on the SR MOS accurately and quickly and improve the conversion efficiency of the LLC converter. The inductor voltage v_{Lr} is large voltage amplitude, and the anti-interference performance is excellent. The strategy can work in the wide frequency range of the resonant converter. At the same time, the issues of bulky size and high cost caused by using a current transformer SR method are solved.

Section 2 describes the detailed steps of operations, which demonstrate that the RLV method covers a wide operating range of frequencies from below to above and loads from heavy to light. The realization of a driving strategy based on RLV-SR is also introduced in this section. In Section 3, experimental results are presented to verify the effectiveness of the proposed RLV method. The conclusion is provided in Section 4.

2 RLV-SR driving strategy

To illustrate this method, the LLC topology circuit is shown in Figure 2. A full-bridge structure is adopted for the inverter part, and the rectifier part is a half-bridge structure. The system inverter part *Q1/Q4* is a group of identical signals, and *Q2/Q3* is a group of identical signals, which are sent out by the controller as known signals.

The implementation of the proposed driving scheme is shown in Figure 3. The resonant inductor voltage v_{Lr} and the output voltage V_{out} are input signals, which are input to the high-speed A/D converter through the signal conditioning circuit of the operational amplifier. The A/D conversion results are given to the FPGA module. The MOS drive signal on the primary side is also used as the input of the FPGA module.

The FPGA module uses the RLV-SR strategy to determine the PON stage according to v_{Lr} and V_{out} and the driving signals of the primary side. Simultaneously, the duration of the P stage (t_{stage_p}) and the duration of the N stage (t_{stage_N}) are measured. The on and off period of the SR signal is determined according to the RLV algorithm.

Before the SR drive signals are output, some output limits are set to avoid MOS shoot-through. When the upper and lower transistors of the SR signal are turned on, a dead time is set to prevent the MOS from being shoot-through. At the same time, when V_{out} drops below the safe range, the DSP will turn off all MOS to avoid short-circuiting.

For LLC converters, according to the relationship between the current i_{Lr} flowing in the resonant inductor and the current i_{Lm} in the magnetizing inductance, the operating modes can be divided into three categories: *P* stage, N stage, and O stage. If $i_{Lr} > i_{Lm}$, the system is in the *P* stage, and the equivalent circuit is shown in Figure 4A, the upper half of the rectifier part is turned on, and the equivalent voltage is nV_{out}.

If $i_{Lr} = i_{Lm}$, the system is in the O stage, and the equivalent circuit is shown in Figure 4B, the resonant inductor *Lr* and the magnetizing inductance *Lm* participate in the resonance together, no current flows in the rectifier part, and the voltage source on the right is 0.

If $i_{Lr} < i_{Lm}$, the system is in the N stage, and the equivalent circuit is shown in Figure 4C, the lower half of the rectifier part is turned on, and the equivalent voltage is reversed, which is $-nV_{out}$.

The RLV-based SR signal needs to be completed through the following steps.

Step 1: Measure the resonant inductor *Lr* voltage v_{Lr} of the LLC resonant converter and the system output voltage V_{out} in real time.

Step 2: Judge the working stage of the LLC converter according to the value of v_{Lr} before or after the edge time of the primary-side control signals V_{Q1} and V_{Q2} and the value of v_{Lr} at the jumping time. The specific working stage judgment method is described in detail later.

Step 3: Measure the duration of the P stage (t_{stage_p}) and the duration of the N stage (t_{stage_N}) according to the circuit working stage.

Step 4: Using the current working stage obtained in Step 2 and the duration of each stage measured in Step 3, under the condition that the system output voltage is stable and the system output frequency is stable, output the synchronous rectification signals V_{S1} and V_{S2}.

When the system enters the P state: $V_{S1} = 1$, $V_{S2} = 0$, when $t = t_{stage\_P}$, $V_{S1} = 0$, $V_{S2} = 0$.

When the system enters the N state: $V_{S1} = 0$, $V_{S2} = 1$, when $t = t_{stage\_N}$, $V_{S1} = 0$, $V_{S2} = 0$.

When the system is in the O state: $V_{S1} = 0$, $V_{S2} = 0$.

If the system output voltage or system output frequency is unstable, waiting for stabilization is needed to output the SR signal.

In Step 2, the current working stage of the resonant circuit needs to be judged, and the judgment method is different under different working frequencies. The RLV-SR strategy will be introduced from three aspects: the resonant converter works below the resonant frequency, above the resonant frequency, and under light-load conditions.

2.1 Below resonant frequency region

When the operating frequency (f_s) of the system is below the resonant frequency (f_r) of the LLC converter ($f_s < f_r$), as shown in Figure 5, the following method of using v_{Lr} to judge the stage of the system is applied. From the time of the falling edge of V_{Q2} to the time of the falling edge of V_{Q1}, including the time of $V_{Q1} = 1$, it is the first half cycle of the system. The first half cycle is shown in the period from t_0 to t_2.

(1) The controller measures the resonant inductor v_{Lr} in real time, and the falling edge time of the control signal V_{Q2} is recorded as t_0. The corresponding voltages of the resonant inductor *Lr* before and after the time t_0 are $v_{Lr,t0-}$ and $v_{Lr,t0+}$, respectively.

$$\lambda\left|v_{Lr,t_{0-}}\right| > nV_o \tag{1}$$

If the system meets condition (1) before t_0 arrives, the system will be in the *P* stage; otherwise, it will be in the O stage. Here, $\lambda = Lm/Lr$, and n represents the transformation ratio between the primary side and the secondary side.

(2) At the time of the rising edge of the control signal V_{Q1}, the voltage of V_{FB} increases from $-V_{in}$ to V_{in}, and the resonant inductor voltage v_{Lr} increases, which is recorded as the first time of the v_{Lr} jump edge.

(3) Continue to judge condition (1), if $\lambda|v_{Lr}| > nV_o$, the system changes to the P state; otherwise, the system continues to be in the O state.

(4) After the system enters the P state, by measuring the resonant inductor Lr voltage v_{Lr}, if the second increase occurs, this moment is recorded as t_1, and the system state will be converted to the O state or the N state. At the time t_1, the resonant capacitor *Cr* voltage is $v_{Cr,t1}$:

$$v_{Cr,t_{1-}} = V_{in} - nV_o - v_{Lr,t1-}. \tag{2}$$

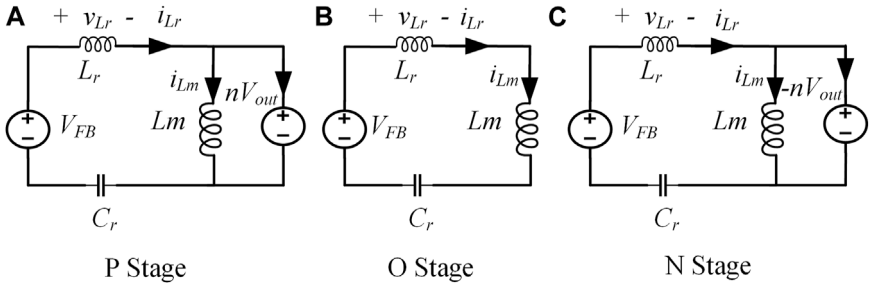

FIGURE 4
Three operation stages for the LLC resonant converter. **(A)** *P* stage. **(B)** N stage. **(C)** O stage.

If it is converted from the P state to the O state, calculate the voltage V_{Lm} of the magnetizing inductance Lm.

$$\begin{aligned} v_{Lm,t1+} &= \frac{\lambda}{\lambda+1}\left(V_{in}-\left(V_{in}-nV_o-v_{Lr,t1-}\right)\right) \\ &= \frac{\lambda}{\lambda+1}\left(nV_o+v_{Lr,t1-}\right) \end{aligned} \tag{3}$$

If the calculated value $|V_{Lm,t1+}| > nV_o$, the system enters the N state; otherwise, it enters the O state.

(5) If the system is at the O stage, the next stage will be the N stage. By measuring the resonant inductor Lr voltage V_{Lr}, calculate the current state magnetizing inductance Lm voltage V_{Lm}. If $|V_{Lm}| = \lambda V_{Lr} > nV_o$, the system enters the N state; otherwise, it remains in the O state until the end of the half cycle.
(6) If the system is converted to the N state, this state remains until the end of the first half cycle, and the end time is the control signal $V_{Q1} = 0$, which is the falling edge of V_{Q1}.
(7) From the time of the falling edge of V_{Q1} to the time of the falling edge of V_{Q2}, including the time of $V_{Q2} = 1$, it is the second half cycle of the system. The second half cycle is shown as the period from t_2 to t_4.

As shown in Figure 6, the waveform of the lower half cycle of the LLC system is symmetrical with the upper half cycle about the time axis, and the O state is the same, while the P state and N state are opposite.

The specific algorithm flow chart of the RLV-SR strategy algorithm for below resonance is shown in Figure 5.

Since the real-time status of the system can be measured by the aforementioned method, the P stage and N stage duration time can be measured synchronously.

2.2 Above resonant frequency region

When $f_s > f_r$, as shown in Figure 7, the method of using v_{Lr} to judge the stage of the system is as follows:

From the time of the falling edge of V_{Q2} to the time of the falling edge of V_{Q1}, including the time of $V_{Q1} = 1$, it is the first half cycle of the system. The first half cycle is shown as the period from t_0 to t_2.

(1) The controller measures the resonant inductor v_{Lr} in real time, and the falling edge time of the control signal V_{Q2} is recorded as

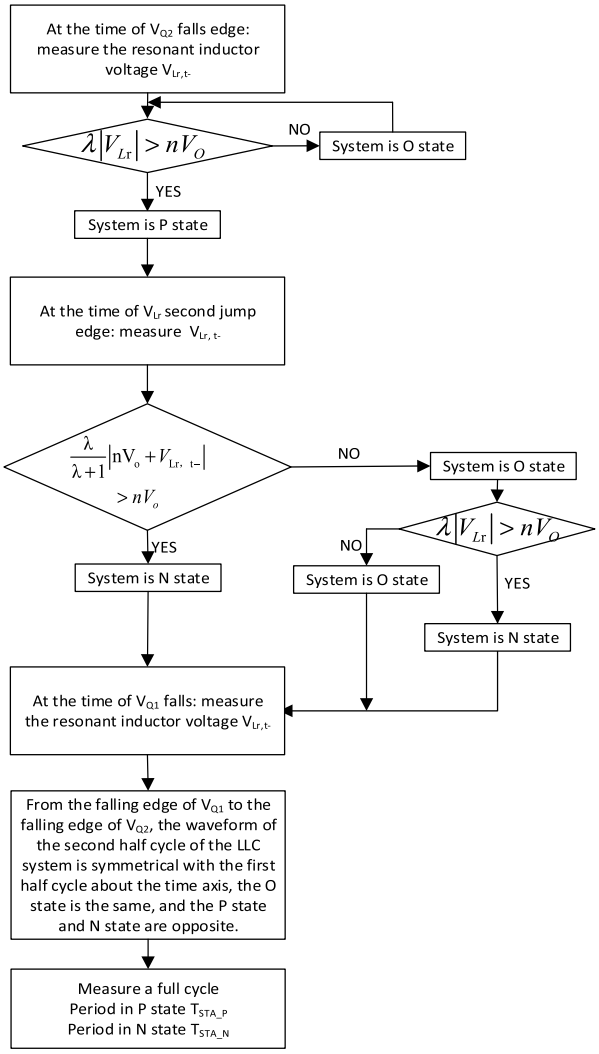

FIGURE 5
Flow chart of the RLV-SR strategy algorithm for below resonance.

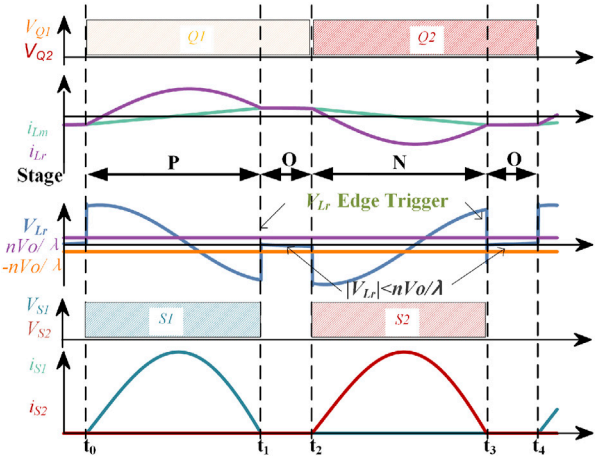

FIGURE 6
Key waveform of the RLV scheme for below resonance.

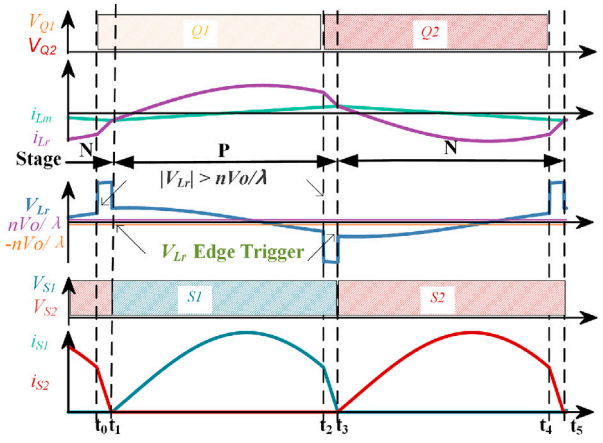

FIGURE 7
Key waveform of the RLV scheme for above resonance.

t_0. The corresponding voltages of the resonant inductor Lr before and after the time t_0 are $v_{Lr,t0-}$ and $v_{Lr,t0+}$, respectively.

If the system meets condition (1) before t_0 arrives, the system will be in the N stage; otherwise, it will be in the O stage.

(2) At the time of the rising edge of the control signal V_{Q1}, the voltage of V_{FB} jumps from $-V_{in}$ to V_{in}, and the resonant inductor voltage V_{Lr} jumps, which is recorded as the first time of the V_{Lr} jump edge.
(3) Continue to judge condition (1). If $\lambda|V_{Lr}| > nV_o$, the system changes to the N state; otherwise, the system continues to be in the O state.
(4) After the system enters the N state, by measuring the resonant inductor Lr voltage V_{Lr}, if the second increase occurs, this moment is recorded as t_1, and the system state will be converted to the O state or the P state. At the time t_1, the resonant capacitor Cr voltage V_{Cr} can be calculated by Eq. 2.

If it is converted from the P state to the O state, calculate the voltage V_{Lm} of the magnetizing inductance Lm with Eq. 3.

If the calculated value $|V_{Lm,t1+}| > nV_o$, the system enters the P state; otherwise, it enters the O state.

(5) If the system is at the O stage, the next stage will be the P stage. By measuring the resonant inductor Lr voltage V_{Lr}, calculate the current state magnetizing inductance Lm voltage V_{Lm}. If $|V_{Lm}| = \lambda V_{Lr} > nV_o$, the system enters the P state; otherwise, it remains in the O state until the end of the half cycle.
(6) If the system is converted to the P state, this state remains until the end of the first half cycle, and the end time is the control signal $V_{Q1} = 0$, which is the falling edge of V_{Q1}.
(7) From the time of the falling edge of V_{Q1} to the time of the falling edge of V_{Q2}, including the time of $V_{Q2} = 1$, it is the second half cycle of the system. The second half cycle is shown as the period from t_2 to t_4.

The flow chart of the RLV-SR strategy algorithm for above resonance is similar to the one shown in Figure 5.

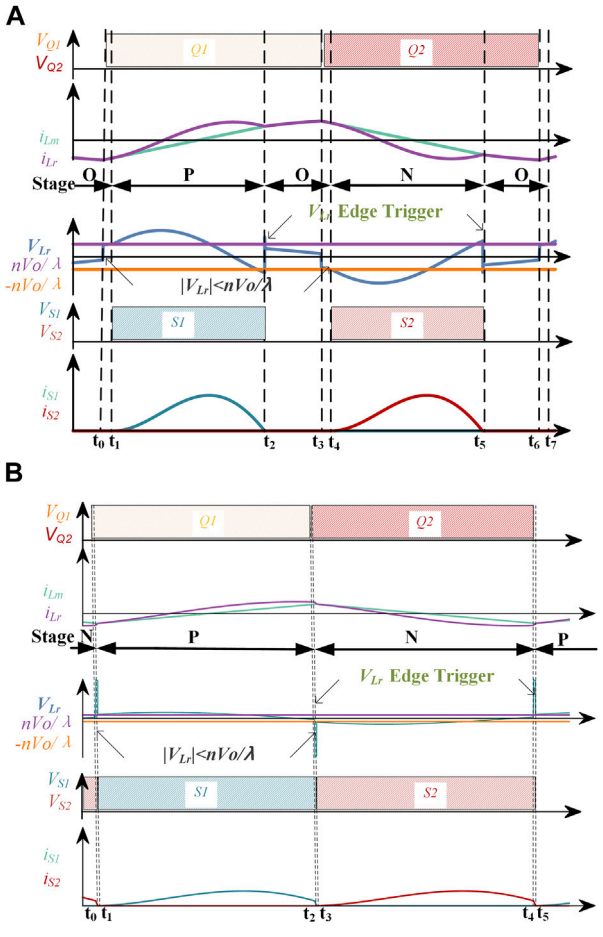

FIGURE 8
Key waveform of the RLV scheme for light-load condition: **(A)** below resonance and **(B)** above resonance.

As shown in Figure 7, the waveform of the lower half cycle of the LLC system is symmetrical with the upper half cycle about the time axis, and the O state is the same, while the P state and N state are opposite. Since the real-time stage can be measured by the aforementioned method, the P stage and N stage duration time can be measured synchronously.

2.3 Light-load condition

When the system works in a light-load condition, it is divided into below and above resonant frequency zones, as shown in Figure 8.

The situation below the resonant frequency with light-load condition is shown in Figure 8A. At time t_0, the voltage of V_{FB} increases from $-V_{in}$ to V_{in}. Since the system is in a light-load condition, the resonant capacitor voltage meets the requirements before the arrival of t_0, so the system stage is O.

During $t_0 \sim t_1$, the system is in the O stage until t_1.At t_1, $\lambda|v_{Lr}| > nV_o$, and the system enters the P stage.

During $t_1 \sim t_2$, the resonant voltage V_{Lr} jumps at time t_2, and the system changes to O stage. During $t_2 \sim t_3$, $\lambda|v_{Lr}| < nV_o$, the system remains in the O stage. At time t_3, V_{FB} increases from V_{in} to $-V_{in}$, and after the transition $\lambda|v_{Lr}| < nV_o$, the system is in the O stage. The state of the system changes is OPO in the first half cycle.

During the second half cycle of $V_{FB} = -V_{in}$. The analysis method is similar to the aforementioned method during $t_3 \sim t_7$, and the stage change in the first half cycle is ONO.

The situation above the resonant frequency with light load is shown in Figure 8B. During $t_0 \sim t_1$, V_{FB} increases from $-V_{in}$ to V_{in} at time t_0. Since the system is in a light-load state and the resonant inductor voltage meets the requirements $\lambda|v_{Lrt0-}| > V_o$ at t_0, the system will change to the N stage.

During $t_1 \sim t_2$, the condition $|V_{Lmt1+}| > nV_o$ is satisfied at t_1, and then the system changes to the P state.

It can be seen from the aforementioned analysis that the state of the system changes from N to P in the first half cycle.

During the second half cycle of $V_{FB} = -V_{in}$, the analysis method for the time during $t_2 \sim t_4$ is similar to the previously mentioned methods, and the state of change in the first half cycle is from P to N.

3 Experimental results

This section presents the experimental results of the proposed RLV strategy based on Table 1. This 100-W/24-V LLC converter is used to provide isolation for single-board power supplies. The RLV-SR strategy is compared with the conventional V_{DS-on} sensing scheme. The comparisons are carried out in the mode below the resonant frequency, above the resonant frequency, and in the light-load mode, respectively.

The experimental converter is shown in Figure 9. A full-bridge inverter on the primary side is controlled by the DSP controller. The RLV-SR control function is completed by the FPGA controller, and the driving signal of the SR is determined by collecting v_{Lr}, V_{out}, and the main switching signal of the primary side. The key components are shown in Table 2.

TABLE 1 Parameters of the LLC resonant converter.

Parameter	Value
Input voltage, V_{in}	24 V
Nominal power, P_{out}	100 W
Nominal output voltage, V_{out}	18–24 V
Switching frequency, f_s	35–60 kHz
Magnetizing inductance, L_m	32.9 μH
Resonant inductor, L_r	6.58 μH
Resonant capacitor, C_r	1.54 μF
Transformer turns ratio, n	5:5:5

Four voltage signals were given in the experimental result figures. While V_{Q1} is the primary-side control signal, V_{S1} is the synchronous rectification control signal of MOS S1, V_{DS-S1} is the DS voltage signals of MOS S1, and I_{S1} is the current signal of MOS S1.

In the below resonant frequency region, the converter operates at the same load and frequency, the results of the conventional V_{DS-on} method are shown in Figure 10A, and the proposed RLV strategy is shown in Figure 10B.

As shown in the bottom part of Figure 10A, V_{DS-S1} is zoomed. Due to stray inductance, the V_{DS-S1} voltage leads I_{S1} and reaches the voltage zero point before the rectified current is 0. At this time, the SR turn-off signal is triggered, and then the body diode of the MOSFET is on, which will cause premature turn-off of the system.

Unlike the conventional V_{DS-on} sensing method, the RLV-SR driving strategy does not use the V_{DS}. The RLV strategy is based on v_{Lr} and V_{out} is a large signal and cannot be disturbed. Therefore, as shown in Figure 10B, the work stage of the converter can be judged by the jumping edge of the v_{Lr} signal and the output voltage signal V_{out}. Then, according to the state and the duration of this state, determine the timing of turning on and turning off the SR signals.

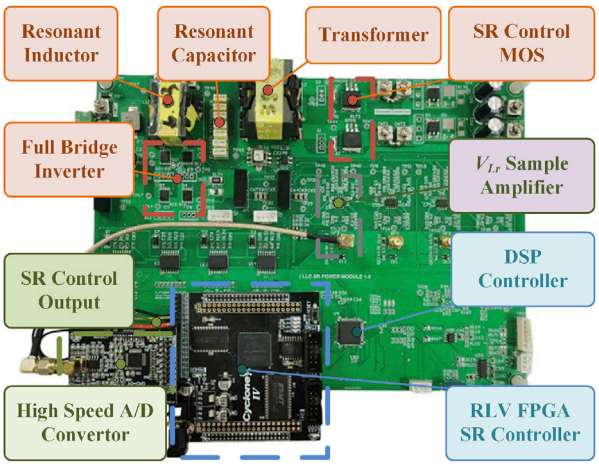

FIGURE 9
Experimental prototype: 100-W/24V resonant converter based on the RLV-SR control strategy.

TABLE 2 Parameters of the SR controller.

Category	Part number	Quantity	Purpose
A/D	AD9226	1	v_{Lr} analog-to-digital conversion
FPGA controller	EP4CE15F256	1	RLV-SR controller
DSP controller	TMS320F28034PNT	1	LLC primary side controller
OPAMP	LMH6626	1	High-speed amplifiers for v_{Lr}
OPAMP	GS8552-SR	1	General purpose amplifiers for V_{out}

V_{S1} is the SR control signal and I_{S1} is the current flowing in the rectifier MOS. V_{S1} is turned on when the system enters the P state and turned off at the zero-crossing time of I_{S1}. The RLV-SR driving strategy can well-realize the function of SR function.

In the operating range above the resonant frequency, when the converter operates under the same load and frequency, the conventional V_{DS-on} sensing strategy and the proposed RLV strategy are compared. The key waveforms are shown in Figures 11AB.

When the operating frequency (f_s) of the system is nearby or above the resonant frequency (f_r) of the LLC converter ($f_s \geq f_r$), the proposed RLV-SR strategy generates the dead time between the two SR switches to avoid shoot-through. The inserted dead time (DT) should be long enough to ward off shoot-through of MOS. In the experimental results, 20 ns dead time (DT) is inserted, and this is 0.1% of the resonant period while f_s = 50 kHz.

It can be seen in the upper part of Figure 11A that V_{DS-S1} is close to 0 while I_{S1} is greater than 0. The V_{DS-S1} signal is amplified, as shown in the lower part of Figure 11A. The control signal V_{S1} of the SR MOSFET *S1* can be turned on when the current is greater than 0, but due to the existence of stray inductance, the V_{DS-S1} signal reaches the threshold voltage in advance, while the current in the MOSFET is still 2.3 A at this time, which will reduce the conversion efficiency.

As shown in Figure 11B, when the converter operates in a mode above the resonant frequency, the RLV strategy effectively determines the zero-current crossing point by detecting the jump edge of V_{Lr} and the operating state of the system.

When the load of the converter is light, the output power of the system is 20 W, and the system works at 36 kHz. The experiment results are shown in Figure 12. The traditional V_{DS-on} sensing strategy and the RLV-based strategy are compared when the output is 20 W.

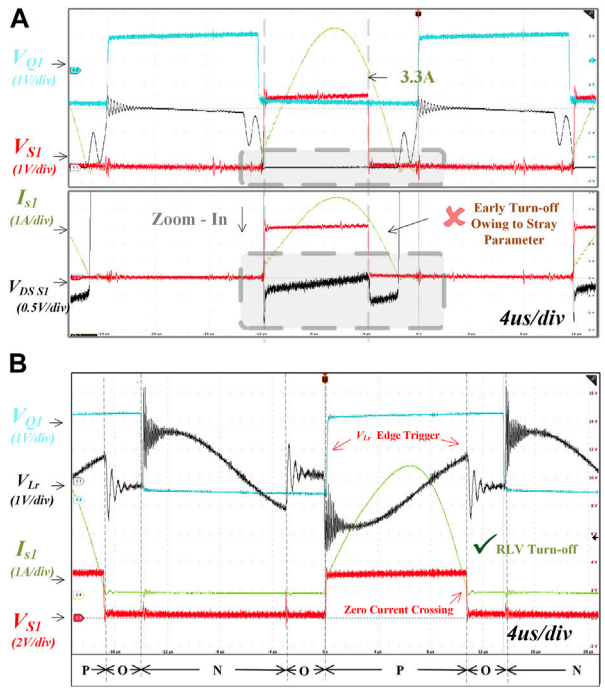

FIGURE 10
Experimental results below resonant frequency at the maximum power, 100 W/36 kHz. **(A)** V_{DS-ON} measurement method shuts down the SR early since the V_{DS} signal has reached the judgment threshold voltage when I_{S1} is 3.3A, while **(B)** the RLV strategy effectively determines the zero-current crossing point by sensing the edge of large and stable *Lr* voltage signals.

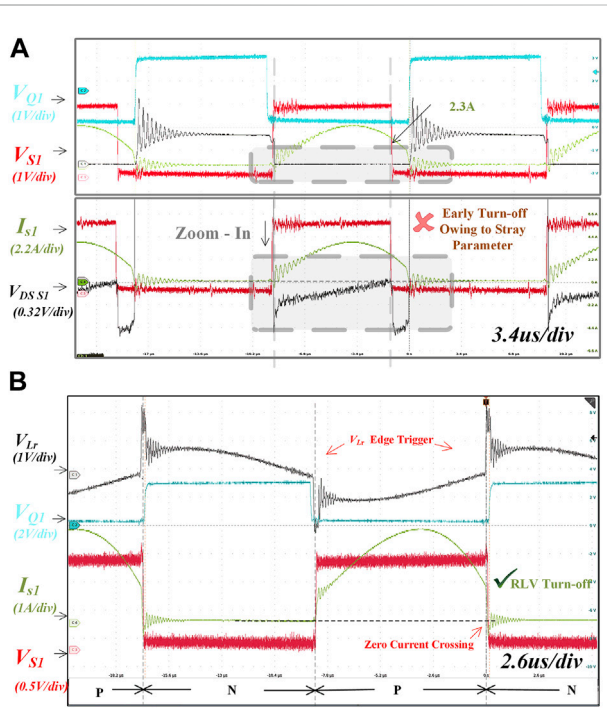

FIGURE 11
Experimental results of above resonant frequency at the maximum current, 3A/58 kHz. **(A)** The V_{DS-on} measurement method turns off the SR MOSFET early due to stray inductance causing V_{DS-S1} to reach the threshold voltage prematurely, while **(B)** the RLV strategy effectively determines the zero-current crossing point by detecting the jump edge of VLR and the operating state of the system.

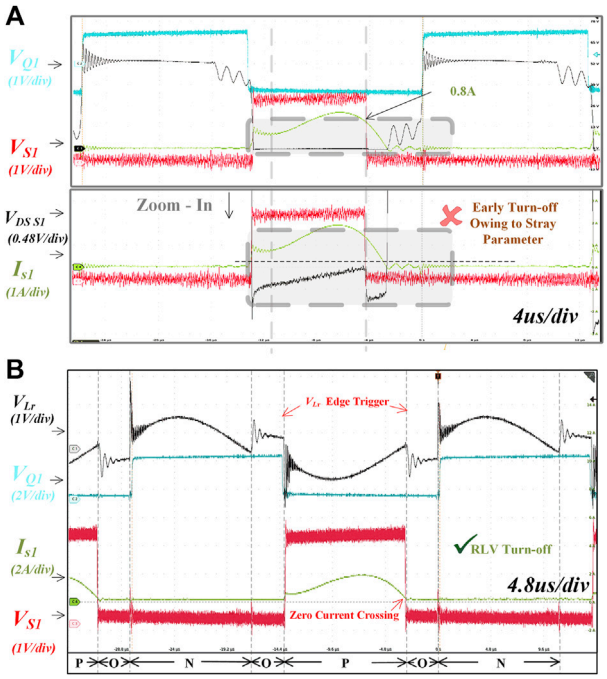

FIGURE 12
Experimental results at a light-load mode below resonant frequency, 20 W/36 kHz. **(A)** The V_{DS-on} measurement method turns off the rectifier MOSFET prematurely because the parasitic inductance causes the threshold voltage to be reached, whereas **(B)** the RLV strategy can effectively identify the switching moment of SR MOSFETs by judging the system state with large and stable *Lr* voltage signals.

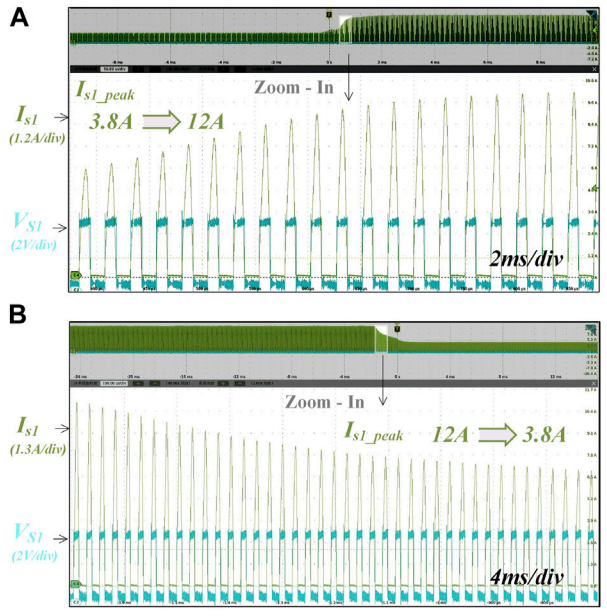

FIGURE 13
Dynamic test waveforms under a large load change: **(A)** I_{s1_peak} from 3.8 A to 12 A and **(B)** I_{s1_peak} from 12 A to 3.8 A.

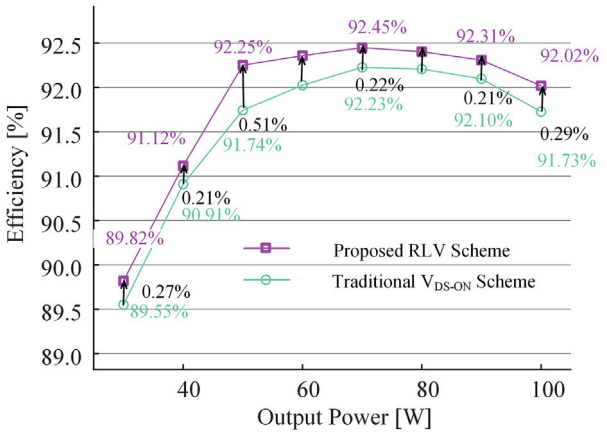

FIGURE 14
Comparison of driving scheme efficiency.

As shown in Figure 12A, the conventional V_{DS-on} sensing strategy can turn on the V_{S1} control signal when I_{S1} just crosses the zero point. However, when it comes to V_{S1} off time, due to the existence of stray inductance, premature off-time can be observed from the signal of V_{DS-S1} zoomed in the lower part of Figure 12, which is ahead of the I_{S1} signal. It is turned off when I_{S1} is 0.8A, after which the MOSFET body diode is turned on. This will miss about 20% of the on-time, which is not conducive to the improvement of system efficiency.

On the contrary, with the RLV-based strategy, the system state can be accurately judged by the magnitude and jump edge of the V_{Lr} voltage signal. As shown in Figure 12B, the on and off points of the SR signal V_{S1} are synchronized with the timing when the I_{S1} current is turned on and off.

The RLV-SR strategy tracks the actual rectifier current conduction time instantaneously under severe current dynamics. The input voltage of the experimental system is fixed. Therefore, the dynamic response results are shown while the load is changed dramatically. The results when the load condition steps up from 20 W to a load of 66 W are shown in Figure 13A. In the figure, I_{S1} represents the output current, and V_{S1} represents the driving signal of SR MOS. There are no spikes in the dynamic waveforms, which means the SRs can operate safely. To regulate the output voltage, the S1 peak current steps up from 3.8 A to 12 A. Figure 13B shows the load step-down response from 62 W to 20 W with a step-up increase in S1 peak current from 3.8 A to 12 A. The zoomed-in figure shows the waveforms after transients. It can be seen that the conducting time of SR can be tracked properly during the transients with the proposed driving scheme.

The experimental results verify that the RLV-based synchronous rectification strategy can effectively cover the operating range from below to above the resonant frequency and can also cover the working scenarios from light load to heavy load. Compared with the conventional V_{DS-on} sensing scheme, the conversion efficiency is improved by improving the accuracy of the MOSFET off time.

A comparison of the different schemes is shown in Table 3. The proposed RLV strategy does not require current sensors, which may introduce volume and cost issues. Although the proposed strategy contains one voltage sensor, it shows excellent performance in low extra power losses, low noise sensitivity, and low circuit, resulting in

TABLE 3 Comparison of different driving schemes.

Detailed group	Reference	Current sensors	Voltage sensors	Extra power losses	Noise sensitivity	Circuit complexity	SR accuracy
Model-based digital driving scheme	9–11	None	None	Low	Low	Low	Medium
Secondary-side current detection	12	Two	None	High	Low	Low	High
Primary-side current detection	13	One	None	Medium	Low	Medium	High
$V_{DS\text{-}ON}$ RC compensate circuits	14–16	None	Two	Low	High	High	Medium
$V_{DS\text{-}ON}$ adaptive control strategy	17–19	None	Two	Low	Medium	Medium	High
Integrating resonant capacitor voltage	20	None	One	Low	Low	High	High
Proposed RLV strategy		None	One	Low	Low	Low	High

high SR accuracy and high efficiency. To summarize, the proposed SR scheme achieves better performance than most of the existing SR schemes of the LLC resonant converter to some extent.

As shown in Figure 14, the converter achieves a peak efficiency of 92.45% with an improvement of 0.5% at 50 W compared to the conventional driving scheme because the current over zero point can be determined by detecting the jump edge of VLR and the operating state of the system.

4 Conclusion

In this paper, an RLV-SR strategy is proposed. This RLV-SR strategy does not use a current sensor, and the working stage of the LLC converter is judged by measuring the magnitude and jump time of the v_{Lr} signal, which is used to output the corresponding SR signals. The function and effectiveness of this strategy are verified by the experiment with a 100W/24V LLC converter.

Compared with the conventional V_{DS-on} sensing strategy, this strategy has better anti-interference performance. More importantly, the method can operate in various modes, including below and above the resonant frequency and in light-load mode. The RLV-SR driving strategy dramatically reduces the turn-on time error caused by the effect of stray inductance. So, the efficiency of the power converter is improved by 0.29% at full load.

Therefore, the RLV-SR strategy proposed in this paper is a simple and effective method to realize the synchronous rectification function of the LLC resonant converter.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material; further inquiries can be directed to the corresponding author.

Author contributions

ZL: writing—original draft and review. ZW and XQ: conceptualization. XX, XD, and QH: formal analysis and revision.

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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Current observer-based critical conduction mode control of a bidirectional DC–DC converter in battery charging/discharging applications

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A current observer-based digital critical conduction mode control of a bidirectional DC–DC converter with full-range soft switching for battery charging/discharging applications is proposed in this paper. Under the proposed control method, the bidirectional DC/DC converter operates in the critical continuous mode (CRM), the full-range zero-voltage switching (ZVS) can be achieved, and the inductor current ripple can be optimized. The CRM control is achieved by the proposed current observer, and the zero-crossing detection (ZCD) analog circuit or current sampling circuit can be eliminated. Therefore, compared with existing methods, the design complexity of the hardware circuit can be simplified. In addition, the proposed current observer can estimate the inductor current over a wide range of load and voltage variations. Therefore, the proposed control method can be applied to a wide range of charging and discharging applications. Finally, a prototype with 30–60 V input voltage, 24 V output voltage, and 75–150 kHz switching frequency is built. The experimental data and waveforms prove the correctness and advantages of the solutions proposed in this paper.

KEYWORDS

bidirectional DC–DC converter, ZVS, critical conduction mode, current observer, soft switch

1 Introduction

With the improvement of power electronics technology and energy storage, the DC microgrid has also been developed rapidly. As one of the cores, the bidirectional DC/DC converters are widely used in new energy power generation and battery charging and discharging applications (Premkumar et al, 2019; Chen et al, 2022; Lu et al, 2022; Madhana and Mani, 2022; Fang et al, 2023; Samad et al, 2023). Due to the simple circuit structure and control strategy, the bidirectional buck/boost circuit is one of the most popular DC/DC converters (Li et al., 2023; Lan et al, 2022). In order to reduce the size of the filter and improve the power density of the system, the converter needs to be operated at a higher switching frequency (Marxgut et al, 2014; Reusch and Strydom, 2015; Tao et al, 2021; Cai et al, 2022). However, under the traditional control methods, the bidirectional buck/boost converter operates in the hard switching state. The increase in switching frequency will lead to a significant increase in switching losses, and the conversion efficiency will be decreased.

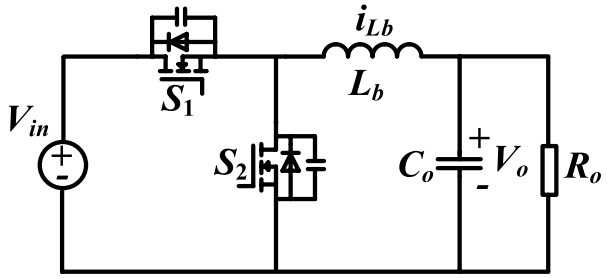

FIGURE 1
Bidirectional buck/boost converter.

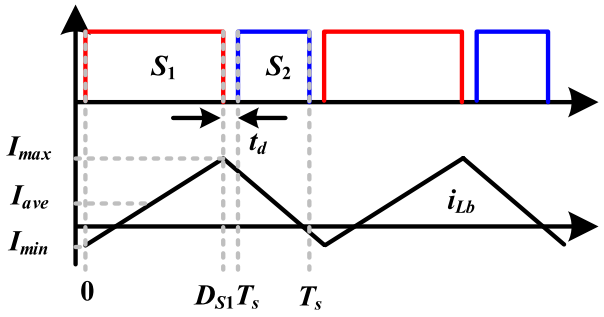

FIGURE 2
Working waveforms of the bidirectional buck/boost converter under the critical continuous mode.

Therefore, the converter topology structure and control method can be improved to optimize the conversion efficiency of the converter.

The realization of soft switching can effectively reduce switching loss and electromagnetic interference (EMI), which is helpful in improving the switching frequency of the converter. Adding an auxiliary resonant network is an effective method to achieve ZVS (Pattnaik et al, 2010; Lee, 2014; Basharat et al, 2021; Hajiheidari et al, 2021). The resonant current flows through the body diode of the MOSFET, which can reduce the drain-source voltage of the MOSFET to zero before it is turned on. Adding the auxiliary switches to achieve ZVS for the main switches is another approach (Chuang and Ke, 2008; Rodrigues et al, 2009; Chuang, 2010; Mohammadi, 2020). Although adding auxiliary devices can enable the converter to achieve soft switching, the overall complexity and volume of the circuit are increased.

In addition to the topology improvement, the optimization of control strategies is also effective. The topology of the bidirectional buck/boost converter is shown in Figure 1 (Sable et al, 1992; Deng et al, 2004; Ji et al, 2017; Sha et al, 2022). When the bidirectional buck/boost converter operates in the critical continuous mode (CRM), the inductor current will reverse during each switching cycle, and all switches can achieve ZVS (Ren et al, 2020; Wang et al, 2021). In addition, under CRM, the inductor current ripple can be minimized. In order to realize CRM control for the bidirectional buck/boost converter, the switching frequency needs to be adjusted according to different load and voltage variations. Usually, the zero-crossing detection analog circuits are used to control the turning-on and turning-off of the freewheeling MOSFET (Lai and Chen, 1993; Hu et al, 2014). In addition, there are many dedicated ZCD chips to achieve CRM control of the converter, which can further improve the integration of the converter. However, the analog detection circuits are sensitive to sampling noise, which could lead to the incorrect operation of MOSFETs. At present, digital power supply is gaining popularity, and the analog scheme will be limited. Hence, many digital CRM control strategies (Baek et al, 2013; Liu et al, 2020), which are more flexible, are proposed. Usually, in digital control, the inductor current or input and output currents need to be sampled to obtain power information, and then the optimal switching frequency is calculated according to the sampling value. Due to the simple circuit structure and computational complexity, the digital CRM control can be achieved more conveniently and flexibly. However, in the existing digital CRM control strategies, the high-precision current sensor is necessary, which is relatively expensive, and the overall volume is also increased.

A current observer-based CRM control is proposed in this paper. The traditional detection and sampling circuits are replaced by the proposed current observer. Hence, only the voltage sampling at the input and output terminals is required. The proposed solution has the following two main advantages:

1) The proposed CRM control method can achieve full-range ZVS without any current sensor or ZCD circuit. Hence, the circuit complexity and the sampling noise sensitivity are reduced.
2) The proposed current observer can accurately estimate the average value of the inductor current over a wide range of load and voltage variations, which is suitable for a wide range of charging and discharging applications.

2 Digital CRM control

2.1 Operation principle

The working principles of forward transmission and reverse transmission are similar, and the former is analyzed in detail in this paper. As shown in Figure 1, the MOSFETs S_1 and S_2 of the bidirectional buck/boost converter work in complementary conduction. The output voltage V_o can be controlled by the MOSFETs. D_{s1} is defined as the duty cycle of the upper switch S_1. The bidirectional buck/boost converter operates in the critical continuous mode. Hence, the inductor current will reverse during each switching cycle, and both S_1 and S_2 can achieve ZVS soft switching. The working waveforms of the bidirectional buck/boost converter under the critical continuous mode are shown in Figure 2.

2.2 ZVS analysis

Under CRM, the inductor current could be reversed; hence, the minimum value of filter inductor current I_{min} is lower than zero. Before S_1 conduction, all MOSFETs are turned off due to the dead time, and the filter inductor current will flow through the body diode of the MOSFET S_1. At time 0, S_1 can achieve zero-voltage soft

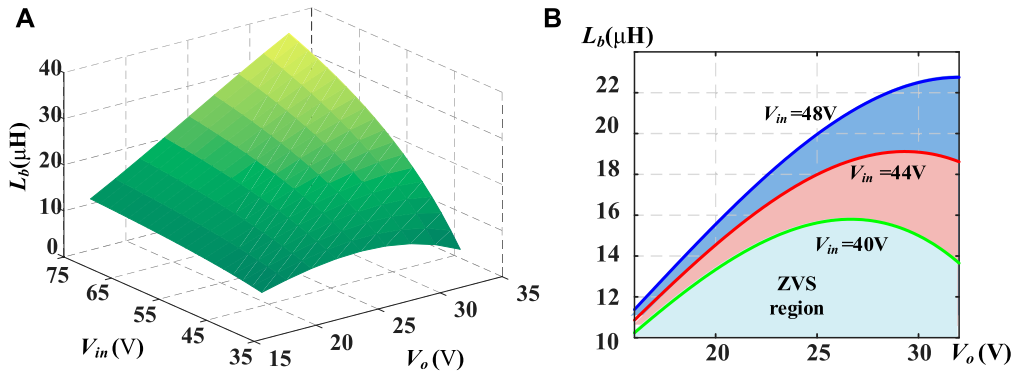

FIGURE 3
ZVS region. **(A)** Three-dimensional graph. **(B)** Two-dimensional graph.

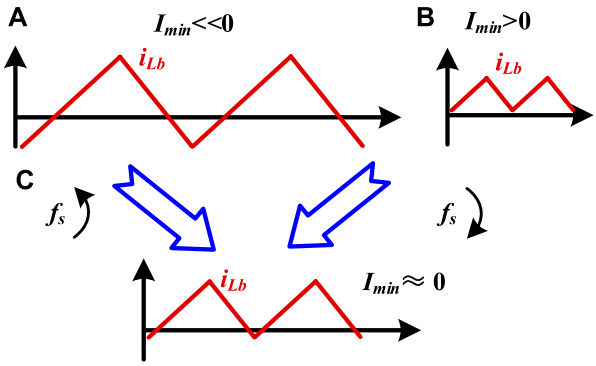

FIGURE 4
Switching frequency regulation for the critical conduction mode. **(A)** f_s is too low. **(B)** f_s is too high. **(C)** f_s is appropriate.

switching. During the duration of [0- $D_{s1}T_s$], the filter inductor current will rise to its maximum value I_{max}. After S_1 is turned off, the filter inductor current will also flow through the body diode of the MOSFET S_2. Hence, S_2 can also be turned on with ZVS.

Based on the analysis, at forward transmission, the maximum value of the filter inductor current I_{max} must be higher than zero; hence, the MOSFET S_2 must realize ZVS. However, the minimum value of the filter inductor current might be higher than zero, and S_1 might lose ZVS. Therefore, the peak-to-peak value of the filter inductor current should be twice higher than its average value:

$$I_{\max} - I_{\min} > 2I_{ave} = \frac{2P_t}{V_o}, \tag{1}$$

where P_t represents the transmission power.

In order to ensure sufficient energy to complete the charging and discharging of the MOSFET output capacitor, the valley current needs to be satisfied:

$$\frac{1}{2}L_b I_{\min}^2 > C_{oss}V_o^2, \tag{2}$$

where C_{oss} is the output capacitance of MOSFET.

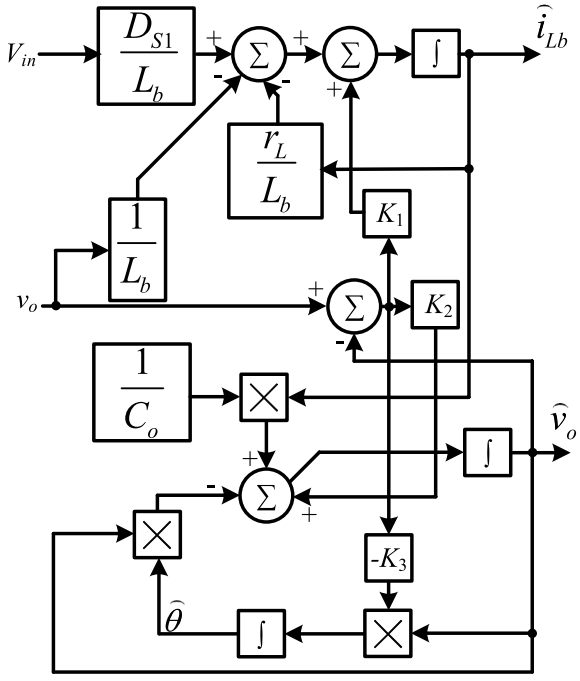

FIGURE 5
Observer block diagram.

In addition, because the dead time is relatively short, the inductor current can be approximately equivalent to a constant current source within the dead time. The dead time T_d also needs to be long enough to ensure the realization of ZVS, which can be expressed as

$$T_d > \frac{2C_{oss}V_o}{|I_{\min}|}. \tag{3}$$

According to (Eq. 1) and the voltage-second balance principle, the soft-switching condition for the MOSFET S_1 can be expressed as

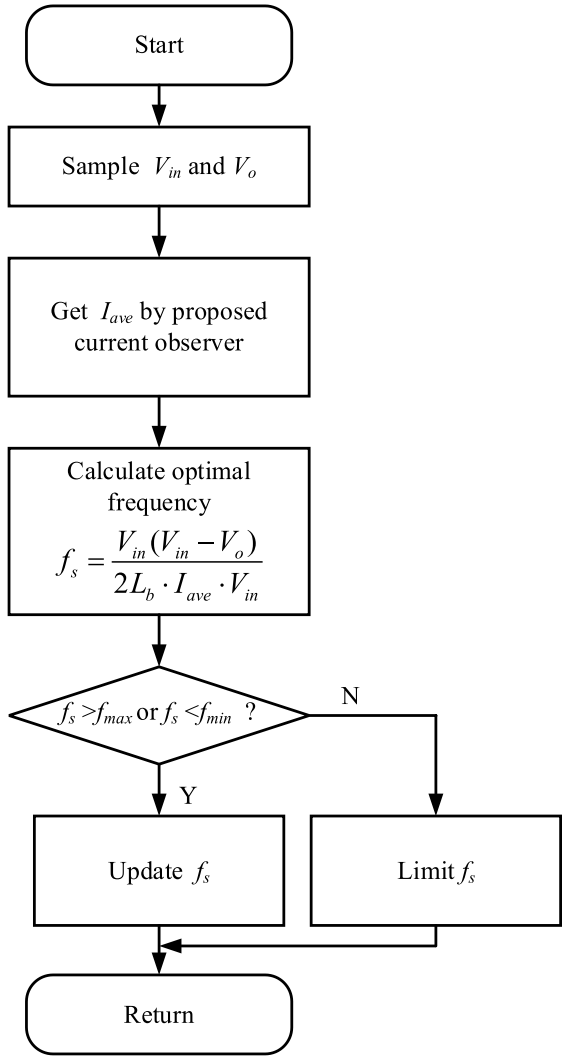

FIGURE 6
Flow chart of the current observer-based CRM control.

$$\begin{cases} i_{Lb}(t) = i_{Lb}(0) + \dfrac{V_{in}-V_o}{L_b}(t)\ (0, D_{S1}T_s), \\ i_L(t) = i_{Lb}(D_{S1}T_s) - \dfrac{v_C}{L}(t)\ (D_{S1}T_s, T_s), \end{cases} \quad (4)$$
$$\Rightarrow L_b < \frac{V_o^2(V_{in}-V_o)}{2f_s P_t V_{in}}.$$

According to (Eq. 4), it can be seen that when the transmission power and switching frequency are high, it is difficult to achieve ZVS. Therefore, the filter inductance needs to be small enough to ensure ZVS. However, a smaller filter inductance will lead to a higher circulating current and conduction loss. Therefore, it is necessary to design an appropriate filter inductance based on the working conditions, as shown in Figure 3. In order to ensure the full load range of ZVS, it is necessary to design L_b under the full load and minimum frequency. In Figure 3A, below the surface lies the ZVS region. In order to ensure the ZVS and optimize the circulating current, the inductance value can be designed as a boundary value. The 2D graph of boundary inductance values under different input voltages is shown in Figure 3B. It can be seen that when the input voltage is low, the inductance boundary value is low.

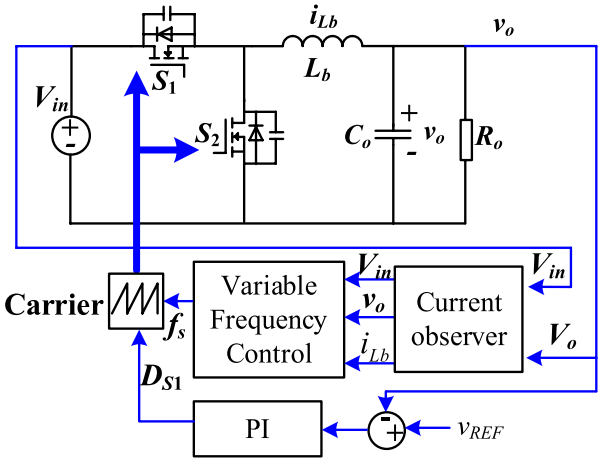

FIGURE 7
Control block diagram of the proposed method.

2.3 Control strategy

After designing the filter inductor, it is necessary to adjust the switching frequency based on the working voltage and power to achieve CRM, as shown in Figure 4. When the load is light, I_{min} will be much lower than zero, and the circulating current will be higher, so it is necessary to increase the switching frequency. On the other hand, when I_{min} is above zero, the ZVS soft switching will be lost, so the switching frequency needs to be reduced. After adjusting the switching frequency, I_{min} will be slightly below zero, and the converter will operate in the critical conduction mode.

Based on the ZVS condition (Eq. 4), the optimal switching frequency for CRM operation can be derived as

$$f_s == \frac{V_o(V_{in}-V_o)}{2L_b \cdot I_{ave} \cdot V_{in}}. \quad (5)$$

According to (Eq. 5), it can be seen that in order to adjust the switching frequency, it is necessary to sample the input and output voltages and the average value of the filter inductor current. However, high-precision current sensors and sampling circuits are usually more expensive. Therefore, this paper proposes a CRM control method based on the current observer, which can save current sensors and reduce hardware circuit complexity.

3 Current observer-based method

3.1 Inductor current observer

In order to observe the inductance current in a wide load range, a load adaptive current observer needs to be designed. The state

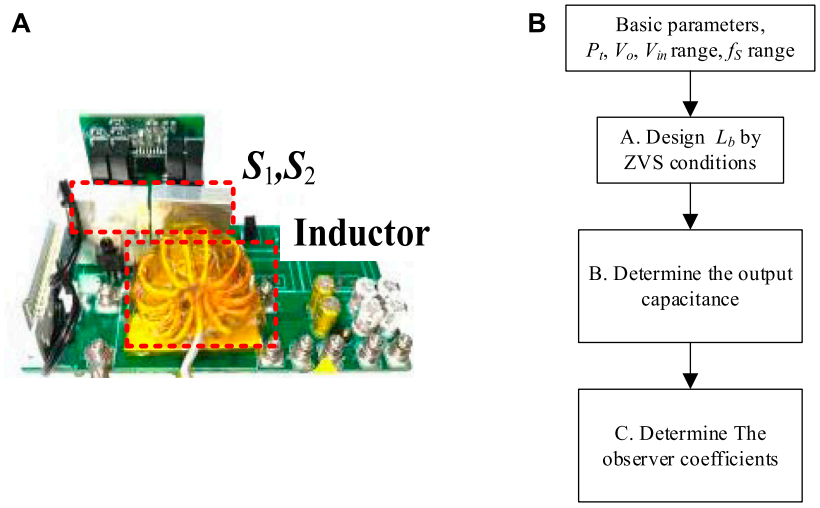

FIGURE 8
Experimental prototype and design process. **(A)** Photograph of the prototype. **(B)** Parameter design process.

TABLE 1 Specific parameters.

Parameter	Value
Input (V_{in})	30–60 V
Output (V_o)	24 V
Rated power	100 W
Filter inductance (L_b)	10 μH
Output capacitance (C_o)	100 μF
Switching frequency (f_s)	50–150 kHz
g_1	−90000
g_2	20000
g_3	10000

equation of the switching average model for the bidirectional buck/boost converter can be expressed as

$$\begin{bmatrix} i'_{Lb} \\ V'_o \end{bmatrix} = \begin{bmatrix} -r_L/L_b & -1/L_b \\ 1/C_o & -1/(R_oC_o) \end{bmatrix} \begin{bmatrix} i_{Lb} \\ V_o \end{bmatrix} + \begin{bmatrix} V_{in}/L_b \\ 0 \end{bmatrix} D_{S1}, \quad (6)$$

where r_L is the parasitic resistor of the filter inductor.

The designed current observer can be expressed as

$$\begin{cases} \hat{i}'_{Lb} = \dfrac{V_{in}}{L} \cdot D_{S1} - \dfrac{r_L}{L_b}\hat{i}_{Lb} - \dfrac{\hat{v}_o}{L_b} + g_1\left(v_o - \hat{v}_o\right), \\ \hat{v}'_o = \dfrac{\hat{i}_{Lb}}{C_o} - \hat{\theta}\hat{v}_o + g_2\left(v_o - \hat{v}_o\right), \\ \hat{\theta} = \dfrac{1}{\hat{R}_oC_o}, \end{cases} \quad (7)$$

where $g_{n(n=1,2,3)}$ is the observer coefficient.

The error of the observed variables can be expressed as

$$\begin{cases} \tilde{i}_{Lb} = i_{Lb} - \hat{i}_{Lb}, \\ \tilde{v}_o = v_o - \hat{v}_o, \\ \tilde{\theta} = \theta - \hat{\theta}. \end{cases} \quad (8)$$

Substituting formula (6) and Eq. 8 into formula (8), the state equation of the observation variables error can be expressed as

$$\begin{cases} \tilde{i}'_{Lb} = -\dfrac{r_L}{L_b}\tilde{i}_{Lb} - \dfrac{\tilde{v}_o}{L_b} + g_1\tilde{v}_o, \\ \tilde{v}'_o = \dfrac{\tilde{i}_{Lb}}{C_o} - \theta\tilde{v}_o - \tilde{\theta}\hat{v}_o - g_2\tilde{v}_o. \end{cases} \quad (9)$$

The Lyapunov function for observed variable errors can be written as

$$V = \frac{1}{2}\tilde{i}_{Lb}^{\,2} + \frac{1}{2}\tilde{v}_o^{\,2} + \frac{1}{2g_3}\tilde{\theta}^2. \quad (10)$$

The derivative of function (Eq. 10) can be derived as

$$V' = \left(\frac{1}{C_o} - \frac{1}{L_b} - g_1\right)\tilde{v}_o\tilde{i}_{Lb} - \frac{r_L}{C_o}\tilde{i}_{Lb}^{\,2} - \theta\tilde{v}_o^{\,2} - g_2\tilde{v}_o^{\,2} + \left(\frac{1}{g_3}\tilde{\theta}' - \tilde{v}_o\hat{v}_o\right)\tilde{\theta}. \quad (11)$$

In order to stabilize the observer, formula (11) must converge to zero. Therefore, the designed observer coefficients can be derived as

$$\begin{cases} g_1 = \dfrac{1}{C_o} - \dfrac{1}{L_b}, \\ g_2 > 0, \\ \hat{\theta}' = -g_3\tilde{v}_o\hat{v}_o. \end{cases} \quad (12)$$

Finally, the designed filter inductor current observer can be expressed as

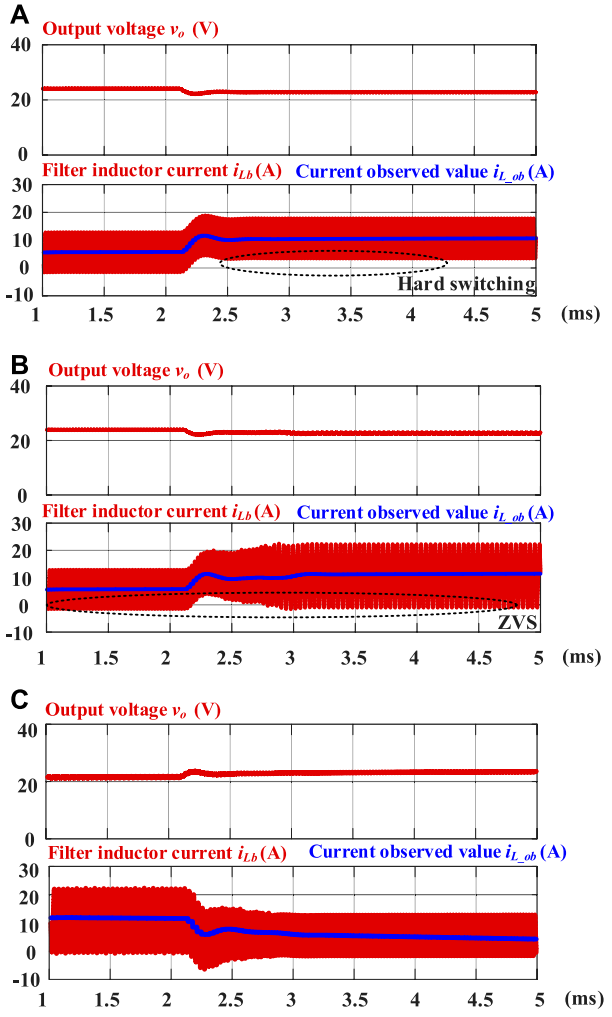

FIGURE 9
Comparison of simulation waveforms. **(A)** Fixed frequency control. **(B)** Proposed CRM control (half load to full load). **(C)** Proposed CRM control (full load to half load).

$$\begin{cases} \hat{i}'_{Lb} = \dfrac{V_{in}}{L_b} \cdot D_{S1} - \dfrac{r_L}{L_b}\hat{i}_{Lb} - \dfrac{\hat{v}_o}{L_b}, \\ \quad + \left(\dfrac{1}{C_o} - \dfrac{1}{L_b}\right)\left(v_o - \hat{v}_o\right), \\ \hat{v}'_o = \dfrac{\hat{i}_{Lb}}{C_o} - \hat{\theta}\hat{v}_o + g_2\left(v_o - \hat{v}_o\right), \\ \hat{\theta}' = -g_3\left(v_o - \hat{v}_o\right)\hat{v}_o. \end{cases} \tag{13}$$

According to (14), the observer block diagram can be drawn as shown in Figure 5. Only the input voltage and output voltage need to be sampled. g_1, g_2, and g_3 are parameters of the observer, which can be designed according to (Eq. 12). In the proposed observer, besides the observation equations of output capacitor voltage v_o and inductance current i_{Lb}, there is also the observation equation of load θ. The proposed observer can adaptively observe the filter inductor current average value when the load varies in a wide range.

3.2 Proposed control strategy

After the filter inductor current is observed, according to the CRM working conditions, the optimal inductor current ripple can be calculated, which is approximately equal to $2I_{ave}$. Therefore, the optimal switching frequency can also be calculated.

The flow chart of the proposed CRM control is shown in Figure 6, which mainly includes the following three steps:

1) V_{in} and V_o are obtained through the voltage sensor.
2) Based on the designed current observer, I_{ave} can be obtained.
3) The switch frequency is adjusted according to formula (5).

The proposed CRM control method does not require a current sensor. The method proposed in this paper is cost-effective and easy to achieve because of the absence of ZCD or a current sensor.

The control block diagram is depicted in Figure 7. The converter adopts the traditional single-voltage loop PI control to control the output voltage constant. The proposed observer is applied to estimate the filter inductor current. Finally, f_s can be derived from the proposed CRM control strategy. Under the proposed control strategy, the full range ZVS and the lowest current ripple can be realized.

4 Simulation and experimental results

To prove the availability and practicability of the proposed method, a simulation model and experimental prototype with 30 V–60 V input voltage, 24 V output voltage, and 75 kHz–150 kHz switching frequency is established, as shown in Figure 8A. The parameter design process is shown in Figure 8B. First, the basic circuit parameters, such as P_t, V_o, V_{in} range, and f_S range, need to be determined. Then, based on the ZVS condition, the filter inductance value can be determined. Furthermore, based on the output voltage ripple coefficient, the output capacitance can be determined. Finally, the observer coefficients can be calculated. The specific parameters are shown in Table 1.

A comparison of the simulation waveforms of fixed frequency control and the proposed control strategy is shown in Figure 9. It follows that the designed current observer can accurately estimate the average inductance current during load switching. Under traditional fixed switching frequency control, the filter inductor current average value increases as the load increases. Due to the fixed switching frequency, the inductor current ripple is also constant. When the minimum value of the filter inductor current is greater than zero, the converter will operate in a hard switching state, so the switching loss increases and the conversion efficiency decreases. Under the proposed CRM control, the switching frequency will be adaptively modified in accordance with the operating conditions, ensuring the implementation of ZVS soft switching and achieving the lowest current ripple.

The steady-state experimental waveforms under half- and full-load are depicted in Figure 10. When the input voltage changes, the duty cycle will change accordingly to control the constant output voltage. In addition, under the proposed CRM control, when the load and working voltage change, the switching frequency will be adaptively adjusted, which is the basis of the implementation of ZVS

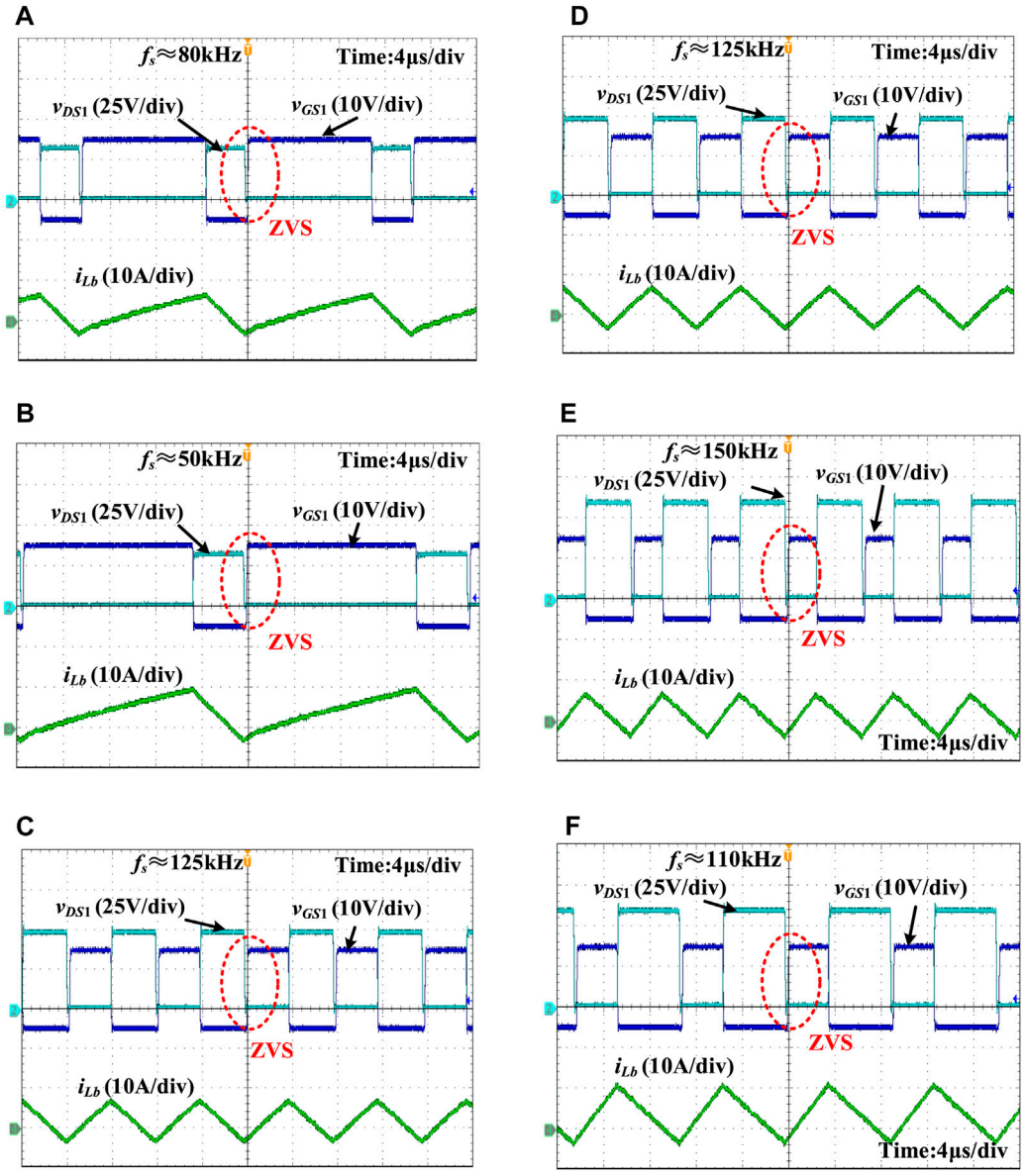

FIGURE 10
Steady-state waveforms. **(A)** Input 30 V, half load. **(B)** Input 30 V, full load. **(C)** Input 48 V, half load. **(D)** Input 48 V, full load. **(E)** Input 60 V, half load. **(F)** Input 60 V, full load.

and optimization of the current ripple. Because S_2 is the synchronous rectifier MOSFET and can certainly achieve ZVS, only the ZVS waveforms of S_1 are shown. These waveforms set forth the important fact that the drain-source voltage of MOSFET has been decreased to zero before it is turned on. According to the ZVS analysis, ZVS is difficult to achieve under full load and easy to achieve under light load. Therefore, according to the experimental results, we can conclude that the proposed control method can achieve full-range ZVS.

The load-changing dynamic experimental waveforms are shown in Figures 11A, B. If the load steps from full to half load, the switching frequency increases rapidly to achieve ZVS and minimize the current ripple. Similarly, if the load steps from half to full load, the switching frequency decreases rapidly and soft switching is always ensured. The dynamic experimental waveforms of input voltage change are displayed in Figures 11C, D. When the input voltage changes, the output voltage can always be clamped at 24 V. Therefore, under the proposed CRM control, the bidirectional buck/boost converter has good dynamic performance. The experimental results demonstrated the proposed CRM control to be effective.

The measurement efficiency comparison between the traditional fixed frequency (FF) control and the proposed CRM control is shown in Figure 12. Under the fixed frequency control, the switching frequency is always equal to 100 kHz. It can be seen that under the same operating conditions, the conversion efficiency of the proposed CRM control strategy is higher than that of the traditional fixed frequency control.

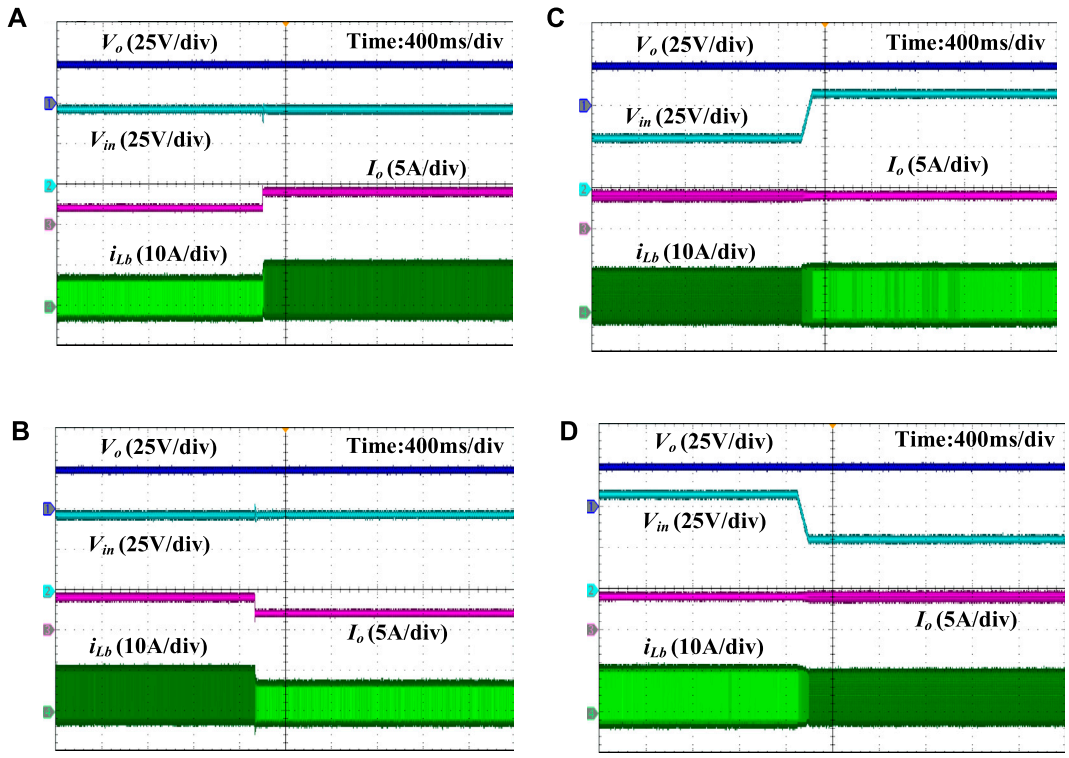

FIGURE 11
Dynamic waveforms. **(A)** Half to full load. **(B)** Full to half load. **(C)** 30 V–60 V. **(D)** 60 V–30 V.

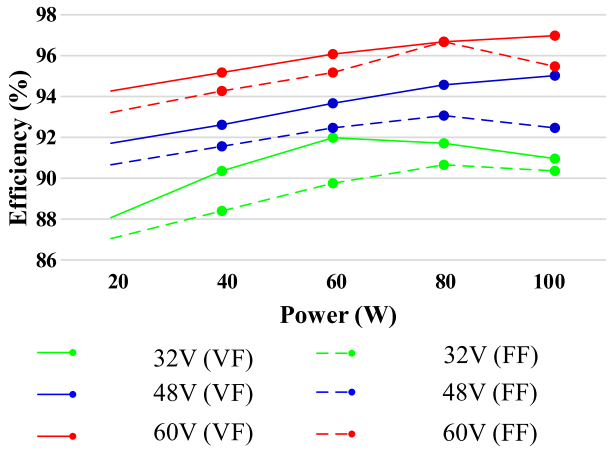

FIGURE 12
Measurement efficiency curve.

5 Conclusion

A current observer-based digital critical conduction mode control of a bidirectional DC–DC converter with full-range soft switching is explored in this paper. The bidirectional DC/DC converter works in the CRM mode, and full-range ZVS and optimal current ripple can be achieved. The proposed CRM control is achieved by the designed current observer without any ZCD circuit or current sensors. In addition, the proposed current observer can estimate the inductor current over a wide range of load and voltage variations. Therefore, the proposed control method can be applied to a wide range of charging and discharging applications. Finally, a prototype is built, and the simulation and experimental results prove the correctness and advantages of the proposed method.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material; further inquiries can be directed to the corresponding author.

Author contributions

All authors listed have made a substantial, direct, and intellectual contribution to the work and approved it for publication.

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Conflict of interest

Authors DW and LL were employed by the company Country State Grid Hunan Electric Power Company Limited Research Institute.

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The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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Topology and control strategy optimization of an auxiliary resonant commutated pole-based, soft-switching grid-connected inverter

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With the development of new energy industries such as photovoltaics, microgrids, or distributed energy sources require many DC-AC grid-connected interfaces. Reducing the switching loss of the inverter is important to improve the transmission efficiency of the inverter, reduce the heat generation of the inverter, promote the high frequency and miniaturization of the inverter, and efficiently use the distributed energy. Therefore, considering the wide application of DC-AC power electronic interfaces in microgrid and distributed energy, and to make up for existing deficiencies in traditional hard-switching inverters, an optimal control strategy and topology for an optimal-auxiliary resonant commutated pole (O-ARCP) inverter is proposed in this article. Firstly, this paper introduces the proposed inverter topology and analyzes the operation mode of the circuit with the control strategy. Then simulation experiments in islanding mode are carried out to verify the rationality of the content, and finally simplified experimental verification is carried out based on the simulation results. Simulation and experimental testing reveal that all switches of the proposed topology are in soft-switching mode, which proves the effectiveness of the proposed control strategy and analysis. The analysis and validation of this paper provide assistance in the development of control strategies and structures for soft-switching inverters.

KEYWORDS

inverter, auxiliary resonant commutated pole, soft switching, zero voltage switching, zero current switching

1 Introduction

The development of renewable energy can effectively reduce dependence on fossil fuels and environmental pollution. As a result, distributed energy sources such as photovoltaic power, wind power, and hydropower have been developing rapidly.

Many distributed energy sources can be efficiently arranged and managed when they are connected to a microgrid in a uniform manner. Therefore, the development of microgrids can help reduce carbon emissions, improve the utilization of clean energy, and solve the problem of local consumption of renewable energy. However, the large amount of distributed energy access requires more efficient power electronic interfaces, of which DC-AC power electronic converters are an important component. Further reducing the loss of the DC-AC converter and ensuring its efficient and stable operation is a key issue.

The conventional hard-switching inverter has a dramatic increase in switching losses as the pulse width modulation (PWM) frequency rises, and soft-switching techniques have been developed to reduce the losses caused by the increase in switching frequency (Zhang et al., 2010; Li and Xu, 2013; Mishima et al., 2013; Li, 2015; Pal A and Basu K. A, 2018; Samani et al., 2018).

The earliest soft-switching inverter is the resonant DC-link inverter proposed by Divan (1989), which was epoch-making for soft-switching inverter technology development. This topology is very simple, and only one set of LC devices is required to make the whole circuit work in soft-switching mode. However, it also has a very clear drawback: when resonance occurs, the DC bus voltage's resonant peak is too high, significantly increasing the stress on the bus voltage. Active clamped resonant DC-link inverters are proposed to solve this problem. Moreover, many new solutions have been proposed in recent years for resonant losses and control techniques (Divan and Skibinski, 1989; Deshpande et al., 1997; Jafar and Fernandes, 2002; Gurunathan and Bhat, 2007; Amirabadi et al., 2014).

Some scholars have proposed a parallel resonant DC link inverter to replace the resonant DC link resonant inductor connected in series among the bus power, where the resonant inductor is connected in parallel among the power channels. This structure bus voltage stress is not higher than the DC voltage, and the inverter can use PWM modulation. However, frequent bus voltage over zero can affect the efficiency of soft switching (Chibani and Nakaoka, 1992; Hui et al., 1996; Chen, 1998; De Andrade et al., 2001; Behera et al., 2004; Pan and Luo, 2004; Pan and Luo, 2005; Mandrek and Chrzan, 2007; Kedarisetti and Mutschler, 2011; Wang et al., 2014).

The auxiliary resonant commutated pole (ARCP) inverter was proposed in 1989 with bus voltage not periodically resonating to zero. The auxiliary circuit only works at the moment of current change, with little loss to itself and low loss to the circuit. This approach is the best choice to achieve efficient soft switching under high power, but the voltage of the midpoint capacitor is not easy to stabilize due to the use of voltage-dividing capacitors. Subsequent scholars have proposed many improvement strategies.

Cai et al. (2019) proposed a novel ARCP inverter that achieved good results by replacing the position of the midpoint capacitor with a switching device.

Chu et al. (2014) and Chu et al. (2016) also utilized switching devices for current conversion, but too many auxiliary devices increase the losses.

Other studies (Yu et al., 2009; Chu et al., 2014; Chu et al., 2019; Wang and Wang, 2020; Chu et al., 2022) do not use a midpoint capacitor for current conversion, but their control strategy has an auxiliary circuit operating at both dead times within a single PWM cycle, which leads to an increase in losses.

The DC-AC power electronic converter interface assumes an important role in grid-connected or off-grid microgrids. The overall efficiency of the inverter cannot be improved due to the switching losses during the transmission of the DC-AC power electronic converter, and there are problems such as limited switching frequency, oversized filters, and heat generation. A new soft-switching topology of the auxiliary resonant commutation stage is proposed to address the switching losses in the transmission process of the grid-connected inverter. The control strategy and topology are simplified to address the complex control problem of the traditional soft-switching topology. The soft-switching process only occurs in the dead time of the inverter, and only half of the auxiliary switches are required to work every half cycle to make the inverter work in the soft-switching mode. Based on this topology, the switching losses of the grid-connected inverter can be reduced, the conversion efficiency of the inverter can be improved, and the inverter can be operated at a higher frequency to reduce the harmonics.

2 Materials and methods

2.1 Introduction to auxiliary circuits

The soft-switching topology is shown in Figure 1. One of the phases is used as a reference to analyze its operating principle, and its equivalent circuit diagram is shown in Figure 1B.

The auxiliary circuit consists of switching S_1 and S_4, resonant capacitors C_1, C_2, and C_3, auxiliary diodes D_5–D_{10}, and resonant inductors L_1–L_4.

L_1, D_7, and C_3 provide the ZCS turn-on condition for S_2. C_3 provides the ZVS turn-off condition for S_2. L_2 and C_1 provide the ZCS turn-on and ZVS turn-off conditions for S_1.

C_3 and L_3 provide the ZCS turn-on condition for S_3. C_3 provides the ZVS turn-off condition for S_3. L_4 and C_2 provide the soft-switching condition for S_4.

2.2 Basic working principle

To facilitate the analysis of the entire circuit structure, the article takes one of the three equivalent phases for analysis. The topological circuit divides the circuit into two time periods with positive and negative load current directions, respectively. Its switching equivalent control schematic representation and partial voltage and current are shown in Figure 2.

Figure 2A includes the $S_1 - S_4$ switching operation mode when the load current direction is positive during the time period of $t_0 - t_4$, the change in inductor current i_L flowing through the auxiliary inductor L_1, and the change in voltage U_{c3} across the auxiliary capacitor C_3.

Figure 2B includes the S_1–S_4 switching operation mode when the load current direction is negative during the t_5–t_9 time period, the change in inductor current i_L flowing through the auxiliary inductor L_3, and the change in voltage U_{c3} across the auxiliary capacitor C_3.

Where the signal is high level, S_1–S_4 represents the switch turn-on state; when the signal is low level, S_1–S_4 represents the turn-off state. For S_2, S_3, each drive interval has a certain dead time to turn on the auxiliary circuit to achieve the effect of soft switching.

As can be seen from Figure 2, under the control strategy proposed in this paper, only switch S1 is required to work when the load current direction is positive to achieve the soft-switching effect. Similarly, only switch S4 is required to work when the load current direction is negative. Compared with the control strategy proposed by Chu et al. (2016), the additional losses due to the need to turn on S1 and S4 alternately for each PWM cycle are greatly reduced. Compared to the control strategy in this paper, Chu et al. (2014) required multiple auxiliary switches to work alternately, which both complicates the control strategy and adds additional losses.

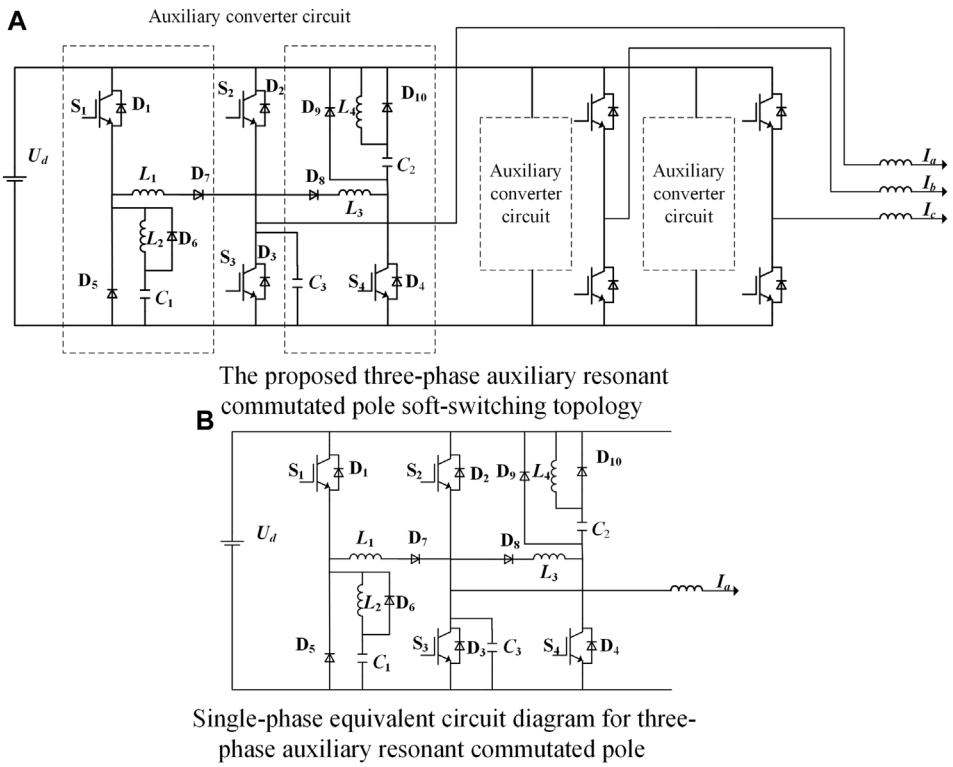

FIGURE 1
Topology schematic representation. **(A)** Three-phase circuit diagram; **(B)** single-phase equivalent schematic representation.

An analysis of the circuit yields the equivalent circuit diagram shown in Figure 3.

2.3 Operation mode with positive load current

When the load current direction is positive, the current mainly flows through switch S_2 only when a group of auxiliary components corresponding to S_1 is in working condition.

The operating mode is divided into five operating time periods, and, assuming it is in an ideal state, the principle of the circuit is analyzed as follows:

Mode t_0: At this stage, switch S_2 is turned on, the auxiliary circuit does not work, and the load current flows from switch S_2 to the load.

Mode t_1: Switch S_3 is in the off state at this stage. When switch S_2 needs to be turned off, the voltage across container C_3 does not change suddenly, the magnitude of the voltage across capacitor C_3 is still the bus voltage, and the U_{C3} voltage drops to zero after a period of time. The voltage across switch S_2 is zero. Therefore, switch S_2 is the ZVS turn-off. When switch S_2 needs to be turned on, the auxiliary circuit needs to work to provide the ZVS turn-on condition for S_2.

At this time, the voltage across U_{c3} decreases linearly, as shown in the following equation:

$$\boldsymbol{U_{c3} = U_d - U_d t},$$

where U_d is the busbar voltage.

Mode t_2: S_3 is turned on at this stage. Because the capacitive voltage across U_{c3} has been reduced to zero in mode t_1, S_3 is the ZVS turn-on.

Mode t_3: S_1 turns on, and the resonant current i_{L1} begins to rise nonlinearly. Because L_1 and L_2 will obstruct the instantaneous current, the auxiliary switch S_1 is the ZCS turn-on. When the resonant current reaches the value of the load current, the resonant current i_{L1} is in the constant current stage. The voltage at both ends of capacitor U_{c3} starts to rise. When it reaches the bus voltage, diode D_2 conducts, so S_2 is the ZVS turn-on. At the same time, part of the current flows through L_2 and C_1, and the voltage across C_1 begins to rise in preparation for the ZVS turn-off of S_1.

The relevant changes are analyzed as shown in the following equations. The current i_{L1} flowing through L_1 is shown in the following equation:

$$\boldsymbol{i_{L1}(t) = \frac{U_d}{Z_r} sin\omega t + I_a.}$$

The current i_{L2} flowing through L_2 is analyzed as shown in the following equation:

$$\boldsymbol{i_{L2}(t) = \frac{U_d}{Z_1} sin\, \omega_1 t.}$$

The maximum current I_{s1max} flowing through S_1 is shown in the following equation:

$$\boldsymbol{I_{s1\,max}(t) = i_{L1}(t) + i_{L2}(t).}$$

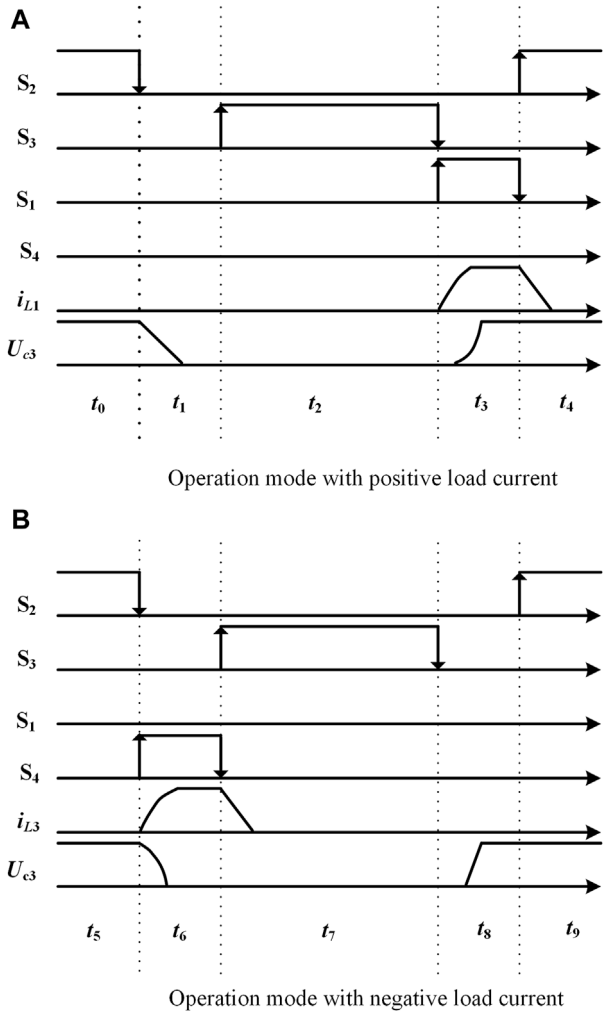

FIGURE 2
Switching control strategy and main waveforms for positive and negative load current directions. **(A)** Operation mode with positive load current; **(B)** Operation mode with negative load current.

The change in voltage across C_1, C_3 is shown in the following equation:

$$U_{c3} = U_d\,(1 - cos\omega t),$$

where $\omega = 1/\sqrt{L_1C_3}$, $Z_r = \sqrt{L_1/C_3}$, $\omega_1 = 1/\sqrt{L_2C_1}$, $Z_1 = \sqrt{L_2/C_1}$, and I_a is the load current.

Mode t_4: When the voltage across C_1 reaches the bus voltage, the voltage across C_1 does not rise due to the clamp effect of diode D_6. When S1 needs to be turned off, the voltage across S_1 is zero due to the presence of capacitor C_1. Therefore, the S_1 turn-off belongs to the ZVS turn-off. When S_1 is turned off, the resonant current i_{L1} decreases at a linear rate.

2.4 Operation mode with negative load current

When the load current direction is negative, it is divided into five action time zones according to the action time sequence, and, assuming that the circuit is in an ideal state, the corresponding time range in Figures 2, 3 is the t_5–t_9 time period, which is analyzed as follows.

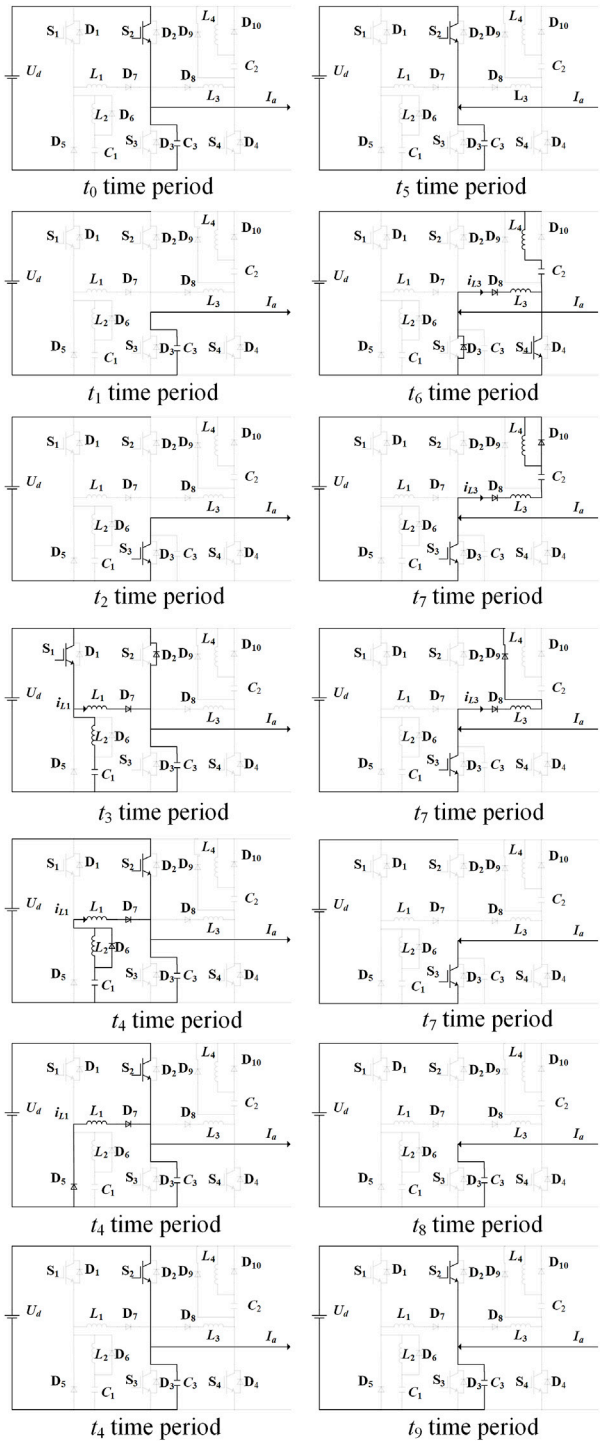

FIGURE 3
Equivalent circuits in different operating modes.

Mode t_5: At this time, switch S_2 remains on, but the load current direction is negative.

Mode t_6: S_4 turns on, and the resonant current i_{L3} begins to rise nonlinearly. Because L_3 and L_4 will obstruct the instantaneous current, the auxiliary switch S_4 is the ZCS turn-on. The

TABLE 1 Simulation parameters of the three-phase ARCP inverter.

Component	Parameter
Output power	1 kW
DC voltage supply (U_d)	200 V
Switching frequency	10 kHz
Output frequency	50 Hz
Dead time	1 μs
L_1, L_3	8 μH
L_2, L_4	1 μH
C_1, C_2	100 pF
C_3	10 nF

capacitance voltage U_{c3} begins to decrease until the D_3 begins to conduct. At this time, the capacitance voltage across C_2 begins to rise in preparation for the ZVS turn-off of S_4.

At this time, the current i_{L3} flowing through the inductor L_3 changes, as shown in the following equation:

$$i_{L3}(t) = \frac{U_d}{L_3} sin\, \omega_2 t.$$

The current i_{L4} flowing through inductor L_4 changes as shown in the following equation:

$$i_{L4}(t) = \frac{U_d}{\sqrt{L_4/C_2}} sin\, \omega_3 t.$$

The current I_{s4} flowing through switch S_4 changes as shown in the following equation:

$$I_{s4} = i_{L3}(t) + I_a + i_{L4}(t).$$

The voltage across the capacitor C_3 changes as shown in the following equation:

$$U_{c3}(t) = U_d \cos \omega_2 t.$$

Here, $w_2 = 1/\sqrt{L_3C_3}$, $w_3 = 1/\sqrt{L_4C_2}$, I_a is the load output current, and U_d is the busbar voltage.

Mode t_7: At this time, the S_3 anti-parallel diode has been on, and the switch S_3 should be turned on at this time. Therefore, the switch S_3 is the ZVS turn-on. Because the voltage at both ends of C_2 is the bus voltage, the voltage at both ends of switch S_4 is zero, and S_4 meets the condition of the ZVS turn-off. With the closing of S_4, the energy stored in C_2, L_3, and L_4 is released back to the bus.

Mode t_8: When the switch S_3 turns off, the voltage across the capacitor C_3 cannot change abruptly. Therefore, switch S_3 reaches the condition for the ZVS turn-off.

Mode t_9: Because C_2 has stored enough energy before S_2 turns on, the voltage across S_2 is zero to meet the condition of the ZVS turn-on. Then, S_2 turns on and enters a new cycle.

3 Simulation data and analysis of an O-ARCP DC-AC power electronic converter in islanding mode

To verify the correctness of the analysis, the proposed three-phase ARCP inverter topology is simulated using MATLAB simulation software. Because some parameters of the three-phase circuit are the same, only one-phase parameters are listed.

The simulation parameters are shown in Table 1.

3.1 Parameter design when the load current direction is positive

3.1.1 Design of resonant inductor and resonant capacitor

The design of the L_1 and C_3 parameters depends on the resonant frequency f_r and the maximum load current I_{omax}, which must first be satisfied to achieve soft switching.

$$\frac{U_d}{Z_r} < I_{omax}.$$

Namely,

$$Z_r > \frac{U_d}{I_{omax}}.$$

The equation can be rewritten as follows:

$$Z_r = K\frac{U_d}{I_{omax}},$$

where K > 1, and the resonance duration period is defined by

$$T_r = \frac{1}{f_r} = 2\pi\sqrt{L_1C_3}.$$

The auxiliary switch opening time cannot be less than t. t can be determined by the following equation:

$$t = \frac{1}{4}T_r = \frac{\pi}{2}\sqrt{L_1C_3}.$$

Meanwhile, the duration of t should satisfy

$$t < t_{dead},$$

where t_{dead} is the dead time to prevent the upper and lower bridge arms from conducting at the same time.

Combining the aforementioned equations yields

$$t = K_1 t_{dead} = \frac{\pi}{2}\sqrt{L_1C_3},$$

where $K_1 < 1$. It can be concluded that

$$C_3 = \frac{I_{omax}}{KU_d} \cdot 2K_1\frac{t_{dead}}{\pi},$$

$$L_1 = \frac{KU_d}{I_{omax}} \cdot 2K_1\frac{t_{dead}}{\pi},$$

where $K_1 < 1$ and $K > 1$.

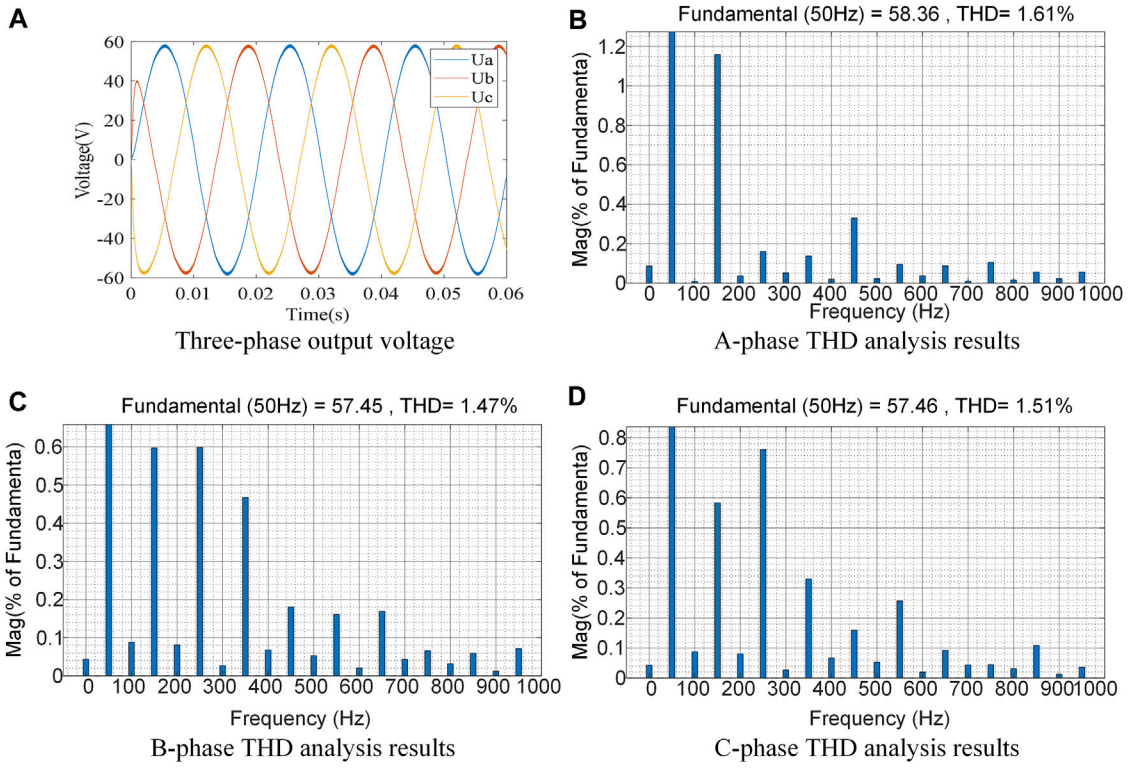

FIGURE 4
Output three-phase voltage waveform and THD analysis results. **(A)** Three-phase output voltage; **(B)** A-phase THD analysis results; **(C)** B-phase THD analysis results; **(D)** C-phase THD analysis results.

3.1.2 Parameter design of C1, L2

This phase has a small resonance duration, so only $t_1 < t$ needs to be satisfied.

$$t_1 = \frac{\pi}{2}\sqrt{L_2 C_2}.$$

Its peak resonant current can be given by

$$i_{L2} = \frac{U_d}{\sqrt{L_2/C_2}}.$$

The design should satisfy $i_{L2} < i_{L1}$ in order to reduce losses and current stress.

Therefore, it is obtained that

$$t_1 = K_2 t = K_2 \frac{\pi}{2}\sqrt{L_1 C_3},$$

$$i_{L2} = K_3 i_{L1} = K_3\left(\frac{U_d}{Z_r} sin\omega t + I_a\right),$$

where $K_2 < 1$ and $K_3 < 1$.

To simplify the design, i_{L1} can be simplified. This yields

$$L_2 = \frac{K_2}{K_3}L_1,$$

$$C_1 = K_2 K_3 C_3.$$

3.2 Parameter design when the load current direction is negative

The analysis process is the same as when the load current direction is positive.

$$L_3 = \frac{KU_d}{I_{omax}} \cdot 2K_1 \frac{t_{dead}}{\pi},$$

$$L_4 = \frac{K_2}{K_3}L_3,$$

$$C_2 = K_2 K_3 C_3.$$

3.3 Simulation verification

The output three-phase voltage and its harmonic analysis are shown in Figure 4.

Figure 4A shows the output three-phase voltages, Figure 4B shows the results of the A-phase total harmonic distortion (THD) analysis with a value size of 1.61%, Figure 4C shows the results of the B-phase THD analysis with a value size of 1.47%, and Figure 4D shows the results of the C-phase THD analysis with a value size of 1.51%, which is not significantly different from the experimental tests in Section 4 and meets the design expectations.

Figure 5 shows the simulation diagram of the operation mode with positive load current direction, where the first picture shows

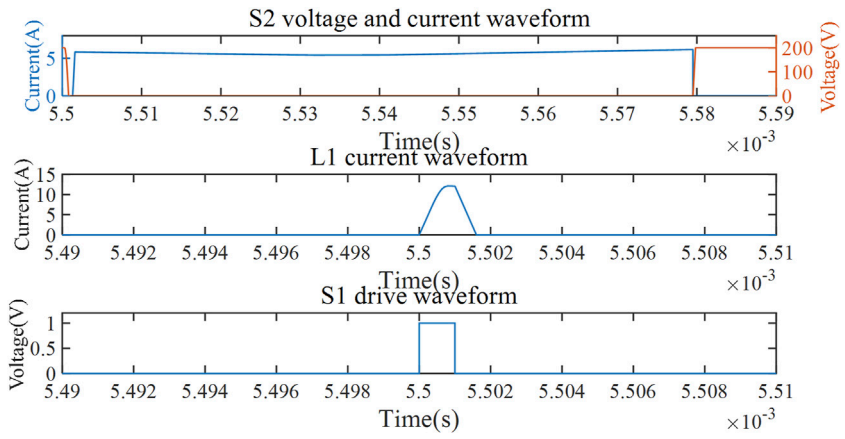

FIGURE 5
Key waveform with a positive load current direction.

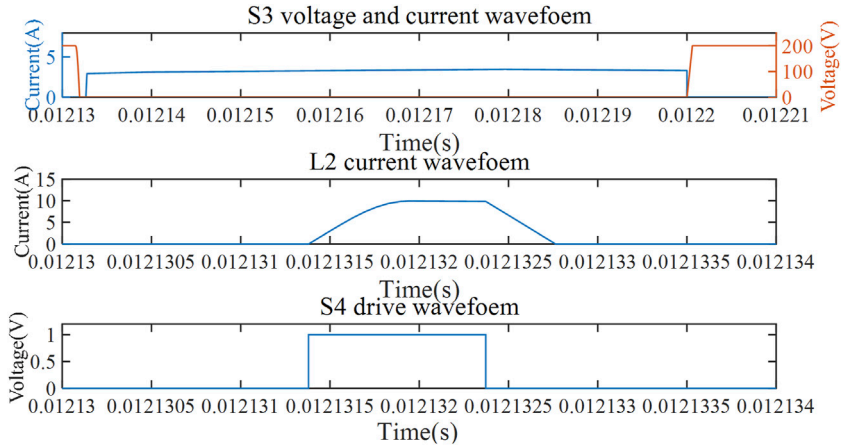

FIGURE 6
Key waveform with a negative load current direction.

the current and voltage waveforms on the switch side of S_2, the second picture shows the current flowing through inductor L_1, and the third picture shows the driving pulse of auxiliary switch S_1.

A comparison with Figure 2 shows that the proposed topology achieves the desired soft-switching effect in the simulation verification.

Figure 6 shows the simulation diagram of the operation mode with negative load current direction, where the first picture shows the current and voltage waveforms on the switch side of S_3, the second picture shows the current flowing through inductor L_2, and the third picture shows the driving pulse of auxiliary switch S_4. The comparison with Figure 2 is consistent with the analysis, and the desired soft-switching effect is achieved.

The first graph in Figure 7 shows the turn-off waveform of auxiliary switch S_1 in the operation mode with a positive load current direction. The second graph shows the turn-off waveform of auxiliary switch S_4 in the operation mode with a negative load current direction. It can be seen that the proposed topology can satisfy the ZVS turn-off of the auxiliary switch and reduce the switching loss.

4 Experimental verification and analysis

Experimental verification was carried out to verify the correctness of the simulation strategy. In this verification, the parameters of the three-phase circuit were partially consistent, so only one-phase parameters are listed. The simulation parameters are shown in Table 2.

Figure 8 shows the hardware experimental platform of the proposed O-ARCP converter, including the basic circuits such as the main circuit, the auxiliary converter circuit, the filter, the main control circuit, and the driver circuit.

Figure 9 shows the output three-phase voltage waveform.

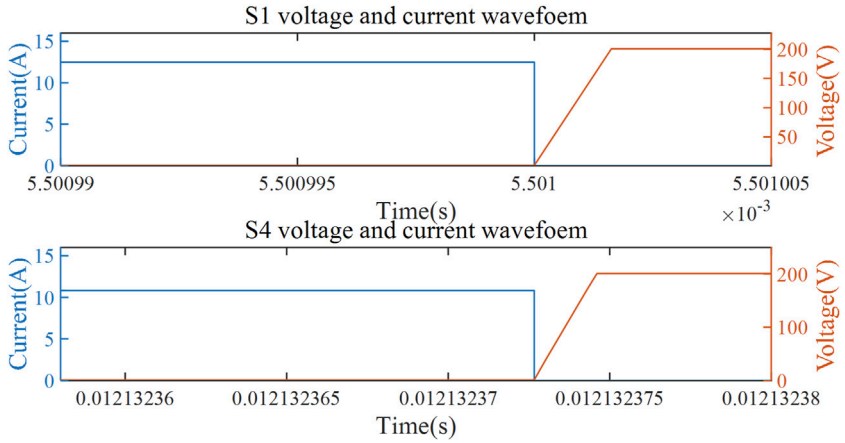

FIGURE 7
Auxiliary switch off waveform with positive and negative load current directions.

TABLE 2 Experimental parameters.

Component	Parameter
Control board	DSP TMS320F28335
S_1–S_4	IRF640 (200 V, 18 A)
D_5–D_{10}	SRA4E (400 V, 10 A)
Output power	500 W
DC voltage supply (U_d)	100 V
Switching frequency	10 kHz
Output frequency	50 Hz
Dead time	1.5 μs
L_1, L_3	6.8 μH
L_2, L_4	1 μH
C_1, C_2	10 nF
C_3	100 nF

Figure 9A shows the inverter output three-phase voltage, and Figure 9B shows the inverter THD analysis results. From Figure 9A, we can see that the inverter output voltage waveform Vpp is 85.94 V, and the frequency is 50.01 HZ. As can be seen from Figure 9B, the THD analysis results for all three channels are 1% and meet the design criteria. The experimental results do not have large errors with the simulation results.

Figure 10 shows the experimental graph of the ZVS turn-on and the ZVS turn-off waveform.

Figure 10A shows the waveform diagram of the main switch ZVS turn-on moment, Figure 10B shows the waveform diagram of the main switch ZVS turn-off moment, and Figure 10C shows the waveform diagram of the auxiliary switch ZVS turn-off moment. The red lines represent the main switch drive signals, and the blue lines represent the voltage signals at both ends of the main switch.

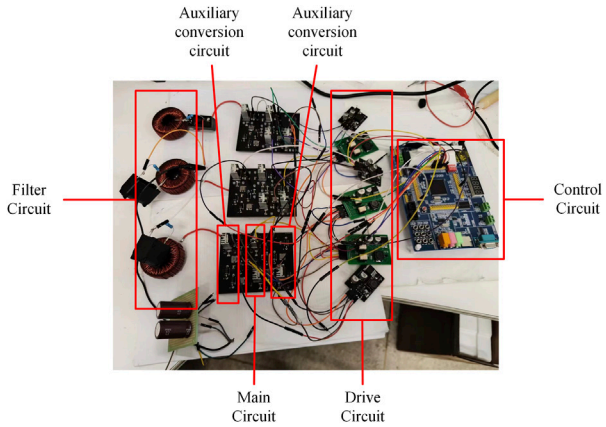

FIGURE 8
Experimental hardware platform.

It can be observed in Figure 10A that the voltage at both ends has changed to zero before the main switch is turned on. Therefore, the main switch meets the condition of the ZVS turn-on. In Figure 10B, after the main switch is turned off, the voltage at both ends is zero and rises slowly to the bus voltage after a period of time. Therefore, the main switch meets the condition of the ZVS turn-off. In Figure 10C, when the auxiliary switch is turned off, the voltage across the auxiliary switch is zero after taking approximately 2 μs to reach the bus voltage. Therefore, the auxiliary switch meets the conditions for the ZVS turn-off.

5 Comparison and analysis of inverters

5.1 Comparison of the number of devices used

Table 3 compares the number of components used in the auxiliary circuit.

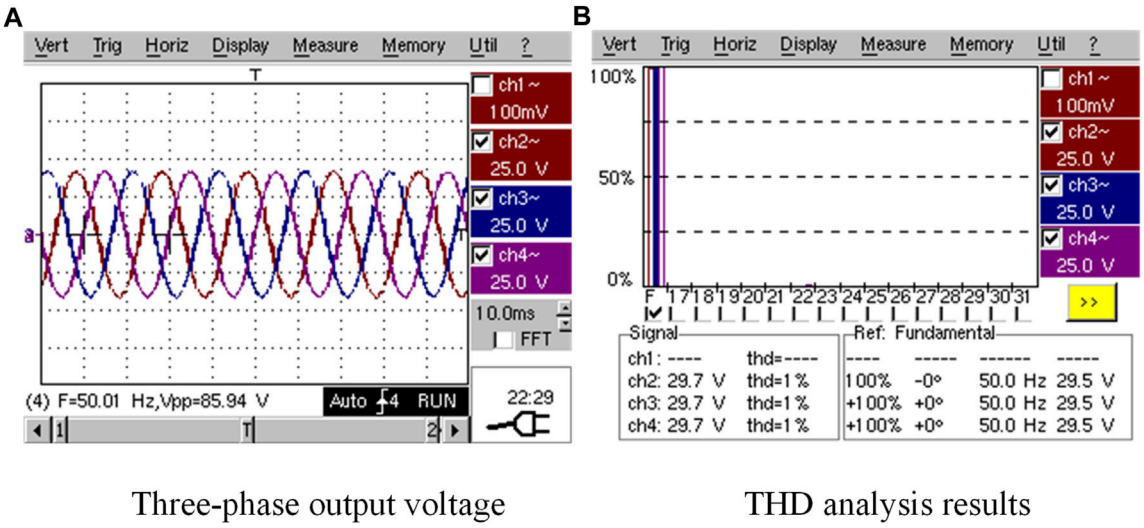

FIGURE 9
Three-phase voltage output and THD analysis results. **(A)** Three-phase output voltage; **(B)** THD analysis results.

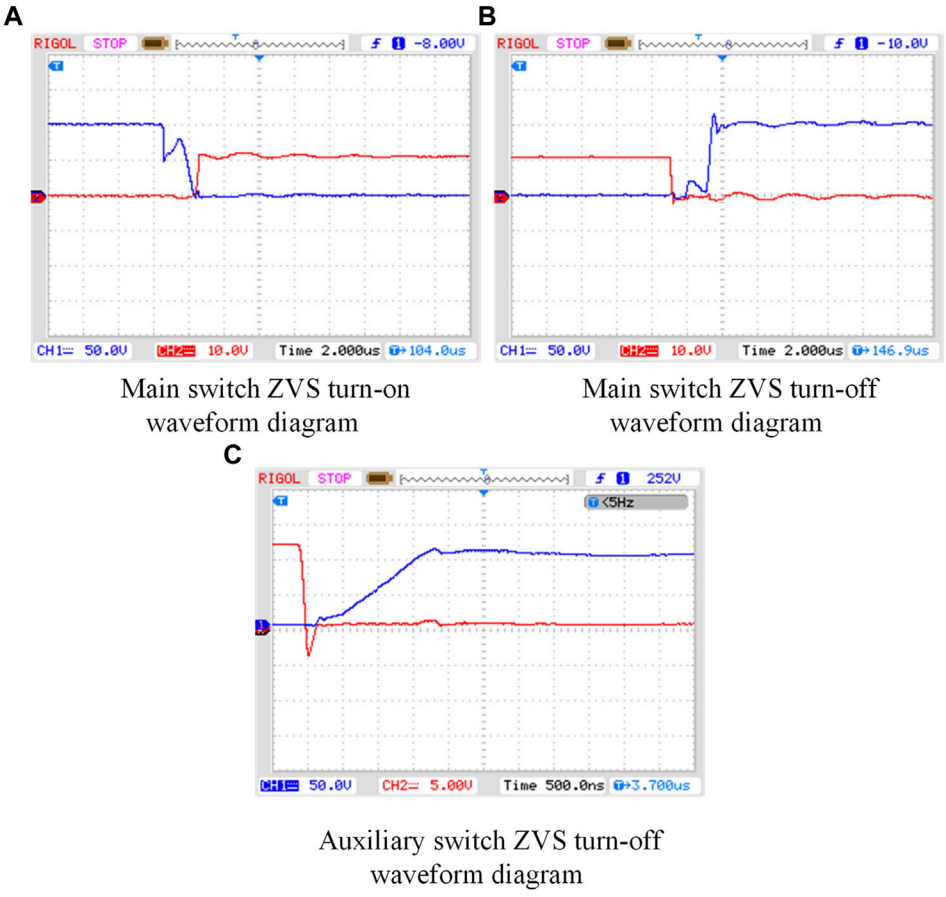

FIGURE 10
Experimental waveforms on both sides of the main and auxiliary switches. **(A)** Main switch ZVS turn-on waveform diagram; **(B)** Main switch ZVS turn-off waveform diagram; **(C)** Auxiliary switch ZVS turn-off waveform diagram.

TABLE 3 Comparison of the number of auxiliary components.

Number of components	Paper (Chu et al., 2014)	Paper (Cai et al., 2019)	Paper (Chu et al., 2016)	This paper
Auxiliary switch	12	12	6	6
Auxiliary diode	24	12	24	18
Resonant capacitor	18	12	18	9
Resonant inductor	12	6	12	12

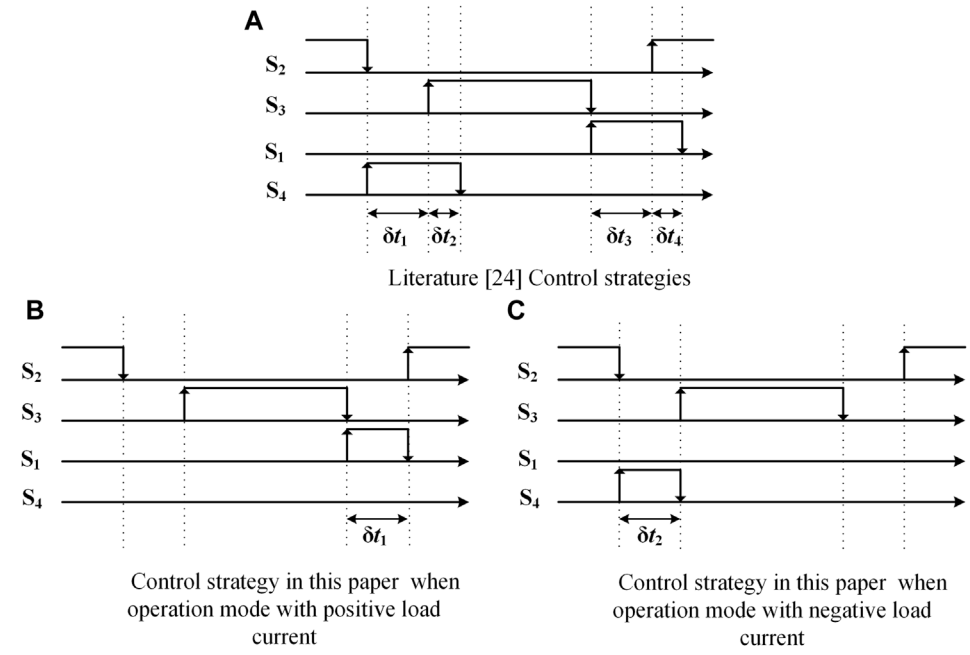

FIGURE 11
Control strategy comparison analysis chart. **(A)** Literature [24] Control strategies; **(B)** Control strategy in this paper when operation mode with positive load current; **(C)** Control strategy in this paper when operation mode with negative load current.

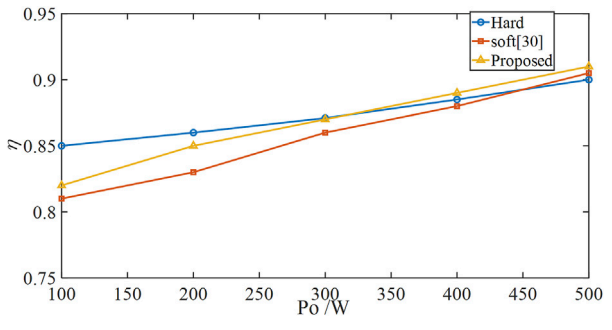

FIGURE 12
Efficiency comparison chart.

Under the control strategy proposed in this paper, only half of the components are working in each sine wave cycle on average, so in practice, three auxiliary switches are working in each cycle, in addition to nine auxiliary diodes, five resonant capacitors, and six resonant inductors. The two groups of devices work alternately within the whole cycle, reducing the loss of the auxiliary circuit.

5.2 Comparative analysis of control strategies used

Figure 11 shows a comparison of the auxiliary switch control strategy described by Chu et al. (2016) and this paper. It can be seen from Fig. 11A that Chu et al. (2016) do not divide the action of the auxiliary switch into two moments according to the load current direction, and it is necessary to operate both switches S1 and S4 in one PWM cycle. In this paper, the control strategy is divided into two types according to the load current flow direction. Only the auxiliary switch S1 needs to be operated in each PWM cycle when the load current direction is positive, and only the auxiliary switch S4 needs to be operated in each PWM cycle when the load current direction is negative, thus avoiding the problem of operating both auxiliary switches S1 and S4 in each PWM

cycle. The control strategy described by Chu et al. (2016) is longer than the one proposed in this paper by one δt2 and one δt4, and the losses generated by the auxiliary circuit in this control strategy are larger than those in this paper.

5.3 Efficiency comparison and analysis

Figure 12 shows the experimental efficiency curve of the proposed soft-switching inverter. When the output power is less than 300 W, both the soft-switching inverter proposed in this paper and the soft-switching inverter proposed by Chu et al. (2014) have less efficiency than the conventional hard-switched inverter. The reason is that the added auxiliary circuit generates more losses than the switching losses generated by the conventional hard-switched inverter.

When the output power is greater than 300 W, the efficiency of the soft-switching inverter proposed in this paper starts to be greater than that of the conventional hard-switched inverter. In contrast, the soft-switching inverter described by Chu et al. (2014) is still smaller than the conventional hard-switched inverter.

The main reason for this effect is that the number of auxiliary devices used in this article is less than that described by Chu et al. (2014). Therefore, the losses generated by the auxiliary circuits are smaller. The second reason is that the auxiliary switching control strategy used by Chu et al. (2014) is similar to that described by Chu et al. (2016). The control strategy in this paper has a relatively short operating time of the auxiliary circuit. As a result, fewer additional power losses are incurred.

6 Conclusion

An efficient soft-switching topology is proposed in this paper, and after theoretical analysis and simulation experiments, the following conclusions are drawn.

1. Compared with the control strategies proposed in the literature (Chu et al., 2014; Chu et al., 2016), under the control strategy proposed in this paper, only one set of auxiliary components is under operation in every half cycle, and the auxiliary components work only once in a cycle, which greatly reduces the losses due to the auxiliary circuit.
2. Compared with Chu et al. (2014), the proposed topology in this paper reduces the number of auxiliary components used and reduces the size and cost of the inverter.
3. It is verified by simulation and experiment that the transmission efficiency of the grid-connected inverter can be improved in grid-connected or islanded mode.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary material; further inquiries can be directed to the corresponding author.

Author contributions

CL and YW developed the idea. CL developed the theory, the calculations, and the simulations. YW supervised and reviewed this work. All authors contributed to the article and approved the submitted version.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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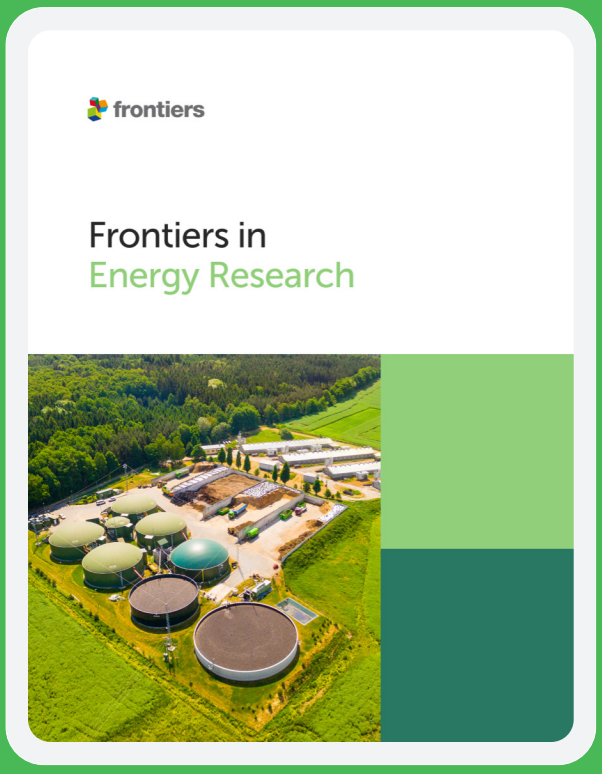

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